A Load-Current-Estimating Scheme With Delay Compensation for the Dual-Active-Bridge DC–DC Converter

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***Abstract*—The dual-active-bridge (DAB) dc–dc converter is a promising candidate for the isolated dc–dc power transferred applications, such as in the dc distribution system, the solid-state transformer, and the energy storage system. In these applications, the fast-dynamic response is usually a core requirement, especially under load changes. To improve the dynamic performance of the DAB dc–dc converter, this article proposes a simple load-current-estimating (LCE) scheme with delay compensation for fast dynamic performance. Based on the current flowing model of the DAB dc–dc converter, the LCE strategy is proposed with single-phase-shift modulation method. Moreover, the inherent switching-period delay phenomenon of the LCE scheme is analyzed. Therefore, the corresponding delay compensation method is proposed for further boosting dynamic responses, and the dynamic limitation of the LCE scheme may be obtained for DAB dc–dc converter. Then, for the proposed LCE scheme, a damping coefficient is introduced to restrict the potential instability caused by the measurement noise, and the fast-dynamic response will be influenced a little when the load resistor is changed. In addition, the extended rule for the optimized triple-phase-shift modulation method is discussed. Finally, the simulation result and the experimental result both validate the fast-dynamic performance of this proposed LCE strategy without or with delay compensation.**

***Index Terms*—Current sensorless, dual-active-bridge (DAB) dc–dc converter, dynamic performance, load-current-estimating (LCE) scheme.**

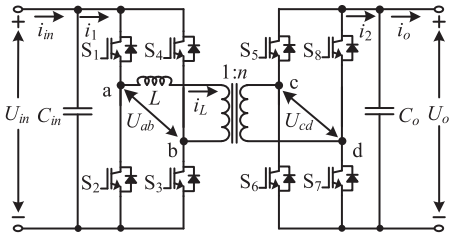

Fig. 1. Topology of the DAB dc–dc converter.

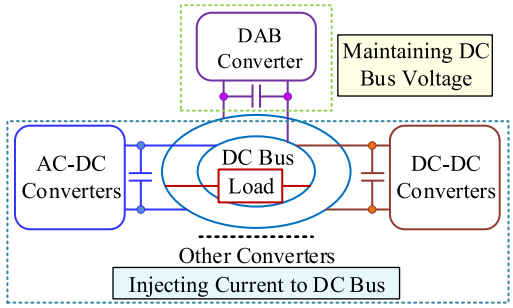

Fig. 2. Potential application of the DAB dc–dc converter.

I. Introduction

THE dual-active-bridge (DAB) dc–dc converter, as shown in Fig. 1, is originally proposed at the beginning of the 1990s [1]. Due to the advantage of high-power density, soft switching performance, bidirectional power flow capability, and high efficiency potential, the DAB dc–dc converter has attracted more and more attention in the dc–dc power systems as shown in Fig. 2, such as the energy storage system [2], [3], the automotive application [4], [5], the dc microgrid [6], [7], and the railway traction [8].

In these power conversion systems, the DAB dc–dc converter has to face the variations of the load condition and the input voltage, which may result in the disturbances of the output voltage and affect the stability of DAB-based system. Thus, the robust and fast dynamic response is an essential requirement for DAB dc–dc converters in these applications [9], [10]. Traditionally, the single-loop voltage controller can be employed to deal with the change of the input voltage and the load [10], [11]. However, since the regulation of the output voltage is mainly dependent on the PI controller, the dynamic performance of the DAB dc–dc converter is limited. To improve the dynamic performance of the DAB dc–dc converter, a load current feed-forward control method is proposed in [12] to improve the dynamic performance for load change, where the lookup table with the offline precomputation is required. Based on the natural switching surface of inductance current, the fast-transient boundary control scheme can provide excellent dynamic performance without visible disturbance of output voltage for the DAB dc–dc converter

Manuscript received June 1, 2021; revised August 3, 2021; accepted September 2, 2021. Date of publication September 10, 2021; date of current version November 30, 2021. This work was supported by Future Energy Systems initiative funding from the Canada First Research Excellence Fund and Alberta Innovates Graduate Student Scholarship from the Alberta Innovates. Recommended for publication by Associate Editor H. S. Krishnamoorthy. *(Corresponding author: Yue Zhang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3111854.

Digital Object Identifier 10.1109/TPEL.2021.3111854

when the load resistor and the input voltage are changed [13]. However, two current sensors and two voltage sensors are needed to measure the load current and control the inductance current, which increases the cost of the hardware design. By reducing the inductance current sensor, a virtual-direct-power control strategy is proposed for the similar excellent dynamic performance under the disturbances of the load resistor and the input voltage [14]. Moreover, a nonlinear model predictive control scheme with less parameter sensitiveness is proposed for the DAB dc–dc converter [15]. Similarly, a moving-discretized-control-set model-predictive control method is proposed to supply the pulsed power loads [16]. These two model predictive control strategies can both provide excellent dynamic performance.

In the above-mentioned advanced schemes, it is necessary to measure the load current for fast-dynamic performance [13]–[18]. To eliminate the requirement of current sensor, a current sensorless control scheme with the nonlinear disturbance observer is proposed to obtain the fast-dynamic performance for the DAB dc–dc converter [19]. Moreover, without load-current sensor, a disturbance-observer-based control scheme is also proposed to boost the dynamic performance of the DAB dc–dc converter [20]. However, these two current sensorless controls mainly rely on the general control concepts, where the positive feedback value is added to the control value and the control model is not accurate enough for the DAB dc–dc converter. Moreover, the inherent switching-period delay phenomenon which restricts the expected limits of the dynamic performance is not considered in the existing current sensorless methods for the DAB dc–dc converter.

To perfect the current sensorless control, this article proposes a simple load-current-estimating (LCE) scheme with delay compensation, which ensures excellent dynamic performance for the DAB dc–dc converter. The rest of this article is organized as follows. In Section II, the single-phase-shift (SPS) modulation method is discussed, and the reason why the current sensorless control method is required is analyzed. Then, the LCE strategy is proposed in Section III, and the inherent switching-period delay of the LCE strategy is discussed and compensated. Then, a damping coefficient is introduced to restrict the potential instability caused by the measurement noise of the proposed LCE scheme, and the implementation rules for other advanced phase-shift modulation methods are discussed. Moreover, in Section IV, the simulation results are employed to verify the effectiveness of the theoretical analysis, and an experimental hardware prototype of DAB dc–dc converter is also developed to verify the excellent dynamic performance of the proposed LCE scheme with delay compensation. Finally, Section V concludes this article.

II. Current Transferred Characteristic of DAB DC–DC Converter Under SPS Modulation Method

The phase-shift modulations are widely applied in the DAB dc–dc converter, especially the SPS modulation method. The SPS modulation method is originally presented with the invention of the DAB dc–dc converter in [21], which can be illustrated in Fig. 3.

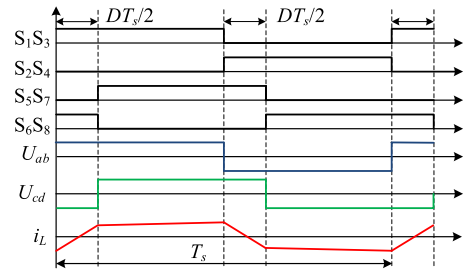

Fig. 3. Waveforms of the SPS modulation method.

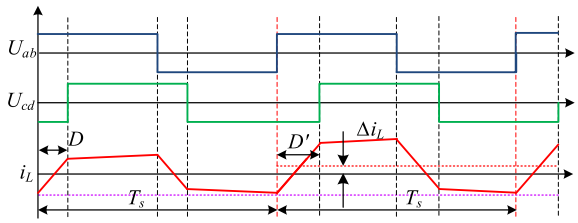

Fig. 4. Waveforms of the SPS modulation method during the transient process.

As shown in Fig. 3, S_1–S_8 are the square-wave gate driving signals with 50% duty ratio of the corresponding switches. U_{ab} and U_{cd} are the output voltages of the primary-side and secondary-side H Bridges, respectively. T_s is the switching period, and i_L is the current of the equivalent inductance L between two H bridges. D is the phase-shift ratio for controlling the power transfer of the DAB dc–dc converter. Then, the transferred power under SPS modulation method can be expressed as follows:

$$P = \frac{U_{in}U_oD(1-D)T_s}{2nL}. \tag{1}$$

As shown in (1), the amount of the transferred power P can be directly determined by the input voltage U_{in}, the output voltage U_o, the switching period T_s, the transformer turn ratio n, the equivalent inductance L, and the phase-shift ratio D.

However, (1) only demonstrates the transferred power of the DAB dc–dc converter at the steady-state condition. In fact, the transferred power of the DAB dc–dc converter often changes during the transient process in practical applications. When the DAB dc–dc converter is on a transient process, the phase-shift ratio D has to be adjusted to meet the new load-current requirement. Then, the waveforms of the SPS modulation method in this phenomenon can be shown in Fig. 4.

As shown in Fig. 4, since the input voltage and the output voltage can be regarded as the same in a switching period, the transferred power of the DAB dc–dc converter can be calculated by the new phase-shift ratio D' as follows:

$$\begin{aligned} P &= \frac{1}{T_s}\int_0^{T_s}\frac{U_{cd}}{n}(i_L+\Delta i_L)dt = \frac{1}{T_s}\int_0^{T_s}U_{ab}(i_L+\Delta i_L)dt \\ &= \frac{2}{T_s}\int_0^{\frac{T_s}{2}}U_{in}i_Ldt + \frac{\Delta i_L}{T_s}\int_0^{T_s}U_{ab}dt \\ &= \frac{2}{T_s}\int_0^{\frac{T_s}{2}}U_{in}i_Ldt = \frac{U_{in}U_oD(1-D)T_s}{2nL}. \end{aligned} \tag{2}$$

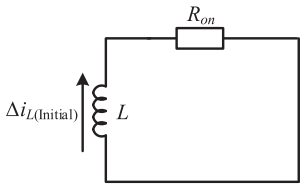

Fig. 5. Equivalent circuit for the dc offset of the inductance current at steady-state condition.

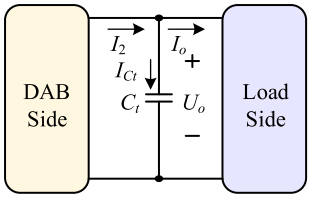

Fig. 6. Average model of the output side for the DAB dc–dc converter.

Compared (1) with (2), the relationship between the transferred power and the phase-shift ratio is the same at steady-state condition and during the transient process. In addition, the dc offset of the inductance current can be consumed by the conducting resistor R_{on} of the DAB dc–dc converter. Since U_{ab} and U_{cd} are total ac components at steady-state condition which cannot generate dc inductance current, the equivalent circuit can be shown in Fig. 5. Then, the dc offset of the inductance current Δi_L can be consumed by the conducting resistor R_{on} of the DAB dc–dc converter gradually, which affects the transferred power of this converter slightly with the tiny conducting resistor.

III. Proposed CEL Strategy With Delay Compensation for DAB DC–DC Converter

A. Simple LCE Strategy for the DAB DC–DC Converter

According to (1) and combining the average modeling concept [22], the transferred current I_2 of the DAB dc–dc converter can be expressed as follows:

$$I_2 = \frac{P}{U_o} = \frac{U_{in} D(1-D) T_s}{2nL}. \tag{3}$$

Moreover, the average model of the output side for the DAB dc–dc converter can be shown in Fig. 6.

In Fig. 6, C_t is the total equivalent capacitor as $C_o + C_e$ of the DAB dc–dc converter. I_{Ct} is the charging current of the capacitor C_t in a switching period and I_o is the dc component of the load current. As shown in Fig. 6, when the disturbance of load resistor emerges, the variation of the output voltage U_o can be reduced, only if the transferred current I_2 can meet the demand of the load current I_o timely. In the DAB dc–dc converter, the estimated load current I_{LC} can be expressed by the transferred current I'_2 and the charging current I'_{Ct} in the last switching period as follows:

$$I_{LC} = I'_2 - I'_{Ct} = I'_2 - \frac{(U'_o - U_o) C_t}{T_s} \tag{4}$$

where U'_o is the measured output voltage in the last switching period, and U_o can be regarded as the measured output voltage

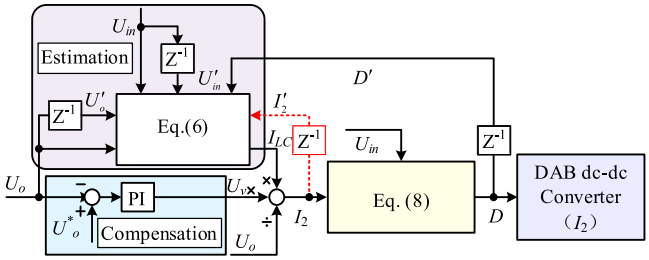

Fig. 7. Control block of the proposed LCE strategy for the DAB dc–dc converter.

in the current switching period. The transferred current I'_2 in the last switching period can be obtained by the phase-shift ratio D' in the last switching period, the average input voltage and the circuit current of the DAB dc–dc converter. Then, according to (3), the transferred current I'_2 in the last switching period can be calculated as follows:

$$I'_2 = \frac{(U_{in} + U'_{in}) D'(1-D') T_s}{4nL}. \tag{5}$$

In (5), the input voltage is represented by the average value of the measured input voltages from the last switching period U'_{in} and the current switching period U_{in}, which can make this operation model more accurate. Then, combining (4) and (5), the required load current I_{LC} can be further expressed as follows:

$$I_{LC} = \frac{(U_{in} + U'_{in}) D'(1-D') T_s}{4nL} - \frac{(U'_o - U_o) C_t}{T_s}. \tag{6}$$

To meet the demand of the load current immediately, the transferred current I_2 in the current switching period should be equivalent to the estimated load current I_{LC}. However, the power losses of the DAB dc–dc converter cannot be omitted, and the PI controller should be employed to compensate for the error between the load current and the transferred current of the DAB dc–dc converter in steady-state status. Then, the required transferred current I_2 in the current switching period can be expressed as follows:

$$I_2 = \frac{U_v}{U_o} I_{LC} \tag{7}$$

where U_v is named as the virtual output voltage, which is the output value of the PI controller. In addition, when the required transferred current I_2 is determined, the required phase-shift ratio D^* can be calculated based on (3) as follows:

$$D^* = \begin{cases} \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2nLI_2}{U_{in} T_s}} (I_2 \geq 0) \\ -\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{2nLI_2}{U_{in} T_s}} (I_2 < 0). \end{cases} \tag{8}$$

Then, according to (8), the required phase-shift ratio D^* in the current switching period can be determined, and once the transferred current can meet the demand of the actual load current, the output voltage of the DAB dc–dc converter can reach its desired value. Combining (6) and (8), the control block of the proposed LCE strategy for the DAB dc–dc converter can be illustrated in Fig. 7. At the beginning of each switching period, the input voltage U_{in} and the output voltage U_o are measured.

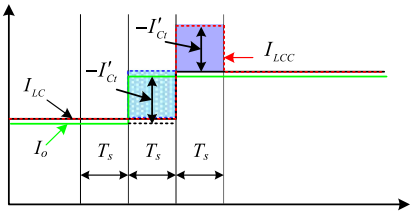

Fig. 8. Schematic diagram of the compensating process.

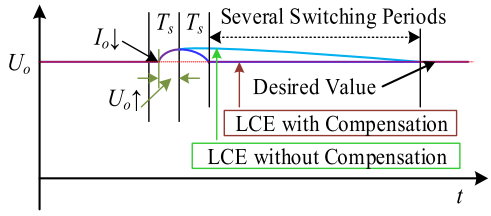

Fig. 9. Expected dynamic behaviors under the LCE strategy with or without delay compensation when the load current is decreased.

Then, based on the difference between the output voltage U_o and its desired value $U^*{}_o$, the virtual output voltage U_v can be obtained by using the PI controller. Moreover, according to (6), the estimated load current I_{LC} can be obtained, and combining (7), the required transferred current I_2 in the current switching period can be calculated. In addition, according to (4), the estimated load current I_{LC} can also be calculated by the transferred current I'_2 and the charging current I'_{Ct} in the last switching period. However, once the input voltage U_{in} is changed in the last switching period, the actual transferred current I'_2 will also be varied, which will make the estimation inaccurate. Finally, according to (8), the needed phase-shift ratio D^* can be determined for controlling the transferred current, which is very close to the required transferred current I_2 in the actual DAB dc–dc converter. Then, the fast-dynamic performance can be provided for the DAB dc–dc converter.

B. Switching-Period Delay Phenomenon and the Corresponding Compensation

According to the estimating principle of the LCE strategy, there is usually a switching-period delay between the actual load current I_o and the estimated load current I_{LC}. Therefore, when the load-current disturbance is determined, the output-voltage disturbance caused by the change of load current in the last switching period should be compensated as shown in Fig. 8. Otherwise, the disturbance of U_o will be compensated by the outer-loop PI controller, which takes more time.

As shown in Fig. 8, the LCE strategy can only detect the variation of load current in the last switching period, and the dynamic response of the estimating scheme is always containing a switching-period delay. Therefore, the dc-link capacitor provides the difference between the transferred current and the actual load current in the last switching period, which results in the disturbance of the output voltage of the DAB dc–dc converter. To offset the change of output voltage, the compensated transferred current I_2 in the current switching period should be calculated as follows:

$$I_2 = \frac{U_v}{U_o}(I_{LC} - I'_{Ct}). \tag{9}$$

Based on (9), with the active compensation for the dc-link capacitor, the disturbance of the output voltage U_o can be eliminated quickly, and the excellent performance of the DAB dc–dc converter can be achieved. The dynamic performances of the LCE strategy with or without delay compensation when the load current is suddenly decreased can be predicted as shown in Fig. 9.

As shown in Fig. 9, when the load current is decreased suddenly, the dc-link capacitor C_t will be charged by the redundant transferred current of the DAB dc–dc converter, and the output voltage will be increased. When the delay compensation is not adopted, the change of the output voltage should be compensated by the PI controller. When the delay compensation is employed, the excess energy of the dc-link capacitor can be released immediately, and the theoretical limitation of the dynamic behavior of the DAB dc–dc converter can be obtained.

C. Potential Sensibility to the Measurement Noise of the Proposed Strategy

Generally, there are three noises which may result in the instability of the DAB dc–dc converter, including the voltage-ripple noise, the quantization noise and the measurement noise [8], and the measurement noise always influences the output voltage obviously. Combining (4)–(7), the required transferred current I_2 in the current switching period can be calculated as follows:

$$\begin{aligned} I_2 &= \frac{U_v}{U_o}\left[\frac{(U_{in}+U'_{in})D'(1-D')T_s}{4nL} - \frac{(U'_o - U_o)C_t}{T_s}\right] \\ &\approx \frac{(U_{in}+U'_{in})D'(1-D')T_s}{4nL} - \frac{(U'_o - U_o)C_t}{T_s}. \end{aligned} \tag{10}$$

However, when the input voltage and the output voltage contain the measurement noises, the disturbances of the output voltage may be emerged [23], and the required transferred current I_{2MN} with measurement noises ΔU_{in} and ΔU_o can be expressed as follows:

$$\begin{aligned} I_{2MN} \approx{}& \frac{[(U_{in}+\Delta U_{in})+(U'_{in}+\Delta U'_{in})]D'(1-D')T_s}{4nL} \\ &- \frac{[(U'_o+\Delta U'_o)-(U_o+\Delta U_o)]C_t}{T_s}. \end{aligned} \tag{11}$$

Then, combining (10) and (11), the error of the estimated required transferred current can be expressed as follows:

$$\begin{aligned} \Delta I_2 &= I_{2ME} - I_2 \\ &\approx \frac{(\Delta U_{in}+\Delta U'_{in})D'(1-D')T_s}{4nL} + \frac{(\Delta U_o - \Delta U'_o)C_t}{T_s}. \end{aligned} \tag{12}$$

Obviously, the estimating error of load current ΔI_2 will bring the error of the phase-shift ratio, continuously. Then, the oscillation of the phase-shift ratio will emerge, and the DAB dc–dc converter will be unstable. In order to illustrate the potential instability clear, the main reason should be acquired. Moreover, the maximum transferred current of the DAB dc–dc converter can be expressed as follows:

$$I_{2M}|_{D=0.5} = \frac{U_{in}T_s}{8nL}. \tag{13}$$

Combing (12) and (13), the ratio r_{lc} of the estimating error can be calculated as follows:

$$\begin{aligned} r_{lc} &= \frac{2D'(1-D')(\Delta U_{in}+\Delta U'_{in})}{U_{in}} + \frac{8nL(\Delta U_o-\Delta U'_o)C_t}{U_{in}T_s^2} \\ &\le \frac{(\Delta U_{in}+\Delta U'_{in})}{2U_{in}} + \frac{8nL(\Delta U_o-\Delta U'_o)C_t}{U_{in}T_s^2} \\ &\approx \frac{8LC_t[n(\Delta U_o-\Delta U'_o)]}{U_{in}T_s^2}. \end{aligned} \tag{14}$$

According to (14), the measurement noise of the output voltage may easily generate instability to the DAB dc–dc converter. In order to restrict the unstable phenomenon, a damping coefficient λ is adopted, and then, (14) can be further expressed as follows:

$$r_{lc} \approx \frac{8LC_t[n(\Delta U_o-\Delta U'_o)]\lambda}{U_{in}T_s^2} < r_{lc\min} \tag{15}$$

where $r_{lc\min}$ is the expected minimum estimating error ratio during the transient process. According to (15), the damping coefficient λ can be calculated as follows:

$$\lambda < \frac{r_{lc\min}U_{in}T_s^2}{8nLC_t(\Delta U_o-\Delta U'_o)_{\max}}. \tag{16}$$

With the damping coefficient λ, (6) can be further expressed as follows:

$$I_{LC} = \frac{(U_{in}+U'_{in})D'(1-D')T_s}{4nL} - \frac{\lambda(U'_o-U_o)C_t}{T_s}. \tag{17}$$

Based on discrete model, the estimating load current in the kth switching period can be further expressed as follows:

$$\begin{aligned} I_{LC}(kT_s) &= I_2[(k-1)T_s] - \lambda I_{Ct}[(k-1)T_s] \\ &= \frac{U_v}{U_o}I_{LC}[(k-1)T_s] - \lambda I_{Ct}[(k-1)T_s] \\ &\approx I_{LC}[(k-1)T_s] + \lambda\{[I_o[(k-1)T_s] \\ &\quad - I_{LC}[(k-1)T_s]\} \end{aligned} \tag{18}$$

where $I_o[(k-1)T_s]$ is the actual load current in the $(k-1)$th switching period. Then, with the damping coefficient, (18) can be equivalent to a first-order low-pass filter which can be expressed as follows:

$$\begin{aligned} Y(kT_s) &= qU(kT_s) + (1-q)Y[(k-1)T_s] \\ &= Y[(k-1)T_s] + q\{U(kT_s) - Y[(k-1)T_s]\} \end{aligned} \tag{19}$$

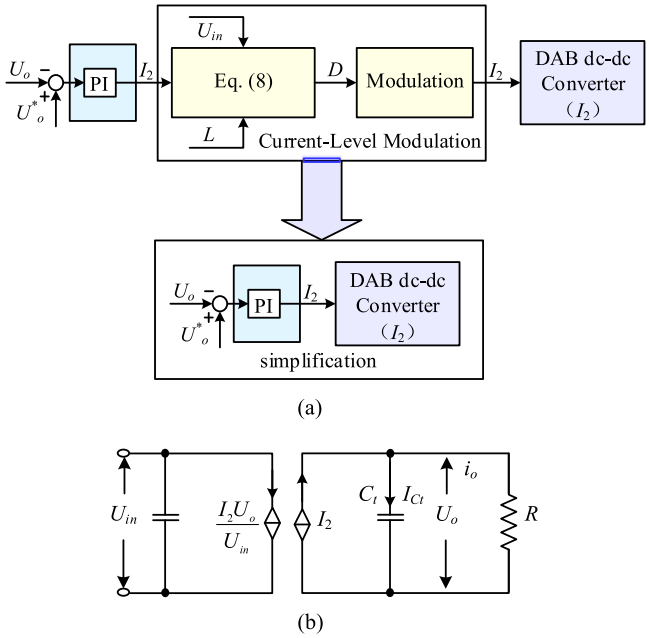

Fig. 10. Derivation of the simplified average model of the DAB converter. (a) Control diagram without feedback loop. (b) Average model of the DAB converter.

where $U(k)$ is the measured value, $Y(k)$ is the measured value after the first-order low-pass filter, and q is the time constant. q can be expressed as follows:

$$q = 2\pi f_c T_s \tag{20}$$

where f_c is the cut off frequency of the first-order low-pass filter. Similarly, the damping coefficient λ can also be called as the time constant. Then, based on this damping coefficient, the stability of the DAB dc–dc converter can be increased under the proposed LCE strategy, and the dynamic performance will be affected a little since the estimated load current is inaccurate in the first several periods with the first-order low-pass filter function. Generally, the difference between the LCE schemes with or without delay compensation will be reduced. Fortunately, the feedback loop can still accelerate the dynamic process.

D. Small Signal Model of DAB DC–DC Converter and the Stability Analysis of the Proposed Strategy

The control model without feedback loop can be shown in Fig. 10(a), where a simplified control diagram can be obtained. Then, since the DAB converter can usually be modeled as a current source [24], [25], the average model of the DAB dc–dc converter can be shown in Fig. 10(b). As shown in Fig. 10(a), the output value of the outer PI controller can be directly related to the transferred current I_2. Then, based on the relationship between the phases-shift ratio D and the transferred current I_2, the current-level modulation operation can be achieved, which can simplify the average model of DAB dc–dc converter obviously as shown in Fig. 10(b).

Then, since the input side is a voltage source, the average model and small signal model of the DAB dc–dc converter can

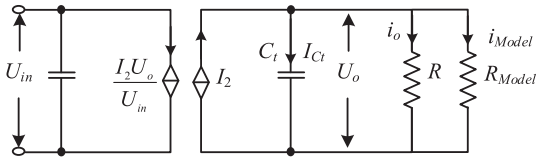

Fig. 11. Average model of DAB dc–dc converter with feedback operation.

TABLE I
PARAMETERS FOR BODE DIAGRAM

k_p	0.105
k_i	0.005
R	30Ω
C_t	0.5mF
T_d	T_s (0.1ms)

be expressed as follows:

$$\begin{cases} C_t \frac{dU_o}{dt} = I_2 - i_o \\ C_t \frac{d\hat{U}_o}{dt} = \hat{I}_2 - \hat{i}_o \,. \end{cases} \tag{21}$$

Moreover, based on Fig. 10(a), the output impedance of the DAB dc–dc converter can be calculated as follows:

$$Z(s) = \frac{R}{sCR+1}. \tag{22}$$

Combining Fig. 10 and (22), the transfer function can be obtained as follows:

$$G_k(s) = G(s)|_{\mathrm{PI}} Z_{out}(s) = \frac{k_p s + k_i}{s} \frac{R}{RC_t s + 1}. \tag{23}$$

In addition, when the ideal load-estimating loop is considered, the average model of the DAB dc–dc converter can be shown in Fig. 11.

In terms of the PI controller branch, the load resistor of the DAB dc–dc converter can be regarded as the equivalent resistor of the actual resistor R and the resistor from the feedback loop R_{Model}. Then, when the feedback loop can compensate the actual resistor accurately by using R_{Model}, there will be no adjustment of the PI controller for providing additional current to the load side. Therefore, in terms of the PI loop, the output side can be regarded as only capacitor C_t. Then, (23) can be further expressed as follows:

$$G_k(s) = G(s)|_{\mathrm{PI}} Z_{out}(s) = \frac{k_p s + k_i}{s} \frac{1}{C_t s} \tag{24}$$

where k_p, k_i, R, and C_t are listed in Table I. Based on Table I, (23) and (24), the bode diagram can be shown in Fig. 12, where the phase margin is always bigger than 45°. So, based on the proposed LCE scheme, this DAB system should be stable. A similar result can be obtained in [25], where the transfer function is based on the phase-shift ratio. Then, with the damping parameter, the bode waveforms will be between the bode waveforms with or without a load estimating loop.

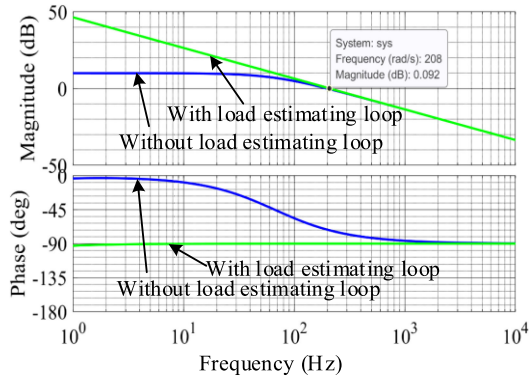

Fig. 12. Bode diagrams for the proposed method without or with an ideal load-estimating loop.

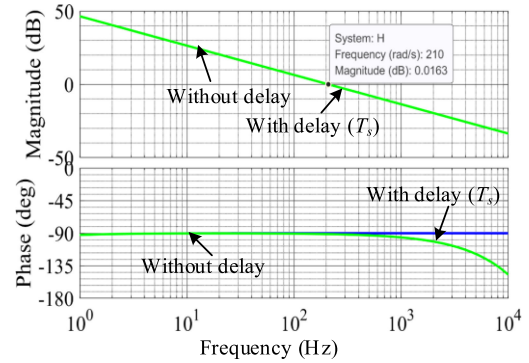

Fig. 13. Bode diagrams for the proposed method without or with delay.

Furthermore, when the delay time is considered, (24) can be further expressed as follows:

$$G_k(s) = G(s)|_{\mathrm{PI}} Z_{out}(s) = \frac{k_p s + k_i}{s} \frac{1}{C_t s} e^{-sT_d} \tag{25}$$

where k_p, k_i, R, C_t, and T_d are listed in Table I. Based on Table I, (24) and (25), the bode diagram can be shown in Fig. 13, where the magnitude is smaller than 0 when the phase margin is smaller than 45°. So, the system should also be stable based on the bode diagram when the delay time is equivalent to the switching period.

$$I_2' = \begin{cases} \frac{(-D\prime_1 + D\prime_2 + D\prime_3 - D\prime_1^2 - D\prime_2^2 - D\prime_3^2 + D\prime_1 D\prime_2 + D\prime_1 D\prime_3) U_{in} T_s}{4nL} \\ \qquad (D\prime_1 \le D\prime_2 \le D\prime_3) \\ \frac{(-D\prime_1 + D\prime_2 + D\prime_3 - D\prime_3^2 - D\prime_1 D\prime_2 + D\prime_1 D\prime_3) U_{in} T_s}{4nL} \\ \qquad (D\prime_2 \le D\prime_1 \le D\prime_3) \end{cases}. \tag{26}$$

E. Extension of the Proposed LCE Strategy for Other Advanced Phase-Shift Modulation Method

Based on the relationship among the transferred current, the capacitor charging current and the load current in the last switching period, the LCE strategy is proposed to obtain the estimated load current I_{LC}. Then, the required transferred current I_2 in

TABLE II
OPTIMIZED SOLUTIONS OF MCSO STRATEGY UNDER DIFFERENT CONDITIONS

Voltage Conditions	Unified Transferred Current I_{2U}	Range of I_{2U}	Middle Variable	Phase-Shift Ratio
$k>1$	$I_{2U}=\frac{8nLI_2}{U_{in}T_s}$	$0\le I_{2U}<2\frac{k-1}{k^2}$	$D_1=1-\sqrt{\frac{I_{2U}}{2(k-1)}}$	$\begin{cases}D_2=(k-1)(1-D_1)\\D_3=D_1\end{cases}$
		$2\frac{k-1}{k^2}\le I_{2U}\le 1$	$D_1=(k-1)\sqrt{\frac{1-I_{2U}}{k^2-2k+2}}$	$\begin{cases}D_2=\frac{k-2}{2(k-1)}D_1+\frac{1}{2}\\D_3=\frac{k-2}{2(k-1)}D_1+\frac{1}{2}\end{cases}$
$k\le 1$		$0\le I_{2U}<2(k-k^2)$	$D_1=1-\sqrt{\frac{I_{2U}}{2k(1-k)}}$	$\begin{cases}D_2=0\\D_3=kD_1-k+1\end{cases}$
		$2(k-k^2)\le I_{2U}\le 1$	$D_2=\frac{1}{2}(1-\sqrt{\frac{1-I_{2U}}{2k^2-2k+1}})$	$\begin{cases}D_1=0\\D_3=2kD_2-D_2-k+1\end{cases}$

TABLE III
CIRCUIT PARAMETERS OF THE DAB DC–DC CONVERTER

L	50μH
n	2
f_s	10kHz
R	30Ω or 60Ω
U_{in}	30 or 40
U^*_o	60V
C_o	0.5mF

the current switching period can be calculated as shown in Fig. 6. Based on an existing hybrid efficiency- and dynamic-optimization concept [3], this proposed LCE strategy with the transferred current I_2 as the outer-loop output value can be easily extended to other advanced phase-shift modulation methods including the dual-phase-shift method [26], the extended-phase-shift method [27], and the triple-phase-shift method [28].

Moreover, based on the optimized triple-phase-shift modulation method for the DAB dc–dc converter [11], [29], the corresponding phase-shift ratios D_1–D_3 can be calculated by the needed transferred current I_2 or its unified value I_{2U} as shown in Table II. Moreover, under the triple-phase-shift modulation method [11], the transferred current I'_2 in the last switching period can be expressed by the employed phase-shift ratios D'_1–D'_3 in the last switching period as in (26). Then, combining Table II and (26), the proposed LCE strategy can be implemented with the optimized triple-phase-shift modulation method.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The simulation and experimental results are both given to verify the effectiveness of the proposed LCE strategy with delay compensation, and the circuit parameters of the DAB dc–dc converter can be shown in Table III. Moreover, the single-voltage loop (SLV) control method is acted as the comparative group for comparing with the proposed LCE strategy without or with delay compensation.

A. Simulation Result

In the simulation part, the results of the proposed LCE strategy without or with delay compensation are provided. When t is equivalent to 0.4 s, U_{in} is changed from 30 to 40 V, and when t is equivalent to 0.5 s, U_{in} is changed from 40 to 30 V as shown in Fig. 10(a). Moreover, when t is equivalent to 0.6 s, R is changed from 30 to 60 Ω, and when t is equivalent to 0.7 s, R is changed from 30 to 60 Ω as shown in Fig. 14(b). Fig. 14(c) shows the simulation result of the proposed LCE strategy without delay compensation, where the dc-link voltage disturbances are smaller than 0.5 V, but the setting time for reaching the desired output voltage again is about 10 ms. Furthermore, with the delay compensation method, the simulation results can be illustrated in Fig. 15. As shown in Fig. 15(a) and (b), a delay compensation of the load current is added in the next switching period after the change of the load resistor. Then, the dc-link voltage disturbances under the change of load resistor are smaller than 0.5 V, and the setting time is only one switching period as shown in Fig. 15(c). Therefore, based on the proposed compensation method, the setting time of the DAB dc–dc converter under the change of load resistor can be reduced in one switching period in the theoretical conditions. The dynamic performances of the DAB dc–dc converter under the LCE scheme with or without delay compensation are the same as theory analysis.

Moreover, when U_{in} is equivalent to 30 V and R is changed between 30 and 60 Ω, Fig. 16 illustrates the simulation result under the SVL control method. In Fig. 16, the setting time of the SVL method is also bigger than 40 ms under the disturbance of load resistor, and the output-voltage disturbances are bigger than 10 V.

In addition, when the voltage white noise at 0.5 V is added in the measured input voltage and output voltage, the calculated damping coefficient is 0.1 by using (16). Then, Fig. 17 shows the simulation results under the LCE scheme without or with delay compensation when the load resistor is changed between 30 and 60 Ω. As shown in Fig. 17(c), the settling times of the LCE scheme without or with delay compensation are close to 6 ms,

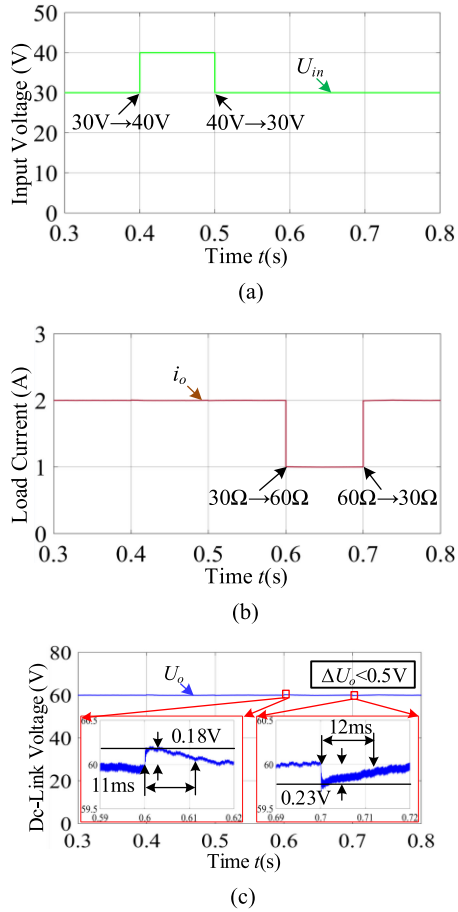

Fig. 14. Simulation results under the LCE scheme without delay compensation. (a) Input voltage. (b) Load current. (c) Output voltage.

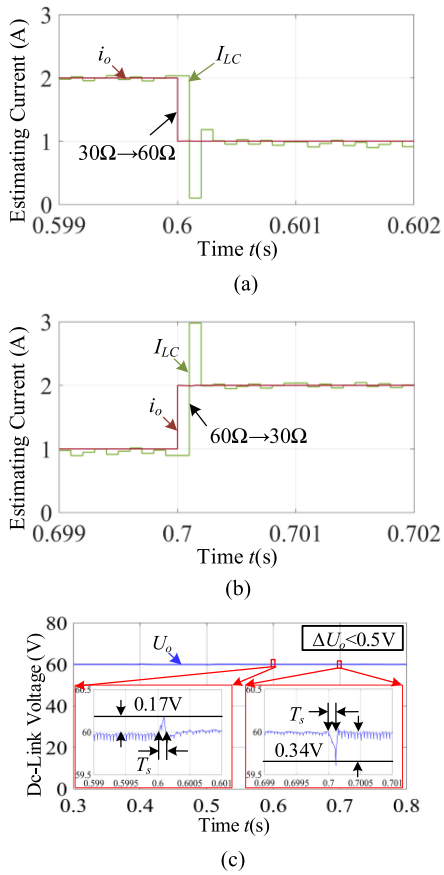

Fig. 15. Simulation results under the LCE scheme with delay compensation. (a) Estimating load current during the load-resistor increase. (b) Estimating load current during the load-resistor decrease. (c) Output voltage.

and the output-voltage disturbances with delay compensation are slightly smaller than those without delay compensation. Furthermore, when the time delay as T_s of the digital controller is considered, the corresponding simulation results can be shown in Fig. 18. As shown in Fig. 18(c), when the T_s time delay is added in the simulation model, the output-voltage waveform is very close to that without time delay. Thus, the timed delay cannot bring an obvious difference to the proposed LCE scheme with damping coefficient. Compared with Figs. 16(b), 17(c), and 18(c), the proposed LCE scheme can provide better dynamic performance for the DAB dc–dc converter.

B. Experimental Result

To further verify the effectiveness of the proposed hybrid control scheme, a dSPACE MicroLabBox DS1202 is adopted to implement the digital control, and the experimental system can be shown in Fig. 19.

Without the damping coefficient λ, the experimental result under the LCE strategy can be shown in Fig. 20, where the input voltage is equivalent to 30 V and the load resistor is equivalent to 30 Ω. As shown in Fig. 20(a), the stochastic oscillation of the phase-shift ratio D is obvious, and the desired dc-link voltage cannot be acquired as illustrated in Fig. 20(b), which is mainly caused by the measurement noise [8]. Thus, to reduce the impact of the measurement noise, the damping coefficient λ should be employed to decrease the disturbances of the phase-shift ratio. Based on this experiment platform, the max measurement noise is about 0.2 V, and $(\Delta U_o - \Delta U'_o)$ is selected as 0.4 V. Then, adopting the expected minimum estimating error ratio $r_{lc\min}$ is 0.02, the damping coefficient λ is calculated as 0.1 according to (16).

Then, when the load resistor is set to 60 Ω, Fig. 21 shows the experimental results of the SVL control, the LCE strategy without delay compensation and the LCE strategy with delay compensation. As shown in Fig. 21(a), based on the SVL control method, it always costs more than 50 ms to acquire the desired output voltage again, and the dc-link voltage disturbances are bigger than 5 V. In addition, as shown in Fig. 21(b) and (c), the excellent dynamic performance of the DAB dc–dc converter under the LCE strategy with or without delay compensation can be obtained, and the output voltage can be regarded as stable.

Moreover, when U_{in} is equivalent to 30 V and R is changed between 30 and 60 Ω, Fig. 22 illustrates the experimental result under the SVL control method. In Fig. 22, the setting time of

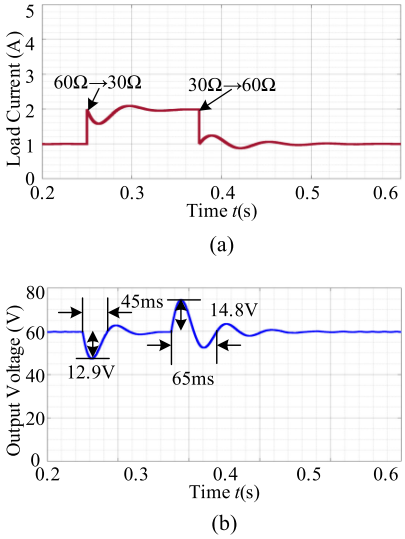

Fig. 16. Simulation results under SVL control. (a) Load current. (b) Output voltage.

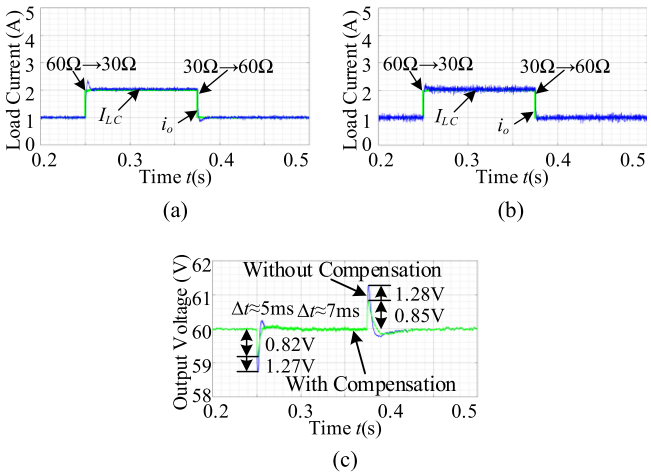

Fig. 17. Simulation results under the LCE scheme with damping coefficient. (a) Without compensation. (b) With compensation. (c) Output voltage.

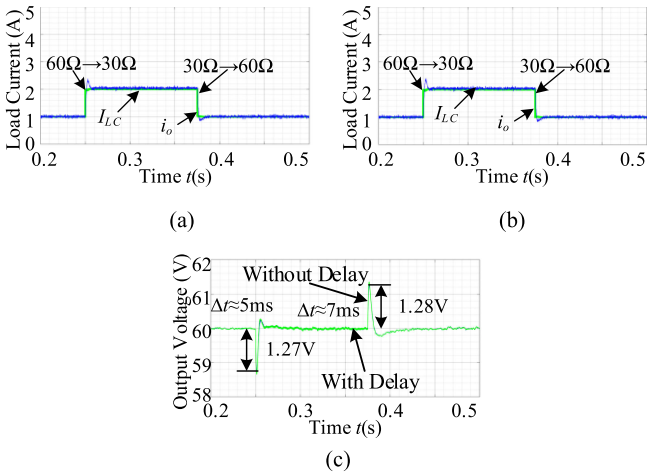

Fig. 18. Simulation results under the LCE scheme with a time delay as T_s. (a) Without time delay. (b) With time delay. (c) Output Voltage.

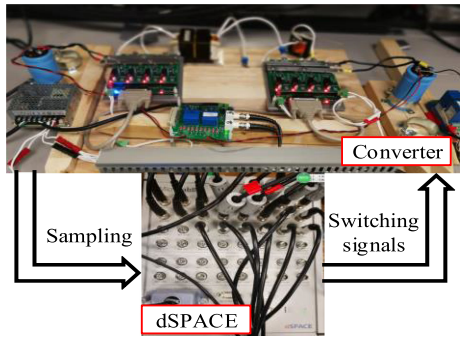

Fig. 19. Experimental system of the DAB dc–dc converter with dSPACE MicroLabBox.

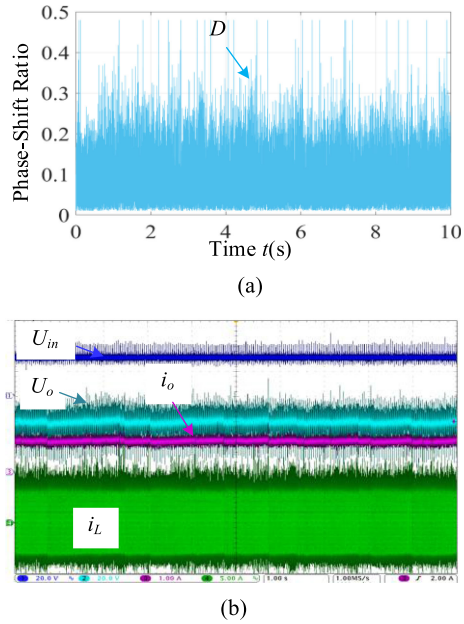

Fig. 20. Experimental results under the LCE strategy without damping coefficient. (U_{in} and U_o: 20 V/div; i_o: 1 A/div; i_L: 5 A/div; time: 1 s/div). (a) Phase-shift ratio. (b) Measured currents and voltages.

the SVL method is also bigger than 50 ms under the disturbance of load resistor, and the output-voltage disturbances are bigger than 10 V. In addition, with the same condition, the experiment results under the load-resistor disturbances by using the LCE strategy with or without delay compensation can be shown in Figs. 23 and 24, respectively.

As shown in Fig. 23(a) and (b), by using the LCE strategy without delay compensation, the dc-link voltage disturbances under the change of load resistor can be reduced to about 1 V, and the setting time for reaching the desired dc-link voltage again is about 10 ms. Then, the estimating load current I_{LC} is a little bigger than the actual load current i_o, which should be caused by the power loss [23]. Furthermore, as shown in Fig. 24, when the delay compensation method is employed, the setting time can be reduced to about 6 ms, and the disturbances of the output voltage U_o are close to 1 V. Therefore, the LCE strategy

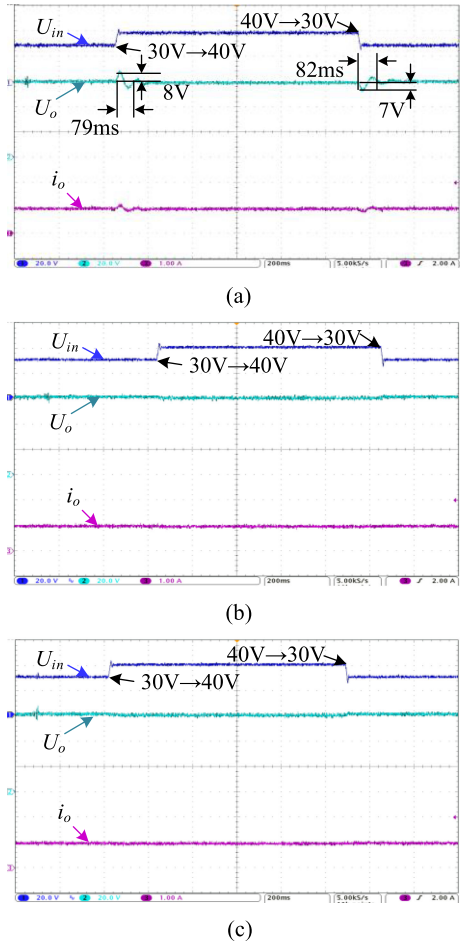

Fig. 21. Experimental results when the input voltage is changed. (U_{in} and U_o: 20 V/div; i_o: 2 A/div; time: 200 ms/div). (a) SVL control. (b) LCE scheme without delay compensation. (c) LCE scheme with delay compensation.

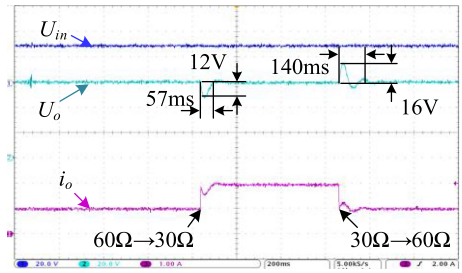

Fig. 22. Experimental results under the SVL control method when load resistor is changed. (U_{in} and U_o: 20 V/div; i_o: 1 A/div; time: 40 ms/div).

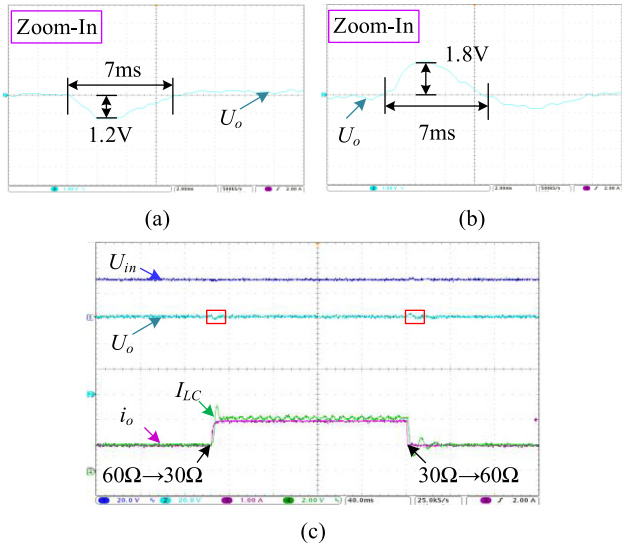

Fig. 23. Experimental results under the LCE scheme without delay compensation when load resistor is changed. (U_{in} and U_o: 20 V/div; i_o and I_{LC}: 1 A/div; time: 40 ms/div). (a) R: 60 Ω→30 Ω. (2 ms/div). (b) R: 30 Ω→60 Ω. (2 ms/div). (c) Measured currents and voltages.

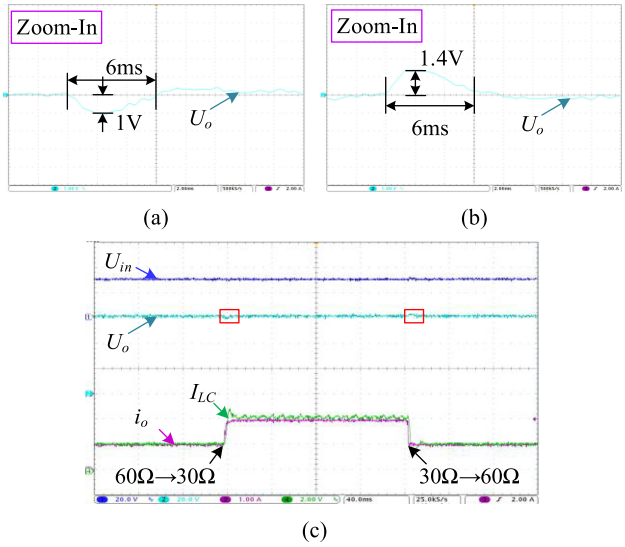

Fig. 24. Experimental results under the LCE scheme with delay compensation when load resistor is changed. (U_{in} and U_o: 20 V/div; i_o and I_{LC}: 1 A/div; time: 40 ms/div). (a) R: 60 Ω→30 Ω. (2 ms/div). (b) R: 30 Ω→60 Ω. (2 ms/div). (c) Measured currents and voltages.

with delay compensation can provide a litter better dynamic response under load-resistor disturbance, compared with the LCE strategy without delay compensation. Noteworthy, when the damping coefficient λ is closer to 1, the dynamic performance can be closer to the theoretical performance as shown in Fig. 15.

V. Conclusion

In this article, a simple LCE strategy is proposed for boosting the dynamic performance of the DAB dc–dc converter. Moreover, the inherent delay phenomenon of the estimating scheme is revealed, and to further improve the dynamic performance of the DAB dc–dc converter, a corresponding compensating method is presented. In addition, based on the error analysis with measurement noise, the potential instability of the LCE strategy is analyzed, and by adding a damping coefficient, the

instability can be easily estimated. The conducted studies are summarized as follows.

1) Compared with the SLV control method, the proposed LCE strategy can provide the fast-dynamic performance for the DAB dc–dc converter, which is very similar to the existing current sensorless control schemes. Furthermore, combining the delay compensation, better dynamic performance can be obtained.
2) Compared with the simulation result and the experimental result, the measurement noise can cause the oscillation of the output voltage under the proposed LCE strategy. In order to reduce the instability of the DAB dc–dc converter, a damping coefficient is adopted, and based on the damping coefficient, this oscillation of the output voltage can be restricted.
3) Although the damping coefficient will influence the dynamic response of the proposed original LCE scheme, the dynamic performance of this proposed method is still better than the single-voltage-loop method. With lower measurement noise, the dynamic response under the proposed method will be closer to the simulation result. Moreover, the damping coefficient will not influence the excellent dynamic response when the input voltage is changed.
4) Since the transferred current of the DAB dc–dc converter is acted as the meddle control value of the load-estimating scheme, this proposed strategy can be easily extended to other phase-shift modulation methods.

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