A High-Efficiency Dynamic Inverter Dead-Time Adjustment Method Based on an Improved GaN HEMTs Switching Model

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***Abstract*—Benefited from the fast switching speed, Gallium nitride (GaN) high electron mobility transistors (HEMTs) have been widely used in high switching frequency converters. However, due to the significant correlation between the turn-OFF time and operating conditions (more than 20 times difference of the turn-OFF time between the high load current and small load current for GaN HEMTs), using a fixed dead time will introduce extra dead-time (DT) losses in inverters where the output voltage and current are constantly varying. Therefore, this article proposes a high-efficiency adaptive method to dynamically adjust the GaN-inverter DT with operating conditions. An improved transient model including the parasitic inductance and output voltage with bidirectional solution flow has been proposed for GaN HEMTs to increase the accuracy of DT adjustment. Based on this model, the dynamic DT adjustment can be realized without extra sensors for GaN-inverters. Using the dynamic DT adjustment, the experimental results show a peak efficiency of 98.25% in a 1200 W inverter with triangular current mode modulation. Compared with using the fixed DT, the dynamic DT method can reduce the power loss by 26.7% under full load and 49.14% under light load.**

***Index Terms*—Dead-time (DT) adjustment, gallium nitride high electron mobility transistor (GaN HEMT), single-phase inverter, transient model.**

I. Introduction

With the motivation towards higher power density, the wide bandgap devices have been widely used in both academic research and industrial application [1]. Among them, GaN HEMTs have the advantages of ultralow gate charge, low output capacitor, and no reverse recovery loss, which make them excellent candidates for high-frequency applications where the switching loss is dominant. Many research articles have proposed high-frequency applications based on GaN HEMTs [2]–[4]. Qiu *et al.* [2] proposed a 600 kHz 190 W *LLC* resonant converter with an efficiency of 96%. A 1 kW 2 MHz online UPS is demonstrated in [3] achieving the 95.2% peak efficiency. In [4], a 1 MHz multi-*CLLC* bidirectional resonant converter was shown to achieve 94.3% peak efficiency.

As the switching frequency increases to the megahertz level, the dead-time (DT) loss which has been ignored in traditional low-frequency applications becomes significant in GaN-based converters. LaBella *et al.* [5] and [6] analyzed the DT loss for the GaN-based converter and acquired the optimal DT by experiment. Because the reverse conduction voltage of GaN HEMTs is much higher than Si MOSFET, setting too long DT will generate higher reverse conduction loss in GaN-based converters. Oppositely, short-circuit will happen when the DT is insufficient. As for the loss introduced by the short-circuit, it is estimated by the energy used to charge/discharge the output capacitance in [5]. However, during the short-circuit, worse "cross-talk" has been observed, which may induce the false turn-ON with huge extra loss. Hence, the effect of insufficient DT is much more serious than mentioned in the previous literature.

As analyzed above, both the redundant and insufficient DT will induce extra DT loss. Thus, using the optimal DT adaptive to the turn-OFF time can benefit to high efficiency. However, the turn-OFF time of GaN HEMTs strongly depends on the operating condition, such as topologies, output current (I_o), input voltage (V_i), and output voltage (V_o). As presented in [7], the turn-OFF time of GaN HEMTs will drop from hundreds to several nanoseconds as the turn-OFF current (I_{off}) rise from 1 A to the rated current. Hence, the optimal DT is matched to the specific operating condition. To minimizing the DT loss, the DT needs to be adjusted dynamically.

In [8]–[21], the high-speed values, such as the drain-source voltage v_{ds} (or dv_{ds}/dt) and gate-source voltage v_{gs}, are sensed and processed by the analog circuit to guide the DT adjustment. Chen *et al.* [8]–[13] proposed the dynamic DT adjustment methods based on the body diode conduction detection (DDCD), where the detectors need to withstand the maximum supply voltage in the power converter. To simplify the detector, Grezaud *et al.* [14] proposed a method based on the detection of the cross-talk voltage on v_{gs}, which is induced by dv_{ds}/dt. However, only sense dv_{ds}/dt, the method will induce extra loss when v_{ds} rises to the turn-OFF voltage (V_{off}) before v_{gs} falls below the threshold voltage (V_{th}). Zhang *et al.* [15] used both v_{gs} and v_{ds} signal, so the DT can be adjusted appropriately whether v_{ds} rises to V_{off} first or v_{gs} falls below V_{th} first. The most practical

Manuscript received March 2, 2021; revised July 7, 2021; accepted September 6, 2021. Date of publication September 16, 2021; date of current version November 30, 2021. This work was supported by the National Natural Science Foundation of China under Grant 52077094. Recommended for publication by Associate Editor M. Nawaz. (*Corresponding author: Cai Chen.*)

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3112694.

Digital Object Identifier 10.1109/TPEL.2021.3112694

and widely used methods for the DT control of *LLC* synchronous rectification are based on DDCD too [16]–[18]. As mentioned in Fu *et al.* [19]–[21], the parasitic inductance will make the turn-OFF signal arrive early, so they proposed improved methods to reduce the effect of the parasitic inductance.

Although the methods based on high-speed values can provide high accuracy and response speed, these methods need complex detection-related circuits because of the nanoseconds-level switching speed of GaN HEMTs and the effect of parasitic inductance. Besides, for inverters, both the upper-side and the lower-sides transistors may work as the active transistor. If using the midpoint voltage for the DT adjustment of both the upper and lower, a high voltage auxiliary power supply is needed to generate the comparison voltage used for DDCD. If using two detectors for the upper and lower, respectively, additional galvanic isolation devices are required. These additional circuits used to sense or process the high-speed values will increase the system volume and cost, and reduce the power density.

Yousefzadeh *et al.*[22] and [23] proposed the strategies of dynamic DT control for dc/dc converters based on maximum efficiency point tracking (MEPT), where the DT is continuously adjusted in a loop to meet the maximum efficiency point. Because the MEPT-based methods only need to detect V_o which is sensed for the closed-loop dc voltage regulation, these methods can be called sensor-less methods. However, these strategies have the drawback of slow transient response. For inverters where V_o is continuously changing, the DT loss is still obvious, especially in high-frequency applications.

Another kind of method is using a mathematic model to calculate the DT based on the low-speed value such as V_i, and $I_{\rm off}$ [24]–[33]. Accordingly, the accuracy of the mathematic model will directly affect the DT adjustment. Hayama *et al.* [24] and [25] calculated the DT through the expression ($2 * V_i * C_{\rm oss}$ / $I_{\rm off}$), where $C_{\rm oss}$ is the output capacitance. This expression is simple and easy to realize but inaccurate. Han *et al.* [26] and [27] proposed more accurate analytical models based on the detailed analysis of the switching transient. Teng *et al.* [28] has improved the previous works [29] and proposed a segmented analytical model for the phase-shift full-bridge converters.

However, to acquire the analytical expression for the desire DT, Hayama *et al.* [24]–[29] have to ignore the parasitic inductance, the nonlinearity of the junction capacitance, and the coupling effect of the power loop and gate loop, which will reduce the accuracy at large $I_{\rm off}$. Besides, the current of the output filter inductance (I_L) is regarded as constant during the turn-OFF process, which will reduce the accuracy at light $I_{\rm off}$. Compared with the analytical DT model, the transient model based on numerical solution shows higher accuracy [30]–[33]. Ahmed *et al.* [30] proposed the transient model to evaluate the switching loss of SiC devices, and Zhang *et al.* [31] and [32] improved it for GaN HEMTs for the DT calculation. Xie *et al.* [33] proposed an improved transient model to analyzed the ultralow turn-OFF losses phenomenon of SiC MOSFETs. However, in [31], the parasitic inductance is ignored. In [30], [32], and [33], I_L is handled as a constant current source during the turn-OFF process like the analytical methods. For inverters, the transistors may work in the Buck or Boost condition, where V_o and the output filter inductance also have significant effects on the DT. Besides, the previous transient models used the unidirectional solution flow. However, the parasitic inductance will induce oscillation in $v_{\rm gs}$. When $v_{\rm gs}$ resonates above $V_{\rm th}$ again, the false turn-ON happens and the desired DT will increase. The unidirectional solution flow cannot reflect the false turn-ON, which may cause an insufficient DT. Therefore, the previous transient models need to be improved to increase the accuracy of DT calculation for inverters.

Even though the optimal DT can be calculated from the mathematic models, how to apply it to practical applications is important, especially in inverters where I_L and V_o are continuously varying. In these mathematic models, $I_{\rm off}$ is used to calculate the DT. However, when $I_{\rm off}$ is acquired by directly detect I_L, the detection delay caused by the propagation delay and response time of the current sensor will induce error in the DT adjustment because of the current ripple of I_L. A parasitics-based current measurement method is proposed in [32], where $I_{\rm off}$ is directly detected by the sense resistor. This strategy can cancel the effect of the parasitic inductance of the sense resistor, but cannot cancel the effect of detection delay. Recently, more and more MHz-level GaN converters with ultra-small filter inductance have been proposed for high power density [34]–[36]. For these converters, it is hard to accurately detect $I_{\rm off}$ every switching cycle and the error caused by the detection delay is more serious. Zhang *et al.* [31] proposed a strategy based on the zero-cross point detection of I_L, which can reduce the error caused by the detection delay. However, this strategy is specific for the converters under triangular current mode modulation [37] (TCM), which requires I_L to cross 0 A every switching cycle. Therefore, a more accurate and effective DT adjustment strategy is needed for high-frequency GaN inverters with small filter inductance.

This article designs to proposed a high-efficiency dynamic DT adjustment method for high-frequency GaN-based inverters. Due to the complex detector of the high-speed value based methods and low response speed of the MEPT-based methods, the proposed method is based on the mathematic model, where the DT is calculated from the low-speed signals which are usually detected for the closed-loop regulation of the inverter. The rest of this article is organized as follows. In Section II, an improved transient model is proposed to acquire more accurate DT. Using the proposed model, the effect of the gate driver, output parameters, and parasitic inductance on the DT is analyzed. According to the results, some parameters ignored by the previous literature also influence the DT significantly. Besides, a short-circuit mode is added in the transient model to analyze the "cross-talk" caused by the insufficient DT short-circuit. In Section III, the specific control strategy for GaN-based single-phase inverters is proposed, where an equivalent method is proposed to implement the proposed model under the bipolar modulation. By detecting the output current, this method can be implemented in both high and small inductance current ripple applications. In Section IV, a 1.2 kW GaN HEMTs based inverter is built to verify the feasibility and effectiveness of the proposed dynamic DT control. Finally, Section V concludes this article.

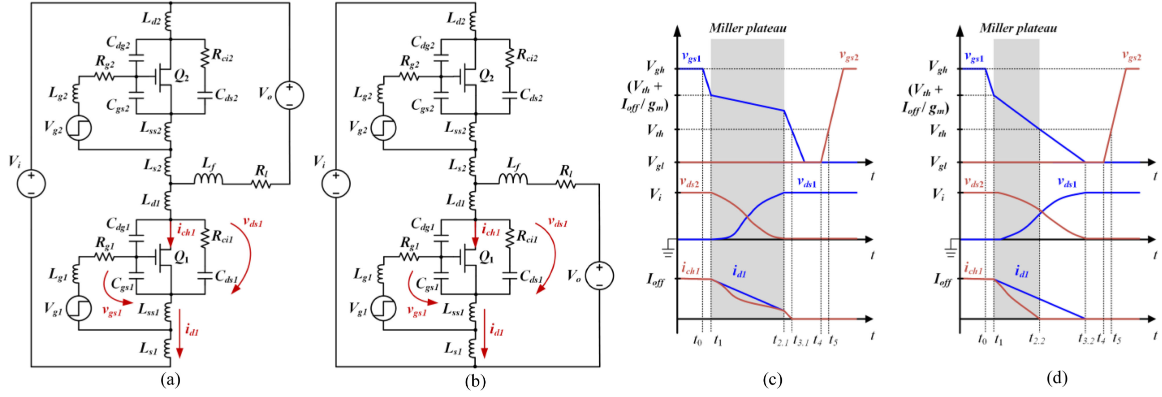


Fig. 1. (a) Equivalent circuit for the buck condition. (b) Equivalent circuit for the boost condition. (c) Waveforms for the final condition 1. (d) Waveforms for the final condition 2.

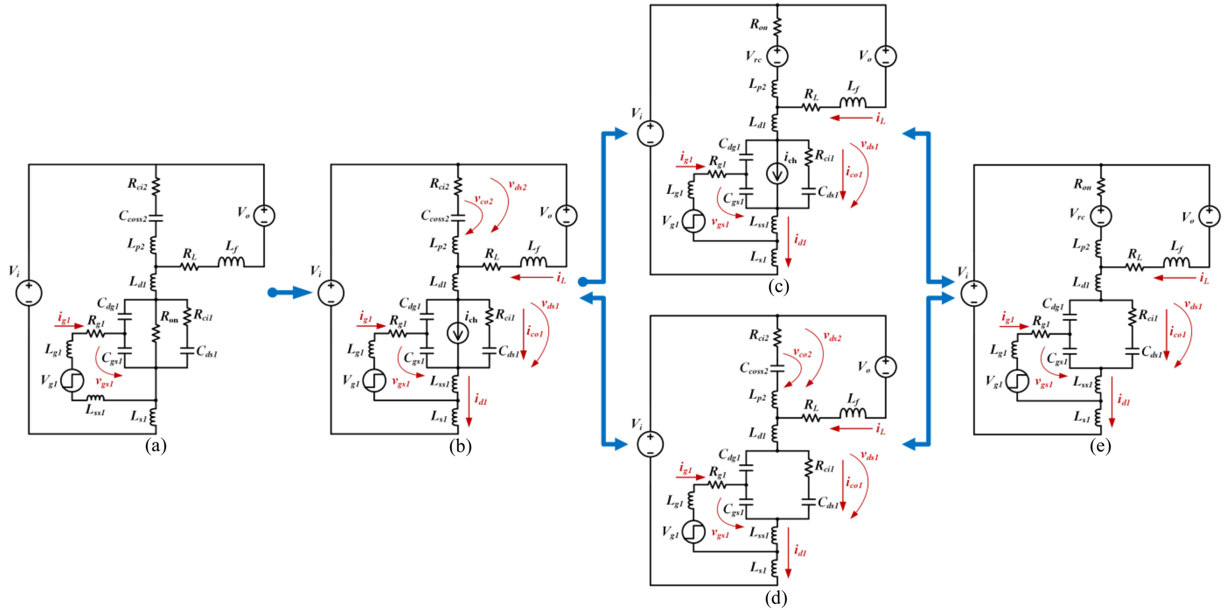


Fig. 2. Turn-OFF transients of GaN HEMTs. (a) $t_0 - t_1$: gate delay period. (b) $t_1 - t_{2.1}$ or $t_{2.2}$: voltage rising period. (c) $t_{2.1} - t_{3.1}$: current falling period. (d) $t_{2.2} - t_{3.2}$: C_{oss} charging period. (e) $t_3 - t_4$: parasitic resonating period.

II. Proposed Transient Model for DT Optimization

A. Turn-Off Transient Model for GaN HEMTs

To canceling the complex detectors, a mathematical model is needed to calculate the optimal DT from the low-speed value, such as the output voltage V_o and turn-OFF current I_{off}. Since the optimal DT is mainly dependent on the turn-OFF time of the device, precisely describing the turn-OFF process of the devices is the key to accurately obtain the optimal DT. Because the analytical models [24]–[29] cannot reflect the parasitic inductance, the nonlinearity of the junction capacitance, and the coupling effect of the power loop and gate loop, this article uses the transient model [30]–[33] for the DT calculation. However, the previous transient models are established based on the typical dual-pulse test (DPT) circuit with the unidirectional solution flow. Therefore, an improved turn-OFF transient model is established in this article for higher calculation accuracy.

The transient model is based on the schematic and simplified transient waveforms depicted in Fig. 1. In inverters, the transistors may work in the buck or boost condition shown in Fig. 1(a) and (b), which are decided by the operation condition. The GaN HEMTs Q_1 and Q_2 are represented by an ideal HEMT with the gate-source capacitance, gate-drain capacitance, and drain-source capacitance (C_{gs}, $C_{gd,}$ and C_{ds}). As claimed in [38], when charged and discharged, the nonlinear junction capacitor of GaN HEMTs consumes energy. Therefore, an equivalent resistor R_{ci} in series with C_{ds} is used to represent the capacitors-related loss as shown in Fig. 1(a) and (b). The gate stray inductance, drain stray inductance, source stray inductance, and the common-source inductance are represented as L_g, L_d, L_s, and L_{ss} in the equivalent circuit. For a particular circuit, the parasitic inductance can be extracted by Q3D simulation. Take the Buck condition as an example, the equivalent circuits for each mode are presented in Fig. 2. The details of transient modes for the active transistor Q_1 are as follows.

1) Mode 0 (Before t_0): Conduction State: The gate driver voltage V_{g1} is still the turn-ON gate drive voltage V_{gh}, and Q_1 is conducting. The inductance current i_L flows through the channel of Q_1, and the drain-source voltage of Q_1 (v_{ds1}) is $i_L * R_{on}$ where R_{on} is the ON-resistance of Q_1. The current of the filter inductor (L_f) at t_0 is defined as the turn-OFF current I_{off}.

2) Mode1 ($t_0 - t_1$): Gate Delay Period: At t_0, V_{g1} goes to the turn-OFF voltage V_{gl}. During this period, Q_1 is still ON conduction, and Q_2 is blocked. Therefore, Q_1 is regarded as a resistance R_{on}, and Q_2 is regarded as the output capacitor C_{oss2}. Although the gate-changing current i_{g1} induces the inductive voltage in the common inductor L_{ss1}, its effect on the power loop is ignorable. Therefore, to accelerate the solving speed, L_{ss1} can be moved into the gate loop to decouple the power and gate. Based on the equivalent circuit as shown in Fig. 2(a), (1) and (2) are derived to express the gate–source voltage (v_{gs1}), and the gate current (i_{g1}) of Q_1

$$v_{gs1} = V_{gl} - i_{g1}R_{g1} - (L_{g1} + L_{ss1})\frac{di_{g1}}{dt} \tag{1}$$

$$i_{g1} = C_{\rm gs1}\frac{dv_{\rm gs1}}{dt} + C_{\rm gd1}\frac{dv_{\rm gd1}}{dt}. \tag{2}$$

The state equations T1, which is shown in the appendix, are derived to solve the gate delay period in MATLAB with the initial conditions: $v_{gs1} = V_{gh}$ and $i_{g1} = 0$. The gate delay period ends when v_{gs1} falls to ($V_{\rm th} + I_{\rm off} / g_m$), where g_m is the transconductance and $V_{\rm th}$ is the threshold voltage. It's worth noting that g_m is a variate influenced by v_{gs}, which can be calculated from the $i_d_v_{gs}$ curve on the datasheet.

3) *Mode* 2 ($t_1 - t_2$): *Voltage Rising Period*: After v_{gs1} falls below ($V_{\rm th} + i_L / g_m$), The channel of Q_1 can be regarded as a current source controlled by v_{gs1}. As the channel current of Q_1 ($i_{\rm ch}$) decreases, i_L flows into the output junction capacitors of Q_1 and Q_2, which results in the rise of $v_{\rm ds1}$. Meanwhile, the commutation of the drain current of Q_1 and Q_2 generates the inductive voltage in the parasitic inductors. Therefore, the gate loop and power loop are coupled, and the equivalent circuit is derived as Fig. 2(b). Equations (3)–(8) are derived to describe the voltage rising period, where i_{d1} is the drain current of Q_1, i_{co1} is the charge current of $C_{\rm ds1}$, v_{co2} is the voltage drop of $C_{\rm ds2}$, i_L is the current of filter inductance, $L_{p1} = L_{d1} + L_{ss1} + L_{s1}$, and $L_{p2} = L_{d2} + L_{ss2} + L_{s2}$

$$V_i - V_o = v_{\rm ds1} + L_{p1}\frac{di_{d1}}{dt} + i_L R_L + L_f\frac{di_L}{dt} \tag{3}$$

$$i_{co1} = C_{\rm ds1}\left(\frac{dv_{\rm ds1}}{dt} - R_{ci1}\frac{di_{co1}}{dt}\right) \tag{4}$$

$$V_i = v_{\rm ds1} + v_{co2} + (L_{p1} + L_{p2})\frac{di_{d1}}{dt} - L_{p2}\frac{di_L}{dt} + R_{ci2}(i_{d1} - i_L) \tag{5}$$

$$\frac{dv_{co2}}{dt} = \frac{1}{C_{\rm oss2}}i_{d1} - \frac{1}{C_{\rm oss2}}i_L \tag{6}$$

$$v_{gs1} = V_{gl} - i_{g1}R_{g1} - (L_{g1} + L_{ss1})\frac{di_{g1}}{dt} - L_{ss1}\frac{di_{d1}}{dt} \tag{7}$$

$$i_{d1} = g_m(v_{\rm gs1} - V_{th}) + i_{co1} + C_{\rm gd1}\left(\frac{dv_{\rm ds1}}{dt} - \frac{dv_{\rm gs1}}{dt}\right). \tag{8}$$

The state equations T2, which is shown in the appendix, are derived from (2)-(8) to solve the voltage rising period in MATLAB. The initial conditions are listed as the following: $v_{\rm ds1} = i_L * R_{\rm on}$; $i_{d1} = I_{\rm off}$; $i_{co1} = 0$; $v_{co2} = (V_i - i_L * R_{\rm on})$; $i_L = I_{\rm off}$; v_{gs1} and i_{g1} are the final values of the gate delay period. As proposed in [8], the voltage rising period will enter two different modes depending on which of the following final conditions is met first: The final condition 1 ($t_{2.1}$): The voltage drop of $C_{\rm ds2}$ and R_{ci2} ($v_{\rm ds2}$), which is calculated by $v_{co2} + R_{ci2} * (i_{d1}$ - $i_L)$, falls below the reverse conduction voltage of GaN HEMTs (V_{rc}) which is calculated by (- $V_{\rm th} + V_{gl} + R_{\rm on}*(i_{d1}$ - $i_L)$); The final condition 2 ($t_{2.2}$): $v_{\rm gs1}$ falls below $V_{\rm th}$.

4) Mode 3.1 ($t_{2.1} - t_{3.1}$): *Current Falling Period for the Final Condition* 1: After $v_{\rm ds2}$ falls below V_{rc}, Q_2 conducts reversely. Therefore, Q_2 can be regarded as a voltage source V_R in series with $R_{\rm on}$ as shown in Fig. 2(d), where V_R is (- $V_{\rm th} + V_{gl}$). Since v_{gs1} has not fallen below $V_{\rm th}$, Q_1 is still the controlled current source. Based on the equivalent circuit, (9) is derived to replace (5)

$$V_i = v_{\rm ds1} + (L_{p1} + L_{p2})\frac{di_{d1}}{dt} + V_R + R_{\rm on}(i_{d1} - i_L) - L_{p2}\frac{di_L}{dt}. \tag{9}$$

The state equations T3, which is shown in the appendix, are derived from (2)–(4), and (6)–(9) to solve the current falling period. the initial conditions $v_{\rm gs1}$, i_{g1}, $v_{\rm ds1}$, i_{d1}, i_{co1}, and i_L are the final value of the voltage rising period. After $v_{\rm gs1}$ falls below $V_{\rm th}$, Q_1 is fully turned OFF, and this period ends.

5) Mode 3.2 ($t_{2.2} - t_{3.2}$): $C_{\rm oss}$ Charging Period for the Final Condition 2: After v_{gs1} falls below $V_{\rm th}$, the channel of Q_1 has been fully blocked and the equivalent circuit is shown in Fig. 2(d). In the previous model, the discussed circuit is the typical DPT circuit, and L_f is regarded as a constant current source, so the C_{oss} charging period tends to infinity when $I_{\rm off}$ tends to 0. In practice, as (V_i - V_o - $v_{\rm ds1}$) is implemented on L_f, i_L rises and discharges the output capacitance. Whether v_{co2} can be discharged to V_{rc} depends on V_i, V_o, L_f, and i_L. To acquire more accurate results, V_o and L_f are added to the proposed model. Based on the equivalent circuit, the $C_{\rm oss}$ charging period can be described as T2 by setting g_m to 0. This period ends when v_{co2} falls below V_{rc} to force Q_2 to conduct reversely.

6) Mode 4 ($t_{3.1}$ or $t_{3.2}$–): Parasitic Resonating Period: Before this period, Q_1 has been fully turned OFF and Q_2 conducted reversely. As shown in Fig. 2(e), the junction capacitance resonates with the parasitic inductance in this period, which will generate an overshoot on $v_{\rm ds1}$. During this process, the energy stored in the parasitic inductance dissipates in the resistance of the power loop. According to the equivalent circuit, the parasitic resonating period can be described as T3 by setting g_m to 0.

Through the above process, the state equations for the Buck condition have been established. The state equations for the Boost condition are similar to the Buck, which can be acquired

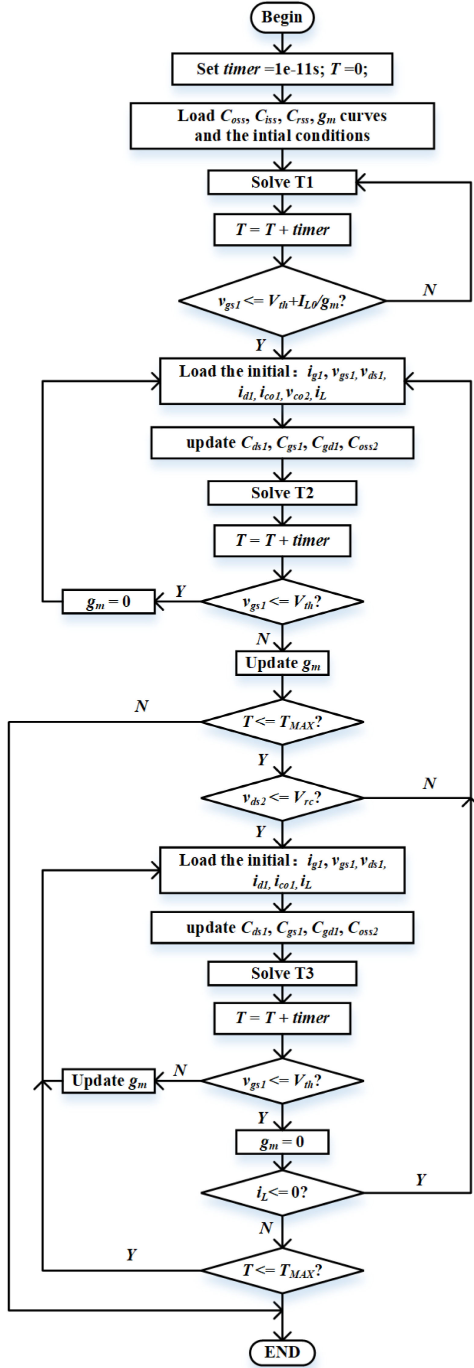


Fig. 3. Solution flow chart in MATLAB.

through replacing (5)

$$V_o = v_{\mathrm{ds1}} + L_{p1}\frac{di_{d1}}{dt} + i_L R_L + L_f\frac{di_L}{dt}. \tag{10}$$

For GaN HEMTs, the junction capacitance and g_m are nonlinear, so these state equations are nonlinear. Therefore, they are numerically solved in a loop within an interval that is short enough to regard them as linear. Fig. 3 illustrates the solution flow in MATLAB. At the first, the curves of C_{ds}-v_{ds}, C_{gd}-v_{ds}, C_{gs}-v_{ds}, and g_m-v_{gs} are loaded into the program. After one

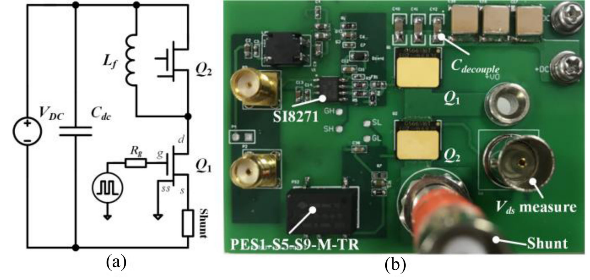


Fig. 4. (a) Schematic of the DPT circuit. (b) Prototype of DPT circuit.

TABLE I
PARASITIC PARAMENTS OF DPT CIRCUIT

Part.	Value	Part.	Value
Q_1, Q_2	GS66516T	Gate driver	Si8271
V_{DC}	400V	V_{gh}	6V
V_{gl}	-3V	V_{th}	1.5V
R_{dson}	0.025Ω	R_{ci}	0.6Ω
$R_g + R_{gin}$	(2+0.34)Ω	R_L	0.016Ω
$L_g + L_{gin}$	(3.7+3.1)nH	L_{p1}	3.1nH
L_{p2}	1.7nH	$L_{ss} + L_{ssin}$	(0.03+0.15)nH
V_o	0V	L_f	150uH

interval, C_{ds}, C_{gd}, C_{gs}, and g_m are updated based on the final conditions. Compared with the previous works, the solution process is improved as follows: v_{gs} is oscillating during the turn-OFF process because of the parasitic inductance. The resonance will introduce the false turn-ON when v_{gs} resonates above V_{th}. The previous transient models cannot reflect the false turn-ON because the solution flow is unidirectional. In the proposed model, the solution flow from the C_{oss} charging period to the voltage rising period and the parasitic resonating period to the current falling period are bidirectional. When v_{gs1} resonates above V_{th}, the solving process returns to the previous mode to reflect the false turn-ON. When $V_o > 0.5{*}V_{\mathrm{DC}}$, v_{ds1} cannot rise above V_{DC} when I_{off} is not enough. Therefore, an upper limit of the solution time $T_{\max}$ is set to avoid the program falling into an infinite loop. After Q_2 conducts reversely, the negative voltage (V_{DC} - v_{ds1} -V_o) is applied on the filter inductor, which will force i_L to decline. When i_L falls to 0, Q_2 stops conducting reversely, and v_{ds1} begins to resonate with L_f again. To reflect this phenomenon, when i_L falls below 0 in the parasitic resonance period, the solution flow returns to the C_{oss} charge period in the proposed model.

A DPT circuit as shown in Fig. 4 is established to verify the proposed model. The GaN HEMTs are driven by Si8271 from Silicon Laboratories. The drain current i_d is measured by a 10 mΩ shunt SSDN-10 from T&M Research Products. The waveforms are recorded by a 1GHz Lecroy oscilloscope with PP018 passive probes. The related paraments of the DPT circuit are given in Table I, where the parasitic parameters are extracted by Q3D simulation. The internal gate resistance ($R_{gin} = 0.34$ Ω) is read from the datasheet. The internal common-source inductance ($L_{ssin} = 0.15$ nH), and the internal gate inductance ($L_{gin} = 3.1$ nH) is read from the Ltspice model provided by the manufacturer.

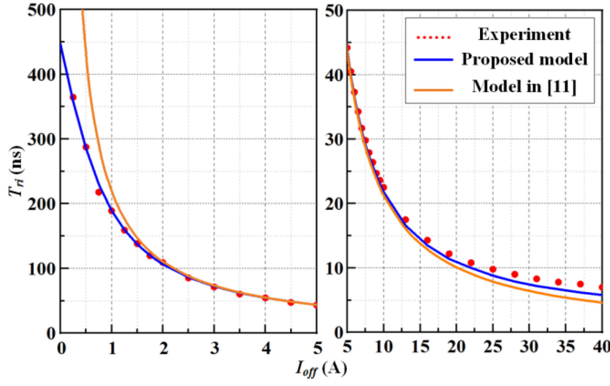


Fig. 5. T_{ri} acquired by the experiment, proposed model, and analytical model in [7] with different I_{off}.

The time taken for v_{ds1} to rise from the on-voltage to V_{DC} (T_{ri}) can be directly read from the results of DPT, which corresponding to (t_1 to $t_{2.1}$) or (t_1 to $t_{3.2}$) in the proposed transient model. To verify the proposed model, T_{ri} acquired by the experiment and the transient model are shown in Fig. 5. Besides, the results calculated by the analytical model as (11) [26] are also listed for comparison

$$T_{ri} = \left(2Q_{\mathrm{oss}}|_0^{V_{\mathrm{DC}}} - R_g C_{iss} V_{th} g_m \ln((V_{th} + I_{\mathrm{off}}/g_m)/V_{th})\right)/I_{\mathrm{off}}. \tag{11}$$

As we can see from Fig. 5, the analytical model can fit well with the experiment in the middle section. However, as I_{off} increases or decreases, the difference between the analytical model and experiment increases. As for the proposed transient model, because it can reflect the resonance process between the junction capacitors and L_f, T_{ri} acquired by the proposed model can fit well with the experiment at small I_{off}. At large I_{off}, the effect of the power loop on the gate loop gets considerable. Larger I_{off} will lead to higher charge current through C_{gd} and higher induced voltage on L_{ss}, both of which will slow down the falling speed of v_{gs}. Since the proposed model includes the parasitic inductors and junction capacitors, it can reflect the coupling effect between the power loop and gate loop. Therefore, T_{ri} acquired by the proposed model is more accurate at large I_{off}. Further more, the experiment and simulation waves of v_{ds} and i_{ds} at 40 A and 2 A I_{off} are compared in Figs. 6 and 7. Since the transient model can reflect the effect of the parasitic inductance, as the results show, the proposed model can fit well with the experiment waveforms at both large and small currents, which means this model can acquire the relatively accurate DT under the influence of parasitic inductance.

The optimal DT used after the active transistor Q_1 is turned OFF ($\mathrm{ODT_a}$) is ($t_{3.1}$ or $t_{3.2} - t_0 - t_5 + t_4$), where ($t_{3.1}$ or $t_{3.2} - t_0$) can be directly acquired from the proposed turn-OFF transient model and ($t_5 - t_4$) is the turn-ON gate delay period of Q_2. After $t_{3.1}$ or $t_{3.2}$, Q_1 has been fully turned OFF, and then Q_2 is turned ON at t_4. Since Q_2 conducts reversely, v_{ds2} only falls from the reverse conducting voltage to the ON-voltage, and i_{d2} is almost unchanged. Therefore, the effect of the power loop on the gate loop can be ignored and the turn-ON gate delay period of Q_2 can

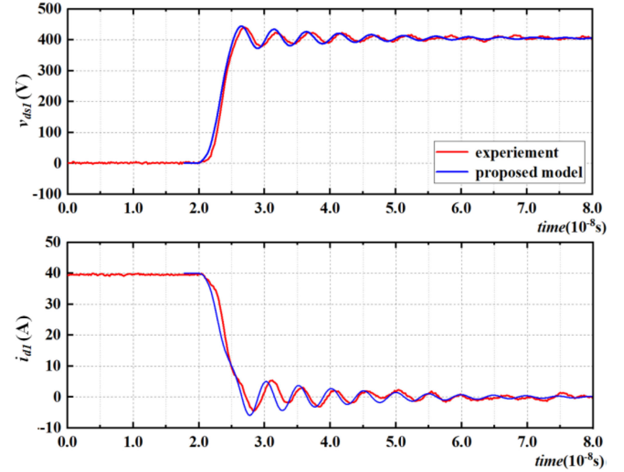


Fig. 6. Experiment and simulation waveforms at 40 A I_{off}.

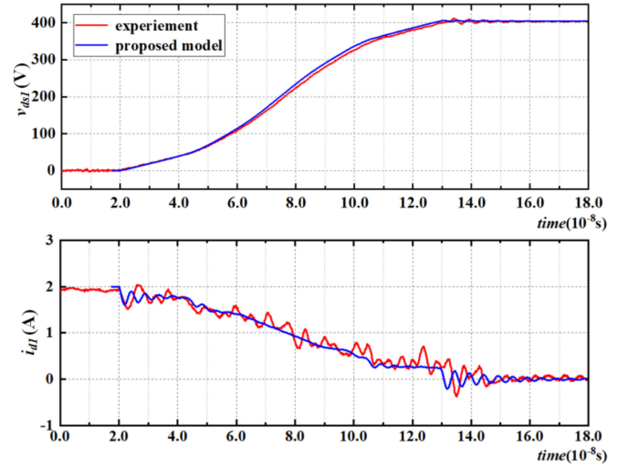


Fig. 7. Experimental and simulation waveforms at 2 A I_{off}.

be regarded as the charging process for the input capacitance of Q_2 (C_{iss2}). Equations (12) and (13) are derived to described this period with the initial condition: $v_{\mathrm{gs2}} = V_{gl}$ and $i_{g2} = 0$. This period ends when v_{gs2} rises to V_{th} to turn-ON the channel of Q_2

$$v_{\mathrm{gs2}} = V_{gh} - i_{g2}R_{g2} - (L_{g2} + L_{ss2})\frac{di_{g2}}{dt} \tag{12}$$

$$i_{g2} = C_{iss2}\frac{dv_{\mathrm{gs2}}}{dt}. \tag{13}$$

As for the optimal DT used after the freewheeling transistor Q_2 is turned OFF (ODT_f), it is equal to the turn-OFF time of Q_2 minus the turn-ON gate delay time of Q_1. Ignoring the effect of the power loop on the gate loop, the turn-OFF process of Q_2 can be described by (13) and (14) with the initial condition: $v_{\mathrm{gs2}} = V_{gh}$ and $i_{g2} = 0$. This period ends when v_{gs2} falls to V_{th}. The turn-ON gate delay period of Q_1 is similar to Q_2, which can be calculated by (12) and (13). Since these two periods are hardly affected by v_i, v_o and i_L, a constant DT can be used for ODT_f

$$v_{gs2} = V_{gl} - i_{g2}R_{g2} - (L_{g2} + L_{ss2})\frac{di_{g2}}{dt}. \tag{14}$$

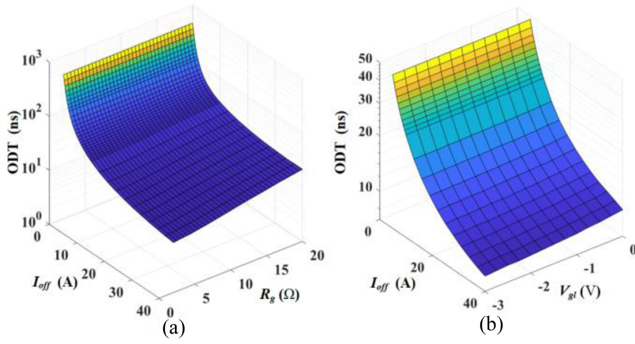


Fig. 8. ODT at different I_{off}. (a) With varying R_g. (b) With varying V_{gl}.

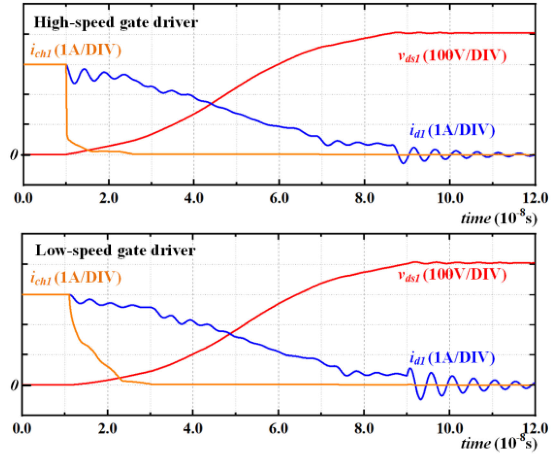


Fig. 9. Simulation waveforms at $I_{\text{off}} = 3$ A with high-speed gate driver ($R_g = 2\ \Omega$ and $V_{gl} = -3$ V) and low-speed gate driver ($R_g = 10\ \Omega$ and $V_{gl} = 0$ V).

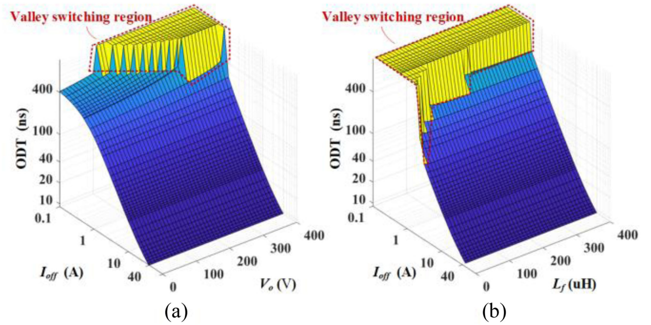


Fig. 10. (a) ODT with varying V_o at different I_{off}. (b) ODT with varying L_f at 300 V V_o.

As mentioned above, the proposed turn-OFF transient model can not only provide a more accurate optimal DT but also simulate the turn-OFF transient waveforms well. Hence, the proposed model can be used instead of DPT to analyze the effects of circuit parameters on the turn-OFF process and optimal DT, which can save the designer lots of work. Because of the introduction of the buck and boost operating condition, it is easy to apply the proposed model to converters constructed by the half-bridge structure.

B. Analysis About the Effects of the Circuit Parameters on DT

In the previous studies for the DT optimization, the effects of I_{off} and V_i have been considered in particular. However, little work has analyzed the effects of other circuit parameters such as the gate parameters (R_g and V_{gl}), the output parameters (V_o and L_f), and the stray inductance (L_{ss}, L_g, and L_p). Thanks to its good fit to the turn-OFF transient waveform, the proposed model can be used to analyze the effect of these parameters intuitively. The following section will take ODT$_a$ as an example to analyze the effects of these circuit parameters. Except for the parameter being discussed, the others are the same as Table I.

First, the effects of the gate parameters are analyzed. Fig. 8(a) and (b) shows ODT with different R_g and V_{gl}. At large I_{off}, the effect of the gate parameters is obvious. Increase the gate drive speed (decrease R_g and V_{gl}) can significantly decrease ODT. This is because using more negative V_{gl} or smaller R_g can provide higher -i_g, which can accelerate the decrease of v_{gs}. Since the channel current i_{ch} decreases as v_{gs} decreases, using more negative V_{gl} or smaller R_g can make the current flows into two C_{oss} more quickly, which can accelerate the rise of v_{ds}. However, as I_{off} decrease, the effect of gate parameters gets smaller. When I_{off} is smaller than 3 A, the effect of gate parameters on ODT is ignorable. To explain this phenomenon, the waveform of i_{d1}, v_{ds1}, and i_{ch1} at 3 A I_{off} with a low-speed gate driver ($R_g = 10\ \Omega$, $V_{gl} = 0$ V) and high-speed gate driver ($R_g = 2\ \Omega$, $V_{gl} = -3$ V) simulated by the proposed model are shown in Fig. 9. As analyzed above, the gate paraments affect the rising speed of v_{ds} through i_{ch}. As i_{ch} declines, the current used to charge C_{oss1} and C_{oss2} increases, which can be expressed as $(i_L - i_{ch1})$. When the device is turned OFF at a small I_{off}, although increasing the gate drive speed will accelerate the decline speed of i_{ch1}, it takes a long time for i_L to charge the output capacitance to V_{DC} even if i_{ch1} falls to 0. Since the C_{oss} charging period dominates ODT at small I_{off}, the effect of v_{gs} becomes negligible. Therefore, enhancing the gate driver capability cannot effectively reduce the needed DT at small I_{off}. For converters that may operate at the small current region, the problem of DT cannot be solved by adjusting the gate drive speed.

Besides, V_{gl} will affect the reverse conduct voltage V_{rc}. Using more negative V_{gl} will lead to more negative V_{rc}, and then affect the turn-OFF voltage of the active transistors which can be expressed as ($V_i - V_{cr}$). For devices used in high-voltage applications, such as 650V GS66516T, compared with V_i, V_{cr} is ignorable, so this effect is ignorable too.

As for the output paraments, ODT at different V_o is shown in Fig. 10(a). Unlike the gate parameters, V_o makes difference at small I_{off}, but has little effect at large I_{off}. At large I_{off}, i_L can be regarded as a constant current source, so the effect of output parameters can be ignored. However, at small I_{off}, the fluctuation of i_L cannot be ignored. Because i_{ch} falls to 0 very quickly, the C_{oss} charging period can be approximate to the resonance process between L_f, C_{oss}, and V_o. Therefore, V_o affects the turn-OFF time significantly at small I_{off}. As we can

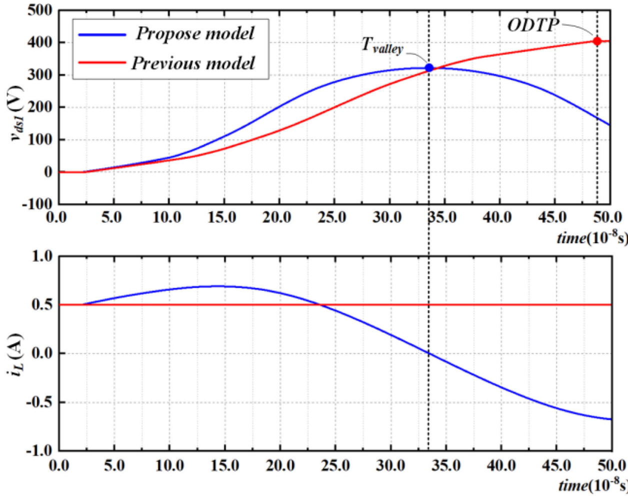


Fig. 11. Simulation waveforms of v_{ds1} and i_L at 300 V V_o / 0.5A I_{off} / 40 uH L_f acquired the proposed model and the previous model.

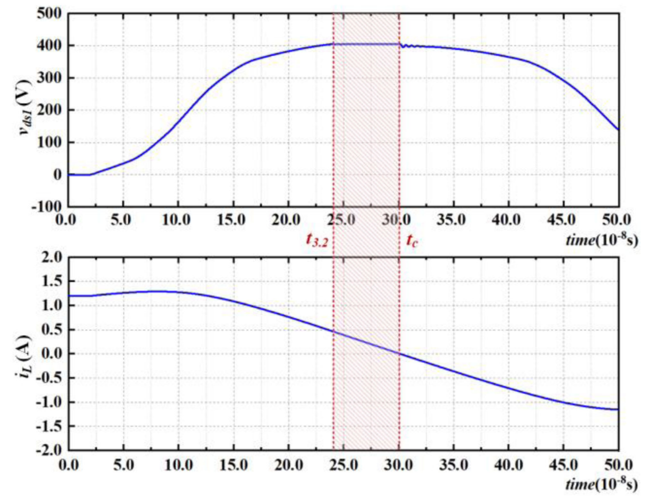


Fig. 12. Waveforms of v_{ds1} and i_L at 300 V V_o / 1.2 A I_{off} / 40 uH L_f.

see from Fig. 10(a), ODT increases as V_o rises. Then, when V_o rises above $0.5{*}V_o$ and I_{off} is below a critical value (called the critical I_{off} in this article) shown as the valley-switching region in Fig. 10(a), ODT trends to infinite because v_{ds1} cannot resonate to ($V_{\mathrm{DC}} + V_{rc}$). Fig. 11 shows the simulated waveforms in the valley-switching region. Using the improved circuit structure and solution flow, the proposed model can reflect the valley switching phenomenon, and then the time when v_{ds1} reaches the peak value (T_{valley}) can be used as ODT to minimize the switching loss. The simulation results acquired by the previous transient models are also shown in Fig. 11. Since I_L is regarded as constant during the turn-OFF process, the simulated v_{ds1} can still be charged to ($V_{\mathrm{DC}} + V_{rc}$). As shown in Fig. 11, the previous models can not reflect the valley switching, and the calculated dead-time (ODTP) is much longer, which will induce extra losses compared with using T_{valley}.

Besides V_o, L_f affects the critical I_{off} too. Fig. 10(b) shows ODT with different L_f at 300 V V_o. As L_f increases, the critical I_{off} decreases. Fig. 12 shows the waveforms of v_{ds1} and i_L near the boundary of the valley-switching region. After Q_2 conduct reversely, (-V_i -V_o) is applied on L_f, so I_L begins to decrease. When i_L falls to 0 A (shown as t_c in Fig. 12), Q_2 stops reversely conducting, so v_{ds1} begins to resonate with L_f again. Since v_{ds2} rises from the reverse conduction voltage, turning ON Q_2 after t_c will generate extra switching loss. Therefore, using too long DT not only will cause a huge reverse conduction loss at high I_{off}, but also may introduce the extra switching loss at small I_{off}. Since I_L drops faster with a smaller L_f, the time between $t_{3.2}$ to t_c gets shorter in the applications with smaller L_f. In these applications, an accurate DT model can help to ensure the zero-voltage turn-ON of Q_2.

Finally, the effects of the stray inductance are analyzed. Fig. 13(a) and (b) show ODT with different L_g and L_p, both of which increase ODT at large I_{off}. Although their effects on ODT are slight, L_g and L_p affect the overshoot of v_{gs} and v_{ds} significantly. Fig. 14 (a) and (b) shows the overshoot of v_{gs} and

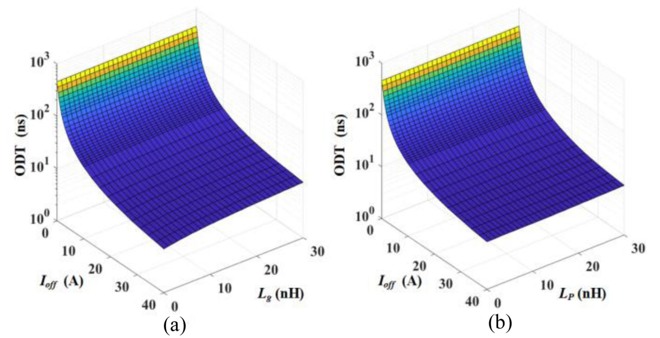


Fig. 13. ODT at different I_{off}. (a) With varying L_g. (b) With varying L_p ($L_{p1} = L_{p2} = 0.5{*}L_p$).

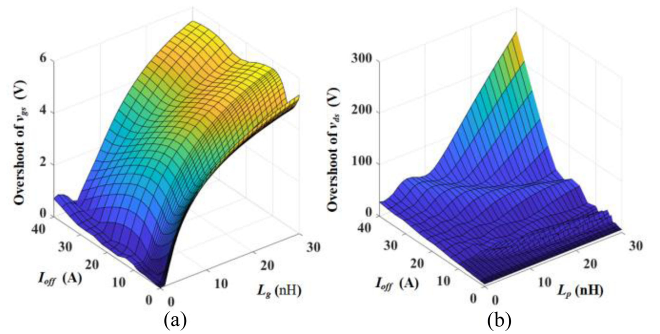


Fig. 14. (a) Overshoot of v_{gs} ($V_{gl} - V_{\mathrm{gsmin}}$) with varying L_g at different I_{off}. (b) Overshoot of v_{ds} ($V_{\mathrm{dsmax}} - V_{\mathrm{DC}}$) with varying L_p at different I_{off}.

v_{ds} with different L_g and L_p. As L_g and L_p increase, the huge overshoot generates, which would damage the device. Fig. 14 shows ODT with different L_{ss}. Using bidirectional solution flow, the proposed model can better reflect the effect of the v_{gs} oscillation on the optimal DT. As L_{ss} and I_{off} increase into a certain area as the false turn-ON area in Fig. 14(b), ODT increases sharply. This is because L_{ss} will induce serious v_{gs} oscillation at large I_{off}, which would cause the false turn-ON of

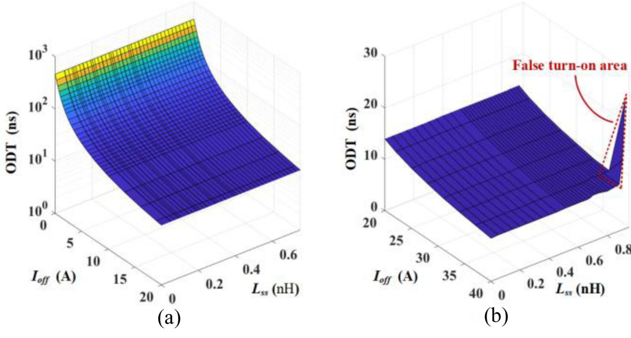


Fig. 15. ODT with varying L_{ss}. (a) At I_{off} from 0 to 20A. (b) At I_{off} from 20 to 40 A.

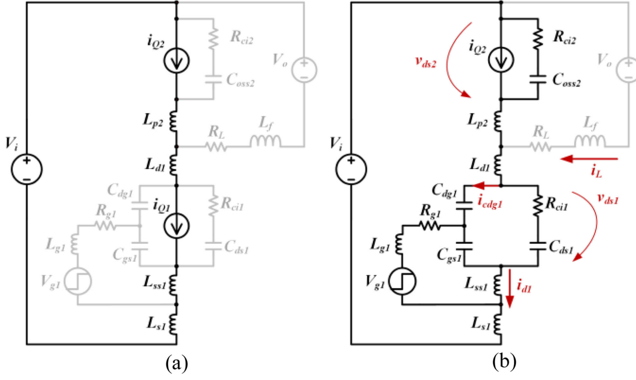


Fig. 16. Equivalent circuit of the short-circuit. (a) Happening before v_{gs1} falls below V_{th}. (b) Happening in the C_{oss} charge period.

Q_1. Compared with L_g and L_p, the effect of L_{ss} is much more serious. When I_{off} is 40 A, only 0.9 nH L_{ss} will induce a severe false turn-ON. As the simulation results show, the effect of the stray inductance gets more serious as I_{off} increases. Therefore, for converters operating under heavy load, the stray inductance should be designed carefully.

As analyzed above, besides I_{off} and V_i, other circuit paraments, such as V_o and L_{ss} also have significant influences on the optimal DT. Including these paraments, the proposed model can offer more accurate results. Besides, this model can be used to evaluate the overshoot of v_{ds}, and the oscillation of v_{gs}, which are related to the safe operation of the devices.

C. Cross-Talk Induced By Insufficient DT Short Circuit

The effect of DT on switching loss has been detailly analyzed in the previous literature. Compared with Si MOSFETs, GaN HEMTs have higher voltage drop when conduct reversely. Hence, GaN-based converters suffer higher reverse conduction loss in the redundant DT. With an insufficient DT, short-circuit will happens even if there is no overlap between the driver signals of the active and freewheeling transistors. The DT short-circuit can be divided into two categories according to when it occurs. For the short-circuit happening before v_{gs1} falls below V_{th}, the equivalent circuit is depicted in Fig. 16(a). Since the channel of Q_1 is still on, V_i is directly connected by the channel of Q_1 and Q_2. Therefore, a huge impulse current flows through Q_1 and Q_2, which will generate luge loss and damage the device. The short-circuit happening before v_{gs1} falls below V_{th} must be avoided because of the destructive impulse current. For the short-circuit happening in the C_{oss} charge period (C_{oss} short-circuit), the equivalent circuit is depicted in Fig. 16(b). During this process, V_i charges C_{oss1} through the channel of Q_2, and C_{oss2} discharges through the channel of Q_2. In the previous literature, the loss generated by the C_{oss} short-circuit is evaluated by the energy stored in C_{oss}. However, as C_{oss1} is charged through the channel of Q_2, dv_{ds1} / dt and i_{d1} rise sharply. dv_{ds1} / dt and i_{d1} influence the gate loop of Q_1 through C_{gd} and L_{ss}, which is known as the "cross-talk" in the traditional hard switching process. When the "cross-talk" is serious enough, a false turn-ON will happen in Q_1 and generate extra losses. Using the proposed model, the effect of the "cross-talk" is further analyzed below.

To use the proposed model, the transient model of the C_{oss} short-circuit period is established. To accelerate the solving speed, the turn-ON transient of Q_2 is ignored. Since i_{d2} is very high during the short-circuit, Q_2 cannot be regarded as a resistor but a current source controlled by v_{ds2} according to the "I_{DS} versus V_{DS} Characteristic" curve in the datasheet. Base on the equivalent circuit in Fig. 16(b), (15) and (16) are derived to describe the transient process during the C_{oss} short-circuit. To solve this period in MATLAB, the state equations T4, which is shown in the Appendix, is derived from (2)–(5), (8), (9), (15), and (16)

$$C_{\text{oss2}} \frac{dv_{co2}}{dt} = i_{d1} - i_L - i_{Q2}(v_{ds2}) \tag{15}$$

$$V_i = v_{\text{ds1}} + v_{co2} + (L_{p1} + L_{p2}) \frac{di_{d1}}{dt} - L_{p2} \frac{di_L}{dt} + R_{ci2} C_{\text{oss2}} \frac{dv_{co2}}{dt}. \tag{16}$$

First, the turn-OFF transient is solved as the flow chart in Fig. 3. When the DT ends, the process enters the C_{oss} short-circuit period, and T4 is solved in the same loop. The C_{oss} short-circuit period ends when v_{ds2} falls below 0. The following period is the current fall or parasitic resonance period depending on whether v_{gs1} has fallen below V_{th}. It is noteworthy that V_R in T3 becomes 0V because Q_2 has been turned ON. Fig. 17 shows the simulation waveforms of v_{gs1}, v_{ds1}, and i_{d1} at 1A I_{off} with 90 ns DT, 5Ω R_g, and 0V V_{gl}.

As shown in Fig. 17, after Q_2 is turned OFF at t_0, v_{gs1} falls below V_{th} soon. When the short-circuit happens at t_{sc}, the rising speed of v_{ds1} increases sharply. Higher dv_{ds1} / dt causes larger i_{cdg1}, which makes v_{gs1} rise suddenly. At the present simulation situation, the peak value of v_{gs1} reaches 1.619 V, so the false turn-ON occurs. Under the combined action of the C_{oss} charging current and false turn-ON current, i_{d1} rises sharply, which induces a huge voltage on L_{ss}. The inductive voltage will aggravate the v_{gs}-oscillation. At $t_{2.1}$, v_{ds2} falls below 0V, the C_{oss} short-circuit period ends. As analyzed in the previous section, when the device is normally turned OFF at a small I_{off}, the overshoot of v_{ds1} is small. However, because of the increasing

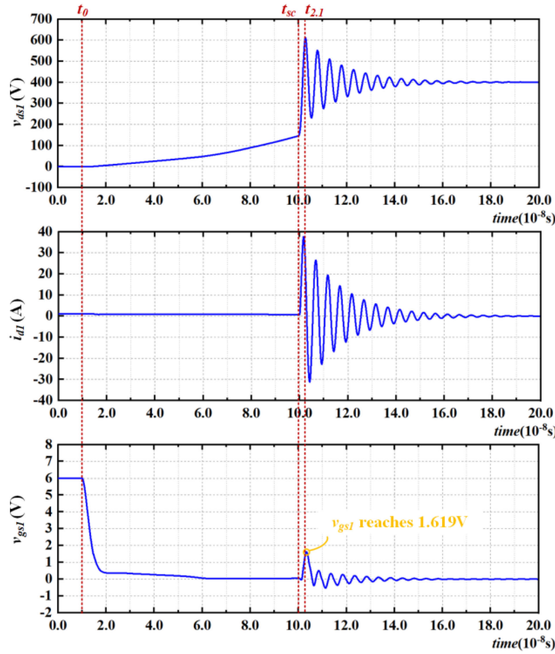


Fig. 17. Simulation waveforms of $v_{\rm gs1}$, $v_{\rm ds1}$, and i_{d1} at 1A $I_{\rm off}$ with 90 ns DT, 5 Ω R_g, and 0 V V_{gl}.

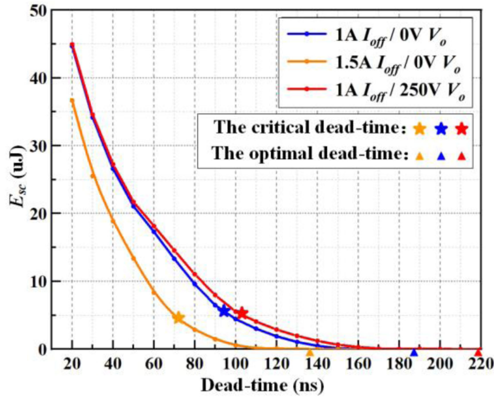


Fig. 18. Short-circuit loss with different DT at 400 V V_i.

i_{d1} caused by the C_{oss} short-circuit, the induced voltage on L_{ss1}, L_{d1}, and L_{s1} is huge, which will generate huge overshoot on v_{gs1} and v_{ds1}.

Fig. 18 shows the short-circuit loss dissipate on the channel of Q_1 and Q_2 (E_{sc}) with different DT, which is calculated by (17). When the DT decreases below the optimal DT ODT, the C_{oss} short-circuit happens and E_{sc} arises. Near ODT, $E_{\rm sc}$ increases slightly as the DT decreases, which conforms to the C_{oss}-storage loss mentioned in the previous literature. When the DT decreases below a critical value, which is called "the critical dead-time" (CDT) in this article, the "cross-talk" makes $v_{\rm gs1}$ rise above $V_{\rm th}$. Then, because of the false turn-ON, $E_{\rm sc}$ increases sharply as the DT decreases. As shown in Fig. 18, when the DT decreases to 20 ns, E_{sc} reaches 44.9 uJ at 1A $I_{\rm off}$ / 250 V V_o, which is far more than the 14.1 uJ C_{oss}-stored energy provided by the manufacturer

$$E_{\rm sc} = \int_{t_{sc}}^{t_{2.1}} v_{\rm ds2} i_{q2} dt + \int_{t_{2.1}}^{t_0+T_{\max}} R_{\rm on}(i_{d1} - i_L)^2 dt - \int_{t_{2.1}}^{t_0+T_{\max}} R_{\rm on} {i_L}^2 dt + \int_{t_{2.1}}^{t_0+T_{\max}} g_m(v_{\rm gs1} - V_{th}) v_{\rm ds1} dt. \quad (17)$$

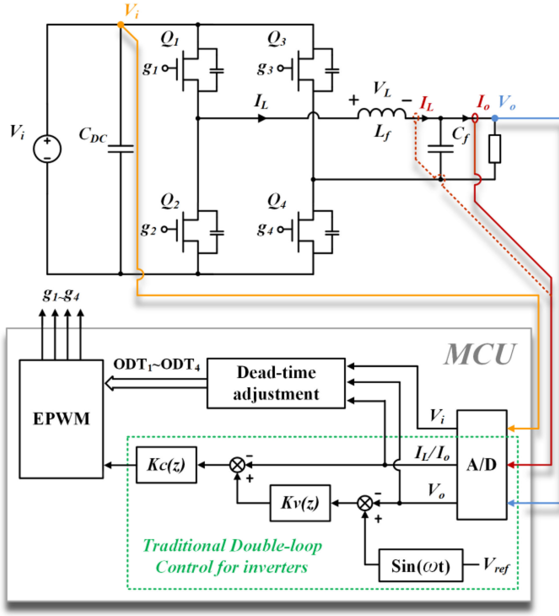
As analyzed above, only considering the C_{oss}-storage loss, the C_{oss} short-circuit loss may be much lower than the reality. As Fig. 18 shows, CDT will change with $I_{\rm off}$ and V_o. Therefore, in inverters, the DT short-circuit loss is more significant if not well optimized. Luckily, the DT loss can be minimized by dynamically adjusting the DT adaptive.

III. Control Strategy of Dynamic DT Adjustment for Single-Phase Inverters

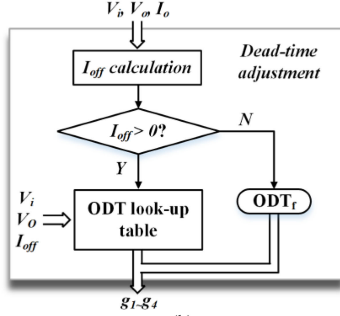
The system control structure of the proposed dynamic DT adjustment for single-phase inverters is depicted in Fig. 19(a). For the single-phase inverter, the operating parameters such as the output voltage V_o and output current I_o are continuously varying, so the DT needs to be dynamically adjusted. As analyzed above, once the input voltage $V_{\rm i}$, V_o, and turn-OFF current $I_{\rm off}$ are determined, the proposed model can calculate the corresponding optimal DT. To realize the dynamic DT adjustment in the microprogrammed control unit (MCU), a lookup table of the optimal dead-time ODT versus $V_{\rm i}$, V_o, and $I_{\rm off}$ is obtained by running the proposed transient model in MATLAB, and then loaded into MCU. Therefore, the MCU can look up the ODT table based on V_i, V_o, and $I_{\rm off}$ to acquire the corresponding ODT.

In the inverter, V_i is usually detected for the over/under voltage protection, and V_o is detected for the output voltage regulation, so V_i and V_o are directly reused for the DT adjustment. As for $I_{\rm off}$, when it is acquired by directly reading I_L while the transistor is turned OFF, the detection delay will induce errors. According to the analysis in Section II, the error of $I_{\rm off}$ will significantly affect the calculation results of the optimal DT. In applications where the ripple of I_L is ignorable, the error caused by detection delay is slight. However, for high-frequency converters with high inductance current ripple [34]–[36], the error caused by the detection delay is very huge. To realize the effective dynamic DT adjustment in both high and small inductance current ripple applications, $I_{\rm off}$ used to look up for ODT is calculated from I_o in this article. The details of the I_o-based calculation method are as follows.

In single-phase inverters, except for the DT, the operation modes are shown in Fig. 20. In modes 1–4 as shown in Fig. 20(a), Q_1 and Q_4 are turned ON, and Q_2 and Q_3 are turned OFF. Hence, the voltage on the filter inductance (V_L) is V_i - V_o, and dI_L / dt is (V_i - V_o) / L_f. In modes 2–4 and modes 1–3, V_L is -V_o, and dI_L / dt is - V_o / L_f. In modes 2–3, V_L is - V_i -V_o, and dI_L / dt is



(a)



(b)

Fig. 19. (a) System control structure of the proposed dynamic DT control for single-phase inverters. (b) Logic diagram of the dynamic DT adjustment.

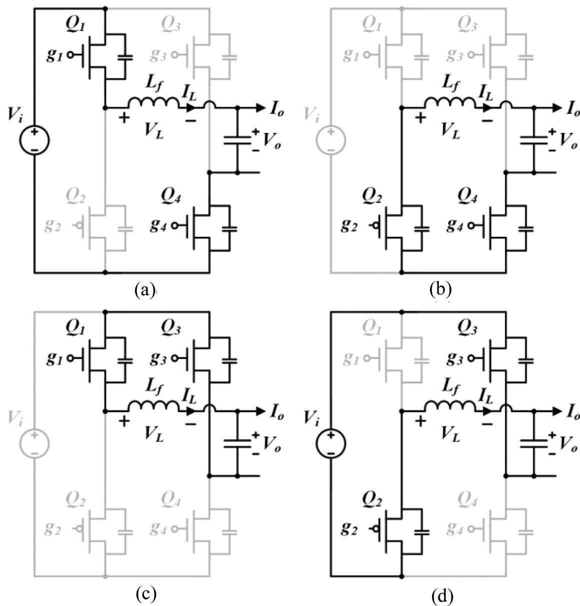


Fig. 20. Operation modes of the single-phase inverter (a) Modes 1–4. (b) Modes 2-4. (c) Modes 1–3. (d) Modes 2–3.

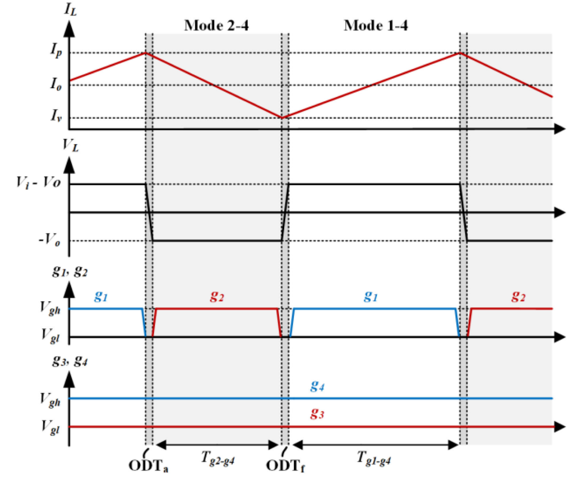


Fig. 21. Typical operation waveforms of the single-phase inverter.

$(- V_i - V_o) / L_f$. Take the operation waveforms shown in Fig. 21 as an example, (18)–(20) are derived to calculate I_{off}.

When Q_1 and Q_4 are turned ON, $(V_{\mathrm{in}} - V_{\mathrm{out}})$ is applied on L_f, and I_L rises linearly from the valley current (I_v). After the turn-ON time of Q_1 and Q_4 ($T_{g1\text{-}g4}$), I_L reaches the peak current (I_p), and Q_1 is turned OFF. Then, the freewheeling transistor conducts reversely, and $-V_{\mathrm{out}}$ is applied on L_f to force I_L to decreases linearly for $T_{g2\text{-}g4}$. In this case, I_p is the I_{off} of Q_1, and $-I_v$ is the I_{off} of Q_2. Based on the operating waveforms, (18) is derived to describe the relationship of I_v, I_p, and I_o. Since I_o and dV_o / dt can be regarded as constant within one sampling period. Equation (19) and (20) are derived to calculate I_v and I_p, where $D_{1\text{-}4}$ is dI_L / dt in modes 1–4; $D_{2\text{-}4}$ is dI_L / dt in modes 2–4; T_s is the sampling period, and $V_o{}'$ is the output voltage sampled in the previous sampling period. For the other operation modes, I_{off} can be acquired by using the corresponding dI_L / dt and turn-ON time

$$\frac{T_B(I_p + I_v)}{2} - \int_0^{T_B} I_o dt = \int_0^{T_B} C_f \frac{dV_o}{dt} dt \tag{18}$$

$$I_p = I_o + \frac{D_{1-4}}{2} T_{g1-g4} + C_f \frac{V_o - V_o'}{T_s} \tag{19}$$

$$I_v = I_o - \frac{D_{2-4}}{2} T_{g2-g4} + C_f \frac{V_o - V_o'}{T_s}. \tag{20}$$

The logic diagram of the dynamic DT adjustment is shown in Fig. 19(b). Acquiring V_{i}, V_o, and I_{off}, a direction judgment is used to judge whether the transistors work as the active or freewheeling transistors. When I_{off} is positive (the current flows from drain to source), the transistor work as the active transistor. Otherwise, it works as the freewheeling transistor. Take Fig. 21 as an example, when I_p and I_v are both positive, Q_1 works as the active transistor, while Q_2 works as the freewheeling transistor. After the direction judgment, ODT_a or ODT_f is acquired by looking up the ODT table. Since the gate charge of GaN HEMTs is very small, ODT_f is very short, so 10 ns constant ODT_f with some margin is proposed in this article to avoid the short circuit.

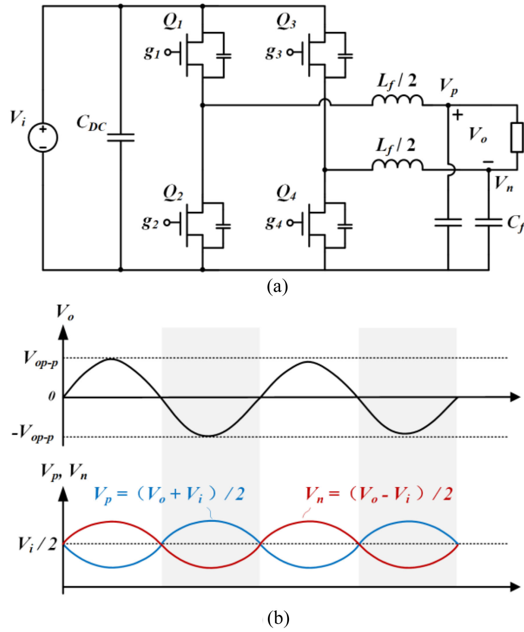


Fig. 22. (a) Approximated dual-buck circuit for the inverter under the bipolar modulation. (b) Output voltage waveforms of the approximated circuit.

For single-phase inverters under the unipolar modulation, the proposed model can be directly used. Under the bipolar modulation, the inverter only operates in modes 1–4 and modes 2–3, and two transistors are turned OFF at the same time. To implement the proposed model, the inverter under the bipolar modulation is approximated as the dual-buck circuit shown in Fig. 22. To operate as same as the inverter, the node voltage of the dual-buck circuit V_p and V_n are $(V_i + V_o)/2$ and $(V_i - V_o)/2$ respectively. After approximation, the L_f used in the transient model is the half of the practical filter inductance ($L_f 2$), and the V_o used in the transient model is respectively V_p for Q_1, Q_2, and V_n for Q_3, Q_4. When the $I_{\rm off}$ of Q_1 or Q_3 is positive, V_i charges V_o through L_f, so they work in the Buck condition. When the $I_{\rm off}$ of Q_2 or Q_4 is positive, V_o and L_f charge V_i, so they work in the Boost condition. The state equations used for the buck and boost conditions are different as analyzed in Section I.

Using the proposed strategy, the DT can be adjusted dynamically based on the low-speed value $V_{\rm i}$, V_o, and I_o. Compared with the nanoseconds-level $v_{\rm ds}$ and $v_{\rm gs}$, these values are easier to detect, and often used in the closed-loop control of inverters (I_o can be used in the double-loop control to increase the dynamic response and reduces the total harmonic distortion of inverters [20]). Therefore, for inverters with the double-loop control, the dynamic DT adjustment can be realized without extra sensors.

IV. Experimental Results

A GaN HEMTs based inverter is established to verify the proposed dynamic DT adjustment strategy. The prototype of the inverter is shown in Fig. 23. The schematic of this inverter is depicted in Fig. 19. The main operating parameters of the converter are given in Table II, and the gate driver design is the same as the DPT circuit shown in Fig. 4. The inverter is designed

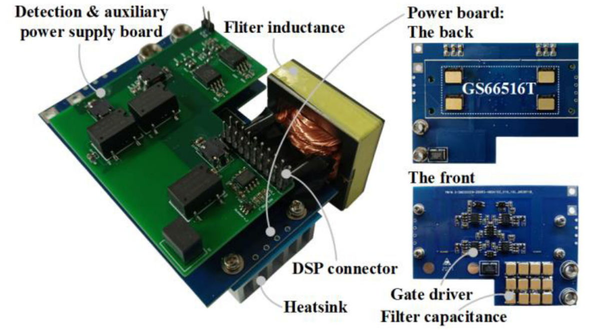


Fig. 23. Prototype of the inverter.

TABLE II
Main Operating Parameters of the Inverter

Part.	Specification
GaN HEMT	GS66516T
Input voltage	400V
Output voltge	220V,50Hz
Rated output power	1200W
Switching frequency	100kHz~1.2MHz
Filter inductance	50uH
Filter capacitance	12uF

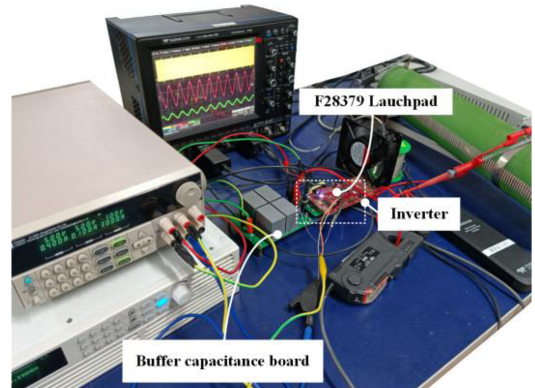


Fig. 24. Schematic diagram of the experimental test platform.

as a layer-stacked structure. The detection and auxiliary power supply circuit are on the top board, and the gate driver and transistors are on the bottom board. Fig. 24 shows the experimental test platform. An external buffer capacitor board is connected in front of the converter to compensated the dc side current ripple. The inverter is controlled by the TMS320F28379D Launchpad mounted on the detection and auxiliary power supply board.

TCM is used to increase efficiency [38]. Under TCM, the inductance current is modulated as the triangular and reverse before the freewheel ends. Because of the reverse inductance current, the active transistors can be turned ON under zero voltage over the full operating range. To ensure the realization of the zero-voltage turn-ON, an extra −0.5 A is added to the reverse current in this inverter. Fig. 25 shows the TCM operating waveforms of the $v_{\rm ds}$ of Q_2, V_o, and I_L (Q_1 and Q_4 work as the active transistor while Q_2 and Q_3 work as the freewheel transistor). As shown in Fig. 25, when the active transistor is

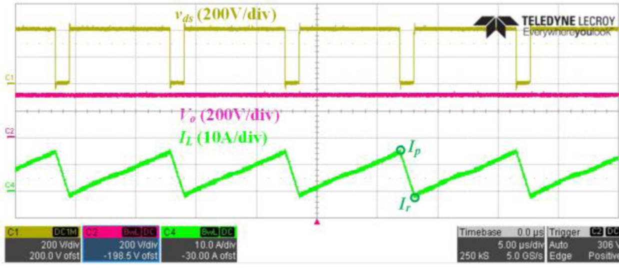


Fig. 25. TCM operation waveforms of the v_{ds} of Q_2, V_o, and I_L.

TABLE III
PARASITIC PARAMENTS OF DPT CIRCUIT

Part.	Device	Value
L_g	Q_1 / Q_2	4.0nH / 4.4nH
	Q_3 / Q_4	3.6nH / 4.1nH
L_{p2}	Q_1 / Q_2	2.6nH
	Q_3 / Q_4	2.6nH
L_{p1}	Q_1 / Q_2	3.3nH
	Q_3 / Q_4	3.3nH

turned ON, the inductance current I_L rises linearly to the peak value I_p. The active transistor is turned OFF at I_p and then I_L begins to fall linearly. When I_L falls to the reverse current I_r, the freewheeling transistors are turned OFF, and then the reverse inductance current will force the active transistors to conduct reversely. The relationship between I_p, I_r, and I_o can be approximately expressed as (21). To realize the reverse inductance current I_r, the ripple of I_L in one switching cycle is double I_o. Because of the large ripple of I_L, it is difficult to accurately measure I_{off} from I_L. The switching period T_B under TCM can be approximately calculated as (22). Since the calculated switching frequency increases above 4MHz at the zero-cross point of I_o, the practical switching frequency in this inverter is limited to 1.2 MHz to avoid excessive loss

$$I_p + I_r = 2I_o \tag{21}$$

$$T_B = \frac{L\cdot(I_p - I_r)}{V_i - V_o} + \frac{L\cdot(I_p - I_r)}{V_i + V_o} + \mathrm{dead} - \mathrm{time}. \tag{22}$$

As shown in Fig. 25, because I_L has reversed, the freewheeling transistors are turned OFF at a positive i_d under TCM. Therefore, the turn-OFF process of the freewheeling transistors is the same as the active transistor, and ODT$_a$ is used for all the transistors. The extracted parasitic inductance of the inverter is given in Table III. Using the proposed model, the ODT lookup table is shown in Fig. 26 (In the valley switching region, the time when v_{ds1} reaches the peak value is used as ODT$_a$). Since the inverter works under bipolar modulation, the corresponding ODT tables for buck operating state and boost operating state are given. Considering the difference of GaN HEMTs in practice, a 5-ns margin is added to the ODT lookup table to avoid the short-circuit.

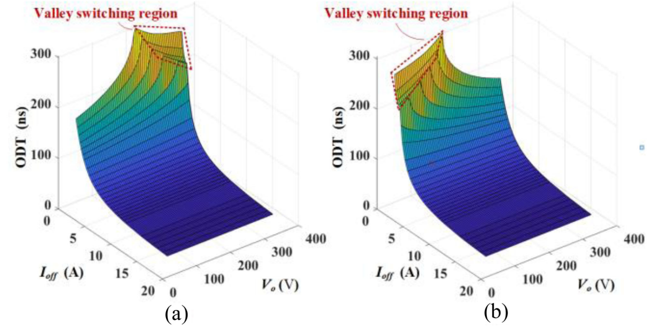


Fig. 26. ODT*a* table. (a) Under Buck operating state. (b) Under Boost operating state.

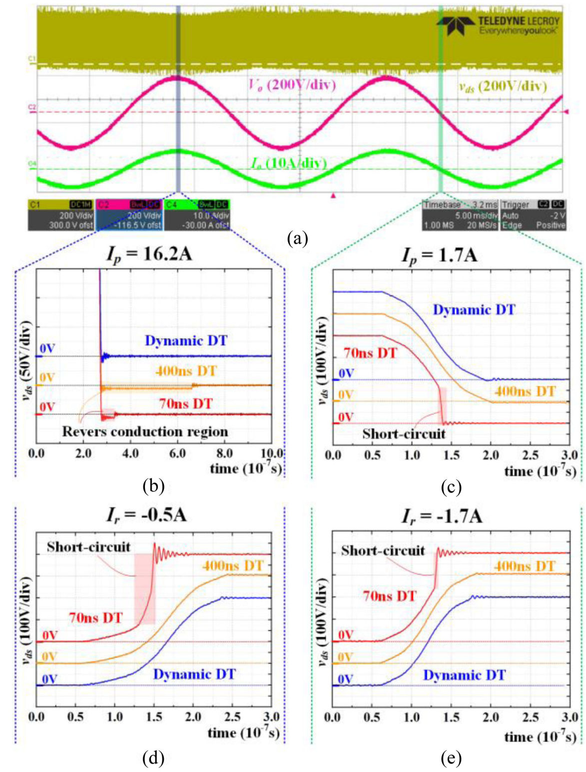


Fig. 27. Operation waveforms of the inverter under 1200 W P_o with the fixed 70 ns, 400 ns, and the dynamic DT. (a) Waveforms of the v_{ds} of Q_2, V_o, and I_o. (b) v_{ds} waveform when the active transistor is turned OFF at the peak output current. (c) v_{ds} waveform when the active transistor is turned OFF at the zero-cross point of output current. (d) v_{ds} waveform when the freewheeling transistor is turned OFF at the peak output current. (e) v_{ds} waveform when the freewheeling transistor is turned OFF at the zero-cross point of output current.

Fig. 27(a) shows the operating waveforms of the v_{ds} of Q_2, V_o, and I_o under 1200 W output power (P_o). Compared with I_L, the ripple of I_o is ignorable. Therefore, it is recommended to calculate I_{off} from I_o for the TCM inverter. The dynamic DT adjustment is compared with the fixed 70 and 400 ns DT in Fig. 27(b)–(e). When the inverter is operating at the peak output current, the active transistors are turned OFF at 16.2A I_p while the freewheeling transistors are turned OFF at -0.5A I_r. Using 400ns DT can avoid the short-circuit at I_r, but the transistors suffer huge reverse conduction loss at I_p. With 70 ns DT, although

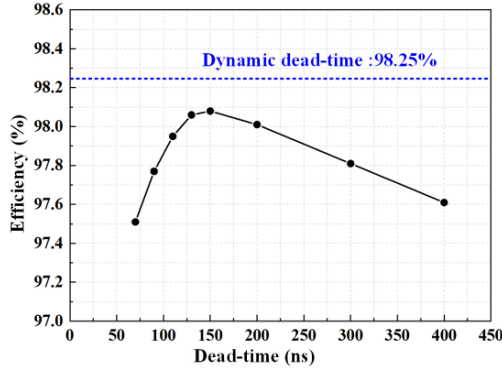


Fig. 28. Efficiency with the different fixed DT and dynamic DT adjustment under 1200 W load.

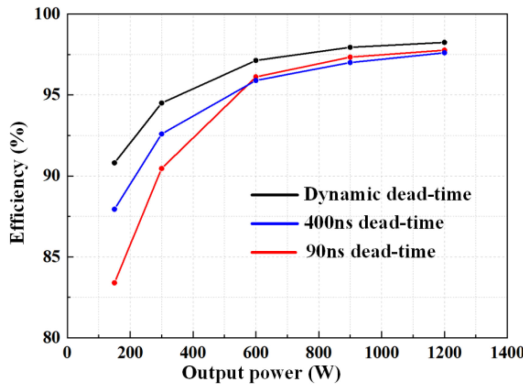


Fig. 29. Efficiency with the fixed 90 and 400 ns, and the dynamic DT adjustment under different loads.

the reverse conduction region at I_p has been reduced, a serious short-circuit happens at I_r. Compared with the fixed DT, when the dynamic DT adjustment is implemented, two different DTs are read from the ODT look-up table according to I_p and I_r. Therefore, the short-circuit and reverse conduction regions have been eliminated at both I_p and I_r.

When the inverter is operating at the zero-cross point of I_o, I_p cannot fall to 0 A because the switching frequency is limited to 1.2 MHz. At this point, the active transistors are turned OFF at 1.7 A I_p while the freewheeling transistors are turned OFF at −1.7 A I_r. As we can see, the short-circuit happens at both I_p and I_r with 70 ns DT. Using the dynamic DT adjustment, the DT has been adjusted according to I_o and V_o. Therefore, these high-loss regions can be eliminated even if the operating condition changes.

Fig. 28 shows the efficiency under 1200 W P_o with the different fixed DT and dynamic DT. Using the fixed DT, a peak efficiency of 98.08% has been realized around 150 ns, and both increasing and decreasing the DT will decrease the efficiency. Since the reverse conduction and short circuit loss can be eliminated at the same time, using the dynamic DT adjustment further increases the efficiency to 98.25%.

Fig. 29 shows the efficiency with the fixed 90, 400 ns, and the dynamic DT adjustment under different loads. Although the efficiency is 97.77% with 90ns DT under 1200 W P_o, the efficiency falls sharply as P_o decreases. Fig. 30 shows

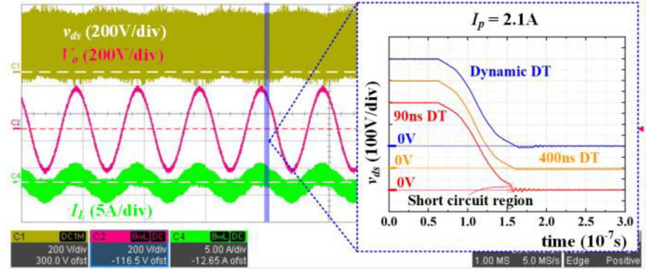


Fig. 30. Operation waveforms of the v_{ds} of Q_2, V_o, and I_L under 150 W load.

the operating waveforms at 150 W P_o. As we can see, with 90ns DT, the short-circuit has happened at I_p near the peak output current. Because of the extended short-circuits area and increased switching frequency, the efficiency with 90 ns DT falls to 83.41% at 150 W P_o. Using 400 ns DT although can avoid the short-circuit under light load, the reverse conduction loss is huge under heavy load. Compared with the fixed DT, the dynamic DT adjustment increases the efficiency over all the load range. Compared with using 400-ns DT, the total loss has been reduced by 27.26% under 1200 W P_o, while the loss under 150W P_o has been decreased by 49.14% compared with using 90 ns. In conclusion, using the dynamic DT adjustment can improve global efficiency, especially under the light load.

V. Conclusion

This article has proposed a model-based method of dynamic DT adjustment for single-phase inverters to minimize the DT loss. First, a more accurate turn-OFF transient model for GaN HEMTs has been proposed to acquire the optimal DT. This model has improved the previous works as following:

1) Proposed model is established based on the buck and boost operating condition for inverters. Compared with the previous transient model based on the DPT circuit, this structure can reflect the effect of the filter inductance and output voltage.

2) Improved directional solution flow is proposed for the transient model. Therefore, the false turn-ON and "valley switching region" can be demonstrated.

3) Short-circuit mode has been established to analyze the "cross-talk" induced by the C_{oss} short-circuit, which can be used for the evaluation of the DT losses.

Then, based on the proposed model, a control strategy of dynamic DT adjustment for single-phase inverters is proposed. This article uses an I_o-based method to calculate I_{off}, which can greatly reduce the influence of detection delay compared with the direct sense method. Under unipolar modulation, the proposed model can be used directly, while an equivalent method is proposed for bipolar modulation. Finally, the dynamic DT adjustment is implemented in a GaN-based TCM inverter with the load varying from 150 to 1200 W. Compared with the traditional fixed DT, using the proposed dynamic DT adjustment can improve the efficiency around all the load range with the peak efficiency up to 98.25%.

APPENDIX

$$\begin{bmatrix} \frac{dv_{\mathrm{gs1}}}{dt} \\ \frac{di_{g1}}{dt} \end{bmatrix} = \begin{bmatrix} 0, \frac{1}{C_{iss1}} \\ -\frac{1}{(L_{g1}+L_{ss1})}, -\frac{R_{g1}}{(L_{g1}+L_{\mathrm{ss1}})} \end{bmatrix} \begin{bmatrix} v_{\mathrm{gs1}} \\ i_{g1} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{V_{gl}}{(L_{g1}+L_{ss1})} \end{bmatrix} \tag{T1}$$

$$\left[\frac{di_{g1}}{dt}, \frac{dv_{\mathrm{gs1}}}{dt}, \frac{dv_{\mathrm{ds1}}}{dt}, \frac{di_{d1}}{dt}, \frac{di_{co1}}{dt}, \frac{dv_{co2}}{dt}, \frac{di_L}{dt}\right]^T = A_2[i_{g1}, v_{\mathrm{gs1}}, v_{\mathrm{ds1}}, i_{d1}, i_{co1}, v_{co2}, i_L]^T + B_2 \tag{T2}$$

$$A_2 = \begin{bmatrix} -\frac{R_{g1}}{L_{g1}+L_{ss1}}, -\frac{1}{L_{g1}+L_{ss1}}, \frac{L_{ss1}L_f+L_{ss1}L_{p2}}{L_p^2(L_{g1}+L_{ss1})}, \frac{L_fL_{ss1}R_{ci2}}{L_p^2(L_{g1}+L_{ss1})}, 0, \frac{L_fL_{ss1}}{L_p^2(L_{g1}+L_{ss1})}, \frac{L_{p2}L_{ss1}R_L-L_fL_{ss1}R_{ci2}}{L_p^2(L_{g1}+L_{ss1})} \\ \frac{1}{C_{\mathrm{gs1}}}, -\frac{g_m}{C_{\mathrm{gs1}}}, 0, \frac{1}{C_{gs1}}, -\frac{1}{C_{\mathrm{gs1}}}, 0, 0 \\ \frac{1}{C_{gs1}}, -\frac{g_m(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}}, 0, \frac{C_{\mathrm{gd1}}+C_{gs1}}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}}, -\frac{C_{\mathrm{gd1}}+C_{\mathrm{gs1}}}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}}, 0, 0 \\ 0, 0, -\frac{L_f+L_{p2}}{L_p^2}, -\frac{L_fR_{ci2}}{L_p^2}, 0, -\frac{L_f}{L_p^2}, \frac{L_fR_{ci2}-L_{p2}R_L}{L_p^2} \\ \frac{1}{C_{\mathrm{gs1}}R_{ci1}}, -\frac{g_m(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}R_{ci1}}, 0, \frac{C_{gd1}+C_{gs1}}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}R_{ci1}}, -\frac{C_{ds1}C_{\mathrm{gd1}}+C_{\mathrm{ds1}}C_{\mathrm{gs1}}+C_{\mathrm{gd1}}C_{\mathrm{gs1}}}{C_{\mathrm{ds1}}C_{\mathrm{gd1}}C_{\mathrm{gs1}}R_{ci1}}, 0, 0 \\ 0, 0, 0, \frac{1}{C_{\mathrm{oss2}}}, 0, 0, -\frac{1}{C_{\mathrm{oss2}}} \\ 0, 0, -\frac{L_{p2}}{L_p^2}, \frac{L_{p1}R_{ci2}}{L_p^2}, 0, \frac{L_{p1}}{L_p^2}, \frac{-L_{p1}R_L-L_{p2}R_L-L_{p1}R_{ci2}}{L_p^2} \end{bmatrix}$$

$$B_2 = \Big[\frac{-(L_fL_{ss1}+L_{ss1}L_{p2})V_i+L_p^2V_{gl}+L_{ss1}L_{p2}V_o}{L_p^2(L_{g1}+L_{ss1})}, V_{\mathrm{th}}\frac{g_m}{C_{gs1}}, V_{\mathrm{th}}\frac{g_m(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}}, \frac{(L_f+L_{p2})V_i-L_{p2}V_o}{L_p^2}, V_{\mathrm{th}}\frac{g_m(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}R_{ci1}}, 0, \frac{L_{p2}V_i-(L_{p1}+L_{p2})V_o}{L_p^2}\Big]^T$$

where $L_p^2 = L_{p1}L_{p2} + L_{p1}L_f + L_{p2}L_f$

$$\left[\frac{di_{g1}}{dt}, \frac{dv_{\mathrm{gs1}}}{dt}, \frac{dv_{\mathrm{ds1}}}{dt}, \frac{di_{d1}}{dt}, \frac{di_{co1}}{dt}, \frac{di_L}{dt}\right]^T = A_3[i_{g1}, v_{\mathrm{gs1}}, v_{\mathrm{ds1}}, i_{d1}, i_{co1}, i_L]^T + B_{3.1} \tag{T3}$$

$$A_3 = \begin{bmatrix} -\frac{R_{g1}}{L_{g1}+L_{ss1}}, -\frac{1}{L_{g1}+L_{ss1}}, \frac{L_{ss1}L_f+L_{ss1}L_{p2}}{L_p^2(L_{g1}+L_{ss1})}, \frac{L_fL_{ss1}R_{on}}{L_p^2(L_{g1}+L_{ss1})}, 0, \frac{L_{p2}L_{ss1}R_L-L_fL_{ss1}R_{\mathrm{on}}}{L_p^2(L_{g1}+L_{ss1})} \\ \frac{1}{C_{\mathrm{gs1}}}, -\frac{g_m}{C_{\mathrm{gs1}}}, 0, \frac{1}{C_{\mathrm{gs1}}}, -\frac{1}{C_{\mathrm{gs1}}}, 0 \\ \frac{1}{C_{\mathrm{gs1}}}, -\frac{g_m(C_{\mathrm{gd1}}+C_{gs1})}{C_{\mathrm{gd1}}C_{gs1}}, 0, \frac{C_{\mathrm{gd1}}+C_{\mathrm{gs1}}}{C_{\mathrm{gd1}}C_{gs1}}, -\frac{C_{\mathrm{gd1}}+C_{gs1}}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}}, 0 \\ 0, 0, -\frac{L_f+L_{p2}}{L_p^2}, -\frac{L_fR_{\mathrm{on}}}{L_p^2}, 0, \frac{L_fR_{\mathrm{on}}-L_{p2}R_L}{L_p^2} \\ \frac{1}{C_{gs1}R_{ci1}}, -\frac{g_m(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}R_{ci1}}, 0, \frac{C_{\mathrm{gd1}}+C_{\mathrm{gs1}}}{C_{\mathrm{gd1}}C_{gs1}R_{ci1}}, -\frac{C_{\mathrm{ds1}}C_{\mathrm{gd1}}+C_{ds1}C_{\mathrm{gs1}}+C_{\mathrm{gd1}}C_{\mathrm{gs1}}}{C_{ds1}C_{\mathrm{gd1}}C_{gs1}R_{ci1}}, 0 \\ 0, 0, -\frac{L_{p2}}{L_p^2}, \frac{L_{p1}R_{\mathrm{on}}}{L_p^2}, 0, \frac{-L_{p1}R_L-L_{p2}R_L-L_{p1}R_{\mathrm{on}}}{L_p^2} \end{bmatrix}$$

$$B_{3.1} = \Big[\frac{-(L_fL_{ss1}+L_{ss1}L_{p2})V_i+L_p^2V_{gl}+L_{ss1}L_{p2}V_o+L_fL_{ss1}V_R}{L_p^2(L_{g1}+L_{ss1})}, V_{\mathrm{th}}\frac{g_m}{C_{gs1}}, V_{\mathrm{th}}\frac{g_m(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}}, \frac{(L_f+L_{p2})V_i-L_{p2}V_o-L_fV_R}{L_p^2}, V_{\mathrm{th}}\frac{g_m(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{gd1}}C_{gs1}R_{ci1}}, \ldots\ldots \frac{L_{p2}V_i+L_{p1}V_R-(L_{p1}+L_{p2})V_o}{L_p^2}\Big]^T$$

$$\left[\frac{di_{g1}}{dt}, \frac{dv_{\mathrm{gs1}}}{dt}, \frac{dv_{\mathrm{ds1}}}{dt}, \frac{di_{d1}}{dt}, \frac{di_{co1}}{dt}, \frac{di_L}{dt}\right]^T = A_2[i_{g1}, v_{gs1}, v_{\mathrm{ds1}}, i_{d1}, i_{co1}, i_L]^T + B_4 \tag{T4}$$

$$B_4 = \Big[\frac{-(L_fL_{ss1}+L_{ss1}L_{p2})V_i+L_p^2V_{gl}+L_{ss1}L_{p2}V_o-L_fL_{ss1}R_{ci2}i_{q2}}{L_p^2(L_{g1}+L_{ss1})}, V_{\mathrm{th}}\frac{g_m}{C_{\mathrm{gs1}}}, V_{\mathrm{th}}\frac{g_m(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}}, \frac{(L_f+L_{p2})V_i-L_{p2}V_o+L_fR_{ci2}i_{q2}}{L_p^2}, V_{\mathrm{th}}\frac{g_m(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{gd1}}C_{\mathrm{gs1}}R_{ci1}}, \ldots\ldots -\frac{i_{q2}}{C_{\mathrm{oss2}}}, \frac{L_{p2}V_i-(L_{p1}+L_{p2})V_o-L_{p1}R_{ci2}i_{q2}}{L_p^2}\Big]^T.$$

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