Time-Domain Characterization and Detection of Open-Circuit Faults for the H-Bridge Power Cell

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***Abstract*—This article presents the time-domain characterization of semiconductor open-circuit switch faults (OCSFs), such as an open switch with a healthy diode and switch–diode pair open for the H-bridge power cell. The inverter fault signatures under diagonally opposite open switch fault conditions with a healthy diode are approximately similar; therefore, this article presents a detection algorithm with a unique identification of each faulty switch within the H-bridge power cell. The proposed algorithm is also designed to detect and identify multiple OCSFs. The nonideal characteristics of semiconductor switches are considered for the identification of switch faults. The well-known unipolar sinusoidal pulsewidth modulation technique is used for the switching of semiconductor devices for the single power cell. The mathematical expressions have also been derived to find out the effect of the switch fault using a double Fourier integral solution and the switching states. The analytical expressions have been developed for the switched output voltage waveforms under ideal switching conditions. The behavior of the switch faults has been analyzed using inverter output voltage, load current, and total harmonic distortion of the pulsewidth-modulated inverter output voltage.**

***Index Terms*—Cascaded H-bridge (CHB), double Fourier series, fault detection, fault identification, harmonic distortion, open switch faults, parasitic capacitance.**

I. Introduction

THE Probability of fault occurrence in the power electronics system increases with the increased number of power semiconductor devices, and therefore, the reliability of the system decreases. The optimal productivity with improved output qualities and operational safety are the primary conditions for industries and production tools. It covers the fault detection in a short time period to avoid hazards. The fault detection system not only reduces the maintenance cost but also prevents the partial or full shutdown of the complete system. Thus, the optimal productivity can be achieved by employing a fault detection system. According to the survey and research on 80 companies and more than 200 industrial processes, 21% of faults were detected in power semiconductor devices and 13% in solders. In total, 34% of faults in a converter are due to the failure of the device module. The rest of the faults are divided into dc-link capacitor faults, load faults, and gate driver faults [1], [2].

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Multilevel inverters (MLIs) are the most promising structure in the area of medium- and high-power applications and for every industrial process with reduced operational cost and quality production [3]. Several basic structures of MLIs are available in the literature such as: neutral point clamped, flying capacitor, and cascaded H-bridge (CHB) [4], [5]. The CHB inverters are one of the most popular and promising MLI topology, where number of series-connected power cells is used to produce the stepped inverter voltage output. There are several applications of the CHB MLI, such as renewable energy systems, ac motor drives, reactive power compensation, and hybrid energy systems, where fault-tolerant capabilities improve the power quality and operational hours.

The possibilities of faults occurred in a power semiconductor device are due to external and internal causes. The external possibilities of the switch failure may be swelling or dip from the external supply connected to the terminals of MLIs, high dynamic changes at the load side, short circuit of the load, etc. On the other side, the internal possibilities of switch failures may be thermomechanical fatigue, gate misfiring, saturation of semiconductor materials, etc. Due to the aforementioned causes, the power switches may be either permanently opened or closed. This phenomenon is defined as fault in the switching device. If switch is permanently open, then it is defined as open-circuit switch faults (OCSFs), and if the switch is permanently closed, then it is defined as short-circuit switch faults (SCSFs) [6]. The antiparallel diode across the switching device has also possibilities of open-circuit or short-circuit fault.

In literature, several fault-tolerant-controlled operations of medium- and high-voltage converters are reported in [7] and [8], especially for the CHB MLI in [9] and [10] and modular multilevel converters with the phase-shifted carrier modulation technique in [11]. The SCSFs are severe in nature and can cause immediate damage to the complete system. Therefore, fast detection and isolation / protection circuitry are required. Fast acting fuses or fast acting gate drive circuit protections are generally used for the protection purpose. The SCSF should be clear within $t_{\rm sc}$ ($\approx$ 10 μs), where $t_{\rm sc}$ depends on the semiconductor chip and gate driver voltage, i.e., the reduction in the gate–emitter voltage $V_{\rm GE}$ reduces the fault current magnitude increasing the short-circuit time $t_{\rm sc}$ [12]. In OCSF conditions, the MLI can operate under a faulty condition with reduced output quality because of inherent switching redundancy. However, this may lead to increased voltage stress across the other healthy switches and may be the cause of the complete system damage. Therefore, to make the system fault tolerant, the fault must be

detected and the fault location must be identified in minimum time duration.

In literature, several OCSF detection and identification techniques are reported. These techniques are classified in general as hardware-based fault detection methods and computational-based fault detection methods (C-FDMs) [13], [14]. The hardware-based techniques are used to detect severe faults such as short-circuit faults in modules and shoot through of legs. Such faults can be isolated using advanced inbuilt gate driver protection circuits, where fault isolation is required within 10 μs [12], [15]. The fault detection methods based on gate signal monitoring are used to detect SCSFs and OCSFs; they are presented with additional voltage / current sensors and the comparison of measured quantities with defined threshold values in [16] and [17].

On the other hand, for nonsevere faults, C-FDMs are used, which require additional processing of measurement data. Such computational methods use either an extracted feature like switching frequency component of the module or the output states of the system to detect and localize the faults. The C-FDMs can be further categorized as model-based fault detection methods (M-FDMs) and feature-based fault detection methods (F-FDMs). The main advantage of the model-based fault detection technique is to minimize the inclusion of additional sensors needed for the measurement of featured quantities. The occurrence of the OCSF in any active switch of an H-bridge affects the inverter output voltage. Several M-FDMs are available in the literature, where high bandwidth voltage sensors are used to measure either the inverter output voltage across each H-bridge module [18] or the CHB MLI per phase output voltage [13], [19], [20]. Since for the detection of OCSFs, switching states are used for the comparison of respective inverter output voltage and load current, therefore, M-FDMs are much faster. The mathematical modeling of the switch faults diagnosis in multilevel-inverter drive (MLID) systems is very difficult due to many switching devices and their nonlinear effects, therefore, an artificial intelligence and fast Fourier transform with neural network-based fault diagnostic method for CHB MLID is presented in [21]. Several literatures are based on the model predictive control algorithm, which predicts the future states and used to compare against the actual state for fault detection [22], [23]. The accuracy of diagnosis depends on the predicted values of future states and if the parameters are inaccurate with respect to real time, the probability of the diagnostic accuracy reduces. The extracted characteristics of the system outputs are used to detect the fault under F-FDMs. Switching-frequency-based harmonic component analysis is one of the popular characteristics of the F-FDMs [24], [25]. In harmonic component analysis, the threshold level is categorized in dc components, side-band components, and base-band components. Similar to the harmonic component-based open-circuit fault detection method, few other F-FDMs are available in the literature such as: electromagnetic interference (EMI) based and conduction based [26], [27].

In this article, fast detection algorithms for a single H-bridge power cell are proposed and detection logic designs have been developed to minimize the detection time and identify the accurate switch fault locations for different type of OCSFs. The following three different open switch fault categories are considered for the analysis:

1) switch open-circuit faults with a healthy diode $SF_{xy\mathrm{soc}}$ (where subscripts *x* and *y* represent the upper/lower switch and *leg* number in the power cell and "soc" represents switch open circuit with healthy diode);

2) diode open-circuit faults with a healthy switch $SF_{xy\mathrm{DOC}}$ (where "DOC" represents diode open circuit with healthy switch);

3) open-circuit faults $SF_{xy\mathrm{oc}}$ (where "oc" represents switch–diode pair is under fault).

In the H-bridge power cell, the fault signatures of diagonally opposite switch faults are approximately similar, therefore, it is difficult to identify the unique switch fault location. Therefore, a unique fault detection algorithm is developed for the identification of individual switches within the power cell. The proposed switch fault detection and identification technique is also able to detect multiple open switch faults. The role of nonideal behavior of semiconductor switches is used for the identification of switch faults. The phase-shifted pulsewidth modulation (PSPWM) technique is used to generate switching logics for semiconductor devices. The primary contributions of this article are as follows:

1) the detection logic designs are developed for OCSFs;

2) fault appeared in any of the switch within the H-bridge power cell can be uniquely identified within couple of switching intervals;

3) the proposed detection logic designs are presented for rapid detection and identification;

4) the designed algorithm can detect multiple open switch faults;

5) mathematical relations are developed under OCSFs conditions;

6) experimental results are also presented for the verification of the proposed algorithm.

II. IGBT Switching Characteristics

The switching behavior of an IGBT depends on the structure, inner/outer resistances, and internal capacitances. The half-bridge structure with an input gate resistance R_{GI} and internal capacitances C_{GC} and C_{GE} is presented in Fig. 1(a). The voltage-dependent low-signal capacitances play major role during turn-ON and turn-OFF of the transistors. These voltage-dependent parasitic capacitances are classified as input capacitance ($C_{\mathrm{ies}} = C_{\mathrm{GC}} + C_{\mathrm{GE}}$), reverse transfer capacitance ($C_{\mathrm{res}} = C_{\mathrm{GC}}$), and output capacitance ($C_{\mathrm{oes}} = C_{\mathrm{GC}} + C_{\mathrm{CE}}$); where C_{GC}, C_{GE}, and C_{CE} are internal capacitances between gate–collector, gate–emitter, and collector–emitter, respectively [28]. The collector–emitter capacitance is considered equivalent to the antiparallel diode capacitance.

The equivalent simplified model of the IGBT switch circuit seen from the gate to the emitter is presented in Fig. 1(b). The circuit model is developed without the consideration of base resistor small modulation voltage and the small turn-ON voltage of the diode in the internal bipolar junction transistor for the IGBT. Therefore collector–emitter voltage V_{CE} is equivalent to

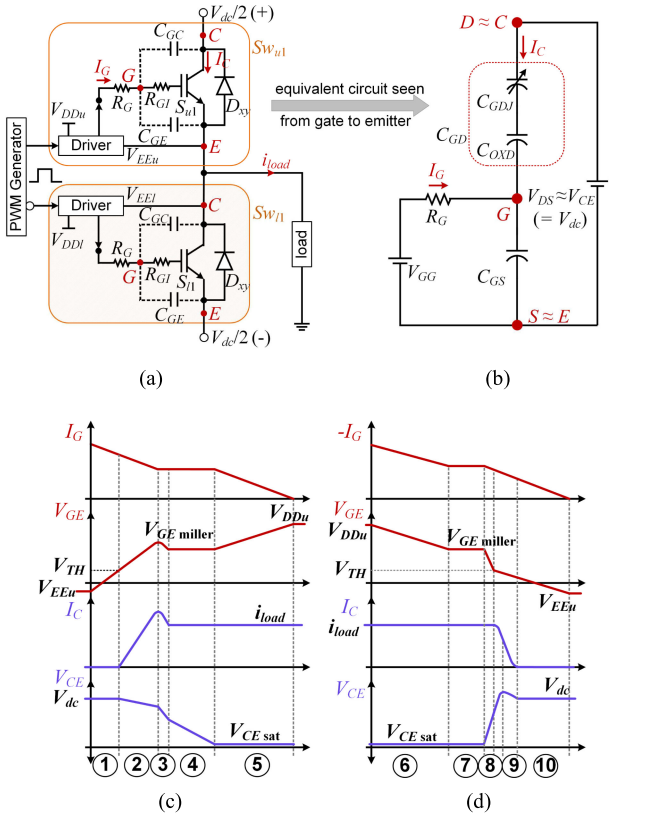

Fig. 1. Switching characteristics of the IGBT. (a) Circuit diagram of a single PWM inverter *leg*. (b) Equivalent switch circuit model. (c) Turn-ON behavior. (d) Turn-OFF behavior.

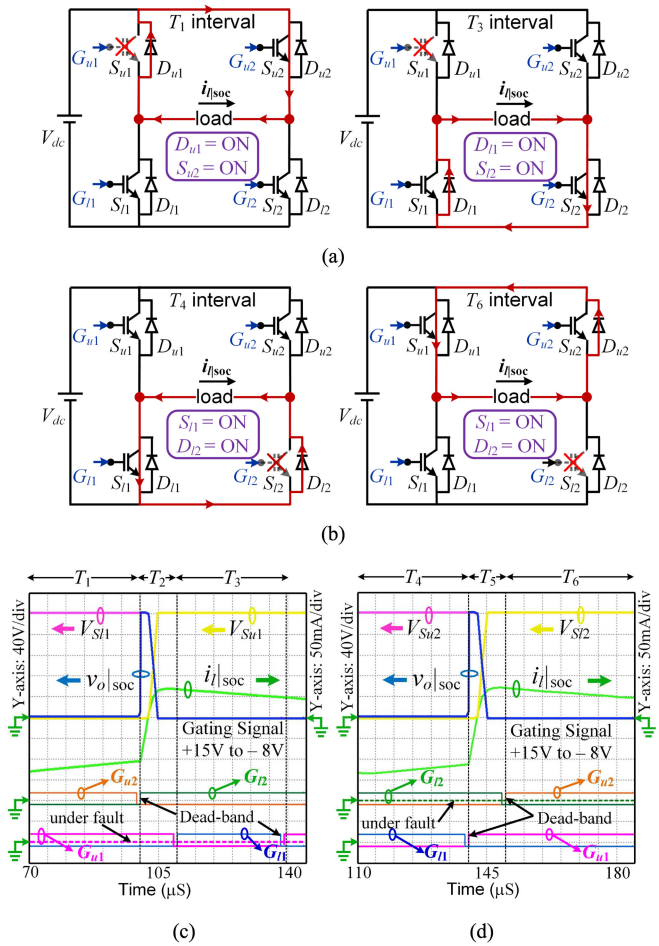

Fig. 2. Characterization of switch faults. (a) and (b) H-bridge cell with load current path under $SF_{u1\mathrm{SOC}}$ and $SF_{l2\mathrm{SOC}}$, respectively. (c) and (d) Switch voltages across faulty *leg*, output voltage, load current, and switching states under $SF_{u1\mathrm{SOC}}$ and $SF_{l2\mathrm{SOC}}$, respectively.

drain–source voltage V_{DS}. The gate to drain region is of major concern because of higher mobility of carriers in the channel during turn-ON process, the capacitance of this region C_{GD} can be modeled using variable depletion zone capacitance C_{GDJ} and fixed oxide zone capacitance C_{OXD} [29]. The turn-ON and turn-OFF characteristics of the transistor are shown in Fig. 1(c) and (d), respectively. The explanation of all the regions is readily available [2], [30]. The switching logics of both the switches in the same *leg* are complementary in nature. Furthermore, if the upper switch Sw_{u1} is switched-OFF, then the voltage developed across the switch is V_{dc}. To make the switch Sw_{u1} turned-ON, the gate charge is needed and it is fulfilled by the gate current I_G. Similarly, the total gate charge required for the turn-ON and turn-OFF process of the transistor is supplied from the driver circuit.

The effect of nonidealities of semiconductor switches is used during turn-ON and turn-OFF to identify the specific switch fault location. According to the behavior of the output voltage, current characteristics, and switching logics, the unique identification technique is developed for OCSFs. Fig. 2(a) and (b) shows the current path during fault in S_{u1} with a healthy diode ($SF_{u1\mathrm{SOC}}$) and fault in S_{l2} with a healthy diode ($SF_{l2\mathrm{SOC}}$) for a three-level H-bridge or a power cell of CHB inverter, respectively. The two legs (i.e., *leg* 1 and *leg* 2) of a power cell consist: two upper switches S_{u1} and S_{u2} and two lower switches S_{l1} and S_{l2} with antiparallel diodes D_{u1}, D_{u2} and D_{l1}, D_{l2}, respectively. The combination of the switch–diode pair is represented as Sw_{xy}, where x is upper/lower switch and y is *leg* number. The switching behavior of an international rectifier AUIRGP4063D (IGBT with ultrafast soft recovery diode) is captured using MultiSim software and is plotted in Fig. 2(c) and (d) under $SF_{u1\mathrm{SOC}}$ and $SF_{l2\mathrm{SOC}}$, respectively, which shows the voltages across the switches in the respective faulty *leg*, load current $i_l|_{\mathrm{soc}}$, and pulsewidth-modulated inverter (PWMI) output voltage $v_o|_{\mathrm{soc}}$. These cases are possible only with the healthy diode operation where the freewheeling action of the current is possible. The switching behavior under $SF_{u1\mathrm{SOC}}$ can be discussed for three different intervals as follows.

1) T_1: S_{u1}—Under fault, and S_{u2}—ON. The switch voltages $V_{Su1} \approx 0$ (small ON-state diode voltage), $V_{Sl1} = V_{\mathrm{dc}}$ and $v_o|_{\mathrm{soc}} \approx 0$; the current direction is negative and the load current path is shown in Fig. 2(a), i.e., from D_{u1} to S_{u2} to load.

2) T_2: Transition state (TS). The direction of the current changes from negative to positive, therefore, antiparallel diode D_{l1} is switched-ON and the voltage developed across V_{Sl1} is released through load; the load current path is changed from T_1 interval to T_3 interval.

3) T_3: S_{l1}—ON and S_{l2}—ON. The switch voltages $V_{Sl1} \approx 0$, $V_{Su1} = V_{\mathrm{dc}}$, and $v_o|_{\mathrm{soc}} \approx 0$; the current direction is positive and

TABLE I
OPERATING MODES

Operating modes	mode 1	mode 2	mode 3	mode 4
v_{mod1}	positive	positive	negative	negative
i_l	positive	negative	positive	negative

load current path is shown in Fig. 2(a), i.e., from D_{l1} to load to S_{l2}.

Similarly, the operation can be discussed for the diagonally opposite switch fault $SF_{l2\mathrm{SOC}}$ as follows.

4) T_4: S_{l2}—Under fault and S_{l1}—ON. The switch voltages $V_{Sl2} \approx 0$ (small ON-state diode voltage), $V_{Su2} = V_{\mathrm{dc}}$ and $v_o|_{\mathrm{soc}} \approx 0$; the current direction is negative and the load current path is shown in Fig. 2(b), i.e., S_{l1} to D_{l2} to load.

5) T_5: Transition state (TS). The direction of the current changes from negative to positive, therefore, antiparallel diode D_{u1} is switched-ON and the voltage developed across V_{Su1} is released through load; the load current path is changed from T_4 interval to T_6 interval.

6) T_6: S_{u1}—ON and S_{u2}—ON. The switch voltages $V_{Su2} \approx 0$, $V_{Sl2} = V_{\mathrm{dc}}$, and $v_o|_{\mathrm{soc}} \approx 0$; the current direction is positive and the load current path is shown in Fig. 2(b), i.e., from S_{u1} to load to D_{u2}.

III. CHARACTERIZATION AND IDENTIFICATION OF OPEN SWITCH FAULTS IN H-BRIDGE POWER CELLS

The healthy operation of the H-bridge power cell output with inductive load can be classified into four operating modes with respect to PWMI voltage output and load current characteristics as given in Table I, where v_{mod1} is sinusoidal modulating waveform with zero phase shift. All the four operating modes are possible only under healthy operation with inductive load. Therefore, the detection technique is developed with respect to the PWMI output voltage error v_{err} with respective switching states and load current i_l; where the PWMI output voltage error and v_{err} is the unit resultant of the actual PWMI output voltage to the reference PWMI output voltage.

Fig. 3(a) shows a well-known unipolar sinusoidal pulsewidth modulation (SPWM) technique, where the gating signals are the resultant of comparison between two 180° phase-shifted modulating sinusoidal signals $v_{\mathrm{mod1}}(t)$, $v_{\mathrm{mod2}}(t)$ and a high-frequency triangular carrier signal $v_{\mathrm{tri}}(t)$. The three-level voltage output (i.e., $V_o = +V_{\mathrm{dc}}, 0, -V_{\mathrm{dc}}$) with switching states and load current under healthy operation of the H-bridge power cell is shown in Fig. 3(b). The generated gating logics G_{u1}, G_{l2} and G_{u2}, G_{l1} are shown in Fig. 3(c) and (f), respectively. The PWMI voltage output with all switching states and load current of the H-bridge power cell under $SF_{u1\mathrm{soc}}$, $SF_{l2\mathrm{soc}}$, $SF_{u2\mathrm{soc}}$, and $SF_{l1\mathrm{soc}}$ are shown in Fig. 3(d), (e), (g), and (h), respectively. The instantaneous switching states over a fundamental period under the PSPWM technique are presented. Due to the space constraint, the switch and diode symbols are changed in Fig. 3 as follows: the switches S_{u1}, S_{l1}, S_{u2}, and S_{l2} are replaced by S_1, S_2, S_3, and S_4, respectively, and the diodes D_{u1}, D_{l1}, D_{u2}, and D_{l2} are replaced by D_1, D_2, D_3, and D_4, respectively. The similar switching behavior is achieved under same modes

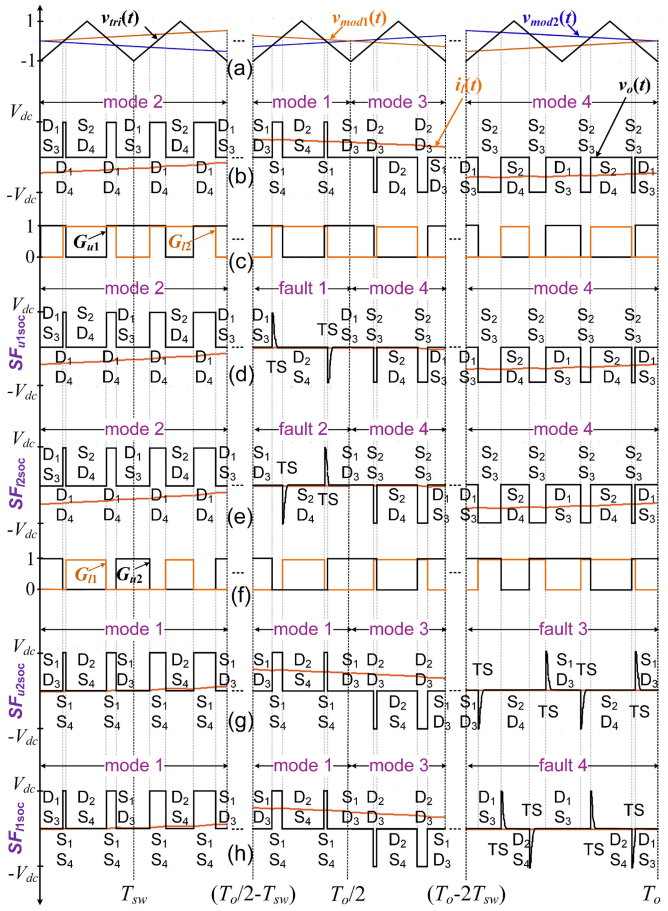

Fig. 3. Switching characteristics and modes of operations of the power cell under different switch fault conditions. (a) Comparison between triangular carrier and modulating signals. (b) PWMI output voltage and load current under healthy condition. (c) Switching signal G_{u1} and G_{l2}. (d) and (e) PWMI output voltage and load current under $SF_{u1\mathrm{soc}}$ and $SF_{l2\mathrm{soc}}$, respectively. (f) Switching signal G_{u2} and G_{l1}. (g) and (h) PWMI output voltage and load current under $SF_{u2\mathrm{soc}}$ and $SF_{l1\mathrm{soc}}$, respectively.

of operation in all fault conditions but a unique fault mode is appeared with different SOC faults. In TS, the load current direction i_l changed with respect to the direction of v_{mod1}. The PWMI voltage output or the fault signature under diagonally opposite switch pairs $SF_{u1\mathrm{soc}}$, $SF_{l2\mathrm{soc}}$ and $SF_{u2\mathrm{soc}}$, $SF_{l1\mathrm{soc}}$ are similar, therefore, a unique detection algorithm is designed for the identification of the faulty switch within the H-bridge power cell. The identification and characterization of three different types of faults are discussed in further subsections.

A. Open Switch Fault Identification With a Healthy Diode ($\mathrm{SF}_{\mathrm{xy}soc}$)

Fig. 4(a) and (b) shows the output of the H-bridge power cell under $SF_{u1\mathrm{soc}}$ and $SF_{l2\mathrm{soc}}$, respectively. It can be seen from the zoomed section that the direction of the current changes during transition states under the fault condition. During $SF_{u1\mathrm{soc}}$ fault, the value of $i_l|_{\mathrm{soc}} > 0$, if the switching logic G_{l2} is high, and $i_l|_{\mathrm{soc}} < 0$, if the switching logic G_{l2} is low. Similarly, under other switch fault conditions, the switching states and load current relation can be identified. The relation between voltage spikes

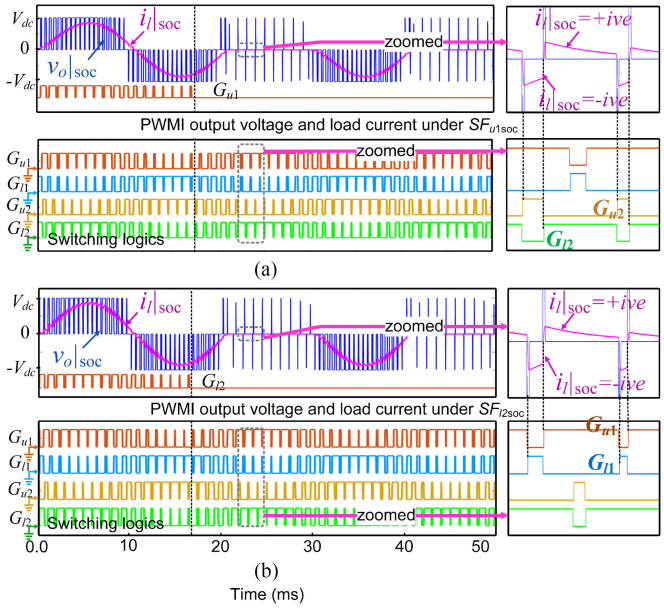

Fig. 4. Load current, PWM output voltage, switching states, and the zoomed view under (a) $SF_{u1\mathrm{soc}}$ and (b) $SF_{l2\mathrm{soc}}$.

and switching logics can also be developed with respect to Fig. 4(a) and (b) for $SF_{u1\mathrm{soc}}$ and $SF_{l2\mathrm{soc}}$, respectively. It can be seen from the zoomed section of Fig. 4(a) that a negative and a positive voltage spike appeared with the rising edge of G_{u2} and G_{l2}, respectively, when $v_{\mathrm{mod1}} > 0$ and $i_l|_{\mathrm{soc}} \approx 0$. The zoomed section of Fig. 4(b) shows that a negative and a positive voltage spike appeared with the rising edge of G_{l1} and G_{u1}, respectively, when $v_{\mathrm{mod1}} > 0$ and $i_l|_{\mathrm{soc}} \approx 0$. Similarly, the relation can be developed between voltage spikes and switching logics for other diagonally opposite switch faults $SF_{u2\mathrm{soc}}$ and $SF_{l1\mathrm{soc}}$.

Fig. 5 shows the unit magnitude of the PWMI output voltage and designing procedure of fault detection techniques with the consideration of different system delays under healthy and $SF_{u1\mathrm{soc}}$ conditions during mode 1, i.e., $v_{\mathrm{mod1}} > 0$ and $i_l > 0$. The unit magnitude of the ideal inverter output voltage can be defined as the summing resultant of G_{u1} and $-G_{u2}$; furthermore, the rising and falling edges of the resultant are shifted with dead time T_d and it is defined as reference PWMI output voltage v_{r}. The voltage sensor outputs are presented as $v_{os|\mathrm{h}}$ and $v_{os|\mathrm{f}}$ under healthy and faulty conditions, respectively. The combined effect of the sensor delay (T_{sd}), processing delay of the controller, and turn-ON / turn-OFF switching delays are considered as T_D. Further with respect to the sampling time (T_s) of the analog-to-digital converter, the voltage that is compared with the reference PWMI output voltage v_{r} is defined as actual PWMI output voltage $v_{\mathrm{act|h}}$ and $v_{\mathrm{act|f}}$ under healthy and faulty conditions, respectively. The counter frequency to switching frequency ratio m is considered as 16. Fig. 5 shows the consideration of the nonideal parameter of system delays, which is responsible for the nonzero values of $v_{\mathrm{err|h}}$, resulting in the counter value reaches $k_{\mathrm{count}} = 6$. Since the value of $k_{\mathrm{count}} = 6$ ($= k_{\mathrm{healthy}}$, i.e., the value of counter under healthy condition), therefore, to reduce the probability of false detection, the value of k_{count} should be greater than k_{healthy}, whereas during the SOC fault, the nonzero instants of $v_{\mathrm{err|f}}$ increases, resulting in the counter value reaches

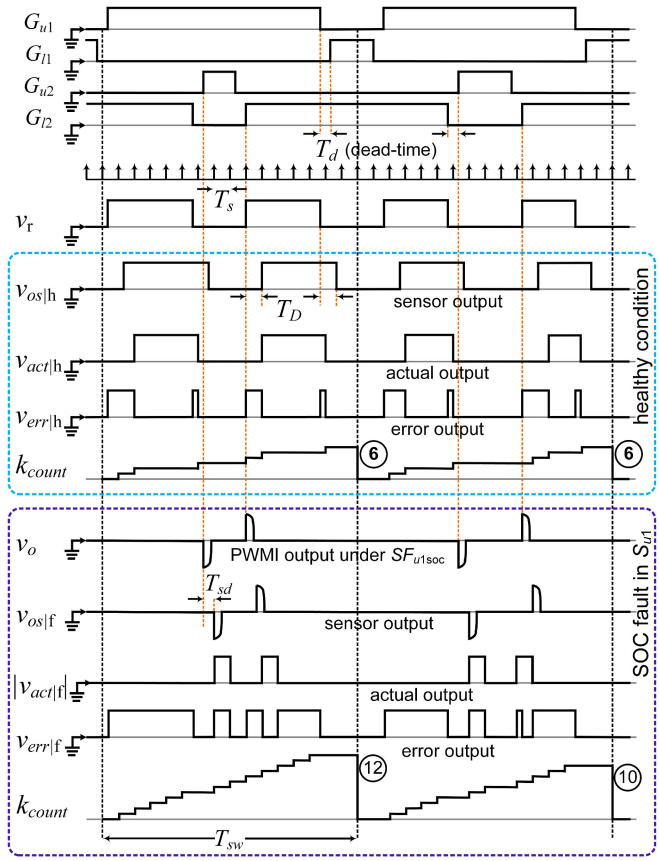

Fig. 5. Characterization of PWMI output voltage under healthy, $SF_{u1\mathrm{soc}}$, conditions in mode 1 (i.e., positive voltage and current) and development of fault detection techniques with the consideration of different system delays.

$k_{\mathrm{count}} = 12$. Since the value of $k_{\mathrm{count}} > k_{\mathrm{healthy}}$, i.e., greater than the counter value under healthy condition, therefore, the fault detection logic signal becomes "high."

Fig. 6 shows the flowchart of the proposed OCSF detection and identification algorithm. The flowchart is divided into two parts and each part is further divided into two subparts. The first part (under orange shade) represents the procedure to detect the fault under diagonally opposite switch pairs, and the subpart is used to reduce the probability of false detection. The counter frequency f_{count} is equal to ($m \times f_{\mathrm{sw}}$), where m is an integer and f_{sw} is the switching frequency. Threshold value N is chosen, such that $k_{\mathrm{healthy}} < N < m$. With the increase in the value of N from k_{healthy}, the probability of false fault identification reduces. It also slighty increases the switch fault identification period. In this manuscript, $N > 0.5 \times m$ is chosen to minimize the false detection, and in real-time implementation, $m = 10$ and $N = 7$ is considered. The second part (under blue shade) represents the identification of a specific switch fault.

The proposed OCSF algorithm is implemented and it is presented as a detection logic design block for SOC faults ($\mathrm{DLDB_{soc}}$) in Fig. 7. The specific fault locations $SF_{xy\mathrm{soc}}$ can be detected and identified using three input variables such as actual output voltage v_{act} (sensor output), respective switching logic, and v_{mod1} (internal signal generated by controller). The relation between switching logics and specific switch faults, the faulty modes, and partial faulty modes under different switch faults

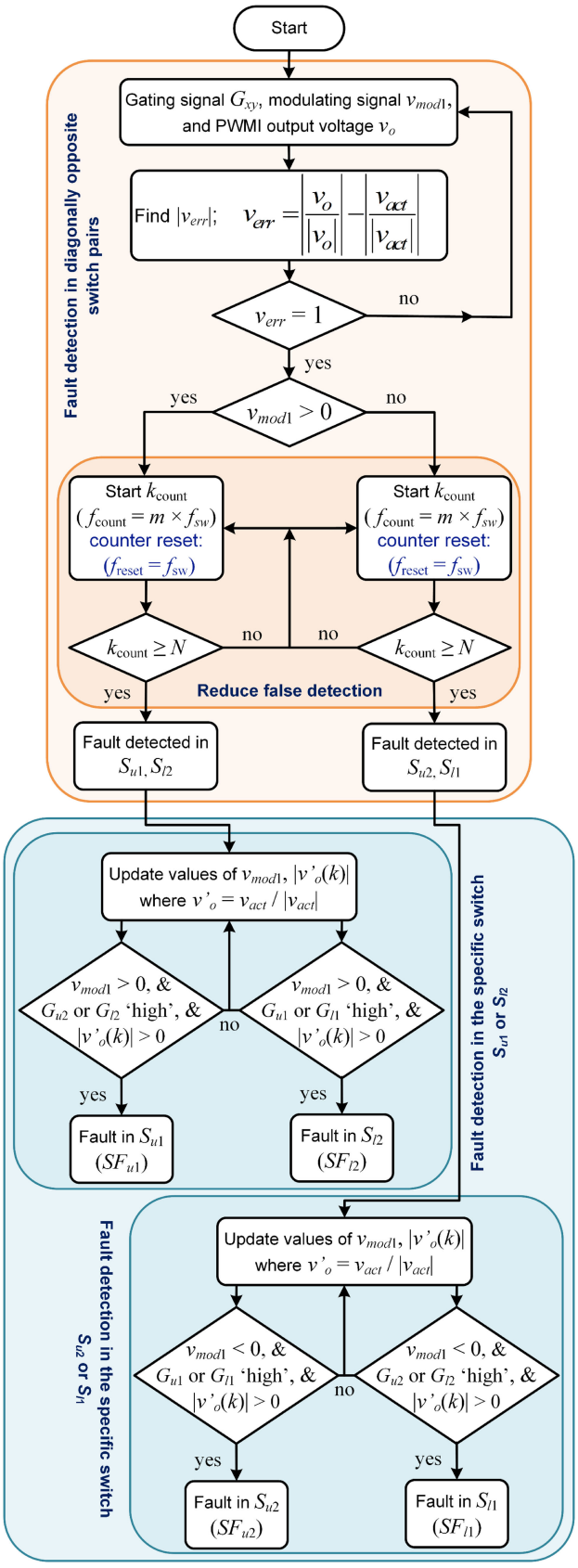

Fig. 6. Flowchart for the proposed OCSF algorithm with fault detection and fault identification.

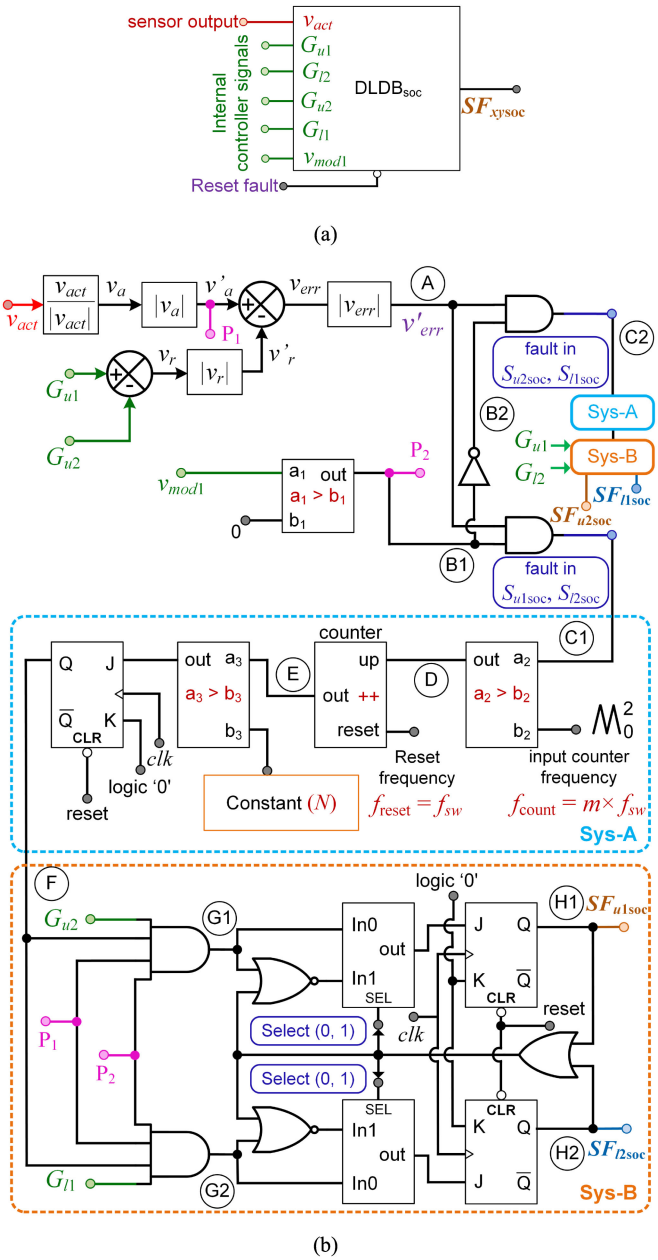

Fig. 7. Proposed SOC fault detection logic design. (a) Block diagram with respective input and output fault logic. (b) Internal schematic diagram for the fault identification system.

TABLE II
FAULT DETECTION SIGNAL UNDER DIFFERENT OCSFS CONDITIONS

Fault location	SF_{u1soc}	SF_{l1soc}	SF_{u2soc}	SF_{l2soc}
Detection signal	G_{l2}	G_{u2}	G_{l1}	G_{u1}
Faulty mode	mode 1	mode 4	mode 4	mode 1,
Partial faulty mode	mode 3	mode 2	mode 2	mode 3

are mentioned in Table II. The internal schematic of DLDB$_{soc}$ is presented in Fig. 7(b). It is divided into the following three parts:

1) the fault signal is bifurcated into diagonally opposite switch pairs;

2) to reduce the probability of false fault detection;

3) the fault signal is bifurcated within diagonally opposite switch pairs, i.e., the specific switch fault locations are identified.

The second and third parts of design logic are similar for all the four switch faults. To generate constant frequency pulse train, a high frequency ($= m \times f_{\rm sw}$) triangular waveform is used. In the simulation results, the value of $m = 100$ is considered, whereas the value of $N = 70$ is chosen. If a continuous high logic output is generated through an AND logic operator at C1 within switching period $T_{\rm sw}$, then the counter generates a ramp with peak magnitude m and frequency $f_{\rm sw}$. It is further compared with a constant value N. If the magnitude of the generated ramp signal is higher than the constant value, then the fault detection logic becomes high and one of the switch pair $SF_{u1\rm soc}$, $SF_{l2\rm soc}$ or $SF_{u2\rm soc}$, $SF_{l1\rm soc}$ is detected within a couple of switching frequencies. Furthermore, the output is processed through Sys-B, through which the exact switch fault location for the SOC fault is identified. Once the fault is detected through the $\rm DLDB_{soc}$, then the system should be reset for the next fault detection and switch identification.

B. Open Diode Fault Identification With Healthy Switch ($SF_{\rm xy\,DOC}$)

The probability of $SF_{xy\rm DOC}$ is very low and uncommon. This type of fault can be detected using three input variables such as load current i_l, modulating signal $v_{\rm mod1}$, and respective switching logic. The detection logic design block for DOC faults ($\rm DLDB_{DOC}$) and internal schematic of $\rm DLDB_{DOC}$ are shown in Fig. 8(a) and (b), respectively. The relationship between input switching logics and output diode fault location is also mentioned in Fig. 8. The counter frequency is m times of the switching frequency. Since the load current becomes zero within two switching period due to the unavailability of the freewheeling current path under the open diode fault, therefore, the counter is reseted after two switching periods. The counter is compared with a constant value ($= 2m - \%r$), where r represents the system delays. The value of r is chosen 4% of the value of m.

C. Switch–Diode Pair Open Fault Identification ($SF_{\rm xy\,oc}$)

The free-wheeling action of the current through the diode under SF_{xyoc} is not possible resulting in a huge voltage spike during switching in the power cell similar to the DOC fault. The healthy PWMI output voltage is also missing similar to the SOC fault. This type of fault can be detected using AND operation of the output of $\rm DLDB_{SOC}$ and $\rm DLDB_{DOC}$. If the output of these two-detection block signal logic "*high*" indicates the fault in the respective switch–diode pair.

IV. Formulation and Analysis of OCSFs

The analytical solutions of OCSFs in the H-bridge power cell with the PSPWM technique can be mathematically derived in time domain using the double Fourier integral with the consideration of ideal switching conditions. The integral solutions are obtained using Jacobi–Anger expansions [31], [32]. The three-level inverter output voltage can be derived using (1), where $u_a(t)$

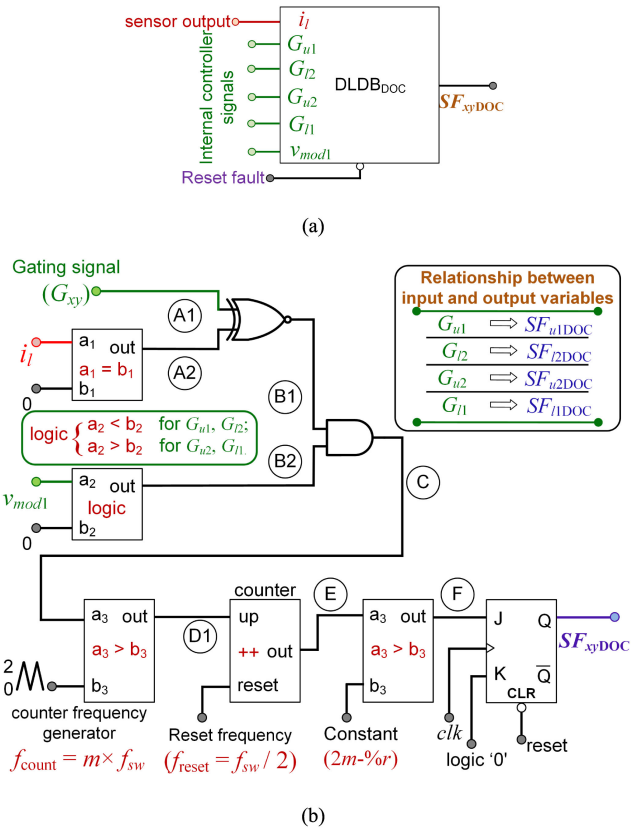

Fig. 8. Proposed DOC fault detection logic design. (a) Block diagram with respective input and output fault logic. (b) Internal schematic diagram of the fault identification system.

and $u_b(t)$ are the analytical expressions of output gating signal generated using PSPWM with phase-shifted modulating signals at $\theta = 0$ and $-\pi$ for *leg* 1 and 2, respectively. The expressions for u_a and u_b are available in [33] and [34] and are presented in (2a) and (2b), respectively; where M is modulation index, ω_o and ω_c are fundamental and carrier frequencies in rad/s, θ_c is the phase shift for the carrier signal, $J_p(\xi)$ is the pth-order Bessel function, and p and q are base band and side band indices, respectively

$$v_o(t) = \left\{ u_a(t)|_{\theta=0} - u_b(t)|_{\theta=-\pi} \right\} V_{\rm dc} = \{u_a - u_b\} V_{\rm dc} \tag{1}$$

$$u_a = \frac{(1 + M\cos\omega_o t)}{2} + \frac{2}{\pi}\sum_{p=1}^{\infty}\sum_{q=-\infty}^{\infty}\frac{1}{p}\left\{\sin\left(\frac{(p+q)}{2/\pi}\right) \times J_q\left(\frac{p\pi M}{2}\right) \times \cos\left(p\left(\omega_c t + \theta_c\right) + q\omega_o t\right)\right\} \tag{2a}$$

$$u_b = \frac{1 + M\cos\left(\omega_o t - \pi\right)}{2} + \frac{2}{\pi}\sum_{p=1}^{\infty}\sum_{q=-\infty}^{\infty}\frac{1}{p}\left\{\sin\left(\frac{(p+q)}{2/\pi}\right) \times J_q\left(\frac{p\pi M}{2}\right) \times \cos\left(p\left(\omega_c t + \theta_c\right) + q\left(\omega_o t - \pi\right)\right)\right\}. \tag{2b}$$

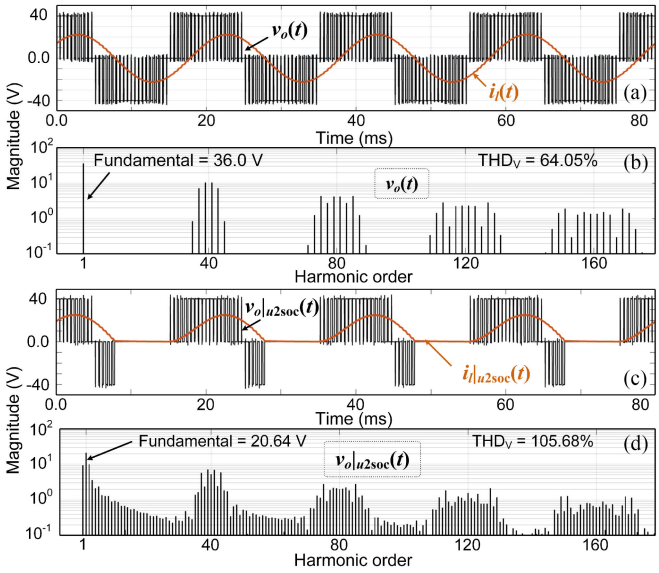

Fig. 9. Analytical results of PWMI output voltage with load current and voltage harmonic spectrum under (a) and (b) healthy condition and (c) and (d) $SF_{u2\mathrm{soc}}$.

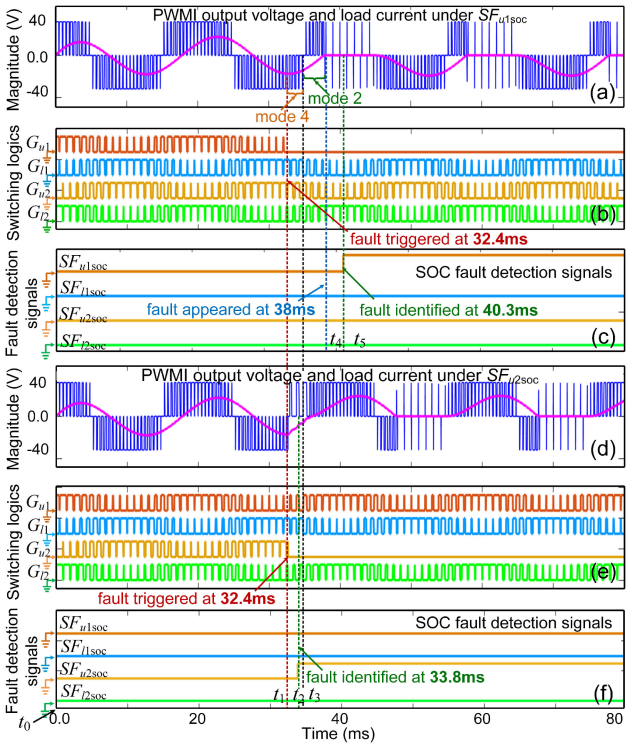

Fig. 10. Characterization, switching states, and identification of SOC fault for (a)–(c) $S_{u1\mathrm{soc}}$ and (d)–(f) $S_{u2\mathrm{soc}}$, respectively.

The PSPWM inverter output voltage $v_o(t)$ (where $v_o(t) = u_o(t) \times V_{\mathrm{dc}}$) and load current i_l under healthy operation can be derived using (2a) and (2b) as follows:

$$u_o(t) = M\cos(\omega_o t) + \frac{4}{\pi}\sum_{p=1}^{\infty}\sum_{q=-\infty}^{\infty}\frac{1}{2p}\times J_{2q-1}(p\pi M)\times$$

$$\cos((p+q-1)\pi)\times\cos(2p(\omega_c t+\theta_c)+(2q-1)\omega_o t) \quad (3)$$

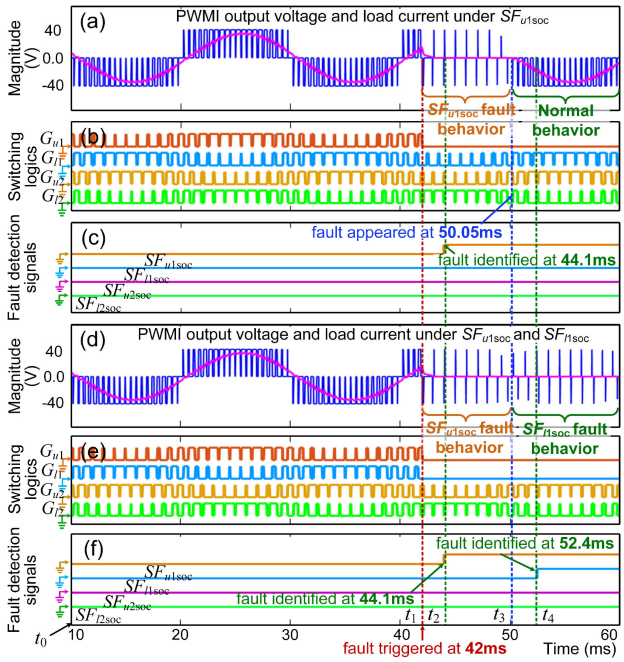

Fig. 11. Characterization, switching states, and identification of SOC faults for (a)–(c) single switch fault $SF_{u1\mathrm{soc}}$ and (d)–(f) multiple switch faults in the same leg $SF_{u1\mathrm{soc}}$, $SF_{l1\mathrm{soc}}$, respectively.

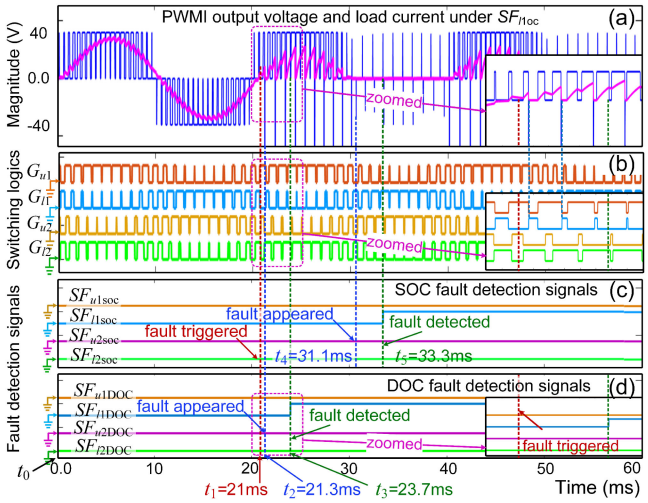

Fig. 12. Detection and identification of OC faults PWMI output voltage with load current, switching states, and fault detection signals under $SF_{l1\mathrm{oc}}$.

$$u_o V_{\mathrm{dc}} - L\frac{di_l}{dt} - Ri_l = 0 \Rightarrow I_l = \frac{V_{dc}}{sL+R}U_o(s). \quad (4)$$

The PWMI output voltage during SOC and OC are similar and it is derived further; whereas under DOC, the PWMI output voltage is similar as healthy operation as given in (3). As discussed in the previous section, some of the modes of the operation are disappeared or affected during $SF_{xy\mathrm{soc}}$. Mathematical relations are developed for the PWMI output voltage $v_o|_{xy\mathrm{soc}}$ and load current $i_l|_{xy\mathrm{soc}}$ and it is presented in (5); whereas different switch fault relations are derived and presented in (6a)–(6d). The first term of (6) represents the unit magnitude of the PWMI output

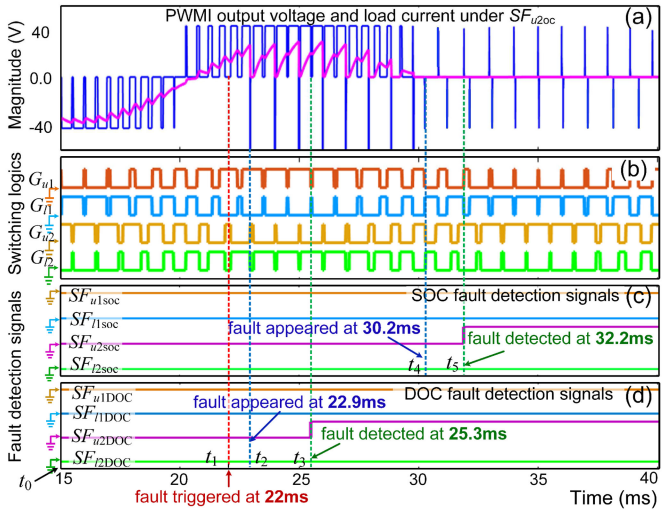

Fig. 13. Detection and identification of OC faults: PWMI output voltage with load current, switching states, and fault detection signals under SF_{u2oc} at switching frequency f_c.

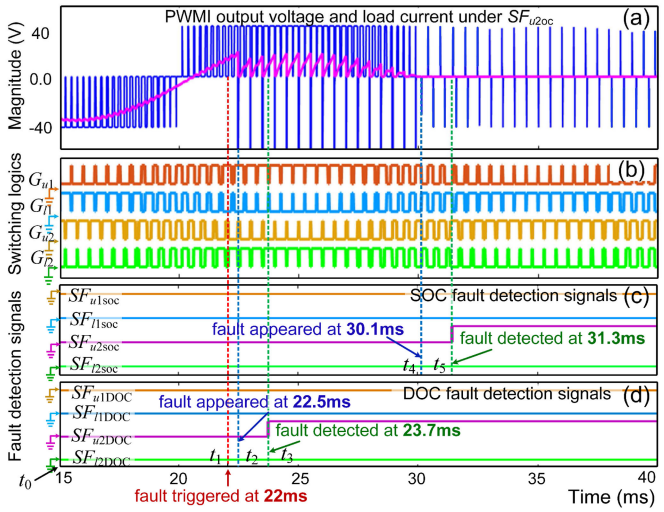

Fig. 14. Detection and identification of OC faults: PWMI output voltage with load current, switching states, and fault detection signals under SF_{u2oc} at switching frequency $2\times f_c$.

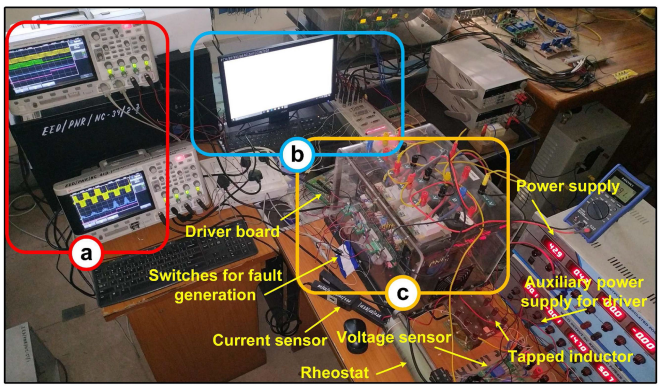

Fig. 15. Experimental setup. (a) Synchronized oscilloscopes. (b) Computer with dSPACE 1104. (c) H-bridge cell with other system components.

TABLE III
PERFORMANCE RESULT OF THE PROPOSED FAULT DETECTION AND SWITCH IDENTIFICATION ALGORITHM

Fault type		Description		Switch fault identification time T_{sid}	Results	Undetected region T_d / comment's
Single switch fault	*a.*	SF_{u1soc}		2.3 ms	Fig. 10 (a)	5.6 ms
		SF_{u2soc}		1.4 ms	Fig. 10 (d)	0 ms / identified under partial fault mode
	b.	SF_{u1soc}		2.0 ms	Fig. 11 (a)	0 ms
	c.	SF_{l1oc}		2.4 ms	Fig. 12	0.3 ms / switch-diode pair fault
		SF_{u2oc}		2.4 ms	Fig. 13	0.9 ms / switch-diode pair fault
	d.	SF_{u2oc}		1.2 ms	Fig. 14	0.5 ms / switch-diode pair fault and at $2\times f_{sw}$
	e.	SF_{u1soc}		2.5 ms	Fig. 16 (a)	2.0 ms
		SF_{l2soc}		2.6 ms	Fig. 16 (b)	9.0 ms
		SF_{u2soc}		2.2 ms	Fig. 16 (c)	9.5 ms
		SF_{l1soc}		2.7 ms	Fig. 16 (d)	10.0 ms
Multiple switch fault	*f.*	*leg*-1	SF_{u1soc}	2.1 ms	Fig. 11 (d)	0 ms
			SF_{l1soc}	2.35 ms		8.05 ms

voltage with the consideration of respective faulty modes as given in Table III, whereas the second term of (6) represents the characteristics of the fault occurred in SF_{u1soc}, SF_{l2soc} and SF_{u2soc}, SF_{l1soc} during $i_l|_{xysoc} > 0$ and $i_l|_{xysoc} < 0$, respectively. It considers the respective partially faulty modes as given in Table III, i.e., the time of fault occurrence follows the current conditions, resulting in the change in the H-bridge inverter switched output voltage

$$v_o|_{xysoc} = u_o|_{xysoc} \times V_{dc} \tag{5a}$$

$$sL\, I_l|_{xysoc} - L\, i_l|_{xysoc}(0) + R\, I_l|_{xysoc} = V_{dc} U_o(s) \tag{5b}$$

$$u_o|_{u1soc} = \underbrace{u_o(t)}_{\text{for all } i_l|_{xysoc} \le 0} - \underbrace{u_b(t)}_{\text{for all } i_l|_{xysoc} > 0} \tag{6a}$$

$$u_o|_{l1soc} = \underbrace{u_o(t)}_{\text{for all } i_l|_{xysoc} \ge 0} + \underbrace{\overline{u_b(t)}}_{\text{for all } i_l|_{xysoc} < 0} \tag{6b}$$

$$u_o|_{u2soc} = \underbrace{u_o(t)}_{\text{for all } i_l|_{xysoc} \ge 0} + \underbrace{u_a(t)}_{\text{for all } i_l|_{xysoc} < 0} \tag{6c}$$

$$u_o|_{l2soc} = \underbrace{u_o(t)}_{\text{for all } i_l|_{xysoc} \le 0} - \underbrace{\overline{u_a(t)}}_{\text{for all } i_l|_{xysoc} > 0}. \tag{6d}$$

V. RESULTS AND DISCUSSION

The system parameters are taken as follows: dc voltage supply for a single power cell $V_{dc} = 40$ V; fundamental (line) frequency $f_o = 50$ Hz; carrier (switching) frequency $f_{sw} = 1$ kHz; modulation index $M = 0.9$; and load impedance $Z_L = 1\ \Omega$, 4 mH; only for the representation of each mode, higher value of *L*/*R* is considered and results are presented in Figs. 9 and 10. Furthermore,

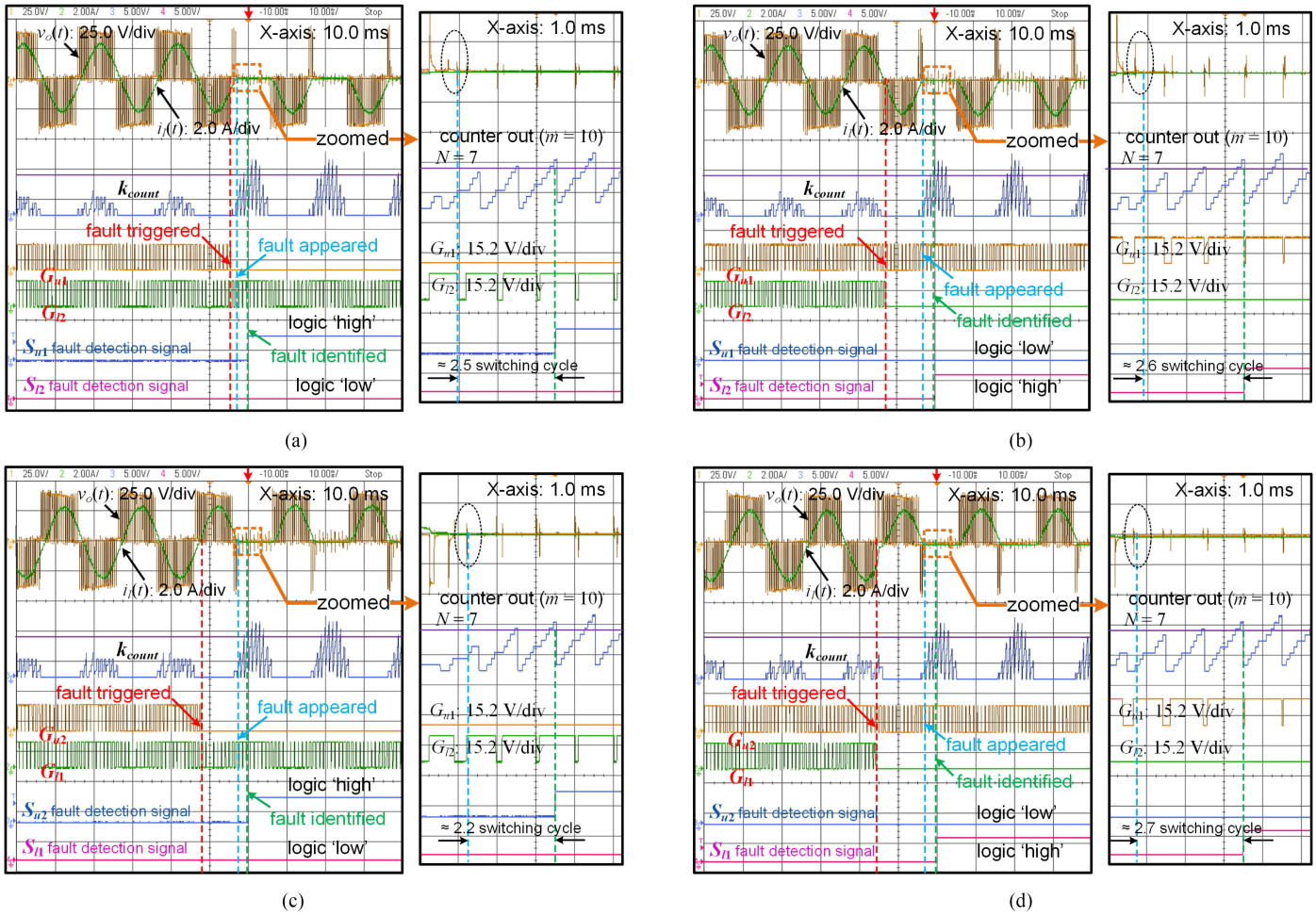

Fig. 16. PWMI output voltage, load current, counter output with threshold level $N = 7$, diagonally opposite switching logics, and respective fault identification signals for (a) $SF_{u1\text{soc}}$ with zoomed section, (b) $SF_{l2\text{soc}}$ with zoomed section, (c) $SF_{u2\text{soc}}$ with zoomed section, and (d) $SF_{l1\text{soc}}$ with zoomed section.

the algorithm is also verified with other load impedance (i.e., $Z_L = 15\ \Omega$, 10 mH; presented in Figs. 11–14 and 16) and switching frequency (i.e., $f_{\text{sw}} = 2$ kHz; presented in Fig. 14). These are only test parameters and the results are equally valid on other system parameters and switching frequencies. Fig. 9(a)–(d) are plotted using respective mathematical relations derived for healthy and SOC fault conditions. The modulating signal is used as a cosine function of time in Fig. 9 for the verification of the proposed detection technique. Since the load current characteristics is the function of the PWMI output voltage, therefore, in the analytical output waveform, it is difficult to consider the effect of $i_l|_{SFu2\text{soc}} < 0$ (i.e., second term of (6.c) or partially faulty mode (*mode* 2) as given in Table II) under the $SF_{u2\text{soc}}$ condition. Since the PWMI output voltage and current waveform changes under fault, therefore, the total harmonic distortion of the output voltage THD_V increases. It can be seen from Fig. 9(b) and (d).

The consideration of partially faulty modes and their effects are presented with the help of MATLAB simulations in Fig. 10. The SOC faults are triggered using gating signals in the upper switches (i.e., S_{u1} and S_{u2}) of the H-bridge cell. The fault is triggered at $t_1 = 32.4$ ms in both the cases under $SF_{u1\text{SOC}}$ and $SF_{u2\text{SOC}}$. After $t = t_1$, inverters in both the conditions are operating under *mode* 4 followed by *mode* 2, which is not a faulty mode for $SF_{u1\text{SOC}}$, therefore, in the first condition, the healthy output is generated and fault appeared after $t_4 = 38$ ms; and at $t_5 = 40.3$ ms, the fault with specific switch location is identified in couple of switching period. It is presented in Fig. 10(a)–(c). Whereas for $SF_{u2\text{SOC}}$, *mode* 4 is a faulty mode and *mode* 2 is a partially faulty mode, therefore, at the duration $t = t_1$–t_3, switch fault occurred because the load current has a negative value as discussed in the second term of (6c) and the PWMI output during this interval is $u_a(t)$; thereafter (i.e., $t > t_3$), the load current has positive value and the PWMI output during this interval is $u_o(t)$ from the first term of (6c). At $t_2 = 33.8$ ms, the fault with specific switch location is identified after couple of switching period. It is presented in Fig. 10(d)–(f).

Furthermore, load impedance $Z_L = 15\ \Omega$, 10 mH, and sinusoidal modulating signal are used for the verification of the proposed algorithm. The algorithm is verified for multiple switch faults in Fig. 11, which may occur due to overcurrent transients in an H-bridge. It may cause for simultaneous open-circuit faults in both the switches of the same leg. Fig. 11(a)–(c) shows the characteristics under a single open switch fault in $S_{u1\text{oc}}$ at

$t_1 = 42$ ms and the OCSF is identified at $t_2 = 44.1$ ms. The switch identification time period $T_{\rm sid}$ (i.e., the time duration between the fault appeared in the inverter output and faulty switch identification) is similar to Fig. 10(a)–(c) with different load. Fig. 11(d)–(f) shows the characteristics under multiple open switch faults in the same leg, i.e., in $S_{u1\rm oc}$, $S_{l1\rm oc}$ at $t_1 = 42$ ms. Similar to the previous case, the fault in $S_{u1\rm oc}$ is identified at $t_2 = 44.1$ ms, whereas $SF_{l1\rm oc}$ is appeared at $t_3 = 50.05$ ms and the faulty switch is identified at $t_4 = 52.4$ ms. This shows the verification of the proposed algorithm with different load and multiple open switch fault conditions.

Fig. 12 shows the detection and identification of the switch–diode pair fault in *Sl*1oc. The OC faults occurred because of a complete breakdown of the switch with antiparallel diode combination, loosely connected wires within the H-bridge *leg*, etc. For such type of fault generation, circuit breakers are used before each switch–diode pair in the H-bridge. In OC faults, the feedback path of the load current is unavailable during the respective switching time region, therefore, the load current becomes zero once in each switching period with single open switch faults, due to which a large voltage spike appeared in each switching interval to make the load current zero within the small-time duration. To verify the OC faults experimentally, circuit breakers / jumpers can be used with switch–diode pair. Fig. 12 shows all the behavior of switch faults discussed before. The circuit breaker across Sw_{l1} is opened at $t_1 = 21$ ms (i.e., $t_0 - t_1$: Healthy operation); the effect of the diode fault occurred after $t_2 = 21.3$ ms, and thereafter, huge voltage spikes appeared at PWMI output, and DOC fault detection logic became high within couple of switching period at $t_3 = 23.9$ ms; again, from $t_4 = 31.1$ ms, the effect of the switch fault occurred, and SOC fault detection logic became high within couple of switching period at $t_5 = 33.5$ ms. The OCSFs (i.e., $SF_{l1\rm soc}$ and $SF_{l1\rm oc}$) can be identified in couple of switching period, and thereafter, the postfault control technique can be implemented. From zoomed sections of the respective Fig. 12, it can be seen that the load current became zero when G_{l1} is high under $SF_{l1\rm oc}$. The similar logics are used to detect OC faults. Since the fault is triggered at $t_1 = 21$ms (i.e., $v_{\rm mod1} > 0$), therefore, initially, the DOC fault is detected, and thereafter, SOC fault is detected.

Furthermore, the proposed detection algorithm is verified with different switching frequencies f_c and $2\times f_c$, and results are presented under open switch fault $SF_{u2\rm oc}$ in Figs. 13 and 14, respectively. Since the frequency of operation is increased, therefore, the results plotted in Figs. 13 and 14 are captured for 25 ms (i.e., 15–40 ms). The open-circuit fault in Sw_{u2} is triggered at $t_1 = 22$ ms (i.e., $t_0 - t_1$: Healthy operation); the effect of the diode fault occurred in the PWMI output voltage at $t_2 = 22.9$ ms (in Fig. 13) and $t_2 = 22.5$ ms (in Fig. 14); thereafter, the DOC fault detection logic became high within couple of switching period at $t_3 = 25.3$ ms (in Fig. 13) and $t_3 = 23.7$ ms (in Fig. 14); again, at $t_4 = 30.2$ ms (in Fig. 13) and $t_4 = 30.1$ ms (in Fig. 14), the effect of the switch fault occurred in the PWMI output voltage and SOC fault detection logic became high within couple of switching period at $t_5 = 32.2$ ms (in Fig. 13) and $t_5 = 31.3$ ms (in Fig. 14). Therefore, for switching frequency f_c, the DOC fault in Sw_{u2} is detected in 2.4 ms, which is further reduced to 1.2 ms if the operating switching frequency is increased to $2\times f_c$; similarly, the SOC fault in Sw_{u2} is detected in 2.0 and 1.2 ms at operating switching frequencies f_c and $2\times f_c$, respectively. The fault signature in diagonally opposite switches Sw_{l1} and Sw_{u2} in an H-bridge power cell at same switching frequency are approximately identical and it can be seen from Figs. 12 and 13, respectively. It can be seen from Fig. 12 that the detection time for the DOC fault in Sw_{l1} is 2.4 ms, and for SOC fault in $Sw_{l1,}$ is 2.2 ms. The fault detection time is reduced with the increase of the switching frequency and it is approximately twice of the switching time period. Since the fault detection algorithm is based on switching logics and PWMI output voltage, therefore, at a higher switching frequency, high-speed controllers are required.

The experimental setup is shown in Fig. 15. It is developed in the laboratory to test and verify the proposed fault detection algorithm and simulated results in real time. The dSPACE 1104 digital controller is used to generate the PSPWM gating signals and implement the fault detection algorithm. The PWMI output voltage is feedback to the controller. The SOC faults are triggered manually with the help of series-connected external switches, which create an interrupt to the respective gating signals. Two *legs* of the H-bridge power cell are used to test the results. For the verification of the proposed algorithm, more than four outputs are required, therefore, two digital storage oscilloscopes are connected and synchronized to capture the results. The same system parameters are taken into consideration for real-time implementation and verification of simulated and analytical results.

The faults in all the four switches are triggered and the resulting PWMI output voltage and load current waveform are captured as shown in Fig. 16. The counter output, diagonally opposite gating signals, and fault identification signals are also presented for $SF_{u1\rm soc}$, $SF_{l2\rm soc}$ and $SF_{u2\rm soc}$, $SF_{l1\rm soc}$ in Fig. 16(a), (b) and (c), (d), respectively. The value of counter start increasing and reaches at a defined threshold level, i.e., $k_{\rm count} = N$, whenever the SOC fault is detected. As discussed in the fault identification algorithm, the counter start counts only with the nonzero values of $|v_{\rm err}|$, i.e., the change in the actual PWMI output voltage waveshape with respect to ideal output. But from Fig. 16, it can be seen that the nonzero counter values are present during healthy operation of switches and the approximate count of the counter is $k_{\rm count} \approx 4 = k_{\rm healthy}$. This value is due to sensor delay, sampling delay of the controller, rise-time and fall-time switching delay of the real time system, and processing delay. Therefore, to reduce the probability of false detection, the value of $N = 7$ is chosen. It can also be seen from the experimental results that diagonally opposite switch faults are approximately similar and each switch fault is detected and specific switch is identified approximately in 2.5 switching cycles.

The performance analysis of the proposed switch fault identification algorithm is presented in Table III. The switch identification time period ($T_{\rm sid}$) is presented for both: single switch faults and multiple switch faults. These faults are identified under several conditions for the verification of the proposed algorithm, such as, open switch faults (*a*, *b*, *e*, *f*), switch–diode pair open faults (*c*, *d*), increased switching frequency of operation (*d*), and

TABLE IV
COMPARISON BETWEEN THE PROPOSED FAULT DETECTION AND SWITCH IDENTIFICATION ALGORITHM WITH AVAILABLE DETECTION METHODS IN LITERATURE

Algorithms from literature	(T_d+T_{sid}) for single switch fault	(T_d+T_{sid}) for multiple switch fault	(T_d+T_{sid}) for switch-diode pair / diode fault	DOSFI under similar PWMI output voltage	Detection criteria	Computational complexity
[35]	~6×T_o	Not possible	Not possible	Not possible	FFT and principle component analysis (PCA)	High
[21]	~6×T_o	Not possible	Not possible	Not possible	Output phase voltage and PCA	High
[19]	~3×T_o	Not possible	Not possible	Not possible	Slope calculations and comparison	Moderate
[24]	~5×T_o	Not possible	Not possible	Not possible	Residual calculations and comparison	Moderate
[22]	~1×T_o	~1×T_o	Not possible	Not possible	Reference current predition and comparison	Moderate
[13]	~1×T_o	~1×T_o	Not possible	Not possible	Comparison of two variables	Low
Proposed method	~{(T_o/2)+(3×T_{sw})}	~{(T_o/2)+(3×T_{sw})}	~{(T_o/2)+(3×T_{sw})}	Possible	Comparison of variables	Low

$T_{\rm sid}$ = Switch identification period; T_d = Undetected region; T_o = Fundamental period; $T_{\rm sw}$ = Switching period; and # DOSFI = Diagonally opposite switch fault identification.

different loads (*a* and *b*, *c*, *d*, *e*, *f*). It shows that the proposed fault detection and switch identification algorithm is potentially able to identify switch fault location under single switch faults, multiple switch faults, open switch faults, switch–diode pair faults, and diagonally opposite switch fault conditions. The time period between the fault occurred and fault appeared at the inverter output is defined as undetected region (T_d), and the value of T_d depends on the instant at which the fault occurred and faulty switch location. The maximum possible value of T_d for the H-bridge power cell will be T_o/2 (i.e., half the fundamental period). Wheareas the switch identification time period ($T_{\rm sid}$) is defined as the time period between the fault appeared at inverter output and faulty switch identification. The switch identification time period ($T_{\rm sid}$) for the proposed algorithm is less than $3\times T_{\rm sw}$, where $T_{\rm sw}$ is the switching time period. Since the magnitude of $T_{\rm sid}$ depends on switching time period, therefore, at a higher switching frequency operation, faster switch fault identification can be achieved. The maximum time required for the fault detection and switch fault identification using the proposed algorithm is less than ($T_o/2 + 3\times T_{\rm sw}$). The comparison between the available OCSFs detection algorithm in the literature and the proposed algorithm is presented in Table IV.

VI. CONCLUSION

The semiconductor OCSFs are less critical than short-circuit faults for power converter operations, but the severity increases with the type of OCSFs. The output qualities and productivity of the power electronics systems are affected and it may also damage the complete system due to large voltage spikes during the switching transitions. Therefore, a fast OCSF detection algorithm is required to identify the switch faults within minimum switching transitions.

In this article, a fast OCSFs detection logic design is proposed for the H-bridge power cell. The OCSF can be detected and faulty switch can be identified within ($T_o/2 + 3\times T_{\rm sw}$) period for the H-bridge cell. In the H-bridge power cell, the fault signatures of diagonally opposite switch faults are approximately similar, therefore, it is difficult to identify unique switch fault location. This article presents a detection algorithm with unique identification for every faulty switch within an H-bridge power cell. The nonideal characteristics of semiconductor switches are used for the identification of OCSFs. The method compares the actual and ideal PWMI output voltage, the instant of voltage spikes due to nonideal switching characteristics with respect to switching states. The proposed algorithm can be applied for the identification of both single open switch fault and multiple open switch faults. It can also be applied for the identification of open switch faults and switch–diode pair fault. The proposed technique requires only one voltage sensor per H-bridge power cell for the SOC fault identification, whereas it requires one voltage and one current sensor per H-bridge power cell for all types of OCSFs. The PSPWM technique is used for the three-level voltage output generation but the proposed method can be further implemented for other modulation techniques and the design can also be extended for the cascaded H-bridge-based multilevel inverters.

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