Proposed System Based on a Three-Level Boost Converter to Mitigate Voltage Imbalance in Photovoltaic Power Generation Systems

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***Abstract*—Voltage imbalance poses a challenge to photovoltaic systems. A modular structure based on a three-level boost converter is proposed to address this problem. The three-level boost converter offers advantages, such as a low current ripple and voltage stress, over a classic boost converter. These advantages offset the use of additional elements in the proposed converter circuit. Two capacitors are used to enable the innovative connection between multiple sources and the three-level boost converter. The second capacitor of the first module is shared with the first capacitor of the second module. This structure is used in conjunction with a controller to balance the voltages in the system. The operating modes of the two-module system in a nominal case are introduced. The controller is based on an indirect sliding model, wherein the input current of each energy source and the output voltage balance are considered. The performance of the current and voltage controllers are studied in two scenarios. The first case involves increasing the reference current and the presence of four sliding surfaces related to the current control and voltage balance, whereas the second case involves the presence and absence of two sliding surfaces related to the voltage balance. The dynamic response of this controller is also compared with the Proportional Integral(PI) controller. Large-signal modeling of the two-module system and the accuracy of this model in two cases of radiation change and panel temperature change is investigated. The robustness of the system is investigated using this large-signal model in two cases that involve changing the inductors and capacitors of the system. A topology consisting of two conventional boost converters is chosen to compare energy stored and efficiency with the proposed topology. The capacitance of the system is calculated for two topologies. The energy stored in the two systems is compared. The two-module system is simulated using Simulink MATLAB software. The simulation and experimental results validate the proposed system.**

***Index Terms*—Modular structure, photovoltaic (PV) panel, three-level boost converter, voltage balance.**

I. INTRODUCTION

SOLAR energy is a main source of renewable energy. This economical resource is available to all. A photovoltaic (PV) system is one of the most important methods of energy production whereby solar energy is converted into electricity [1]–[4]. However, there are problems associated with using this system.

Large-scale PV power plants are installed worldwide. These power plants generate hundreds of kilowatts or even a few megawatts of power using thousands of similar panels that are identically oriented toward the sun [5]. These power plants use high-efficiency inverters with a single dc input that implement a maximum power point tracking (MPPT) algorithm. This method is called field MPPT [6]. This method is not difficult to implement in PV power plants because the central inverter can easily find the maximum power point (MPP) of the power curve in terms of the voltage (P–V) of the entire power plant. However, in practice, several phenomena and events may occur during the life of a PV plant that have not been considered [7]–[10]. PV systems are affected by shading, dust, and relative differences in the orientation and temperature of panels. These factors can produce mismatches in the power generation of the panels, especially by the increased interest in PV applications in urban contexts [6]. This mismatch results in an error in the MPPT algorithm; that is, the MPPT algorithm may not be able to find the maximum absolute power of the system, resulting in an error in the method.

One way of solving this problem is by using dc–dc converters such that each panel has its own converter to implement MPPT control. In this case, the MPPT algorithm does not fail. This method is called distributed MPPT.

However, PV systems have a low output voltage. Therefore, boost dc–dc converters must be used in these systems [11]–[14]. The boost converters can be connected together to increase the output voltage. Each PV cell operates independently according

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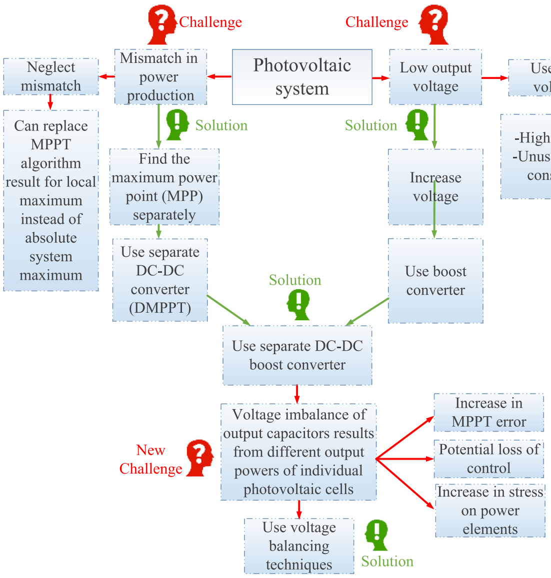


Fig. 1. Challenges posed by PV systems, showing the need for voltage balance.

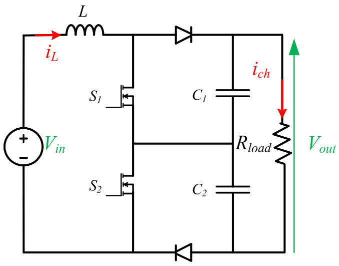


Fig. 2. Simple three-level boost converter.

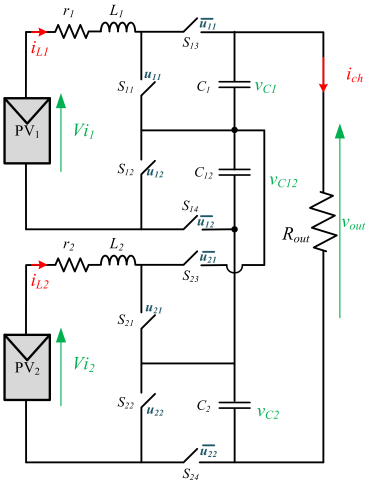


Fig. 3. Proposed method based on two three-level converters.

to the conditions at its location. Therefore, a new problem arises related to the structure of separate series converters. Unequal cell production produces a voltage imbalance at the output terminals of the converters. The voltage imbalance in the system can increase the stress on switches and power elements. The PV system can also lead to an increase in the error of the MPPT algorithm [6]. Fig. 1 presents a summary of the challenges posed by the PV system, showing the need for voltage balance.

Voltage imbalance can be generally classified as arising from source production and/or from devices [6]. We consider voltage imbalance from resource production in this article.

Voltage balancing strategies can be implemented with and without an auxiliary source [15], [16]. Auxiliary equalizers use an additional source to compensate for low-voltage cells.

These equalizers have large volume and weight and are therefore not particularly efficient for transportation system applications [15],[17], [18]–[20]. Equalizers without auxiliary sources may be dissipative or nondissipative.

Dissipative equalizers use a resistor to reduce the voltage of high-voltage cells. These equalizers waste a considerable quantity of energy. Thus, dissipative equalizers have a low efficiency [21], [22]. There are three types of nondissipative equalizers: capacitor-based [23]–[27], converter-based [28]–[34], and other equalizers [35]–[37].

In capacitor-based topologies, several capacitors are connected to sources via multiple switches. The sources are periodically connected to the capacitors. This operation continues until all the cells and capacitors reach the same voltage. Capacitor-based equalizers require a large number of switches and are not cost-effective for large numbers of cells or high-power applications [38], [39]. Several repetitive operations are used to balance the voltage of these equalizers. Consequently, voltage balance takes a long time [26]. Voltage equilibrium is achieved more rapidly in converter-based equalizers. However, the number of switches depends on the number of cells in some converter-based equalizers [29]. A precise controller is also needed to balance the voltage.

Recently, in [37], a converter-based equalizer has been proposed. A full-bridge inverter connected to the high voltage output bus is used to return power through a high-frequency transformer to the lower voltage cells. Even with a small number of switches, using a transformer increases the overall volume of the system.

A voltage balance scheme is proposed in [7], based on two three-level boost converters. A modular design is used to arrange the converters. This modular system balances the voltages of the output capacitors, whereas multiple sources are used to increase the reliability of the system.

A simple three-level boost converter circuit is shown in Fig. 2. The most important feature of this converter is the use of two capacitors [7]. Fig. 3 shows a combination of two three-level boost converters. Consider that the output of PV cells is connected to a three-level converter. Within this arrangement, capacitor C_{12} is common to both converters. As the voltage of capacitor C_1 equals that of capacitor C_{12} and the voltage of capacitor C_{12} equals that of capacitor C_2, all three capacitors have equal voltages. Thus, the desired voltage balance is achieved at the output of the circuit. The proposed structure for voltage balance based on three-level boost converters is analyzed in this article.

In the paper [7], we have briefly introduced the two-module structure. The system was simulated in Simulink/MATLAB. The purpose of the simulation is to show the performance of the system for balancing voltages.

In this study, additional work was performed to further investigate and ensure the performance of the system that we introduced in [7].

The operating modes of the two-module system are introduced. Programmable power supplies are programmed to be emulators as real PVs thanks to the real characteristics of PV. Although both systems use a voltage source instead of a PV panel for the sake of simplicity, the values of a real panel are used in this study.

The controller used in both papers is based on a sliding mode controller, owing to the simplicity of implementation, appropriate dynamic response, and robustness; however, in this study, the dynamic response of this controller is also compared with the PI controller.

In this study, the experimental results of the system and its comparison with simulations are evaluated in two scenarios. The first case involves increasing the reference current and the presence of four sliding surfaces related to the current control and voltage balance, whereas the second case involves the presence and absence of two sliding surfaces related to the voltage balance.

Large-signal modeling of the two-module system and the accuracy of this model in two cases of radiation change and panel temperature change is investigated.

The robustness of the system is investigated using the large-signal model in two cases that involve changing the inductors and capacitors of the system.

The performance of the controller is demonstrated by changing the specifications of the PV panel (current and voltage of the panel).

The capacitance of the system is calculated for the proposed topology and the topology consisting of two conventional boost converters. The energy stored in the two systems is compared because it is directly related to the cost and volume of the system.

The efficiency of the proposed topology is compared with that of the topology with two conventional boost converters while considering the losses.

This article is organized as follows. A literature review is presented in Section I, and in Section II, system equations for the converter structure and the system control are presented. The system is also modeled in Section II. In Section III, the model is used to simulate the two-module system, and the simulation results for different scenarios are presented. The robustness of the proposed system is also investigated. Experimental and simulation results are compared to validate the proposed system. In Section IV, the energy stored and the efficiency of the proposed topology are compared with those of the topology with two-boost converters. Finally, Section V concludes this article.

II. SYSTEM PRESENTATION

The system state equations for the proposed two-module system (see Fig. 3) are first presented. An appropriate controller for this system is then introduced. Finally, a system model is presented.

TABLE I
SYSTEM PARAMETERS

Parameters	Quantity	Value
V_{i1}, V_{i2}	Input voltage	12 V
L_1, L_2	Inductance	0.9 mH
r_1, r_2	Inductor resistance	0.3 Ω
C_1, C_2, C_{12}	Output capacitance	100 µF
f_s	Switching frequency	10 kHz
R_{out}	Load resistance	24 Ω

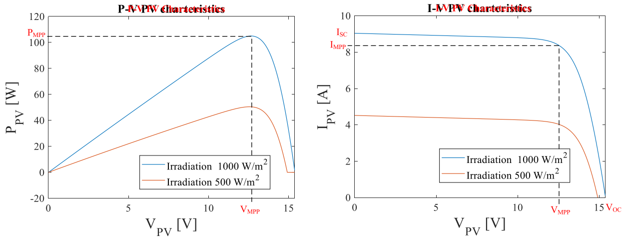


Fig. 4. Characteristics of the PV.

A. Converter Operation

The proposed modular dc–dc converter topology is shown in Fig. 3. This two-module converter consists of two three-level boost converters.

The state variables in the proposed two-module converter are the voltages of capacitors C_1, C_2, and C_{12} and the currents of inductors L_1 and L_2. v_{C1}, v_{C2}, and v_{C12} are the voltages across the capacitors. v_{out} and i_{ch} are the voltage and the load current, respectively. i_{L1} and i_{L2} are the inductor currents for L_1 and L_2, respectively. r_1 and r_2 are the inductor series resistors. R_{out} is the resistive load. The command signal for ON and OFF switching is denoted by u corresponding to the duty cycle d. The signal $\bar{u}$ is the inverse function of the signal u. The introduced parameters are summarized in Table I.

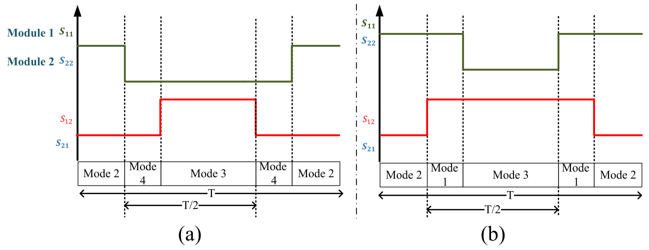
The electrical characteristics of a PV panel (STS-105 M-B4U, Integrated Solar Technology, Santa Fe, NM, USA) are plotted in Fig. 4. These plots put into evidence the following results:

1) short-circuit current ($I_{\text{SC}} = 9.06$ A);
2) open-circuit voltage ($V_{\text{OC}} = 15.39$ V);
3) MPP, at which the current value is $I_{\text{MPP}} = 8.3$ A, the voltage value is $V_{\text{MPP}} = 12.65$ V, and the power $P_{\text{MPP}} = V_{\text{MPP}} \cdot I_{\text{MPP}} = 105$ W.

The panel performance depends on the temperature and irradiance level. Temperature affects V_{OC}, but it has a negligible effect on I_{SC}. Irradiation has a negligible effect on V_{OC}, but it affects I_{SC} [40], [41].

The following assumptions are used to define the system.

1) The switching period is much shorter than the shortest system time constant.
2) Switching signals u and $\bar{u}$ are complementary in the dc–dc converter.
3) The switches are ideal, i.e., zero time is required to turn the switches ON or OFF, and switching occurs instantaneously and without losses.
4) The converter operates in a continuous conduction mode.



(a) (b)

Fig. 5. Switching patterns of switches. (a) With mode 4 (S_{11} and S_{12} turn OFF). (b) With mode 1 (S_{11} and S_{12} turn ON).

5) The PV panels are nonlinear sources, and their static *I–V* characteristics are closely bound to irradiation and temperature. To model such a system, a voltage source or current source can be used. The nature of the model is bound to the converter and its associated control strategy. In this article, we suppose that the MPP is tracked owing to the current. Thus, the converter can be considered at input as a current source, which is why the PV panel is modeled by a nonlinear voltage source with a static characteristic as presented in Fig. 4.

The system state equations are derived from the Kirchhoff's Voltage Law(KVL) and Kirchhoff's Current Law(KCL) equations for the circuit. The KVL rule is used to obtain the derivative of the current of the first inductor (L_1), which satisfies the following relation:

$$L_1 \frac{di_{L1}}{dt} = -r_1 i_{L1} + V_{i1} - (1-u_{11})\, v_{c1} - (1-u_{12})\, v_{c12}. \tag{1}$$

The equation for the current of the second inductor (L_2) can be obtained in the same way as follows:

$$L_2 \frac{di_{L2}}{dt} = -r_2 i_{L2} + V_{i2} - (1-u_{21})\, v_{c12} - (1-u_{22})\, v_{c2}. \tag{2}$$

The KCL law for the voltage of the capacitors C_1 and C_2 can be applied to obtain the following two equations:

$$C_1 \frac{dv_{c1}}{dt} = i_{L1}\ (1-u_{11}) - i_{\text{ch}} \tag{3}$$

$$C_2 \frac{dv_{c2}}{dt} = i_{L2}\ (1-u_{22}) - i_{\text{ch}}. \tag{4}$$

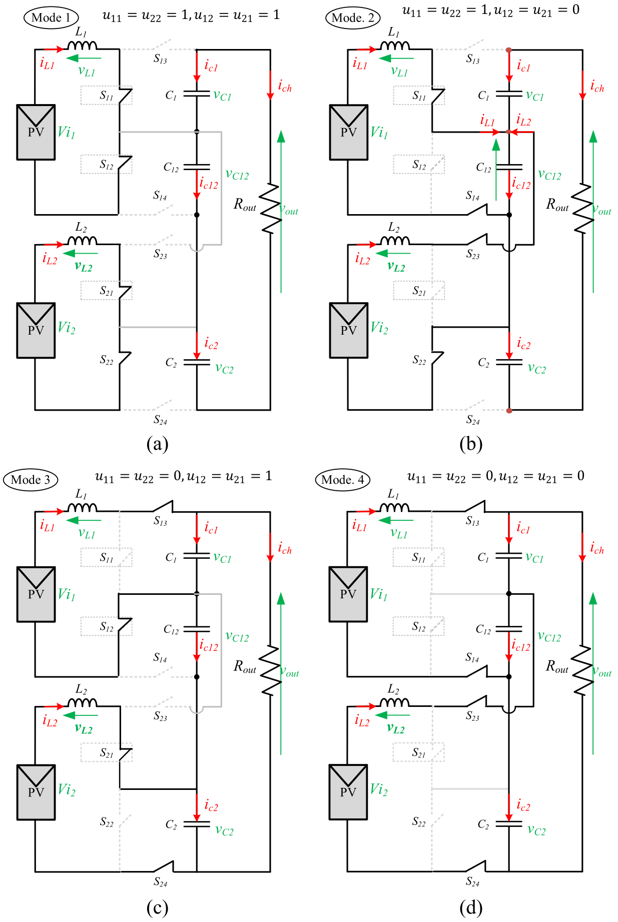
The voltage for the common capacitor C_{12} satisfies the following equation:

$$C_{12} \frac{dv_{c12}}{dt} = i_{L1}\ (1-u_{12}) + i_{L2}\, (1-u_{21}) - i_{\text{ch}}. \tag{5}$$

The equations above are the state equations for the proposed two-module converter.

Now, a steady-state operation of the proposed two-module converter is explained. The switching patterns of the active switches and the operating modes are shown in Fig. 5.

For module 1, two switches S_{11} and S_{12}, are driven by two signals. These signals are 180° out of phase using fixed-frequency pulsewidth modulation (PWM). In other words, the command signal u_{12} turns ON with a delay equal to *T*/2 of the signal u_{11}. This delay is essential for benefiting from the advantages of a three-level boost converter.



(a) (b) (c) (d)

Fig. 6. Equivalent circuits during different operation modes of the proposed converter (case I).

In the same manner, for module 2, two switches S_{21} and S_{22} are driven.

To implement PWM, module 1 is compared with module 2, and basically two possible cases exist. In case I, the triangular signals of PWM are identical for the command signals $u_{11}-u_{22}$ and for the signals $u_{12}-u_{21}$. For case II, the triangular signals of PWM are identical for the command signals $u_{11}-u_{21}$ and for the command signals $u_{12}-u_{22}$.

For example, in the nominal case, the proposed converter can produce three modes of operation through four modes of possible operations.

To simplify the investigation of the operations, the following assumptions are made for the operation and analysis of the converter: 1) output capacitors are sufficiently large to maintain a constant voltage across them; and 2) all components are assumed ideal.

For the first time, four possible modes will be presented. Then, the intervals, in the nominal case, will be explained.

Mode 1: S_{11}, S_{12}, S_{21}, and S_{22} are ON. During this mode, $u_{11} = u_{22} = 1$ and $u_{12} = u_{21} = 1$. All diodes are in the reverse-biased mode, and they are OFF. The equivalent circuit of this mode is shown in Fig. 6(a). Both inductors (L_1 and L_2) charge from the input sources. Capacitors C_1, C_2, and C_{12} discharge.

The voltages across inductors and currents through the capacitors are given by

$$v_{L1} = L_1 \ \frac{di_{L1}}{dt} = V_{i1} \tag{6}$$

$$v_{L2} = L_2 \ \frac{di_{L2}}{dt} = V_{i2} \tag{7}$$

$$i_{c1} = C_1 \ \frac{dv_{c1}}{dt} = \ -i_{\text{ch}} \tag{8}$$

$$i_{c2} = C_2 \ \frac{dv_{c2}}{dt} = -i_{\text{ch}} \tag{9}$$

$$i_{c12} = C_{12} \ \frac{dv_{c12}}{dt} = -i_{\text{ch}}. \tag{10}$$

Mode 2: S_{11} and S_{22} are ON, and S_{12} and S_{21} are OFF. During this mode, $u_{11} = u_{22} = 1$ and $u_{12} = u_{21} = 0$. The equivalent circuit of this mode is shown in Fig. 6(b). Capacitors C_1 and C_2 discharge.

The voltages across inductors and currents through the capacitors are given by

$$v_{L1} = L_1 \ \frac{di_{L1}}{dt} = V_{i1} - v_{c12} \tag{11}$$

$$v_{L2} = L_2 \ \frac{di_{L2}}{dt} = V_{i2} - v_{c12} \tag{12}$$

$$i_{c1} = C_1 \ \frac{dv_{c1}}{dt} = -i_{\text{ch}} \tag{13}$$

$$i_{c2} = C_2 \ \frac{dv_{c2}}{dt} = -i_{\text{ch}} \tag{14}$$

$$i_{c12} = C_{12} \ \frac{dv_{c12}}{dt} = i_{L1} + i_{L2} - i_{\text{ch}}. \tag{15}$$

Mode 3: S_{11} and S_{22} are OFF and S_{12} and S_{21} are ON: $u_{11} = u_{22} = 0$ and $u_{12} = u_{21} = 1$. The equivalent circuit of this mode is shown in Fig. 6(c). Capacitors C_1 and C_2 charge.

The voltages across inductors and currents through the capacitors are given by

$$v_{L1} = L_1 \ \frac{di_{L1}}{dt} = V_{i1} - v_{c1} \tag{16}$$

$$v_{L2} = L_2 \ \frac{di_{L2}}{dt} = V_{i2} - v_{c2} \tag{17}$$

$$i_{c1} = C_1 \ \frac{dv_{c1}}{dt} = i_{L1} - i_{\text{ch}} \tag{18}$$

$$i_{c2} = C_2 \ \frac{dv_{c2}}{dt} = i_{L2} - i_{\text{ch}} \tag{19}$$

$$i_{c12} = C_{12} \ \frac{dv_{c12}}{dt} = -i_{\text{ch.}} \tag{20}$$

Mode 4: S_{11} and S_{22} are OFF and S_{12} and S_{21} are OFF: $u_{11} = u_{22} = 0$ and $u_{12} = u_{21} = 0$. The equivalent circuit of this mode is shown in Fig. 6(d). Capacitors C_1 and C_2 charge.

The voltage across inductors and currents through the capacitors are given by

$$v_{L1} = L_1 \ \frac{di_{L1}}{dt} = V_{i1} - v_{c1} - v_{c12} \tag{21}$$

$$v_{L2} = L_2 \ \frac{di_{L2}}{dt} = V_{i2} - v_{c12} - v_{c2} \tag{22}$$

$$i_{c1} = C_1 \ \frac{dv_{c1}}{dt} = i_{L1} - i_{\text{ch}} \tag{23}$$

$$i_{c2} = C_2 \ \frac{dv_{c2}}{dt} = i_{L2} - i_{\text{ch}} \tag{24}$$

$$i_{c12} = C_{12} \ \frac{dv_{c12}}{dt} = i_{L1} \ + i_{L2} - i_{\text{ch}} \tag{25}$$

TABLE II
DUTY CYCLES IN STEADY STATE

$d_{11} = 1 - \frac{(P_1 + P_2)}{v_{out}} \cdot \frac{V_{i1}}{P_1}$
$d_{12} = 1 - \frac{V_{i1}}{v_{out}} \left(2 - \frac{P_2}{P_1}\right)$
$d_{21} = 1 - \frac{V_{i2}}{v_{out}} \left(2 - \frac{P_1}{P_2}\right)$
$d_{22} = 1 - \frac{(P_1 + P_2)}{v_{out}} \cdot \frac{V_{i2}}{P_2}$

The steady-state operating waveforms during different intervals, using equivalent circuits, are shown in Fig. 7 for case I. For module 1, the switch pairs S_{11}–S_{13} and S_{12}–S_{14} are operated with identical signals. The control signals of these switches (u_{11}, $\overline{u_{11}}$ and u_{12}, $\overline{u_{12}}$) are complementary, as shown in Fig. 7. Two scenarios are presented as follows:

Scenario 1). Fig. 7(a) with mode 4 (S_{11} and S_{12} turn OFF).
  Interval 1: mode 2.
  Interval 2: mode 4.
  Interval 3: mode 3.
  Interval 4: mode 2.
Scenario 2). Fig. 7(b) with mode 1 (S_{11} and S_{12} turn ON).
  Interval 1: mode 1.
  Interval 2: mode 2.
  Interval 3 mode 1.
  Interval 4: mode 3.

For the remainder of the cycle, the intervals are repeated in the same way to complete the full cycle.

For the analysis of the operating modes, the powers $P_1 =$ Ppv1 and $P_2 =$ Ppv2 supplied by the PVs are used, and then one can find the inductor currents i_{L1} and i_{L2} as follows:

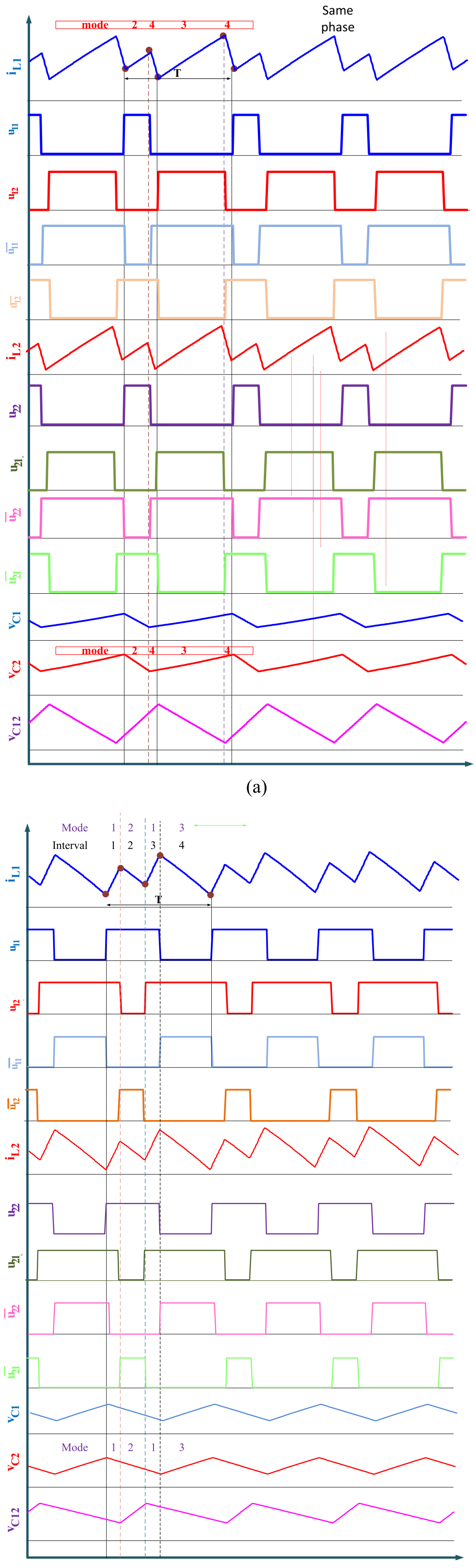
$$i_{L1} = \frac{P_1}{V_{i1}} \tag{26}$$

$$i_{L2} = \frac{P_2}{V_{i2}} \ . \tag{27}$$

The output voltage V_{out} and the voltages V_{C1}, V_{C2}, and V_{C12} (V_{out}/3) can be deduced

$$i_{\text{ch}} = \frac{P_1 + P_2}{v_{\text{out}}} \ . \tag{28}$$

Then, the duty cycles d_{11}, d_{12}, d_{21}, and d_{22} can be obtained as shown in Table II.



(a)

(b)

Fig. 7. Typical operating waveforms. (a) With mode 4 (S_{11} and S_{12} turn OFF). (b) With mode 1 (S_{11} and S_{12} turn ON).

Whatever the sequence, it is easy to show that the differential equations of the system are written as (1)–(5).

The control method used for the system is introduced in the next subsection.

B. Control System

An approach that complies with the nonlinear nature of switch-mode power supplies is represented by sliding mode control [42]. This control method offers several advantages [43], which are as follows:

1) stability even for large line and load variations;
2) robustness;
3) good dynamic response;
4) simple implementation.

Many researchers have studied sliding mode controllers in recent decades to control systems with variable structures [44], [45]. A sliding mode controller is used in the proposed system to control the inductor currents and the voltages of all three capacitors. Four sliding surfaces are defined. An indirect sliding mode approach is used to generate the duty cycles. The technique corresponds to a tradeoff between robustness properties and neccessity to operate at fixed switching frequency.

The sliding surfaces for the current of the inductors L_1 and L_2 are S_{i1} and S_{i2}, which are given as follows:

$$S_{i1} = i_{L1} - i_{\text{ref}1} + K_{i1} \int (i_{L1} - i_{\text{ref}1})\, dt \tag{29}$$

$$S_{i2} = i_{L2} - i_{\text{ref}2} + K_{i2} \int (i_{L2} - i_{\text{ref}2})\, dt \tag{30}$$

Two sliding surfaces S_{V1} and S_{V2} are defined to control and therefore equalize the voltages of capacitors C_1, C_2, and C_{12} as

$$S_{V1} = v_{C12} - v_{C1} + K_{v1} \int (v_{C12} - v_{C1})\, dt \tag{31}$$

$$S_{V2} = v_{C12} - v_{C2} + K_{v2} \int (v_{C12} - v_{C2})\, dt. \tag{32}$$

The general equation $\dot{S} = \; - \lambda \; S$ can be used to derive the following four equations:

$$\dot{S}_{i1} = -\lambda_{i1} S_{i1} \tag{33}$$

$$\dot{S}_{i2} = -\lambda_{i2} S_{i2} \tag{34}$$

$$\dot{S}_{v1} = -\lambda_{v1} S_{v1} \tag{35}$$

$$\dot{S}_{v2} = -\lambda_{v2} S_{v2}. \tag{36}$$

The above four equations can be solved for d_{11}, d_{12}, d_{21}, and d_{22}. PWM is used to obtain the duty cycles, and the command signal is then generated. A schematic of the method presented in this section is shown in Fig. 8

The capacitive differential equations (3)–(5) indicate that the currents flowing into the three capacitors are quite different and strongly dependent on PV currents. As will be shown, without a voltage balancing system, equal sharing of the output dc voltage between capacitors is impossible. Thus, the global controllability and efficiency of the converter can be affected.

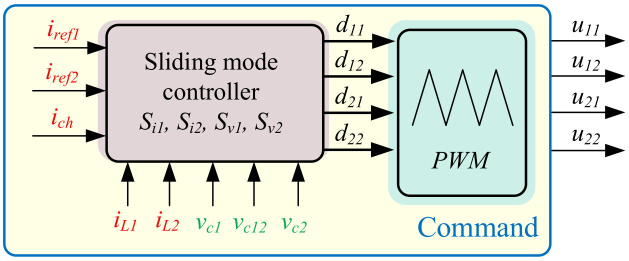


Fig. 8. Command signal block with sliding mode controller for a two- module system.

Therefore, the implementation of a balancing system is mandatory, most importantly to ensure the following properties at a steady state:

$$\begin{cases} v_{C1} = v_{C12} \\ v_{C12} = v_{C2} \end{cases} \rightarrow v_{C1} = v_{C12} = v_{C2}. \tag{37}$$

In this section, the governing equations for the controller and a method for calculating the duty cycle have been presented, which are used to generate the command signal. The proposed two-module system is modeled in the next subsection.

C. Large-Signal Average Modeling of a Two-Module Converter

Static converters can be modeled numerically or analytically. Numerical techniques employ various algorithms to obtain accurate results. Analytical models can be classified as discrete or average. Hypotheses are used in average models to simplify converter relationships. The simplified modeling and mathematical results may not be as accurate as the discrete model. However, simplicity is more important than accuracy in many cases.

A large-signal average model for the two-module system is proposed in this section. The relationships governing the system and the controller are applied. These equations have been presented in the previous two sections. The two-module converter has five state equations.

Two of these equations are related to the currents of inductors L_1 and L_2, and the remaining three are related to the voltages of capacitors C_1, C_2, and C_{12}. Two sliding surfaces to control the currents and two sliding surfaces to control the voltages are also defined.

Therefore, a state vector $X \in \mathbb{R}^9$ can be defined as follows:

$$[X] = \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \\ X_6 \\ X_7 \\ X_8 \\ X_9 \end{bmatrix} = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \\ v_{C12} \\ \int (i_{L1} - i_{\mathrm{ref1}})\, dt \\ \int (i_{L2} - i_{\mathrm{ref2}})\, dt \\ \int (v_{C12} - v_{C1})\, dt \\ \int (v_{C12} - v_{C2})\, dt \end{bmatrix}. \tag{38}$$

In the above equation, X_1 through X_5 are state variables. X_1 denotes the average value of current L_1. X_2 denotes the average value of current L_2. X_3 through X_5 denote the average values of the voltages of the capacitors C_1, C_2, and C_{12} during a switching period. In addition, the X_6 and X_7 integral terms for the sliding surfaces are used to control the currents, and the X_8 and X_9 integral terms for the sliding surfaces are used to control the voltages of the capacitors. The values of the duty cycles (d_{11}, d_{12}, d_{21}, and d_{22}), the state equation, and the control equations can be used to express $\dot{X}$ as

$$\dot{X} = H(X) \tag{39}$$

The matrix $\dot{X}$ is used to analyze the robustness of the system.

The eigenvalues of matrix $H(X_0)$ allow investigating the stability of the large-signal model around the operating point.

Considering an operating point X_0, the proposed model given by (39) is a nonlinear large-signal model in a closed loop. This model considers the controller variables (integral components X_6–X_9 of vector X). Nevertheless, the robustness analysis is performed thanks to the analysis of eigenvalues of dH/dx evaluated around the equilibrium point. The stability enables only the local asymptotic stability to be proven. The validity of the model can be established by a simulation presenting the system behavior obtained with transient events (e.g., irradiation variation).

The calculation of the eigenvalues requires the knowledge of the operating point, e.g., the inductor currents i_{L1} and i_{L2} and the capacitor voltages v_{c1}, v_{c2}, and v_{c12}. The currents are given by the power references in the case of known input voltages (known PV characteristic, therefore known V_{pv}); $i_{L1\mathrm{ref}} = \frac{P_{1\mathrm{ref}}}{V_{i1}}$ and $i_{L2\mathrm{ref}} = \frac{P_{2\mathrm{ref}}}{V_{i2}}$.

For the voltages, voltage balancing is assumed ($v_{c1} = v_{c2} = v_{c12} = \frac{v_{\mathrm{out}}}{3}$), and then the output power is given as

$$V_{i1}\, i_{L1} - r_1\, i_{L1}^2 + V_{i2}\, i_{L2} - r_2\, i_{L2}^2 = v_{\mathrm{out}}^2 / R_{\mathrm{out}}. \tag{40}$$

Therefore

$$i_{L10} = \frac{P_{1\mathrm{ref}}}{V_{i1}}, \quad i_{L20} = \frac{P_{2\mathrm{ref}}}{V_{i2}}, \quad v_{c10} = v_{c20} = v_{c120}$$
$$= \frac{1}{3}\sqrt{R_{\mathrm{out}}\left(V_{i1}\, i_{L1} - r_1\, i_{L1}^2 + V_{i2}\, i_{L2} - r_2\, i_{L2}^2\right)}. \tag{41}$$

In the first step, in the next section, the accuracy of the presented model will be verified by the simulation. In the second step, in Section III, an analysis of the robustness will be presented using a large-signal model for the proposed converter.

D. Accuracy of the Large-Signal Model

For verification of the accuracy of the large-signal model, the system will be simulated using MATLAB/Simulink software. The simulation is performed using the averaged and switched models.

Simulations with the converter modeled in MATLAB/Simscape and the converter modeled by a MATLAB function are performed. Therefore, one can compare the results obtained by these two simulations in the transient regime to show that the averaged model is good.

Fig. 9 shows the first simulation, where the power stage is modeled with MATLAB/Simscape. Fig. 10 shows the second simulation, where the converter is modeled by a MATLAB

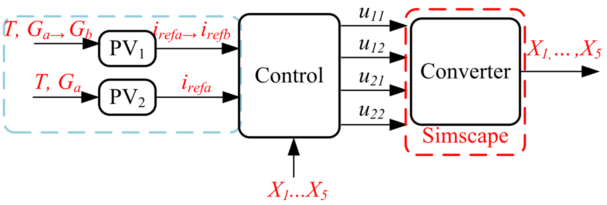


Fig. 9. Simulation (1): converter is modeled in Simscape.

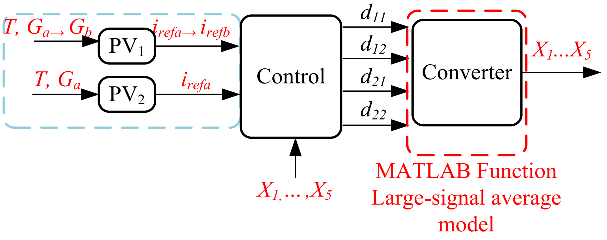


Fig. 10. Simulation (2): converter is modeled by a MATLAB function.

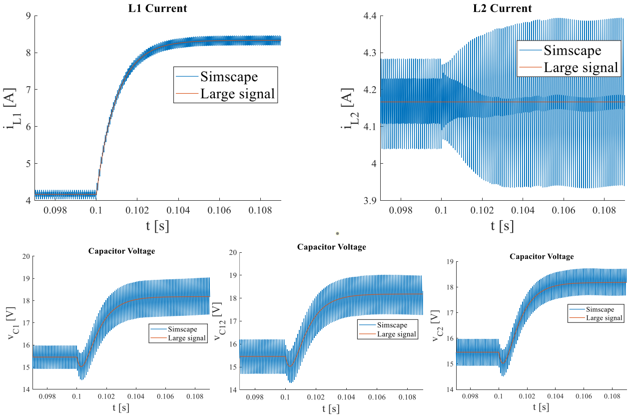


Fig. 11. Comparison of inductor currents and voltage waveforms of large-signal and switched models for a current reference $i_{\mathrm{ref}a}$ for module 2 and i_{ref1} going from $i_{\mathrm{ref}a}$ to $i_{\mathrm{ref}b}$ in one step for module 1.

function. For both simulations, the control part is performed using MATLAB/Simulink.

Irradiation variation for each panel of PVs can be represented by changing the currents. In the same manner, temperature variation can be tested by changing the input voltage of the panels. Therefore, to validate the large-signal model in the transient regime, two scenarios are considered: one in which the inductor current reference is changed and another in which the input voltage is changed.

Case I: PV Current Variation

The reference current is i_{ref1} for module 1 and i_{ref2} for module 2. The value of i_{ref2} is taken as a constant $i_{\mathrm{ref}a}$ and that of i_{ref1} is stepped once from $i_{\mathrm{ref}a}$ to $i_{\mathrm{ref}b}$. This current is applied using a first-order filter to ensure smooth dynamics. For this filter, $w_{i\mathrm{ref}} = 1000$ is considered to accurately reflect the transient state.

Based on the parameters listed in Table I, the transient inductor current waveforms i_{L1} and i_{L2}, and the voltage waveforms of capacitors C_1, C_2, and C_{12} for $i_{\mathrm{ref}a} = 50$ W/12 V $= 4.16$ A and $i_{\mathrm{ref}b} = 100$ W/12 V $= 8.33$ A are presented in Fig. 11.

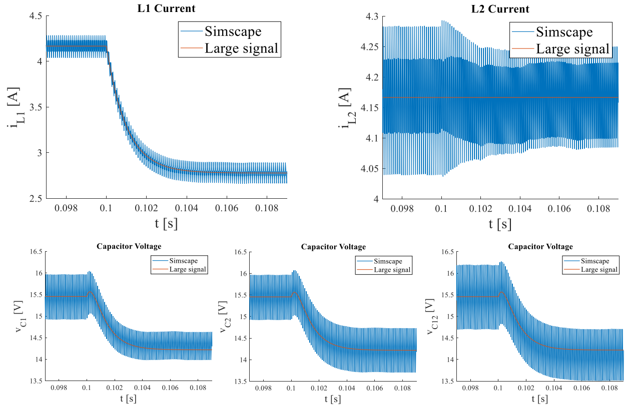


Fig. 12. Comparison of inductor currents and voltage waveforms of large-signal and switched models for an increasing input voltage of module 1, V_{i1} to $k \cdot V_{i1}$ ($k = 1.5$).

The currents and voltages of the proposed large-signal average model track well the currents and voltages of the switched model. In the same manner, one can repeat the test by changing the value of the current for PV$_2$. The conclusions for these results are identical to those of the previous case.

Case II: PV Voltage Variation

From the schematic diagram (see Fig. 3), the input voltage is V_{i1} for module 1 and V_{i2} for module 2. The value of V_{i2} can be taken as a constant and that of V_{i1} is changed from V_{i1} to $k \cdot V_{i1}$ at $t = 0.1$ s ($k = 1.5$ and $k = 0.9$ are two examples to show an increase/decrease in the input voltage V_{i1}). Based on the parameters listed in Table I, the transient inductive current waveforms i_{L1} and i_{L2}, as well as the voltage waveforms of capacitors C_1, C_2, and C_{12} for $k = 1.5$, are presented in Fig. 12.

Once again, one can observe that the currents and voltages of the proposed large-signal average model track well the currents and voltages of the switched model.

The two-module simulation system and the simulation results are presented in the following section.

III. SIMULATION AND EXPERIMENTAL RESULTS

A simulation is performed for several different scenarios using MATLAB/Simulink software. The PV array mathematical model is used thanks to the real characteristics of a PV (STS-105 M-B4U, Integrated Solar Technology).

The simulation results are used to investigate the status of the output voltage of the proposed system. The controller performance and the robustness of the system are subsequently analyzed.

The proposed system is experimentally validated using a test bench developed in the laboratory, as shown in Fig. 13. The test bench consists of digital oscilloscopes, two programmable power supplies, a variable resistance load, and a dSPACE system. Voltage and current probes are used to measure all the required controller signals. The controllers are implemented using MATLAB/Simulink-RTW software and implanted into the dSPACE real-time controller. All the signals are sampled for each switching period $T = \frac{1}{f_s}$ with $f_s = 10$ kHz. The system and control parameters are summarized in Tables I and III,

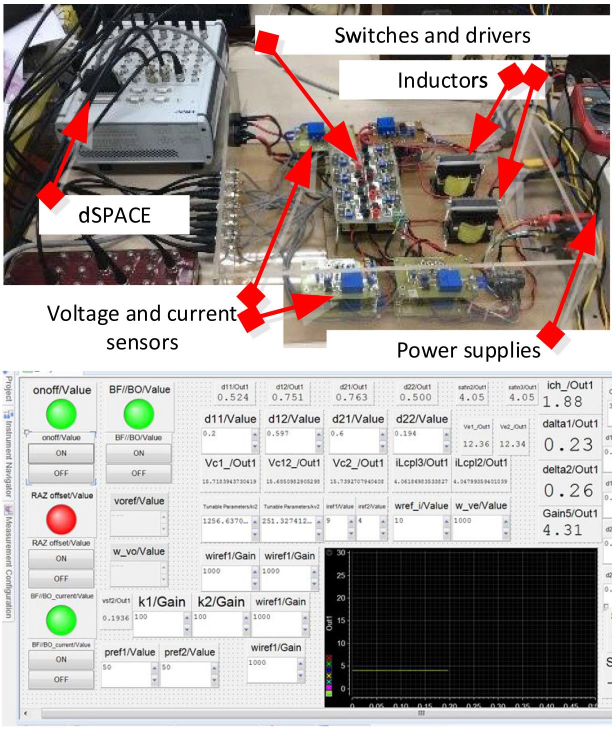


Fig. 13. Test bench for a two-input system and ControlDesk of dSPACE for real-time control.

TABLE III
CONTROL PARAMETERS

Parameters	Value
$k_{ij} = \lambda_i$	1250 rad/s
$k_{vj} = \lambda_v$	250 rad/s

respectively. The bandwidth of the current loop is chosen as $K_i = \lambda_i = 2\pi f_s/50$. The values of the voltage balancing loop parameters are typically selected to be considerably lower than those of the current loop parameters as $K_v = \lambda_v = K_{ij}/5$ [13].

Several scenarios for the two-module system are considered. Within the first scenario, the reference current is increased, and the resulting system behavior is investigated. The capacitor voltage balancing controller is used at all times for this scenario.

The second scenario is implemented to illustrate the performance of the voltage balancing controller. Initially, the voltage balancing controller is switched ON, and the system current is increased by one step at a specified time. The voltage balancing controller is then switched OFF, the system is allowed to reach steady state, and the controller is switched ON again.

A. Scenario 1

Both current and voltage balancing controllers are used in this scenario, and the reference current is increased by one step. This scenario is used to determine the inductor currents and the corresponding reference currents and the effect of switching signals on the inductor current wave and the capacitor voltage diagram. The purpose of this scenario is to investigate the combined performance of the current and voltage balancing controllers. The simulation results for the first scenario are shown in Figs. 14–17.

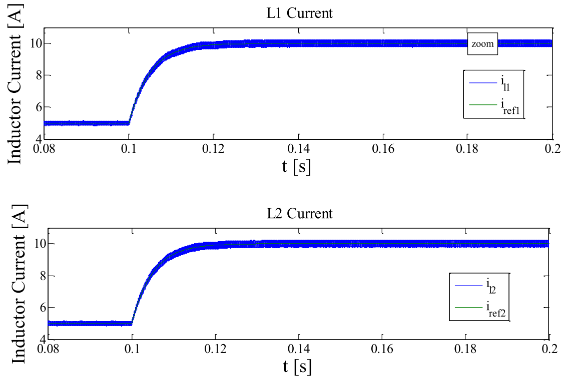


Fig. 14. Simulation results: waveforms of currents for inductors L_1 and L_2 and corresponding reference currents.

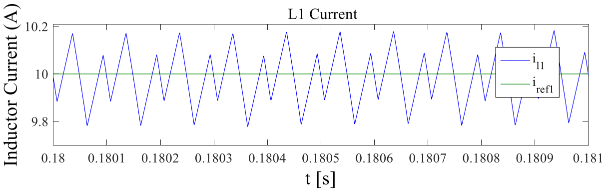


Fig. 15. Simulation results: magnification of waveform for current of inductor L_1 and corresponding reference current.

The reference current is i_{ref1} for converter 1 and i_{ref2} for converter 2. The value of i_{ref1} is increased from 5 to 10 A at $t = 0.1$ s and by one step for i_{ref2} from 5 to 10 A. This current is processed using a first-order filter to ensure smoother dynamics. The behavior of the reference currents is shown in Fig. 14. The sliding mode controller is used to ensure that the inductor currents follow the corresponding reference currents and equalize the output capacitor voltages.

Fig. 14 shows the currents i_{L1} and i_{L2} and the corresponding reference currents i_{ref1} and i_{ref2}. The steady-state inductive current waveform i_{L1} in Fig. 14 is magnified in Fig. 15. The average value of the inductor current waveform 1 is equal to its reference value. Therefore, the inductor current sliding surfaces are effective.

Fig. 16 shows the switching waves of u_{11} and u_{12} and the effect of opening and closing these switches on the inductor current 1. When one of the switches is OFF (i.e., when S_{11} is ON and S_{12} is OFF or when S_{11} is OFF and S_{12} is ON), the current waveform is downward. However, when both switches are ON, the current is upward. As the duty cycle d_{12} is longer than d_{11}, the current reduction is lower when S_{12} is OFF than when S_{11} is OFF.

Fig. 16(d) represents the behavior of the system using the experimental waveforms of the currents and the command signals for the same parameter. These results correspond well with Fig. 16(a)–(c).

Fig. 17(a) shows the voltage waveform of capacitors C_1, C_2, and C_{12} as a function of time. These waveforms change with the reference current and have an increasing phase. Fig. 17(a) shows that changing the reference current at $t = 0.1$ s increases the

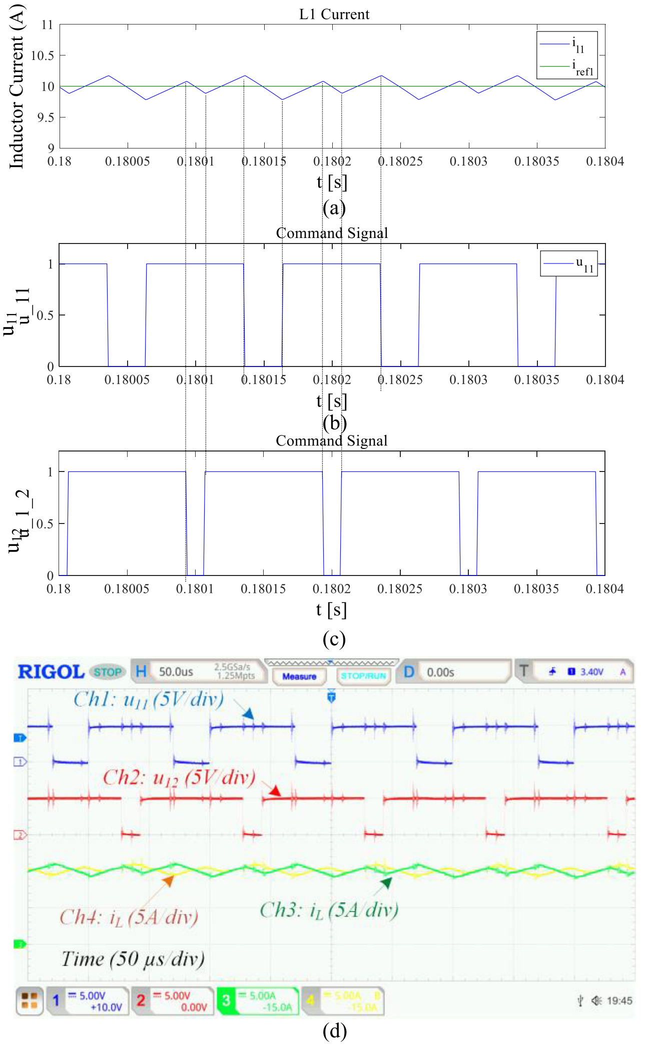


Fig. 16. Simulation (top) and experimental (bottom) results: waveform of current for inductor L_1 and switching signals u_{11} and u_{12}.

capacitor voltage from approximately 17.5 V to approximately 24.5 V.

Fig. 17(b) is a magnification of the voltage waveform of the capacitors over a short period of time and shows that the oscillating nature of the voltage waveform results in equal average voltage waveforms for the three capacitors.

Fig. 17(c) shows the load current waveform for the same step, whereas Fig. 17(d) is its magnification. Again, the experimental results presented in Fig. 17(e) and (f) confirm the results obtained in Fig. 17(a)–(d).

An analysis of Figs. 14–17 shows that the proposed system achieves the goal of following the reference current and balancing the voltages of the output capacitors.

Moreover, even when the input voltage V_{i1} or V_{i2} is changed while the another kept constant, the control objectives are also achieved.

B. Scenario 2

The second scenario is defined as follows.

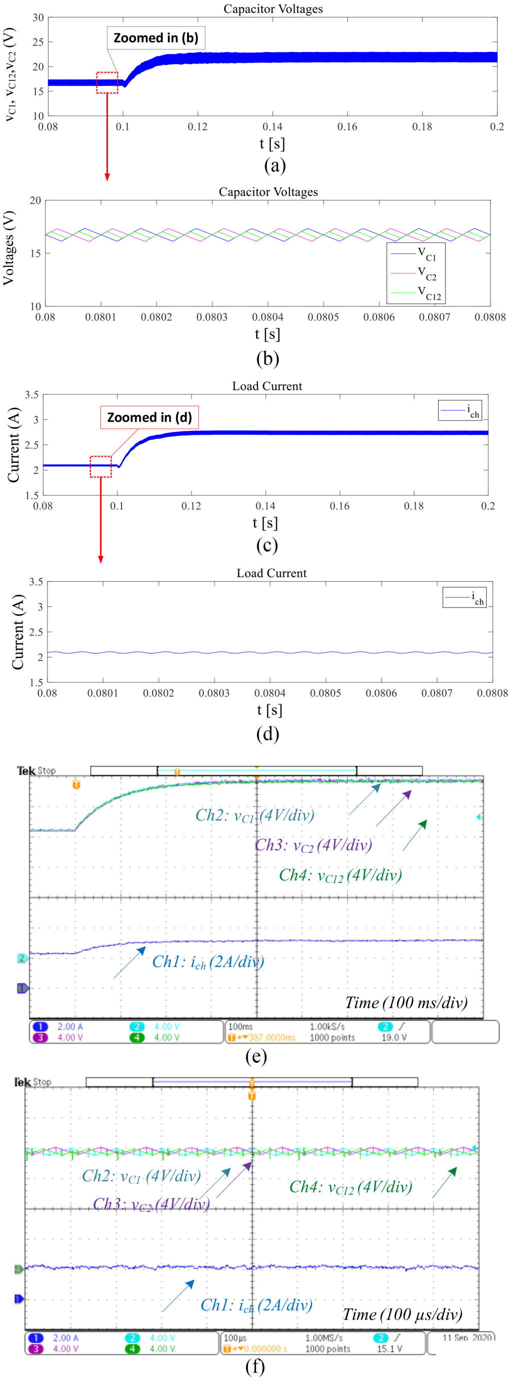


Fig. 17. (Top): Simulation results: (a) Capacitor voltage waveforms for C_1, C_2, and C_{12} resulting from changes in reference current, (b) magnified steady-state voltage waveforms of capacitors, (c) current load waveform, and (d) magnified current load. (c) and (f) (Bottom): Experimental results, capacitor voltage, and current load waveforms.

Zone I: Initially, the control system with four sliding surfaces is operational. The reference currents are then increased from 2 to 4 A at $t = 40$ ms.

Zone II: The controller is changed at $t = 100$ ms by removing the two voltage sliding surfaces.

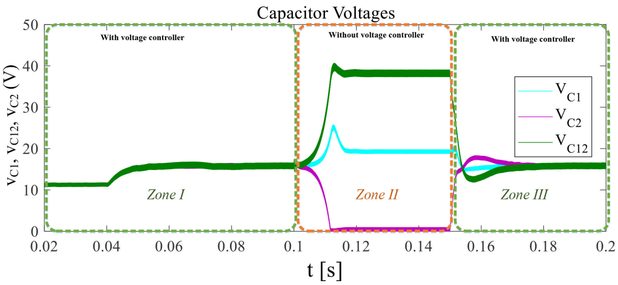


Fig. 18. Capacitor voltage waveforms for regions I, II, and III.

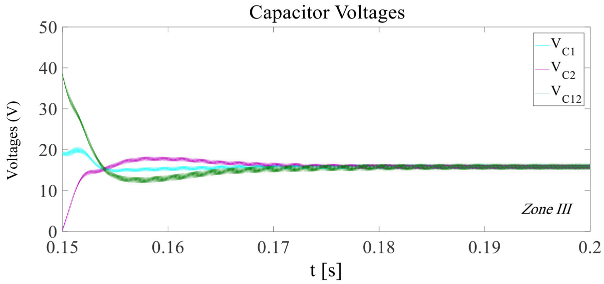


Fig. 19. Magnified capacitor voltage waveform at boundary of zone III, showing resumption of voltage control.

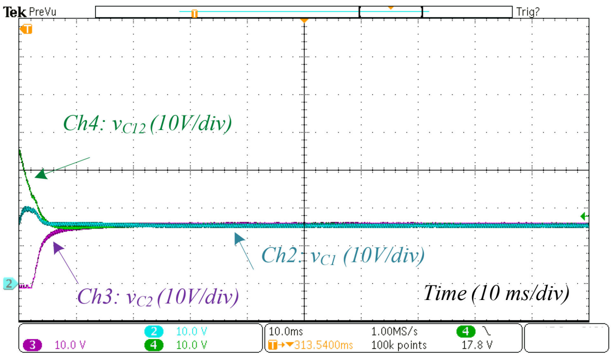


Fig. 20. Experimental result: capacitor voltage waveform at boundary of zones II and III, showing resumption of voltage control.

Zone III: The controller is changed again at $t = 150$ ms by adding the two voltage sliding surfaces back, that is, the system voltage controller is returned to its original state and is active.

Fig. 18 shows the capacitor voltages. Turning OFF the two voltage sliding surfaces results in strong negative and positive surges in the voltage waveforms of the capacitors, but the waveforms recover and become steady. However, the voltages of the three capacitors are no longer equal. Fig. 19 shows the boundary of zone III and the moment at which the voltage sliding surfaces are added back to the system at $t = 150$ ms.

The importance of the voltage controller and its effect on the capacitor voltages is effectively illustrated in the figure. The controller can equalize the voltages of the three capacitors in a short time.

Fig. 20 presents the capacitor voltages. This experimental result can illustrate the behavior of the system. As predicted in the simulation results in Figs. 18 and 19, turning OFF the two voltage sliding surfaces leads to an unbalance in the voltages of the three capacitors. After turning ON the sliding surfaces, the waveforms recover and become steady and equal.

All of these results confirm the theoretical study and the simulation results presented previously.

TABLE IV
OPTIMIZED PI COEFFICIENTS

	Proportional gain	Integral gain
Current	$K_{p_{i1}} = K_{p_{i2}} = 0.2243$	$Ki_{i1} = Ki_{i2} = 1088$
Voltage balancing	$K_{p_{v1}} = K_{p_{v2}} = 0.009114$	$Ki_{v1} = Ki_{v2} = 2.75$

C. Comparison With PI Controller

In this section, a comparison of the controlled system with two controllers PI and the proposed controllers is presented to demonstrate the importance of the sliding mode controller. The modeling, calculation of the transfer functions, and optimal synthesis of the PI controller coefficients are done, resulting in a comparative study.

The open-loop transfer functions are evaluated to design a PI controller for the system.

The PI controller is expressed as $FT_{\mathrm{PI}(s)} = K_p + \frac{K_i}{s}$, where K_{pi} is the proportional gain for current, K_i is the integral gain for current, K_{pv} is the proportional gain for voltage, and K_{iv} is the integral gain for voltage.

An optimized PI controller is designed to achieve the best performance. The pidTuner toolbox in MATLAB is used to determine the PI coefficients for the best performance. Then, the coefficients can be determined by fixing the phase margin, i,e., PM = 45°, and ensuring the minimum overshoot and settling time.

The PI coefficients are obtained by setting the bandwidth $Wc = wFs/10 = 6.2832$ krad/s for the current loop, and bandwidth $Wv = Wc/10 = 628$ rad/s for the voltage loop as shown in Table IV.

The behavior of the balancing of the capacitor voltages is compared using a PI controller and an indirect sliding mode controller.

The behavior of the controlled system during the input power reference for the first module $p_{1\mathrm{ref}}$ shows an increase from 50 to 100 W at $t = 0.04$ s, whereas the input power reference for the second module $p_{2\mathrm{ref}}$ remains constant at 50 W. Then, the input power reference for the second module $p_{2\mathrm{ref}}$ steps from 50 to 100 W at $t = 0.1$ s, whereas the input power reference for the first module $p_{1\mathrm{ref}}$ remains constant at 100 W. Finally, at $t = 0.14$ s, the load resistance changes from R to $R/2$. The dynamics of the input powers and balancing capacitor voltages are shown in Fig. 21. All capacitor voltages of the system observed with the proposed controller are similar. However, for the system with the PI controller, the voltage balancing is lost in the transient state when the input powers or load resistance R are/is changed.

D. Robustness

The large-signal average model presented in the previous section is used to obtain the Jacobian matrix, from which the eigenvalues are determined. Thus, the robustness of the system

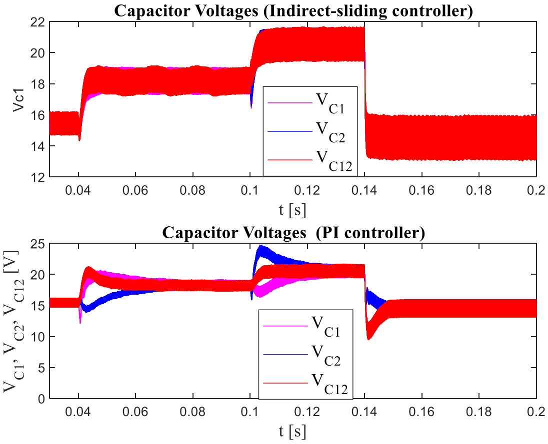


Fig. 21. Comparison between the capacitor voltages of the two controllers. At $t = 0.04$ s, the power reference $p_{1\mathrm{ref}}$ changes from 50 to 100 W. At $t = 0.1$ s, the power reference $p_{2\mathrm{ref}}$ changes from 50 to 100 W. At $t = 0.14$ s, the load resistance changes from R to $R/2$.

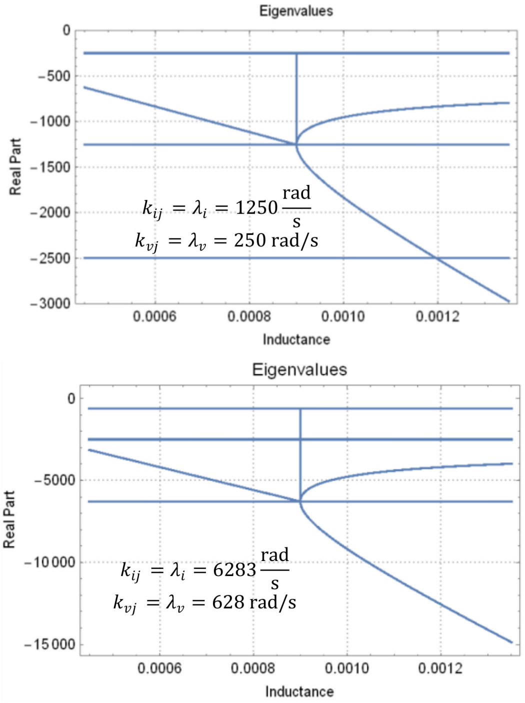


Fig. 22. Evolution of eigenvalues (real part) corresponding to changes in inductances L_1 or L_2 between 50% and 150% of nominal values, for two different sets of controller parameters: $k_{ij} = \lambda_i = 1250$ rad/s and $k_{vj} = \lambda_v = 250$ rad/s (top) and $k_{ij} = \lambda_i = 6283$ rad/s and $k_{vj} = \lambda_v = 628$ rad/s (bottom).

can be investigated for variable or uncertain system parameters [46]–[48].

The robustness of the system is evaluated by analyzing the eigenvalues of the Jacobian matrix when the inductance values L_1 and L_2 or capacitance values C_1, C_2, and C_{12} change. Changes in the inductances or capacitances between 50% greater and less than the nominal values are considered. Figs. 22 and 23 represent the evolution of the system eigenvalues for these changes. These scenarios are studied corresponding to two different sets of controllers parameters.

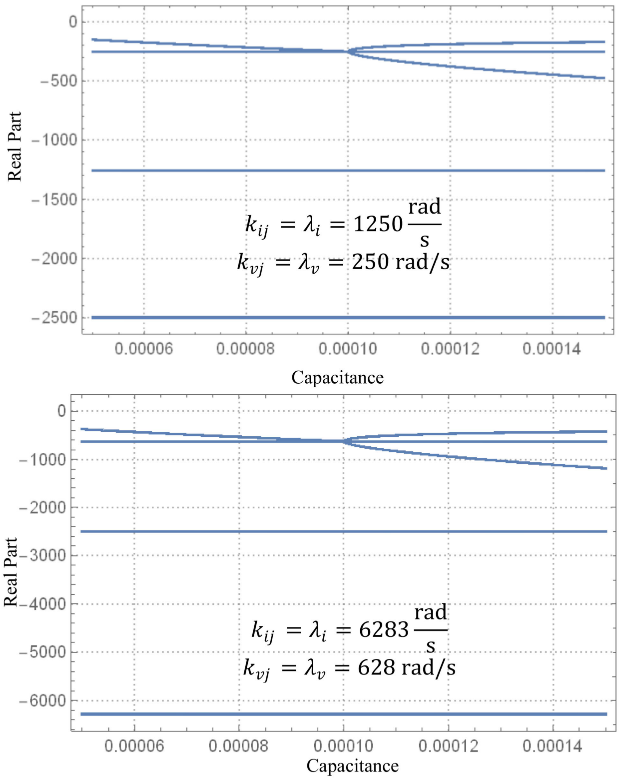


Fig. 23. Evolution of eigenvalues (real part) corresponding to changes in capacitances C_1, C_{12}, or C_2 between 50% and 150% of nominal values, for two different sets of controllers parameters: $k_{ij} = \lambda_i = 1250$ rad/s and $k_{vj} = \lambda_v = 250$ rad/s (top) and $k_{ij} = \lambda_i = 6283$ rad/s, $k_{vj} = \lambda_v = 628$ rad/s (bottom).

Fig. 22 shows the system eigenvalues corresponding to changes between 50% and 150% of the nominal inductances ($L_1 = 0.5L_{1n} : 0.05L_{1n} : 1.5L_{1n}$) or ($L_2 = 0.5L_{2n} : 0.05L_{2n} : 1.5L_{2n}$) with $L_{1n} = L_{2n} = 0.9$ mH. Given that the Jacobian of the system is a 9×9 matrix, nine eigenvalues for the system are at each point of operation. The controller parameters are set as $k_{ij} = \lambda_i = 1250$ rad/s and $k_{vj} = \lambda_v = 250$ rad/s for Fig. 22(top), and $k_{ij} = \lambda_i = 6283$ rad/s and $k_{vj} = \lambda_v = 628$ rad/s for Fig. 22(bottom). Despite the changes in the inductances, the real part of the eigenvalues always remains to the left of the axis. As the real parts of all eigenvalues are negative, this result shows that the system is stable under the investigated changes.

In the same manner, Fig. 23 shows the evolution of the system eigenvalues corresponding to changes between 50% and 150% of the nominal capacitances ($C_{1n} = C_{2n} = C_{12n} = 100\,\mu F$). All eigenvalues of $H(X_0)$ have a negative real part, which proves that the limit cycle described by the state trajectory remains stable for a large range of parameter variations.

E. PV Influence on the Design of the Controller

In this section, the influence of the electrical characteristics of the PV panel on the design of the controller is studied.

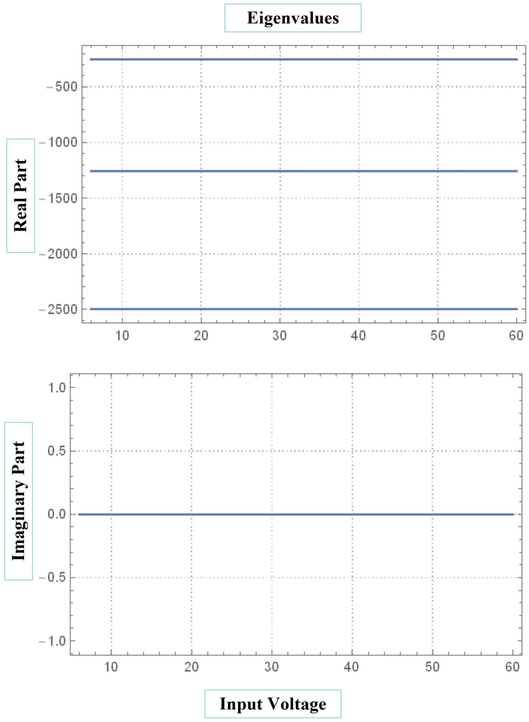


Fig. 24. Evolution of eigenvalues (real part and imaginary part as a function of input voltage variations) corresponding to changes in the input voltages V_{i1} or V_{i2} between 50% and 500% of the nominal values.

The evolution of eigenvalues for all possible operating points (for example, in the case of two irradiations for each panel and different references of PV currents) will be studied. The minimal dynamical performances can be ensured for the current tracking issue and the balancing voltage issue. The poles relative to the current and voltage balancing dynamics do not change substantially.

If the current is near zero, we know that the voltage balancing dynamic will be reduced because we lack sufficient current to quickly change the output capacitor voltage (limit of controllability), and the duty cycle could saturate, so the level of current must be sufficiently high to avoid saturation of the duty cycle. All tests must be performed in the domain for which the controllability of the system is ensured.

Fig. 24 shows the system eigenvalues corresponding to changes between 50% and 500% of the nominal input voltages ($V_{i1} = 0.5\, V_{i1n} : 0.5\, V_{i1n} : 5\, V_{i1n}$ or $V_{i2} = 0.5\, V_{i2n} : 0.5\, V_{i2n} : 5\, V_{i2n}$) with $i_{\text{ref}1} = i_{\text{ref}2} = 5$ A, and $V_{i1n} = V_{i2n} = 12$ V.

Despite the changes in the input voltages, the real part of the eigenvalues always remains to the left of the axis.

Fig. 25 shows the system eigenvalues corresponding to changes between 50% and 500% of the nominal inductor currents ($i_{\text{ref}2} = 0.5\; i_{\text{ref}2n} : 0.5\; i_{\text{ref}2n} : 5\; i_{\text{ref}2n}$ or $i_{\text{ref}1} = 0.5\; i_{\text{ref}1n} : 0.5\; i_{\text{ref}1n} : 5\; i_{\text{ref}1n}$) with $i_{\text{ref}1n} = i_{\text{ref}2n} = 2$ A, and $V_{i1} = V_{i2} = 12$ V.

Once again, one can observe that despite the changes in the inductor current references, the real part of the eigenvalues always remains to the left of the axis.

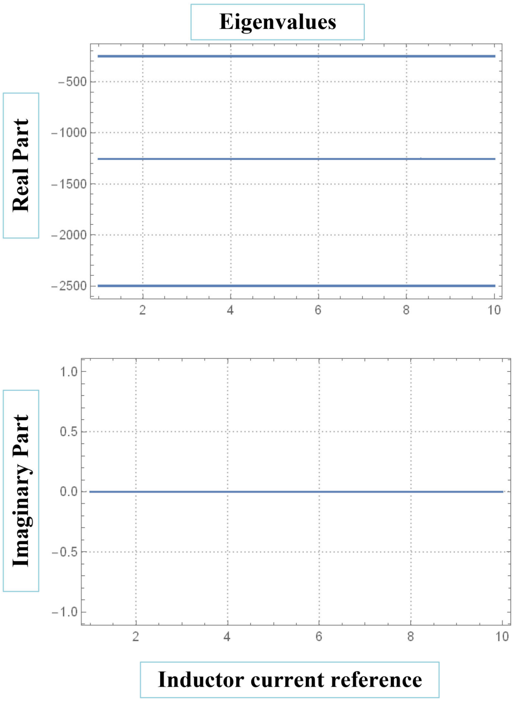


Fig. 25. Evolution of eigenvalues (real part and imaginary part as a function of inductor current variations) corresponding to changes in the inductor currents $i_{\text{ref}1}$ or $i_{\text{ref}2}$ between 50% and 500% of nominal values.

TABLE V
ASSUMPTIONS FOR THE DESIGN

$V_i = V_{i1} = V_{i2}$	Input voltages	(42)
$P_1 = P_2 = P = V_i \cdot I$	Input powers	(43)
$I = i_{L1} = i_{L2}$	Input currents	(44)
$r_1 = r_2 = r$	Inductor resistances	(45)

From Figs. 24 and 25, the eigenvalues are slightly affected by the changes in operating points of the PV panels.

IV. ENERGY ANALYSIS AND EFFICIENCY

In terms of the design, this topology is compared with an equivalent topology built with two independent boosts connected in parallel for the same PV systems and dc output voltage.

A. *Energy*

This section details the design of the capacitance for the proposed topology and the topology with two conventional boost converters. Both topologies are fed by two power sources while supplying only one resistive load. Because both topologies use the same number of inductors but a different number of output capacitors, the size and volume, along with the cost of such capacitors, result in dissimilar topologies.

Proposed two three-level converter

The following assumptions are made to design the system (see Table V).

1) The converter operates in a continuous conduction mode.
2) The input voltages are similar, as in (42).

3) The input power of each module is identified as in (43), and the input currents are the same as in (44).
4) The inductor resistances for the two modules are similar, as detailed in (45).
5) The two switches S_{11} and S_{12} are driven by two signals. These signals are 180° out of phase using fixed-frequency PWM, similar to switches S_{21} and S_{22}.

Considering the loss in the inductor resistances, the output power P^* is

$$P^* = P - r\left(\frac{P}{V_i}\right)^2. \tag{46}$$

Therefore, the output voltage can be calculated using the following equation:

$$\frac{{V_{\text{out}}}^2}{R_{\text{out}}} = 2P^* \Rightarrow V_{\text{out}} = \sqrt{2P^* R_{\text{out}}}\,. \tag{47}$$

Using (42)–(44) and (3), we obtain

$$(1-d)\,\frac{P}{V_i} = \frac{P_{\text{out}}}{V_{\text{out}}} \tag{48}$$

where $P_{\text{out}} = V_{\text{out}} \cdot I_{\text{ch}}$ (I_{ch} is the average value of the load current) and the duty cycles of switches S_{11} and S_{22} are $d_{11} = d_{22} = d$.

Using (47) and (48), we obtain

$$d = 1 - \frac{2P^*}{P}\,\frac{V_i}{V_{\text{out}}} = 1 - 2\left(1 - r\frac{P}{{V_i}^2}\right) \cdot \frac{V_i}{\sqrt{2P^* R_{\text{out}}}}. \tag{49}$$

Similarly, using (5), (43), and (44), we obtain

$$d_{12} = d_{21} = 1 - \frac{P^*}{P}\,\frac{V_i}{V_{\text{out}}} \Rightarrow d_{12} = d_{21} = 1 - \left(1 - r\frac{P}{{V_i}^2}\right) \cdot \frac{V_i}{\sqrt{2P^* R_{\text{out}}}} \tag{50}$$

where $d_{12} = d_{21}$ are the duty cycles of switches S_{12} and S_{21}.

Calculation of $C_1 = C_2 = C$

The ripple of voltage ΔV for C_1 and C_2 in this structure can be obtained using the following equation:

$$C_1\,\frac{\Delta v_{C_{11}}}{d_{11}T} = I_{\text{ch}} = \frac{P_{\text{out}}}{V_{\text{out}}} \Rightarrow \Delta\, v_{C_1} = \frac{d_{11}}{C_1 f_s}\,\frac{P_{\text{out}}}{V_{\text{out}}} = \Delta V. \tag{51}$$

By replacing d_{11} from (49), the capacitance C_1 can be determined as follows:

$$C_1 = \frac{\left(1 - 2\left(1 - r\frac{P}{{V_i}^2}\right) \cdot \frac{V_i}{V_{\text{out}}}\right)}{\Delta V f_s}\,\frac{P_{\text{out}}}{V_{\text{out}}} = C. \tag{52}$$

Calculation of $C_x = C_{12} + C_{21}$

Capacitors C_{12} and C_{21} are connected in parallel, as shown in Fig. 26. Both capacitors can be considered as only one capacitor C_X.

Owing to the interleaved PWM modulation technique, capacitor C_x sees its current containing a double switching frequency $f_{sCx} = 2\,f_s = \frac{2}{T}$.

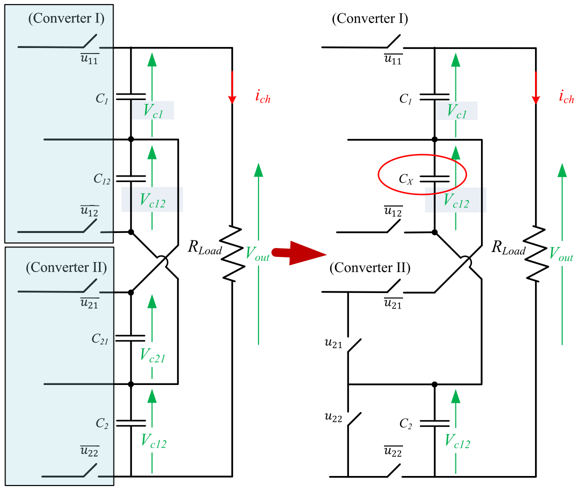


Fig. 26. Proposed topology where $C_X = C_{12} + C_{21}$.

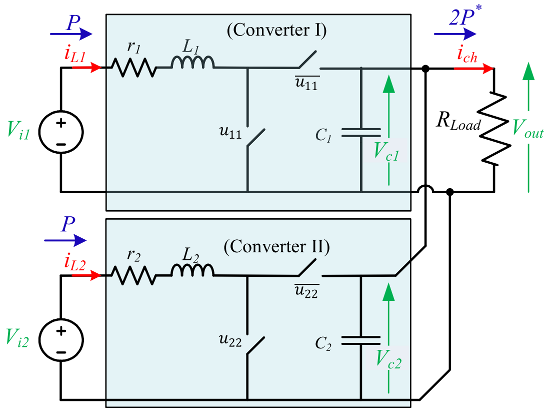


Fig. 27. Topology based on the two-boost converters.

Therefore, the capacitance C_x necessary to maintain the ripple voltage $\Delta\, v_{C_x} = \Delta V$ is

$$C_x = \frac{1 - \left(1 - r\frac{P}{{V_i}^2}\right) \cdot \frac{V_i}{\sqrt{2P^* R_{\text{out}}}}}{2\Delta V f_s}\,\frac{P_{\text{out}}}{V_{\text{out}}} = \frac{C}{2}. \tag{53}$$

Therefore, $C_{12} = C_{21} = \frac{C_x}{2} = \frac{C}{4}$. It can be seen that the capacitance values for C_{12} and C_{21} are one-fourth of those for C_1 or C_2.

Topology based on the two-boost converter

For the topology based on the two-boost converters (see Fig. 27), the assumptions 1)–4) for the proposed topology are held. The switches for the two converters turn ON and OFF simultaneously (synchronized PWM).

Considering the loss in the inductor resistances r, the output power P_{out} is given by

$$P_{\text{out}} = 2\left(P - r\left(\frac{P}{V_i}\right)^2\right) = 2P^*. \tag{54}$$

The ripple of the output voltage in this structure can be obtained using the following equation:

$$\Delta\, V_{\text{out}} = \Delta V = \frac{d}{C_{\text{tot}} f_s} \frac{P_{\text{out}}}{V_{\text{out}}}. \tag{55}$$

The duty cycle d and output voltage V_{out} of the system are calculated as follows:

$$d = 1 - \left(1 - r\frac{P}{{V_i}^2}\right) \cdot \frac{V_i}{V_{\text{out}}}, \quad V_{\text{out}} = \sqrt{2P^* R_{\text{out}}}. \tag{56}$$

The capacitance C_{tot} is defined as follows:

$$C_{\text{tot}} = C_1 + C_2 = \frac{1 - \left(1 - r\frac{P}{{V_i}^2}\right) \cdot \frac{V_i}{V_{\text{out}}}}{\Delta V f_s} \frac{P_{\text{out}}}{V_{\text{out}}}. \tag{57}$$

Comparison of the stored energy in the output capacitors

In this section, these energies are calculated for the two topologies to compare the energy stored in the output capacitors.

1) Proposed Topology: Considering $V_{C1} = V_{C12} = V_{C2} = \frac{V_{\text{out}}}{3}$, we can determine the total stored energy in the three capacitors as follows:

$$W_T = \frac{1}{2}\left[C + 2\frac{C}{4} + C\right]\left(\frac{V_{\text{out}}}{3}\right)^2 = \frac{1}{2}\left[C + 2\frac{C}{4} + C\right]\frac{{V_{\text{out}}}^2}{9}. \tag{58}$$

After simplifying, we obtain

$$W_T = \frac{1}{2}\,\frac{5}{2} C \frac{{V_{\text{out}}}^2}{9} = \frac{5}{36}\, C\, {V_{\text{out}}}^2. \tag{59}$$

2) Topology Based on the Two-Boost Converters: The stored energy in the output capacitors W_B for the two-boost converters can be calculated as follows:

$$W_B = \frac{1}{2}\, C_{\text{tot}} {V_{\text{out}}}^2 \tag{60}$$

where $C_{\text{tot}} = C_1 + C_2$.

3) Comparison: The energy stored in the output capacitors for the proposed topology and the topology based on the two-boost converter is compared, as shown in the following equation:

$$\frac{W_T}{W_B} = \frac{5}{18}\, \frac{\sqrt{2P^* R_{\text{out}}} - 2V_i\left(1 - r\frac{P}{{V_i}^2}\right)}{\sqrt{2P^* R_{\text{out}}} - V_i\left(1 - r\frac{P}{{V_i}^2}\right)} \tag{61}$$

where $P^* = V_i \cdot I_{\text{ref}} - r \cdot {I_{\text{ref}}}^2$ and $P = V_i \cdot I_{\text{ref}}$. Note that, I_{ref} is the input current reference for each module of the two topologies.

Using the parameters listed in Table I with $I_{\text{ref}} = 100$ A, the minimum gain is obtained as follows:

$$\frac{W_T}{W_B} = \frac{5}{18} \times (\approx 1) \Rightarrow \left(1 - \frac{5}{18}\right) \times 100\% = \frac{13}{18} \times 100\% = 72\%. \tag{62}$$

As shown in (62), it can be concluded that even for very high powers, the stored energy gain $(\frac{W_T}{W_B})$ is greater than 72%.

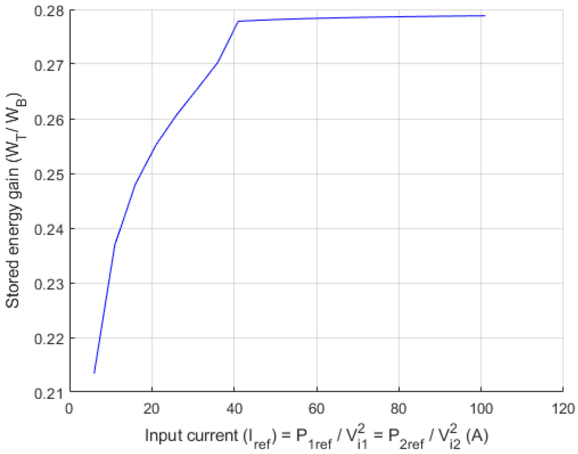


Fig. 28. Comparison of the stored energy in the capacitors, where $I_{\text{ref}} = \frac{P_{1\text{ref}}}{{V_{i1}}^2} = \frac{P_{2\text{ref}}}{{V_{i2}}^2}$.

TABLE VI
SPECIFICATIONS AND PARAMETERS

Symbol	Value	Unit
V_i; V_o	12; 50	V
f_s	10	kHz
C_1, C_2 (for two-boost converter)	100	µF
C_1, C_2, C_{12}	100; 100; 50	µF
ESR C (for two-boost converter)	0.23	mΩ
ESR C1-C2; ESR C_{12}	0.23; 0.12	mΩ
ΔiL	0.25	A
MOSFET IPP019N08NF2S	147 A; 80 V	

In Fig. 28, the stored energy in the capacitors is compared using parameters detailed in Table I. I_{ref} is the current of the input voltage source, and it can be clearly seen that its power (P) has a linear dependence on its current. It can be observed in the curve that the $\frac{W_T}{W_B}$ fraction is less than 0.3, even with high power usage of the system ($I_{\text{ref}} = 100$ A), which means that the stored energy of capacitors in the proposed system is considerably less than that in the two-boost converter.

The work in [49]–[51] have studied the relation between the energy stored in the converters and the cost and volume. As detailed in these studies, a decrease in the stored energy leads to a decrease in the converter cost. The proposed topology has a lower cost and volume compared with the topology using the two-boost converters by considering (61) and (62).

B. *Efficiency*

In this section, the efficiency and losses for both topologies are compared.

For the sake of simplicity, the MOSFETs for all topologies are similar. In addition, the same values of the inductor current ripple and capacitor voltage ripple are considered. The system specifications and parameters are listed in Table VI.

Two topologies are considered. These converters essentially consist of inductors, output capacitors, and bidirectional semiconductor devices. These elements are presented in Table VII.

The inductor power losses (P_{L_j}) include copper losses (P_{copper}) and core losses (P_{Core}) in the inductances. The power

TABLE VII
ELEMENTS AND POWER LOSSES

	Two-boost converter	**Proposed topology**
Switches	S_{11}, S_{12}	S_{11}, S_{12}, S_{13}, S_{14}, S_{21}, S_{22}, S_{23}, S_{24}
Diodes	D_{11}, D_{12}	D_{11}, D_{12}, D_{13}, D_{14}, D_{21}, D_{22}, D_{23}, D_{24}
Inductor	L_1, L_2	L_1, L_2
Capacitor	C_1, C_2	C_1, C_2, C_{12}
Switch power losses	$P_{MOS(S1)}$, $P_{MOS(S2)}$	$P_{MOS(S12)}, P_{MOS(S12)}, P_{MOS(S13)}, P_{MOS(S14)}$ $P_{MOS(S21)}, P_{MOS(S22)}, P_{MOS(S23)}, P_{MOS(S24)}$
Diode power losses	$P_{diode(D1)}$, $P_{diode(D2)}$	$P_{diode(D11)}, P_{diode(D12)}, P_{diode(D13)}, P_{diode(D14)}$ $P_{diode(D21)}, P_{diode(D22)}, P_{diode(D23)}, P_{diode(D24)}$
Inductor power losses	P_{L_1}, P_{L_2}	P_{L_1}, P_{L_2}
Capacitor power losses	$P_{C(C1)}, P_{C(C2)}$	$P_{cap(C1)}, P_{cap(C2)}, P_{cap(C12)}$

loss in capacitor $(P_{C(Cj)})$ is due to the equivalent series resistance (ESR). Both conduction and switching losses in the semiconductors are denoted as (P_{MOS}) and $(P_{\text{diode}(Dj)}$.

Then, the total converter losses include the switch power losses $(P_{\text{MOS}(Sj)})$, diode power losses $(P_{\text{diode}(Dj)})$, inductor power losses (P_{L_j}), and capacitor power losses $(P_{C(Cj)})$. The power losses are presented in Table VII.

The equations for each type of loss are as follows:

$$P_{\text{converter}} = P_{L_j} + P_{\text{MOS}(Sj)} + P_{\text{diode}(Dj)} + P_{C(Cj)}. \quad (63)$$

The model for the switch power losses [50] includes both switching and conduction losses as

$$P_{\text{MOS}} = r_{ds} \cdot I_{\text{MOS}\,\text{rms}}^{2} + (E_{\text{ON}} + E_{\text{OFF}}) \cdot f_s \quad (64)$$

where r_{ds} is the ON-MOSFET resistance, I_{MOSrms} is the rms current of the MOSFET, and E_{ON} and E_{OFF} are, respectively, the switching energy losses depending on the MOSFET parasitic capacitances and their charging profile during the commutation, which are available in corresponding datasheets. For the sake of simplicity, the switching times of each transistor are evaluated for each MOSFET for a defined gate resistance, as in [52].

The diode power losses can be calculated using [52]

$$P_{\text{Diode}} = (2V_D I_1 T (1-d) + \text{Err}) \cdot f_s \quad (65)$$

where I_1 is the average inductor current and Err is the recovery energy.

The losses in the capacitors are caused by their ESR. The ESR value can be determined from the capacitor datasheets or calculated using the loss factor tan(δ), also provided in the datasheets as [53]

$$\text{ESR} = \frac{\tan(\delta)}{2\pi f_s C} \quad (66)$$

where *C* is the capacitance of the considered capacitor.

The capacitor losses can be determined using

$$P_{C(Cj)} = \text{ESR}_\text{j} \cdot I_{Cj\,\text{rms}}^{2} \quad (67)$$

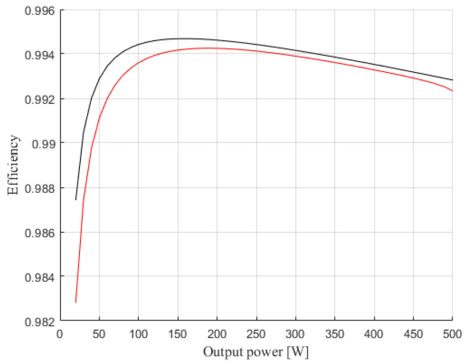


Fig. 29. Efficiency as a function of the output power. (Black) Proposed topology. (Red) Two-boost converter topology.

where $I_{Cj\,\text{rms}}$ is the capacitor current in rms.

The inductor losses $P_{(Lj)}$ include the power losses in the copper coils $(P_{\text{Copper}j})$ and magnetic core $(P_{\text{Core}j})$. They are computed using the following equation:

$$P_{\text{Copper}j} = \text{DCR}_\text{j} \cdot I_{Lj\,\text{rms}}^{2} \quad (68)$$

where DCR is the direct current resistance, and $I_{Lj\,\text{rms}}$ is the rms inductor current

$$\text{DCR} = n \cdot \text{MLT} \cdot \rho / A_{\text{wire}} \quad (69)$$

where n is the number of turns of the coil, MLT is the mean length turn of the coil, ρ is the copper resistivity, and A_{wire} is the magnetic wire section.

The core loss is determined using the following equation:

$$P_{\text{core}} = V_{(L)} \frac{1}{T} \int_0^T k_i^{\text{iGSE}} \left| \frac{dB_L}{dt} \right|^{\alpha} \Delta B_{\text{pp}}^{\beta-\alpha} dt \quad (70)$$

It is based on an improved model of the Steinmetz core losses iGSE [54], where α and β are the Steinmetz parameters, B_L is the magnetic flux density through the core, B_{pp} is the peak–peak value, and $k_i^{i\text{GSE}}$ is a constant coefficient related to the Steinmetz proportional parameters. $V_{(L)}$ is the magnetic core volume.

Using (63)–(70), we can calculate the total losses of both topologies. This leads to the calculation of the efficiency for each topology. These results are presented in Fig. 29. In these figures, the efficiencies for both topologies are compared.

As mentioned earlier, one advantage of the proposed topology is the use of the interleaved technique to reduce the inductor input current ripple Δi_L. Therefore, a lower inductance can be used for the same Δi_L compared with the two-boost converter topology. Then, a low number of turns are required, resulting in a lower copper loss in the inductor.

As shown in Fig. 29, both converters provide high efficiency ($>$ 90%). However, the proposed topology offers a better efficiency compared with the two-boost converter topology.

V. CONCLUSION

A proposed system based on a two-module three-level boost converter for voltage balance is investigated in this study. First, the governing state equations are presented. The steady-state operation of the proposed two-module converter is explained.

The possible operation modes in the nominal case are illustrated. Second, the indirect sliding mode controller is defined to implement the system in a simulation mode. The analysis shows that the proposed system achieves the objectives of following the reference current and balancing the voltages of the output capacitors. Moreover, even when the input voltage of each module is changed, whereas the another kept constant, the control objectives are achieved. The performance of the current and voltage controllers are validated by the experimental results by increasing the reference currents and turning OFF and ON the two voltage sliding surfaces. Without voltage controllers, an unbalance of the voltages of the three capacitors is appeared. After turning ON the sliding surfaces, the waveforms recover and become steady and equal. These experimental results confirm the effective operation of the proposed system for voltage balance and achieve the goal of tracking the reference current.

A large-signal average model for the two-module system is proposed to analyze the robustness thanks to the system eigenvalues. To validate the large-signal model in the transient regime, the inductor current reference and the input voltage are changed. The currents and voltages of the proposed large-signal average model track well the currents and voltages of the switched model.

The comparison of the controlled system with two controllers PI and the proposed controllers is presented to demonstrate the importance of the sliding mode controller. For the system with the PI controller, the voltage balancing is lost in the transient state when the input powers and/or load resistance R are/is changed.

The controller ensures high robustness properties of the system parameter variations. Despite the changes in the inductances and capacitances, the real part of the eigenvalues always remains to the left of the axis. These results show that the system is stable under the investigated changes. In addition, the eigenvalues are slightly affected by the changes in operating points of the PV panels, and the real part of the eigenvalues always remains to the left of the axis.

Comparing the stored energy in the proposed topology and the topology consisting of two conventional boost converters shows that the cost and volume of the proposed system are adequate. In addition, the efficiency of the proposed topology is better than that of the two conventional boost converters.

As a modular topology, the number of PV panels can be extended thanks to the proposed converter. In the future work, PV panels and MPP search algorithms, which will provide the current reference of each panel, can be introduced.

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