High Gain PWM Method and Active Switched Boost Z-Source Inverter With Less Voltage Stress on the Devices

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***Abstract*—This article presents a new circuit topology for high voltage gain active switched boost quasi Z-source inverter (qZSI) and a pulsewidth modulation (PWM) technique. The higher boosting capability with a lower number of elements, the continuous source current, the less voltage stress across the devices, and having the common ground are the main advantages of the proposed structure. The voltage gain of the proposed inverter is twice that of the conventional capacitor-assisted qZSI (sCA-qZSI). Other benefits of the proposed inverter over the sCA-qZSI are the reduction of Z-source passive components and shoot-through current. Compared to the conventional active switched inductor boost qZSI, the proposed inverter has higher output voltage and also lower shoot-through current, while it has fewer components (one fewer inductor, two fewer diodes, but one more capacitor). The boost factor of the proposed inverter is more than twice that of the classic ones. Besides, a high gain PWM technique is proposed, which can be applied to any types of Z-source inverters. Both the simulation and experimental results of the proposed inverter under the proposed PWM technique are examined to validate their operation.**

***Index Terms*—DC-AC power converters, pulse width modulation converters.**

I. Introduction

In TRADITIONAL voltage source inverters (VSI), dc–ac conversion is only achieved in buck mode. To achieve a higher voltage in VSIs, an extra dc–dc converter is required that, which in turn increases the cost, volume, and losses as well as decreases the efficiency of the system. Moreover, as another defect, a short circuit phenomenon occurs in such systems due to the turning ON of both devices located on the same legs. To overcome these problems, impedance source inverter (ZSI) was introduced that not only surmounts the short circuit problems but also increases the boost capability and a higher voltage is achievable [1]. Because of these improved characteristics, in recent years, ZSIs have found significant attention in the literature, industry, and research and many modifications have been done to their structures [2]. One of these modifications led to the proposal of quasi ZSI (known as qZSI) that possess some benefits over the conventional ZSIs such as continuous input current, lower voltage stresses on the passive components such as capacitor, and common ground between the dc-voltage source and the inverter-bridge [3]. Both devices in the same phase leg can be switched on together to charge the inductor in Z-source topologies. In the basic ZSI, by inserting the shoot-through (ST) state in conventional sinusoidal pulsewidth modulation (SPWM), the voltage gain is increased, where no dc–dc boost converter or transformer is required [1]–[3], while in the conventional VSIs, there are dead time limitations. Adding a dc–dc converter between dc source and inverter bridge to achieve higher voltage magnitude brings some problems and large duty cycles are required. Furthermore, dc–dc converters suffer from reverse-recovery problem, and using them, the rating of power devices is increased [4].

The structure of the Z-source impedance network and the total time of ST state influence the boost factor of the inverter. Thus, to achieve a higher voltage gain, some studies have focused on control methods [5]–[7] and others have suggested working on Z-source circuit topologies, such as switched-inductor or adding extra passive components [8]–[14], active-switched topologies [15]–[25], and transformer or coupled-inductor topologies [26]–[29]. In order to increase the voltage gain, TZ-Source inverter and coupled-inductor ZSI were introduced [29], [27], in which a transformer or a coupled inductor are used in Z-source network. These elements add some transient effects and spikes over the inverter's voltage. In order to resolve these drawbacks, achieving good magnetic coupling with low leakage inductance and low parasitic resistance becomes very important.

Using a switched-inductor or a switched-capacitor is another way to increase the voltage gain in ZSIs. The continuous input current switched-inductor quasi-Z-source inverter known as cSL-qZSI [10] has continuous source current and the voltage gain of the inverter is increased, compared to the basic ZSI, but the boost factor is lowered compared to other switched-inductor topologies. However, cSL-qZSI has the same number of elements as switched-inductor ZSIs. Enhanced-boost ZSI with switched Z-impedance was proposed in [13], in which the source current is discontinuous and considering the fewer number of components added to Z-Source network (inductor, capacitor, and

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diode), the boost factor is reduced. Moreover, the inverter and the dc source have separate grounds.

Embedded-switched inductor-qZSI (ESL-qZSI) and improved embedded-switched inductor-qZSI (iESL-qZSI) were proposed in [8]. ESL-qZSI and iESL-qZSI have high boost ability with symmetric voltage on capacitor compared to cSL-qZSI. However, ESL-qZSI and iESL-qZSI have more components in their Z-source networks as in Z-impedance ZSI [13] and cSL-qZSI [10]. The half-bridge structures are proposed to reduce the number of switches which are more favored for the single-phase applications [30]–[32].

Active switched-qZSIs have a high voltage gain with fewer components in comparison with the switched inductor ZSI topologies, but they have one more extra switch in their impedance network. The extra active switch needs an isolated gate driver [15]–[25] that in turn, creates related problems and requires some considerations. The classic topologies [15]–[17] due to low boost factor ability bring some drawbacks and utilizing them, the voltage stress across the power devices is increased. The switched-capacitor quasi switched boost inverter was presented in [18]. This inverter has a high boost factor with wide duty cycle ranges. In other hand, the active switched-inductor boost qZSI (cASLB-qZSI) [19] has a high voltage boosting ability but, in this structure, the impedance network has a high number of elements. Recently, new concepts of active switched ZSIs structures were presented to improve the low voltage gain shortcoming with desire components count [20]–[24]. However, the aforementioned topologies are not able to surmount these defects. Novel high boost active switched inductor quasi Z-source inverter (HBASL-qZSI) [20] was presented to solve the low boost ability of the classic topologies. However, this inverter suffers from high components count on its ZS network and also, due to the limited duty cycle ratio, control of this inverter becomes difficult. High step-up continuous current active-switched boost Quasi-Z-source inverters (ASCB-qZSI and iASCB-qZSI) [21] have the same problems, too. Dual active-switched-capacitor Quasi-Z-source inverter (DASC-qZSI) [22] is another topology, which offers high output voltage. However, the dual extra switches need two separate gate driver circuits. Utilizing two isolated gate driver may increase the cost of the system. In [23], the active-switched boost quasi-Z-source inverter with few components (ASB-qZSI) was proposed to reduce the number of elements of ZS network in comparison with sCA-qZSI. Both aforementioned inverters have the equal voltage gain. The main benefit of ASB-qZSI over the sCA-qZSI is the less components count in impedance network. The proposed high voltage gain active switched qZSI (HGAS-qZSI) offers higher output voltage with proper number of components count. The boost ability of the proposed inverter is higher than twice that of the classic topologies at which the impedance network elements are less than traditional ones, too. At the same modulation index, the proposed inverter generates higher output voltage than the classic high boost active switched quasi-Z-source inverter (HBS-qZSI) [25]. Therefore, the required ratings of the impedance network components as well as the input current ripple are less in the proposed inverter. Based on the other studies [36], [37], the ZSI is a suitable choice for the PV or fuel cells applications. The benefits of proposed inverter over the classic ZSI and dc–dc converters are validate by simulation, experimental results.

In this article, a new active-switched impedance-source inverter is proposed. The advantages of the proposed inverter include the following:

1) continuous source's current;
2) high voltage gain capability;
3) limited initial inrush current;
4) less voltage stress across the power devices;
5) the boost factor of the proposed HGAS-qZSI is twice that of the conventional sCA-qZSI while it has fewer components;
6) larger boost factor compared to cASLB-qZSI with a fewer number of components;
7) less shoot-through current of the inverter compared to sCA-qZSI;
8) low voltage stress on active switch and capacitors.

The important parameters of ZSIs, including the voltage stress on power devices, the voltage gain, the inductor size, and the shoot-through currents of the proposed HGAS-qZSI are investigated (see Section II). In Section III, the comprehensive analyses of the proposed PWM technique are present. In Section IV, the simulation and experimental results of the proposed inverter under the proposed PWM method are presented. Finally, Section V concludes this article.

II. Proposed Configuration

The proposed HGAS-qZSI structure and its equivalent circuits in ST and non-ST states are shown in Fig. 1. The inrush current at start-up mode is limited by the inductor (L_1). In HGAS-qZSI the load side and the dc input voltage side share common ground. The proposed topology has fewer components than the sCA-qZSI, however, it has a larger boost factor with smaller duty cycle ranges and less ST current. Compared with classic cASLB-qZSI, in the proposed HGAS-qZSI, it is possible to achieve high voltage gain and also low ST current, while it has fewer components [two diodes and one inductor are decreased (by one extra capacitor)].

A. Operation Principle

The equivalent circuits and the current paths of the converter during the ST and non-ST states of the proposed HGAS-qZSI topology are shown in Fig. 1(b) and (c). In the ST state, D_1, D_2, and D_3 are OFF while D_4 is conducting. On the other side, in non-ST state, D_1, D_2, and D_3 are ON while D_4 is reverse biased. In ST modes, the switch S_{AS} is ON and it is OFF in non-ST modes. According to Fig. 1(b) and (c), the voltages across the inductors are obtained as

$$\begin{cases} v_{L1,\,\mathrm{ST}} = V_{C4} + V_{C3} + V_{\mathrm{dc}},\ v_{L2,\,\mathrm{ST}} \\ \quad = V_{C2} + V_{C1},\ V_{C2} = V_{C3} \\ v_{L1,\,n\mathrm{ST}} = V_{\mathrm{dc}} - V_{C1}, v_{L2,\,n\mathrm{ST}} = -V_{C2},\ v_{dc,\max} = 2V_{C2}. \end{cases} \tag{1}$$

Considering the volt-second balance principles of the inductors, the voltages across the active switch, the capacitors, the voltage stress of diodes and their current, and peak value of the

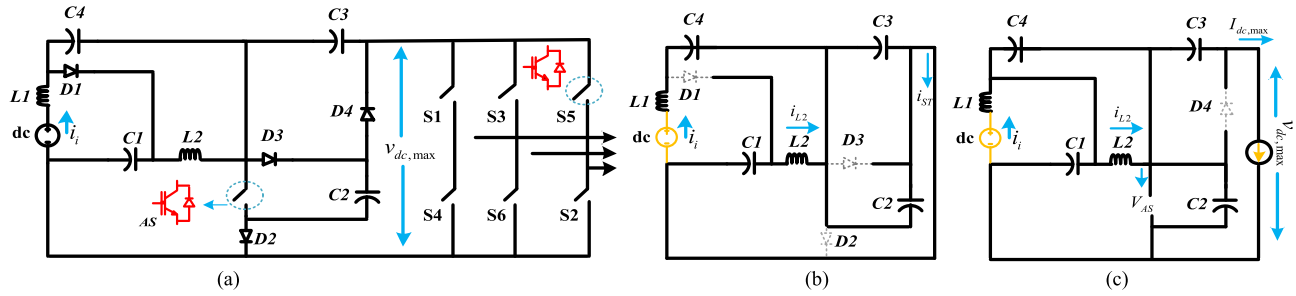

Fig. 1. Proposed power circuit topology and equivalent circuits. (a) HGAS-qZSI. (b) During ST state. (c) During non-ST state.

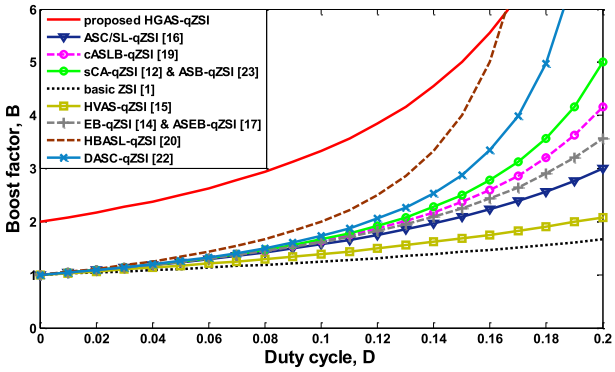

Fig. 2. Variation of B versus D in proposed and classic structures.

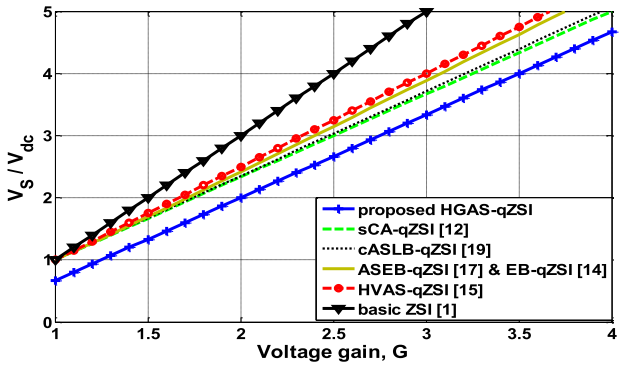

Fig. 3. Variation of $V_S/V_{\rm dc}$ versus G in different inverters with conventional simple boost PWM method (SBC).

dc-link voltage ($v_{\rm dc,max}$) are found as follows:

$$\begin{cases} V_{C1}=\frac{(1-2D)}{(1-4D)}V_{\rm dc} \quad \text{and} \quad V_{C2}=V_{C3}=\frac{1}{(1-4D)}V_{\rm dc} \\ V_{C4}=\frac{2D}{(1-4D)}V_{\rm dc} \quad \text{and} \quad V_{AS}=\frac{1}{(1-4D)}V_{\rm dc} \\ V_{D1}=\frac{2V_{\rm dc}}{(1-4D)}, \quad i_{D1}=\frac{2(1-D)}{1-4D}I_{\rm dc,max} \\ V_{D2,\,D3}=\frac{V_{\rm dc}}{(1-4D)}, \quad i_{D2,\,D3}=\frac{2(1-D)^2}{1-4D}I_{\rm dc,max} \\ V_{D4}=\frac{V_{\rm dc}}{(1-4D)}, \quad i_{D4}=\frac{1}{D(1-4D)}I_{\rm dc,max} \\ v_{dc,\,\rm max}=\frac{2}{(1-4D)}V_{\rm dc}=BV_{\rm dc}. \end{cases} \tag{2}$$

According to (2), the required ratings of the impedance network components are less than dc-link voltage. Fig. 2 shows the boost factor against the duty cycle in the proposed and conventional topologies. As seen in Fig. 2, in terms of boost factor, the proposed topology acts better than other traditional topologies while HGAS-qZSI has fewer components in its impedance network than the sCA-qZSI, cASLB-qZSI, and EB-qZSI. The voltage stress across the switches ($V_S = B.V_{\rm dc}$), if the conventional simple boost PWM control method (SBC [1]) is used to proposed HGAS-qZSI, can be expressed as follows:

$$\begin{cases} G=M.B, M=1-D \quad \text{in SBC PWM} \\ B=2/(1-4D) \text{ in proposed HGAS qZSI} \end{cases} \Rightarrow \frac{V_S}{V_{\rm dc}}=\frac{4G-2}{3}. \tag{3}$$

Fig. 3 demonstrates voltage stress across the switches against voltage gain in the proposed HGAS-qZSI and conventional topologies. According to this figure, in terms of voltage stress across the power devices, the proposed topology acts better than the other classic topologies.

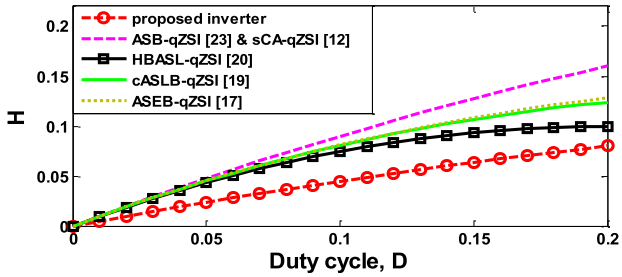

Fig. 4. Variation of $(\Delta i_i\, L)/(V_{\rm dc,\,max}\, T_s) = H$ versus D of the proposed and conventional inverters with the conventional PWM method (SBC).

The input current ripple of proposed inverter by considering (1) can be written as follows:

$$\frac{di_{L1}}{dt}=\frac{v_{L1}}{L}=\frac{2(1-D)V_{\rm dc}}{L(1-4D)}$$

$$\Rightarrow \Delta i_{L1}=\Delta i_i=\frac{DT_S(1-D)V_{\rm dc}}{L(1-4D)}. \tag{4}$$

The input current ripple comparison of the proposed topology and other classic ones, by defining an index $((\Delta i_i\, L)/(V_{\rm dc,\,max}\, T_s) = H)$ at the same dc-link voltage, frequency, and inductance with SBC PWM is shown in Fig. 4. As observed, the input current ripple of the proposed inverter at the same condition is less than the other classic topologies. This is one of the advantages of accessing higher output voltage at the low duty cycle ratio. Also, Table I presents the input current

TABLE I
COMPARISON OF THE INPUT CURRENT

Topology	*Input current*	*ripple*	*Topology*	*Input current*	*ripple*
cASLB-qZSI[19]	Cont	✓	EB-QZSI [14]	Cont	✓
ASEB-qZSI [17]	Cont	✓	HBAL-qZS [20]	Cont	✓
HVAS-qZSI [15]	Cont	✓	ASB-qZSI [23]	Cont	✓
ASC/SL-qZSI [16]	Cont	×	HBS-qZSI [25]	Cont	✓✓✓
sCA-qZSI [12]	Cont	✓	HGAS-qZSI	Cont	✓✓✓

TABLE II
COMPARISON OF THE NUMBER OF COMPONENTS

Topology	*Inductor*	*Capacitor*	*Diode*	*Switch*
cASLB-qZSI[19]	3	3	6	7
ASEB-qZSI [17]	2	2	4	7
HVAS-qZSI [15]	2	2	4	7
ASC/SL-qZSI [16]	2	1	5	7
sCA-qZSI [12]	4	6	3	6
EB-QZSI [14]	4	4	5	6
HBASL-QZSI [20]	3	3	6	7
ASCB-QZSI [21]	3	4	5	7
DASC-QZSI [22]	2	3	4	8
ASB-QZSI [23]	2	3	3	7
HBS-QZSI [25]	2	3	5	7
PROPOSED HGAS-qZSI	2	4	4	7

characteristic of the proposed HGAS-qZSI and the conventional structures.

Table II presents a comparison based on the number of components in the proposed and conventional topologies. As seen, the number of components in impedance network in the proposed HGAS-qZSI is deducted compared to the conventional sCA-qZSI, EB-qZSI, cASLB-qZSI, HBASL-qZSI, and ASCB-qZSI. However, the proposed HGAS-qZSI has a higher voltage gain in high modulation indices compared to sCA-qZSI, EB-qZSI, HBASL-qZSI, and ASCB-qZSI.

B. Comparison of Switches Current (in ST Mode)

This section presents a comparison between the ST current $i_{\rm ST}$ in the proposed inverter and conventional sCA-qZSI. The aim is to perform a comparison between the ST currents in same voltage gain. In lossless condition, the average value of input current (proposed HGAS-qZSI) is obtained as

$$\begin{aligned} V_{\rm dc} I_i &= V_o I_o = P_o \\ I_i &= \frac{v_{\rm ac} I_o}{V_{\rm dc}} = \frac{(v_{\rm ac})^2}{V_{\rm dc}.R} = \frac{(MB)^2 V_{\rm dc}}{8R} \\ V_{\rm ac} &= \frac{1}{\sqrt{2}}\left(MB\frac{V_{\rm dc}}{2}\right) \\ \bar{i}_i &= \bar{i}_{L1} = \frac{12(1-D)^2 V_{\rm dc}}{8R(1-4D)^2} \end{aligned} \tag{5}$$

where *R* is the inverter's load. By applying Kirchhoff current law in the equivalent circuit of the proposed HGAS-qZSI in the ST state in Fig. 1(b), the ST current can be calculated as

$$i_{L1} \approx i_{L2}, \quad i_{\rm ST} = i_{L1} + i_{L2} \approx 2i_{L1}. \tag{6}$$

By substituting the average current of the inductor L_1 (5) in (6), the ST current can be calculated as

$$\bar{i}_{\rm ST} = 2\bar{i}_{L1} = \frac{24(1-D)^2 V_i}{8R(1-4D)^2}. \tag{7}$$

Similarly, in conventional second extension sCA-qZSI [12], the ST current can be written as follows:

$$\begin{cases} i_{L,\,1-4} = \frac{3(1-D)^2 V_i}{8R(1-4D)^2} \\ i_{\rm ST} = 4i_{L1} = \frac{12(1-D)^2 V_{\rm dc}}{8R(1-4D)^2} \end{cases} \text{for conventional sCA - qZSI.} \tag{8}$$

If the classic SBC method is considered for HGAS-qZSI and sCA-qZSI, the relation between duty cycle and voltage gain can be written as follows:

$$\begin{cases} D = \frac{1-G}{1-4G} & \text{for sCA - qZSI} \\ D = \frac{2-G}{2-4G} & \text{for proposed HGAS - qZSI.} \end{cases} \tag{9}$$

By substituting (9) in (8) and (7), Fig. 5 shows the plot of the ST current ($R.\, i_{\rm ST}/V_{\rm dc}$) as a function of voltage gain in HGAS-qZSI and conventional sCA-qZSI. As observed, the ST current in the proposed topology is remarkably low.

When the ST state happens, the inverter bridge is short circuit. Thus, the ST current flows through the inverter bridge. Consequently, decreasing the ST current in HGAS-qZSI can result in reduced conducting losses of the switch in ST modes.

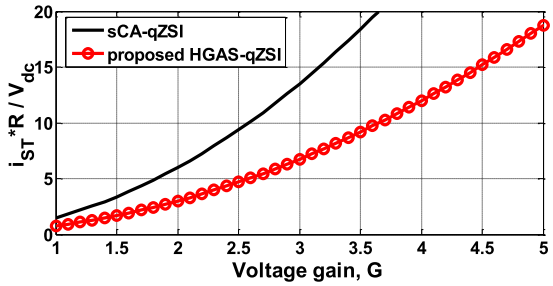

Fig. 5. Variation of $R.\, i_{\rm ST}/V_{\rm dc}$ versus G of proposed and conventional inverters with conventional PWM method (SBC).

C. Calculation of Power Losses

In this part, the power loss calculation of diodes, inductors and switches is given.

1) Power Losses of Diodes: The diodes currents are presented in (2). The total reverse recovery loss of diodes is $P_{\rm loss,\,rrD} = 4.Q_{rr}V_{\rm dc,max}.f_{\rm SW}$. Where $f_{\rm SW}$ is the switching frequency and Q_{rr} is the diode reverse recovery charge. The conducting losses of diode by considering the diode average

and rms current can be calculated as follow:

$$\begin{cases} i_{ave,\,D1}=\frac{2(1-D)^2}{(1-4D)}I_{\mathrm{dc,max}},\ i_{\mathrm{rms},\,D1}=\frac{2(1-D)\sqrt{1-D}}{(1-4D)}I_{\mathrm{dc,max}} \\ i_{ave,\,D2}=\frac{2(1-D)^3}{(1-4D)}I_{\mathrm{dc,max}},\ i_{\mathrm{rms},\,D2}=\frac{2(1-D)^2\sqrt{1-D}}{(1-4D)}I_{\mathrm{dc,max}} \\ i_{ave,\,D3}=\frac{2(1-D)^3}{(1-4D)}I_{\mathrm{dc,max}},\ i_{\mathrm{rms},\,D3}=\frac{2(1-D)^2\sqrt{1-D}}{(1-4D)}I_{\mathrm{dc,max}} \\ i_{ave,\,D4}=\frac{1}{(1-4D)}I_{\mathrm{dc,max}},\ i_{\mathrm{rms},\,D4}=\frac{\sqrt{D}}{D(1-4D)}I_{\mathrm{dc,max}}. \end{cases} \tag{10}$$

Therefore, the power loss dependent on the forward resistance r_D of diodes can be written as follow:

$$P_{\mathrm{loss},\,r_D}=(i_{D1,\,\mathrm{rms}})^2r_D+(i_{D2,\,\mathrm{rms}})^2r_D+(i_{D3,\,\mathrm{rms}})^2r_D+(i_{D4,\,\mathrm{rms}})^2\,r_D. \tag{11}$$

Also, the power loss dependent on the forward voltage drop V_F of diodes can be written as follow:

$$P_{\mathrm{loss},\,V_F}=i_{D1,\,ave}V_F+i_{D2,\,ave}V_F+i_{D3,\,ave}V_F+i_{D4,\,ave}V_F. \tag{12}$$

So, the total losses of the diodes can be calculated as below

$$P_{\mathrm{loss},\,D}=P_{\mathrm{loss},\,V_F}+P_{\mathrm{loss},\,r_D}+P_{\mathrm{loss},\,rrD}. \tag{13}$$

2) Power Losses of Inductor: The inductors current by considering the equivalent circuit of the proposed inverter is calculated as follow:

$$i_{L1}=i_{L2}=\frac{2(1-D)}{1-4D}I_{\mathrm{dc,max}}\ \text{and}\ I_{\mathrm{dc,max}}=\frac{(1-D)V_{\mathrm{dc,max}}}{R}. \tag{14}$$

Here, R is the equivalent resistance of the inverter load. To investigate the power losses of the inductors, the core loss is ignored (because of small current ripple). Therefore, only the conducting loss is considered. So, we have

$$P_{con,\,L1}=(I_{L1,\,\mathrm{rms}})^2.\,r_L,\ P_{con,\,L2}=(I_{L2\mathrm{rms}})^2.\,r_L. \tag{15}$$

Here, r_L is the parasitic resistance of the inductor. The total conducting losses of inductor can be written as follow:

$$P_{con,\,L1,2}=2(I_{L1,\,\mathrm{rms}})^2.\,r_L=2\left(\frac{2(1-D)^2V_{\mathrm{dc,max}}}{R(1-4D)}\right)^2.r_L. \tag{16}$$

3) Power Losses of Switches: The current of the switch located at impedance network in the time interval of (0, DT_S) is derived as follows:

$$i_{AS}=\frac{1}{D(1-4D)}I_{\mathrm{dc,max}}. \tag{17}$$

The average and rms value of the switch current is calculated as follow:

$$i_{AS}=i_{ave,AS}=\frac{I_{\mathrm{dc,max}}}{(1-4D)},\quad i_{\mathrm{rms},AS}=\frac{\sqrt{D}}{D(1-4D)}I_{\mathrm{dc,max}}. \tag{18}$$

So, the switching power losses of this switch is presented in

$$P_{\mathrm{SW},\,AS}=(t_{\mathrm{on}}+t_{\mathrm{off}})/2\times f_{\mathrm{SW}.AS}V_{AS}i_{AS}. \tag{19}$$

Here, f_{SW} is the switching frequency, t_{on} and t_{off} are the turn-ON and turn-OFF delay time of the switch, respectively.

The conducting losses of switch can be calculated as follows:

$$P_{con,\,AS}=(i_{\mathrm{rms}.AS})^2r_{AS}=\left(\frac{\sqrt{D}}{D(1-4D)}I_{\mathrm{dc,max}}\right)^2r_{AS}. \tag{20}$$

Therefore, the total loss of switch is derived as follow:

$$P_{\mathrm{Loss},\,AS}=\frac{t_{\mathrm{on}}+t_{\mathrm{off}}}{2}f_{\mathrm{SW}.AS}\frac{V_{\mathrm{dc}}}{(1-4D)^2}I_{\mathrm{dc,max}}+\left(\frac{\sqrt{D}.I_{\mathrm{dc,max}}}{D(1-4D)}\right)^2r_{AS}. \tag{21}$$

The inverter bridge current (switches of inverter) can be calculated as follows:

$$i_{S,\mathrm{inverter}}=\begin{cases}\frac{i_{\mathrm{ST}}}{3}=\frac{2i_{L1}}{3}=\frac{4(1-D)}{3(1-4D)}I_{\mathrm{dc,max}} & \text{in ST mode}\\ \frac{\sqrt{2}\,v_{\mathrm{ac}}i_{\mathrm{ac}}}{3v_{\mathrm{ac}}\cos\phi\,\pi}=\frac{4v_{\mathrm{ac}}i_{\mathrm{ac}}}{3MBV_{\mathrm{dc}}\cos\phi\,\pi} & \text{in non - ST mode.}\end{cases} \tag{22}$$

The rms current of inverter switches is written as follow:

$$i_{\mathrm{rms},\,S_{\mathrm{inverter}}}=\sqrt{\frac{D}{9}{i_{ST}}^2+\frac{16(1-D)v_{\mathrm{ac}}{}^2{i_{\mathrm{ac}}}^2}{9\pi^2\cos^2\phi\,M^2B^2{V_{\mathrm{dc}}}^2}}. \tag{23}$$

The switching losses of inverter bridge is derived as follows:

$$P_{\mathrm{Loss},\,S_{\mathrm{inverter}}}=6\left(\frac{t_{\mathrm{on}}+t_{\mathrm{off}}}{2}f_{\mathrm{SW}}V_{\mathrm{dc,max}}\frac{i_{\mathrm{ST}}}{3}\right)=6\left(\frac{t_{\mathrm{on}}+t_{\mathrm{off}}}{2}f_{\mathrm{SW}}\frac{V_{\mathrm{dc}}}{(1-4D)^2}\frac{4(1-D)}{3(1-4D)}I_{\mathrm{dc,max}}\right) \tag{24}$$

$$P_{con,\,S_{\mathrm{inverter}}}=6({i_{\mathrm{rms},\,S_{\mathrm{inverter}}}}^2)r_S=6\left(\sqrt{\frac{D}{9}{i_{ST}}^2+\frac{16(1-D)v_{\mathrm{ac}}{}^2{i_{\mathrm{ac}}}^2}{9\pi^2\cos^2\phi\,M^2B^2{V_{\mathrm{dc}}}^2}}\right)^2r_S=6\left(\frac{D}{9}\left(\frac{4(1-D)}{3(1-4D)}I_{\mathrm{dc,max}}\right)^2+\frac{16(1-D)v_{\mathrm{ac}}{}^2{i_{\mathrm{ac}}}^2}{9\pi^2\cos^2\phi\,M^2B^2{V_{\mathrm{dc}}}^2}\right)r_S. \tag{25}$$

The inverter bridge losses can be derived as follows:

$$P_{Loss,\,S_{\mathrm{inverter}}}=6\left(\frac{t_{\mathrm{on}}+t_{\mathrm{off}}}{2}f_{\mathrm{SW}}\frac{V_{\mathrm{dc}}}{(1-4D)^2}\frac{4(1-D)}{3(1-4D)}I_{\mathrm{dc,max}}\right)+6\left(\frac{D}{9}\left(\frac{4(1-D)}{3(1-4D)}I_{\mathrm{dc,max}}\right)^2+\frac{16(1-D)v_{\mathrm{ac}}{}^2{i_{\mathrm{ac}}}^2}{9\pi^2\cos^2\phi\,M^2B^2{V_{\mathrm{dc}}}^2}\right)r_S. \tag{26}$$

Thus, the total switches losses can be calculated as follows:

$$P_{\mathrm{Loss},\,S}=P_{\mathrm{Loss},\,AS}+P_{\mathrm{Loss},\,S_{\mathrm{inverter}}}=\frac{t_{\mathrm{on}}+t_{\mathrm{off}}}{2}f_{\mathrm{SW}.AS}\frac{V_{\mathrm{dc}}}{(1-4D)^2}I_{\mathrm{dc,max}}+\left(\frac{\sqrt{D}}{D(1-4D)}I_{\mathrm{dc,max}}\right)^2r_{AS}$$

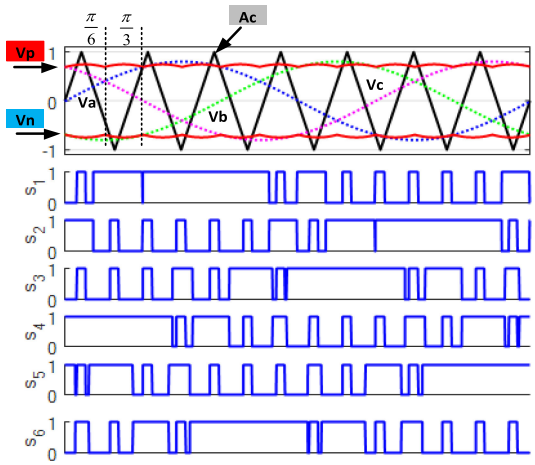

Fig. 6. Typical switching signals of proposed PWM technique.

$$+6\left(\frac{t_{\rm on}+t_{\rm off}}{2}f_{\rm SW}\frac{V_{\rm dc}}{(1-4D)^2}\frac{4(1-D)}{3(1-4D)}I_{\rm dc,max}\right)$$
$$+6\left(\frac{D}{9}\left(\frac{4(1-D)}{3(1-4D)}I_{\rm dc,max}\right)^2+\frac{16(1-D){v_{\rm ac}}^2{i_{\rm ac}}^2}{9\pi^2\cos^2\phi\, M^2B^2{V_{\rm dc}}^2}\right)r_S. \tag{27}$$

As can be seen, the power losses of diodes and switches are associated with the inductor current. Besides, by considering the inductor current relation, it is clear that, in high duty cycle the inductor current is increased. So that, it is important to access high output voltage at low duty cycle to minimize the rating of elements and reduce the losses. One of the benefits of the proposed inverter over the classic ones is providing high voltage gain at low duty cycle. In addition, according to Table II, the components count in the proposed inverter is less, too. So that, the losses in the proposed inverter is decreased.

Total switching device power [33] of diodes and switches by considering the diode and switch voltage and current stress [relations (10) and (22)] can be derived as follow:

$$\begin{cases} SDP_{(\rm peak-diodes)}=\frac{(4D^3-4D^2+1)V_{\rm dc}I_{\rm dc,max}}{D(1-4D)^2} \\ SDP_{(\rm ave-diodes)}=\frac{(4(1-D)^2(2-D)+1)V_{\rm dc}I_{\rm dc,max}}{(1-4D)^2} \\ SDP_{(\rm peak-switches)}=6\left(\frac{8P_o}{3(1-4D)M\cos\phi\,\pi}\right)+\frac{V_{\rm dc}I_{\rm dc,max}}{D(1-4D)^2} \\ SDP_{(\rm ave-switches)}=6\left(\frac{8(1-D)P_o}{3(1-4D)M\cos\phi\,\pi}\right)+\frac{V_{\rm dc}I_{\rm dc,max}}{(1-4D)^2}. \end{cases} \tag{28}$$

III. Proposed Control Method

The switching signal of ZSIs with the proposed novel ST state is demonstrated in Fig. 6. It is obvious that we have 12 sinusoidal shoot-through states (with 30° phase shifted). By using the multiplication of minimum and maximum values of two phase-shifted sets ({0°, 60°, 120°, 180°, 240°, 300°} and {30°, 90°, 150°, 210°, 270°, 330°}) of sinusoidal waveforms, the shoot-through states can be produced. The amplitude of three modulating waves are M and the amplitude of 12 sinusoidal shoot-through waveforms are $\sqrt{M}$. The upper ST state (V_P) and the lower ST state (V_n) in the time interval of (0, 60°) can be calculated as follows. Periodically every $\pi/6$ the ST states are repeated. Therefore, the relation between the modulation index and the duty cycle is calculated as (30). Over the aforementioned interval by integrating (30), the average duty cycle ratio index is found following (31) shown at the bottom of this page:

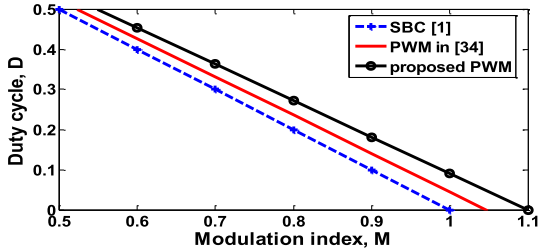

Fig. 7. Variation of D versus M of proposed and other PWM methods.

$$\begin{cases} V_P=\sqrt{M}\sin(\theta-300).\sqrt{M}\sin(\theta-270) & 0\le\theta\le\pi/6 \\ V_P=\sqrt{M}\sin(\theta-300).\sqrt{M}\sin(\theta-330) & \pi/6\le\theta\le\pi/3 \\ V_n=\sqrt{M}\sin(\theta-120).\sqrt{M}\sin(\theta-270) & 0\le\theta\le\pi/6 \\ V_n=\sqrt{M}\sin(\theta-120).\sqrt{M}\sin(\theta-330) & \pi/6\le\theta\le\pi/3 \end{cases} \tag{29}$$

$$D_{\rm ST}(\theta)=\frac{T_0(\theta)}{T_S}=\frac{2-(2M\sin(\theta-300).\sin(\theta-270))}{2}. \tag{30}$$

From (2), the boost factor and voltage gain of the proposed inverter with the proposed PWM method are calculated as follows:

$$B=\frac{2}{3.64M-3}\quad\text{and}\quad G=\frac{2M}{3.64M-3}. \tag{32}$$

A. Comparison of PWM Techniques

The variation of duty cycle versus modulation index is presented in Fig. 7. As seen, the conventional SBC method in which two constant lines are used to insert the ST states does not generate voltage gain when $M=1$. Indeed, maximum boost PWM control method (MBC) was proposed in [35]. In this control method, the duty cycle of ST state has high magnitude in higher modulation index. The ST state is efficacy on inductor

$$\begin{cases} D=\dfrac{\left(\displaystyle\int_0^{\pi/6}2.d\theta-\left(2\int_0^{\pi/6}M\sin(\theta-300).\sin(\theta-270).d\theta\right)\right)}{\displaystyle\int_0^{\pi/6}2.d\theta} \\ \Rightarrow D=1-M\left(\frac{\sqrt{3}}{\pi}+\frac{3}{\pi}\right)=1-0.91M \end{cases} \tag{31}$$

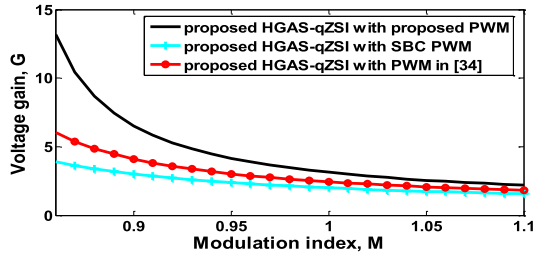

Fig. 8. Variation of G versus M of the proposed inverter with conventional and proposed PWM methods.

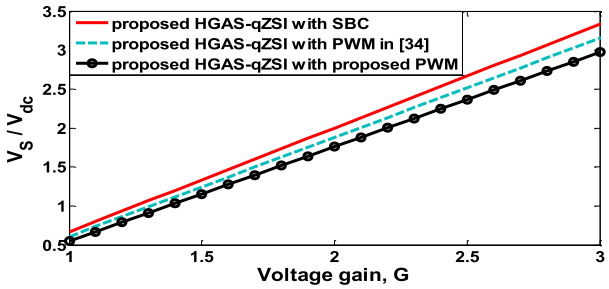

Fig. 9. Variation of voltage stress on power devices versus$G$ of proposed inerter under conventional and proposed PWM methods.

	Conventional PWM methods			proposed PWM
	SBC [1]	MBC [31]	PWM in [34]	
Duty cycle	$1-M$	$1-\frac{3\sqrt{3}}{2\pi}M$	$1-\frac{3M}{\pi}$	$1-0.91M$
Losses	✓✓	×	✓	✓✓
ST current	✓✓	×	✓	✓✓
Δi_L	✓✓	×	×	✓✓
Voltage gain	×	✓✓✓	✓	✓✓
Stress on power devices	×	✓✓✓	✓	✓✓

Fig. 10. Comparison of proposed and traditional PWM method.

current ripple. Designing inductor with large inductor current ripple can increase the size and cost of inductor. Therefore, in maximum boost control method, because of nonconstancy of ST state large inductors are needed in Z-Source network. The proposed PWM technique in high modulation index has a higher duty cycle ratio and almost constant ST states in comparison with conventional PWM methods.

Moreover, in the same modulation index, the proposed PWM technique provides higher ac output voltage compared with other PWM methods (SBC and PWM in [34]). The variation of the voltage gain versus modulation index in the proposed inverter with proposed and conventional PWM methods is shown in Fig. 8. According to this figure, utilizing the proposed PWM technique in the proposed HGAS-qZSI provides higher voltage gain in a high modulation index compared with conventional

TABLE III
PARAMETERS FOR SIMULATION

QUANTITY		*VALUE*
Switching frequency (f_{SW})		$10000Hz$
Reference frequency (f_r)		$50\,Hz$
Boost factor (B)		3.52
Modulation index (M)		0.98, 0.945
Output load	R_L , L_f , C_f	$55\Omega, 1mH, 5\mu F$
Z-source network	C_{1-3}	$220\mu F$
	$L_1 = L_2$	$1mH$
Input voltage (V_i)		$60V$

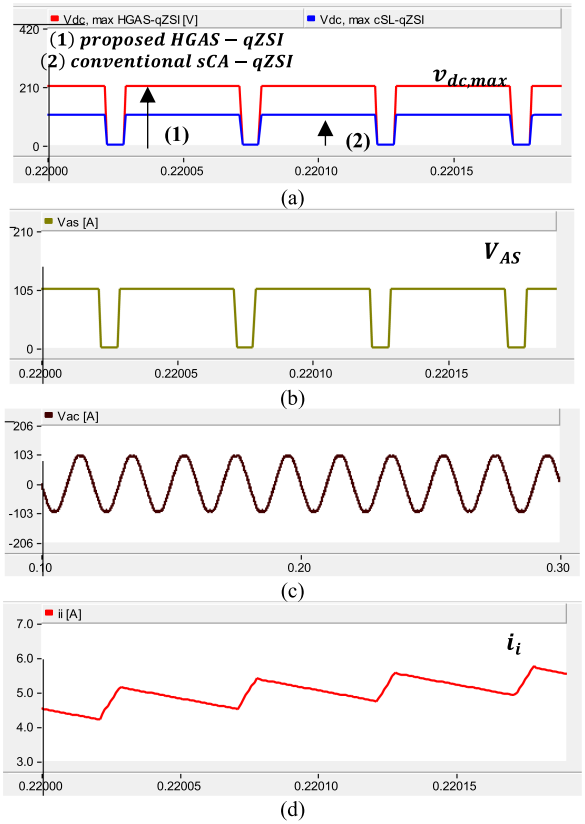

Fig. 11. Simulation results. (a) Dc-link voltage. (b) Voltage on active switch. (c) Output voltage. (d) Source current. When M = 0.98.

PWM methods. The voltage stress across the switches (V_S), if the conventional SBC and high step PWM in [34] is applied to the proposed inverter, can be written as follows:

$$\begin{cases} V_S = BV_{\rm dc} = (\frac{4G-2}{3})V_{\rm dc} & \text{for SBC} \\ V_S = BV_{\rm dc} = (\frac{12G-2\pi}{3\pi})V_{\rm dc} & \text{for PWM in [30].} \end{cases} \tag{33}$$

The voltage stress across the switches (V_S) of the proposed HGAS-qZSI under the proposed PWM technique can be written as follows:

$$\left\{ V_S = BV_{\rm dc} = \left(\frac{3.64G-2}{3}\right) V_{\rm dc} \right. . \tag{34}$$

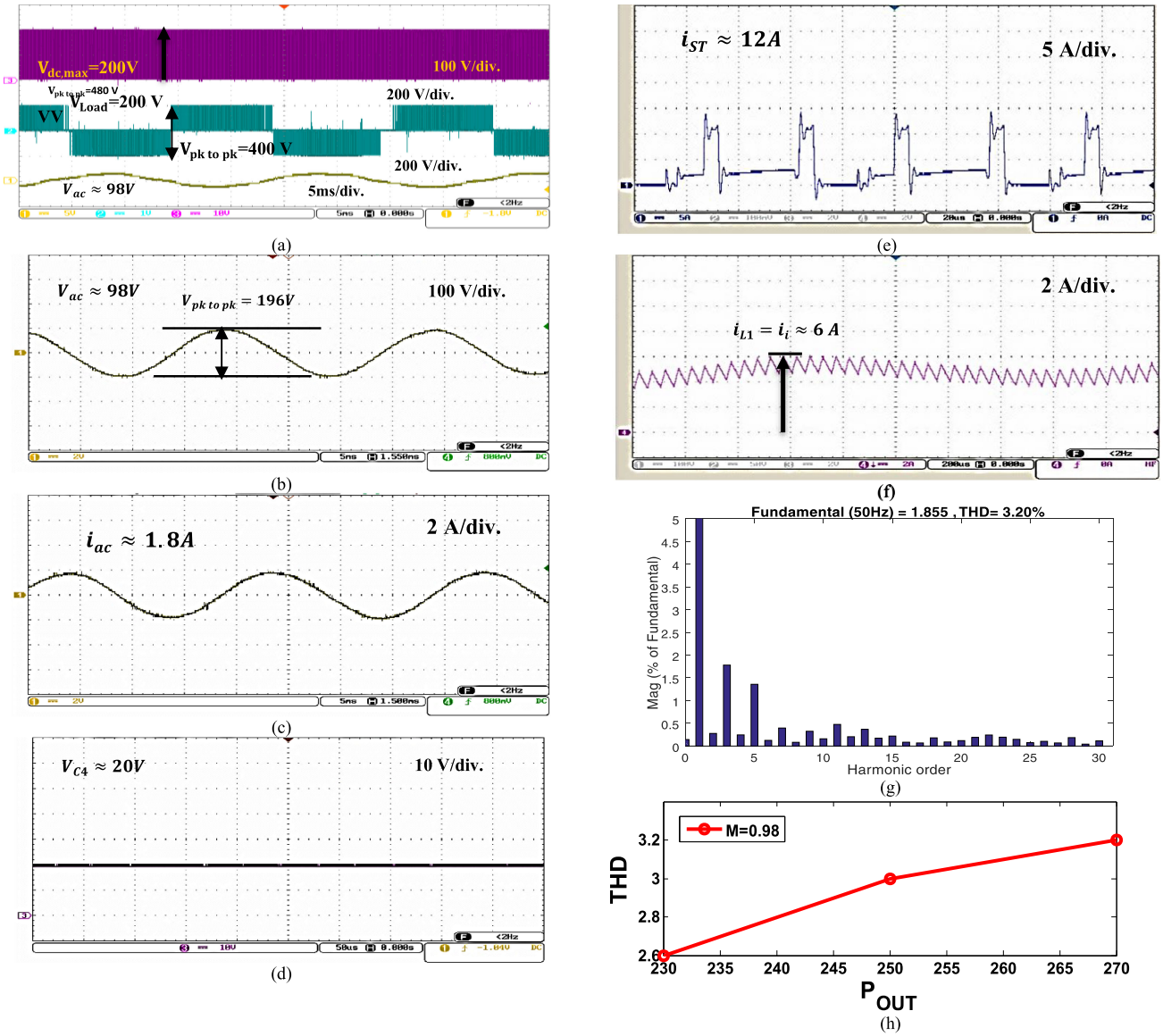

Fig. 12. Experimental results of HGAS-qZSI. (a) Load, ac, and dc-link voltage. (b) AC output voltage. (c) AC output current. (d) Voltage stress across the capacitor (V_{C4}). (e) Shoot-through current. (f) Source and inductor current. (g) Spectrum analysis of output current, for the ac current presented at Fig. 12(c). (h) THDi as function of output power. When M = 0.98.

As is shown in Fig. 9, the voltage stress across the switches of the proposed HGAS-qZSI with the proposed PWM method is improved in comparison with the other classic PWM methods. Fig. 10 presents a comparison between the conventional and the proposed PWM methods considering their pros and cons. At the shoot-through states, the summation current of inductors flows through the inverter bridge switches. In MBC PWM and PWM in [34], the inductor current due to nonconstancy of ST states are high. Therefore, in two classic PWM methods, the conducting losses of the inverter bridge is increased.

IV. Simulation and Experimental Results

In this section, the proposed and conventional inverters are simulated (using ideal components) in power system computer aided design (PSCAD)/electromagnetic transients including DC (EMTDC) with the proposed PMW technique, in the same conditions (see Fig. 11). The parameters used in the simulations and experiments are shown in Table III.

Fig. 11(a) shows the dc-link voltage of HGAS-qZSI and conventional sCA-qZSI. As observed, this voltage in HGAS-qZSI is twice as much as the sCA-qZSI, where the proposed HGAS-qZSI has a fewer number of components. According to Fig. 11(b), it is obvious that the voltage on the active switch of HGAS-qZSI is half of the dc-link voltage. Hence, the required rating of the active switch is less than the dc-link voltage. The ac output voltage and the dc source current are depicted in Fig. 11(c) and (d), respectively. To verify the performance of the proposed topology, under the proposed PWM technique, an experimental setup is developed and the results are presented in this section.

In Fig. 12(a), the load voltage (v_{Load}), the dc-link voltage and the output voltage of HGAS-qZSI when M = 0.98 are presented.

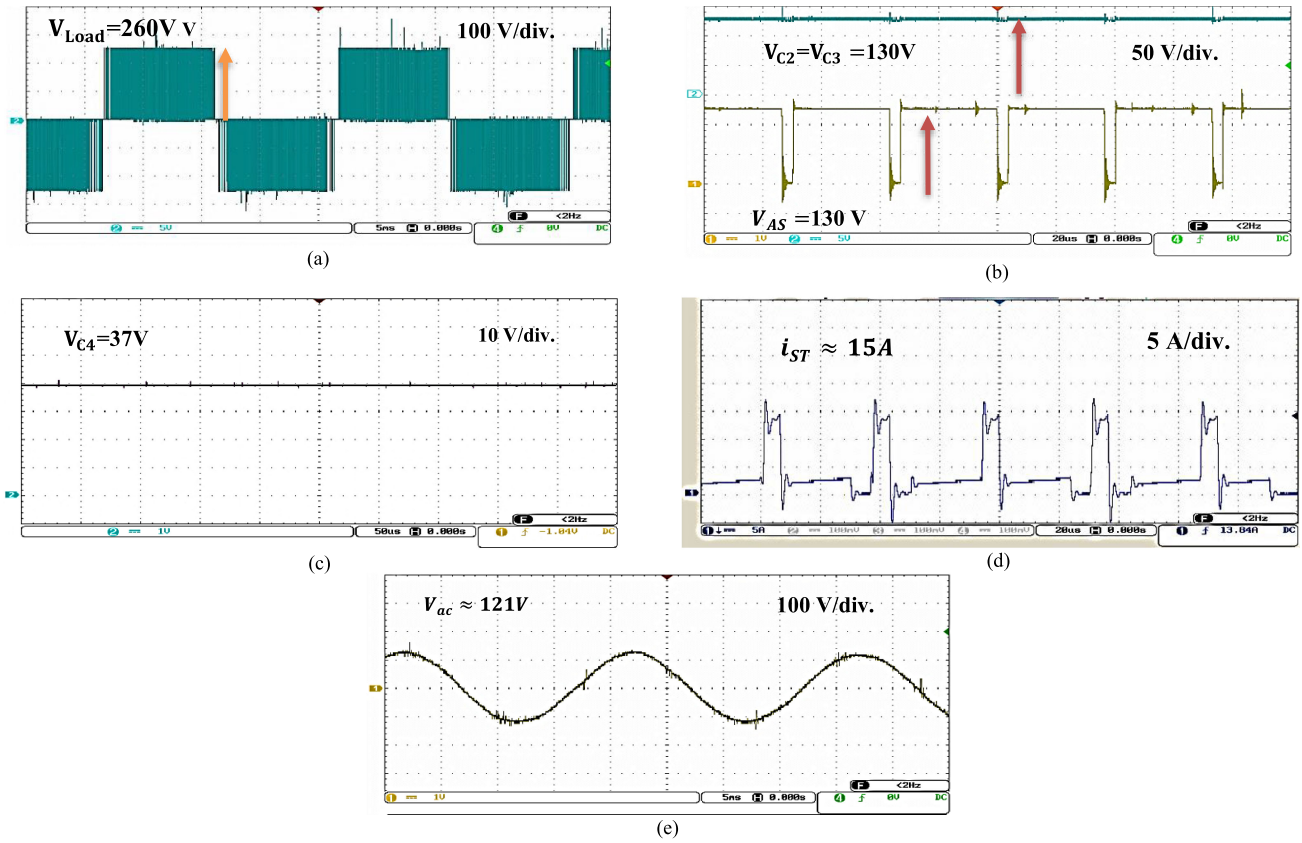

Fig. 13. Experimental results of HGAS-qZSI. (a) Load voltage. (b) Voltage on capacitors and active switch. (c) Voltage stress across the capacitor (V_{C4}). (d) Shoot-through current. (e) AC output voltage when M = 0.945.

As seen, the boost factor is equal to $200/60 = 3.33$ and the ideal boost factor is about 3.52. The ac output voltage and the current are shown in Fig. 12(b) and (c), respectively. The voltage stress of C_4 capacitor is demonstrated in Fig. 12(d). Shoot-through current is shown in Fig. 12(e) and its peak value (6) is about $2i_{L1}$. The source current is continuous where the peak value of this current are about 6A [see Fig. 12(f)]. Fig. 12(g) shows the spectrum analysis of the ac output current. Also, the THDi as function of output power is presented in Fig. 12(h).

In Fig. 13(a), the load voltage (v_{Load}) of HGAS-qZSI when M = 0.945 is presented. It can be seen that the dc-Link is boosted to 260 V from 60 V. Fig. 13(b) consists of the voltage on the capacitors and the active switch. By considering (2) these voltages are half of the dc-link voltage which is measured 130 V. The voltage stress of C_4 capacitor and shoot-through current are depicted in Fig. 13(c) and (d), respectively. Fig 13(e) consists of ac output voltage.

Fig. 14 presents the variation of measured efficiency versus the output power in two modulation indices for the proposed inverters with the proposed PWM method (when $R = 65\,\Omega$, $R = 60\,\Omega$, and $R = 55\,\Omega$). In a high duty cycle, the conducting losses of active and passive components are increased. So that, in a large duty cycle the efficiency of the system is decreased. Due to the high count of components and high summation current of inductors, which is drawn in the inverter bridge in ST mode, the conducting losses of traditional structures are higher than

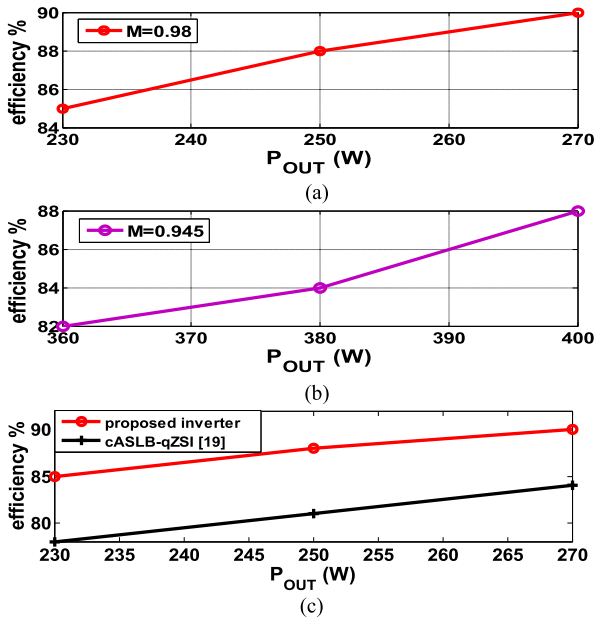

Fig. 14. Measured efficiency. (a) $M = 0.98$. (b) $M = 0.945$. (c) Efficiencies of both proposed and classic cASLB-qZSI [19].

the proposed inverter. All in all, the losses of conventional structures are high. According to Fig. 14 in high output power, the efficiency of the proposed HGAS-qZSI is in a reasonable

range. Besides, at the same operation point, Fig. 14(c) shows the efficiencies of both proposed and classic cASLB-qZSI [19] at which the system efficiency of proposed inverter is high.

V. Conclusion

This article deals with proposing a new circuit topology based on active-switched ZSI. In comparison with classic structures, the proposed HGAS-qZSI can provide high ac output voltage in high modulation index. As result, due to this characteristic, the required ratings of active and passive components in HGAS-qZSI are improved remarkably. In comparison with cASLB-qZSI, for two fewer diodes, one fewer inductor, and one extra capacitor, the ac output voltage of the proposed HGAS-qZSI is higher than twice as much as the cASLB-qZSI. Compared with EB-qZSI and sCA-qZSI, in proposed HGAS-qZSI, it is possible to access approximately double voltage gain where the HGAS-qZSI has fewer components on its impedance network. In ST mode, the summation current of inductors flows in inverter bridge legs. The ST current in the proposed inverter is decreased noticeably. Therefore, the losses are decreased in the proposed HGAS-qZSI. The size, cost, and weight of the system in the proposed HGAS-qZSI, because of reduction of components size is decreased. Due to high voltage gain ability of the proposed PWM at high modulation indices, the voltage stress across the switches is reduced in comparison with the other classic PWM methods. Also, the advantages of the proposed topology are demonstrated by both simulation and experimental results.

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