An MMC-Based IPT System With Integrated Magnetics and ZVS Operations

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***Abstract*—This article proposes a novel high-frequency modular multilevel converter (MMC) for an inductive power transfer (IPT) system. MMCs have many benefits, such as larger modulation depth, more degrees of control, and lower device stresses in comparison to traditional full-bridge converters. However, MMCs are traditionally used for low-frequency applications. Their high-frequency operation differs significantly and has not been reported yet. This article focuses on the 85-kHz operation of an MMC driving the primary compensation circuit of an IPT system. The high-frequency operation of the MMC allowed the proposed design to integrate the dc arm inductors with the primary compensation network of an IPT system, lowering the component count. A digitized modulation scheme is used to regulate the output power while maintaining zero-voltage switching under the range of operating conditions considered. To validate the proposed MMC-based IPT system, an SAE J2954 WPT2/Z2 compliant prototype is built and tested, which achieves up to 93% efficiency when transferring 7.7 kW with a 220% variation in coupling factor and a varying output battery voltage between 280 and 420 V.**

***Index Terms*—Electric vehicle (EV), inductive power transfer (IPT), modular multilevel converter (MMC).**

I. Introduction

INDUCTIVE power transfer (IPT) is becoming one of the most suitable solutions for charging electric vehicles (EVs) [1]. It is convenient, safe in hostile environments, and aesthetically pleasing. IPT also enables autonomous charging for taxi fleets and self-driving vehicles in the future.

IPT-based wireless EV chargers should adhere to international standards such as the SAE J2954 to ensure that interoperability, safety, and performance requirements are met [2]. These standards typically expect the charger to maintain a constant power transfer as the magnetic coupling k between the ground assembly and the vehicle assembly varies in the range between 0.1 and 0.3 (a 300% change). Furthermore, the charger is also expected to deliver the rated power as the state of charge of the EV battery changes by 150% (i.e., the battery voltage V_{batt} changes between 280 and 420 V for a nominal 400-V EV battery or between 560 and 840 V for a nominal 800-V EV battery) [3]. Therefore, the power converters used in an IPT-based EV charger should be capable of efficiently handling load variations up to 450%. However, it is extremely challenging to develop an efficient power converter to operate under these varying conditions while also achieving higher power levels.

The widely used methods to regulate the power output of an IPT system under a large load variation can be classified into two groups: controlling the dc-link voltage and controlling the IPT converters. To control the dc-link voltage, researchers have developed sophisticated power factor correction (PFC) circuits [4] that produce a wide range of output voltages. However, this is done at the cost of using overrated switches and more complex filter and control circuitry [5]. Another popular method to control the dc-link voltage is to use an additional dc–dc converter prior to the IPT primary-side converter [6]. Such a design simplifies the requirements for the PFC unit and the IPT converter. However, it adds an extra power conversion stage into the transmission train, which results in higher cost and lower overall efficiency [3]. IPT systems commonly employ a primary-side control, which typically applies duty-cycle or phase-shift modulation to the primary converter to regulate the power flow. A simple passive rectifier on the secondary side is employed to ensure a simple secondary-side design and a simple control system. However, the primary-side modulation depth required to cope with a 450% load variation significantly increases the converter loss due to unfavorable switching conditions. Often expensive SiC devices have to be used to counter the high losses [7], [8], and in some cases, multiple paralleled SiC devices are used to share the power loss [9]. To reduce the stress on the primary converter in a primary-side controlled system, researchers have developed dual-side control, which enables impedance matching. This method can actively distribute the losses among the primary and secondary magnetic couplers, thus achieving the optimal ac–ac efficiency [10], [11]. However, it increases the complexity of the power electronics on the vehicle side, which is undesirable from the EV manufacturer's point of view.

To accelerate the adoption of wireless EV charging, a simple and low-cost vehicle side design is essential, and therefore, the primary-side-controlled IPT systems are preferred [7]. The industry typically uses full-bridge (FB) as the primary converter of a primary-side-controlled IPT system. However, in contrast to traditional FB converters, multilevel converters can achieve higher power levels at the cost of using more power

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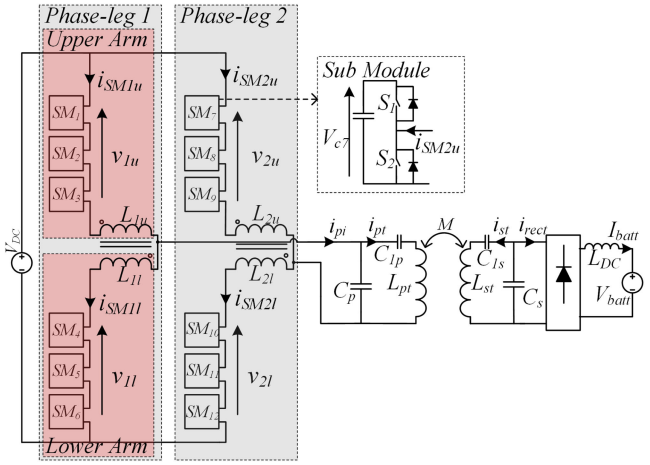

Fig. 1. Proposed MMC-based IPT system.

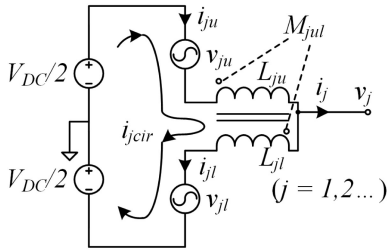

Fig. 2. Per-phase equivalent circuit of the MMC.

semiconductors. They also have added benefits such as large modulation depth, low total harmonic distortion, and the possibility of using lower voltage devices, overriding some disadvantages [12], [13]. Multilevel converters are relatively new in IPT systems. A MARX inverter that can generate staircase waveforms was demonstrated in [14]. Here, each step of the staircase is limited to the dc source voltage. A switched capacitor topology with an added FB stage was proposed in [15]. Such a design uses a higher number of switches, and the staircase waveform steps are also equal to the dc source voltage. A five-level converter consisting of two series-connected half-bridges was presented in [16] and [17]. However, the phase shift between the two half-bridges resulted in an asymmetric waveform. A cascaded H-bridge converter was used in [18] and [19], but such a system requires multiple independent dc sources, which is undesirable.

A modular multilevel converter (MMC) could be suitable to implement a primary-side-controlled high-power IPT system. The use of MMCs in HVdc or medium-voltage drive systems has been thoroughly studied in the literature [20], [21]. However, the MMCs in those systems operate at low frequencies (typically 10s of hertz to 100s of hertz) in comparison to the 85 kHz required in IPT systems. The operation of an MMC in an IPT system significantly differs from low-frequency MMCs reported to date.

This article evaluates a high-frequency MMC suitable for primary-side-controlled IPT systems; the circuit diagram is shown in Fig. 1. On a high level, the highlights and the advantages of the proposed system are shown as follows:

1) the use of MMC topology:
   1) a large freedom of control;
   2) a wide operating range;
   3) converter modularity, easy to scale the power level;
2) the use of integrated magnetics:
   1) dual-purpose arm inductors are also used for the first LCL compensation inductor;
   2) a lower inductor core count;
   3) a large dc equivalent arm inductance, reducing the arm ripple current;
3) the zero-voltage switching (ZVS) operation:
   1) the proposed digitized modulation ensures ZVS for all switches;
   2) the ability to use cheap Si MOSFETs;
   3) high efficiency for high-frequency operation.

The rest of this article is organized as follows. In Section II, this MMC-based IPT system operation is discussed. In Section III, the use of integrated magnetics is explained. In Section IV, a digitized modulation scheme used in the proposed MMC is explained, a primary-side open-loop controller is presented, and a capacitor voltage balancing algorithm is demonstrated. In Section V, a 7.7-kW MMC with 12 submodules (SMs) was built and tested under the SAE J2954 WPT2/Z2 specifications, and the results are discussed in detail. Finally, Section VI concludes this article.

II. MMC-Based IPT System Operations

A. MMC Operation Principles

The per-phase-leg equivalent circuit diagram of the MMC is shown in Fig. 2. The bus voltage $V_{\rm DC}$ is divided into two parts, where the middle point is a virtual ground reference. The series-connected SMs in upper and lower arms form v_{ju} and v_{jl}, where the subscript j denotes the particular phase leg (in this article, j is 1 or 2 since a single-phase system is considered). u and l denote the upper and lower arms. Using the same subscripts, the arm inductors of a phase leg are labeled as L_{ju} and L_{jl}. The current through upper and lower arms of the phase leg is given by [20]

$$i_{ju} = i_{j\rm cir} + \frac{i_j}{2}, \qquad i_{jl} = i_{j\rm cir} - \frac{i_j}{2}. \tag{1}$$

According to [22], an MMC can be characterized by two equivalent circuits: the common mode and the differential mode. The common-mode voltage of a phase leg generates the load current (i_j), while the differential-mode voltage generates the circulating current ($i_{j\rm cir}$), as shown in Fig. 3. The common-mode and differential-mode voltages are given by

$$v_{j\rm common} = \frac{v_{jl} - v_{vju}}{2} \tag{2}$$

$$v_{j\rm diff} = V_{\rm DC} - (v_{ju} + v_{jl}). \tag{3}$$

The circulating current can be separated into a dc part and an ac part. The dc part is equal to the dc current shared by the two phase legs in a single-phase system, and the ac part is due to $v_{\rm diff}$

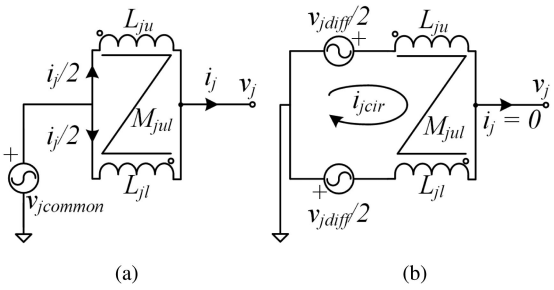

Fig. 3. MMC per-phase equivalent circuit. (a) Common mode. (b) Differential mode.

as given by

$$i_{j\text{cir}} = I_{\text{DC}}/2 + i_{j\text{cirAC}} = \frac{\text{Power}}{2V_{\text{DC}}} + i_{j\text{cirAC}} \tag{4}$$

$$i_{j\text{cir}_{\text{AC}}} = \frac{1}{L_{ju} + L_{jl} + 2M_{jul}} \int v_{j\text{diff}} dt. \tag{5}$$

In traditional MMC applications, where the fundamental frequency of the load current is relatively low, the controller must ensure that v_{diff} is minimized to suppress the ac circulating current. However, in MMC-based IPT systems, the fundamental frequency of the load current is 85 kHz. This leads to significantly lower ac circulating currents due to the arm inductances presenting high impedances. As such, it is not an essential criterion that the controller tries to maintain v_{ju} and v_{jl} equal. In fact, as explained in Section IV, the proposed MMC-based IPT system exploits this feature to develop a digitized modulation scheme that facilitates ZVS.

B. Proposed MMC IPT System Equivalent Circuit

This article considers a primary-side-controlled single-phase MMC-based IPT system, as shown in Fig. 4(a). To help explain the operations, the equivalent circuit models shown in Fig. 4 are used. The arm voltages of the MMC are represented by voltage sources v_{1u}, v_{1l}, v_{2u}, and v_{2l}. The arm inductors are notated as L_{1u}, L_{1l}, L_{2u}, and L_{2l}. To reduce the size of the arm inductors of each phase leg, they are constructed as coupled inductors, where M_{1ul} and M_{2ul} represent the mutual inductance between them. The compensation network of the IPT system is represented by Z_{load}, as shown in Fig. 4(a). As discussed previously, using the per-phase-leg circuit transformation and superposition, the common-mode equivalent circuits can be derived as in Fig. 4(b). The coupled inductors can be further simplified to obtain Fig. 4(c).

Finally, Fig. 4(c) can be equalized to a voltage-source-driven IPT system with an LCL compensation network on the primary side, as shown in Fig. 4(d). The most generic form of the equivalent voltage source (v_{pi}) and the equivalent inductance (L_{pi}) can be expressed by

$$\begin{aligned} v_{pi} &= v_{1\text{common}} - v_{2\text{common}} \\ &= \frac{v_{1l}(L_{1u} - M_{1ul}) - v_{1u}(L_{1l} - M_{1ul})}{L_{1u} + L_{1l} - 2M_{1ul}} \\ &\quad - \frac{v_{2l}(L_{2u} - M_{2ul}) - v_{2u}(L_{2l} - M_{2ul})}{L_{2u} + L_{2l} - 2M_{2ul}} \end{aligned} \tag{6}$$

$$L_{pi} = \frac{L_{1u}L_{1l} - M_{1ul}^2}{L_{1u} + L_{1l} + 2M_{1ul}} + \frac{L_{2u}L_{2l} - M_{2ul}^2}{L_{2u} + L_{2l} + 2M_{2ul}}. \tag{7}$$

The arm inductors L_{1u}, L_{1l}, L_{2u}, and L_{2l} are typically designed to be the same value, and their mutual inductances M_{1ul} and M_{2ul} are usually somewhat identical. Therefore, (6) can be simplified as

$$v_{pi} = \frac{(v_{1l} - v_{1u}) - (v_{2l} - v_{2u})}{2}. \tag{8}$$

The compensation networks employed in the IPT system proposed (i.e., LCL-tuned primary and parallel tuned secondary) are the recommended design in the SAE J2954 standard and have been studied thoroughly in the literature [2], [10]. Therefore, this article will not go into the details of deriving equations to characterize the power transfer through the compensation networks. As discussed in [2] and [10], both primary and secondary compensation networks are tuned to the fundamental frequency f_{sw} of v_{pi}, as given by

$$\omega_{\text{sw}} L_{pt\_\text{eff}} = \omega_{\text{sw}} L_{pt} - \frac{1}{\omega_{\text{sw}} C_{1p}} = \omega_{\text{sw}} L_{pi} = \frac{1}{\omega_{\text{sw}} C_p} \tag{9}$$

$$\omega_{\text{sw}} L_{st\_\text{eff}} = \omega_{\text{sw}} L_{st} - \frac{1}{\omega_{\text{sw}} C_{1\,s}} = \frac{1}{\omega_{\text{sw}} C_s} \tag{10}$$

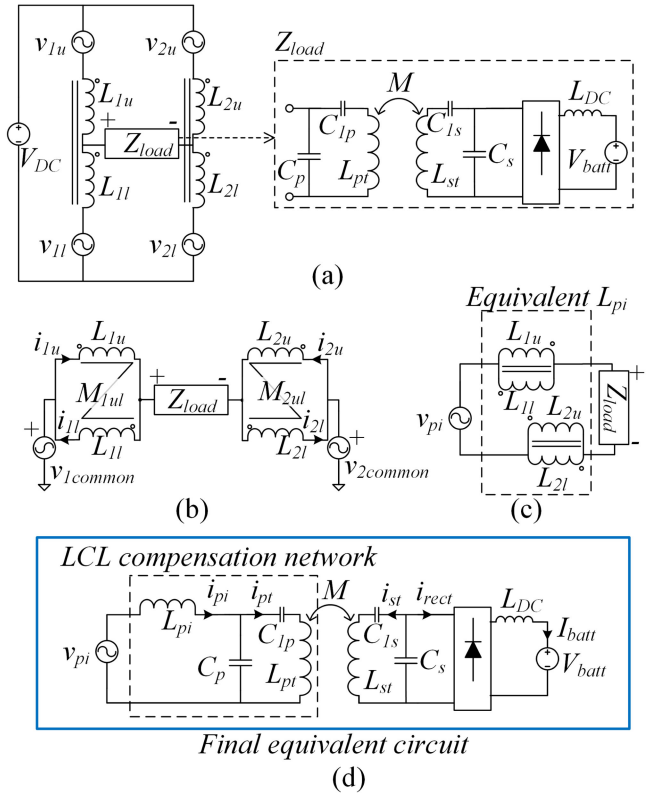

Fig. 4. MMC-based IPT system equivalent circuit transformation. (a) Simplifying arm voltages. (b) Equivalent voltage-source transformation. (c) Equivalent inductor transformation. (d) Final simplification to traditional LCL-P IPT system.

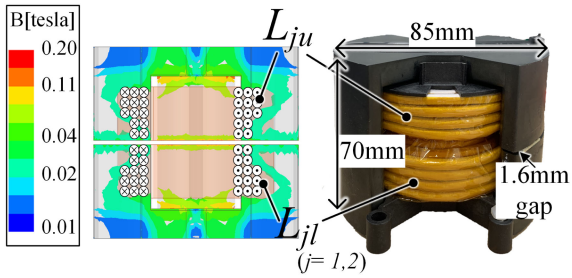

Fig. 5. ANSYS simulation and actual inductor.

where $\omega_{\text{sw}} = 2\pi f_{\text{sw}}$. Under the tuned conditions specified in (9) and (10), most of the power transfer happens at the fundamental frequency, which can be simplified to

$$P \cong \frac{k\sqrt{L_{pt}L_{st}}\hat{v_{pi}}V_{\text{batt}}}{\omega_{\text{sw}}L_{pi}L_{st\_\text{eff}}} \tag{11}$$

where $\hat{v_{pi}}$ is the amplitude of v_{pi}.

III. Integrated Magnetics

This section discusses how the integrated magnetics serve different purposes in the proposed MMC, as shown in the two circuit modes in Fig. 3.

In the differential-mode equivalent circuit, the arm inductors act as an equivalent dc inductor for each phase leg, which can be calculated by

$$L_{\text{armDC(per phase)}} = L_{ju} + L_{jl} + 2M_{jul} \quad (j = 1 \text{ or } 2). \tag{12}$$

This equivalent dc inductor is used to store energy and transfer it to the SM capacitors. It is also used to suppress the circulating current derived in (5). Therefore, the equivalent dc inductance needs to be sufficiently large, and the coupled inductor structure helps achieve a larger dc inductance.

In the common-mode equivalent circuit, the arm inductors act as the equivalent L_{pi} that forms the LCL compensation network. The equivalent circuit transformation is shown in Fig. 4(b)–(d), where the equivalent L_{pi} can be calculated using (7). Unlike L_{armDC}, the equivalent L_{pi} inductance is used for tuning the LCL compensation network. Therefore, its inductance should be within 10% of the desired value [23] to avoid impacting the power transfer. According to the manufacturer data sheet and from ANSYS simulations, each of the coupled arm inductors in a phase leg can be implemented using two windings wound on a single PM 87 core. The equivalent L_{pi} value is proportional to the number of turns and is not sensitive to the air-gap. This is because with a larger air-gap, the coupling factor between the two windings will reduce, but so will the winding inductance itself. As such, the resultant L_{pi} will remain largely unchanged. For example, ANSYS simulations show that an air-gap from 1 to 5 mm results in only a 2.7% variation in the resultant L_{pi} value. The authors used 13 turns of 4-mm-diameter Litz wire to construct the two coupled arm inductors used in the prototype system. The ANSYS simulation and the actual inductors used are shown in Fig. 5, and their specifications are summarized in Table I.

TABLE I
Arm Inductor Specifications

	L_{1u}	L_{1l}	L_{2u}	L_{2l}
Core size & material	PM87 & N87			
Max current rating	50A RMS			
Air gap	1.6 mm			
Number of turns	13			
Inductance (μH)	92.1	90.7	92.7	93.1
Mutual inductance M_{1ul} & M_{2ul} (μH)	77.3		78.7	
Equivalent $L_{pi}(\mu H)$ & $R_{ac}(\text{m}\Omega)$	14.2 & 43			
Equivalent $L_{\text{armDC}}(\mu H)$ & $R_{DC}(\text{m}\Omega)$	337 & 16		343 & 16	

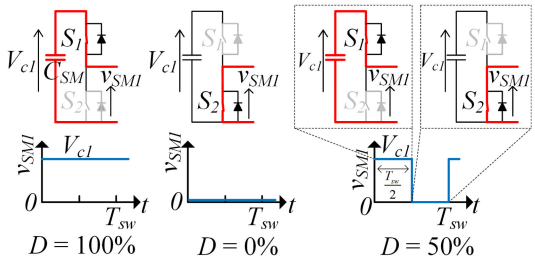

Fig. 6. Three operating modes of an SM when utilizing digitized modulation.

IV. Control of the MMC-Based IPT System

A. Digitized Modulation for MMC

MMCs used in traditional applications usually produce relatively low fundamental frequency components under a few hundred hertz. The modulation schemes for such applications have been studied thoroughly in the literature, and popular options include phase-shifted carrier pulsewidth modulation (PWM), space vector modulation, selective harmonic elimination, and staircase modulation [20]. Such modulation techniques are not suitable for IPT applications as the MMC is required to synthesize a high fundamental frequency. A novel digitized modulation scheme is, therefore, proposed to operate the proposed MMC to synthesize the 85-kHz fundamental required for driving an IPT system. Instead of generating many switching instances within one fundamental frequency cycle, the proposed modulation ensures that no more than one switching instance happens within one fundamental frequency cycle.

Traditional PWM used in MMCs ensures that the capacitor in each SM is maintained at a voltage V_{DC}/N (where N is the number of SMs in that arm, and therefore, in the case shown in Fig. 1, N is 3). However, in the proposed digitized modulation scheme, the voltage of each SM capacitor is a function of the duty cycle that the SM is operating at. Assuming that an SM in a phase leg is operated at a duty cycle, D, where D is the ratio between the time the SM is inserted and the switching period, $T_{\text{sw}} = 1/85$ kHz, with the digitized modulation scheme, each SM can only operate at one of three duty-cycle values. These are 100%, 0%, or 50%, as shown in Fig. 6.

Within each phase leg in the proposed MMC system, during one switching period, it is assumed that an a number of SMs are operated at $D = 100\%$, a b number of SMs are operated at $D = 0\%$, and a c number of SMs are operated at $D = 50\%$.

TABLE II
MMC OUTPUT VOLTAGE LEVELS AT DIFFERENT DUTY-CYCLE PATTERNS WHEN $V_{\mathrm{DC}} = 400$ V

Duty-Cycle Pattern No.	a*	b*	c*	SM voltage (14)	$\hat{v_{pi}}$ (16)
#1	0	0	6	133 V	400 V
#2	1	0	5	114 V	286 V
#3	1	1	4	133 V	266 V
#4	1	2	3	160 V	240 V
#5	2	0	4	100 V	200 V
#6	2	1	3	114 V	171 V
#7	3	0	3	89 V	134 V
#8	3	1	2	100 V	100 V
#9	4	0	2	80 V	80 V
#10	3	2	1	114 V	57 V
#11	4	1	1	89 V	45 V
#12	5	0	1	73 V	37 V

*Note: a = number of SMs running 100% duty cycle in a phase leg, b = number of SMs running 0% duty cycle in a phase leg, and c = number of SMs running 50% duty cycle in a phase leg.

Each combination of a, b, and c represents a duty-cycle pattern, and each duty-cycle pattern will create different SM capacitor voltages and different output voltages. For an MMC consisting of 12 SMs, there could be a total of 28 unique duty-cycle patterns, of which 12 are meaningful duty-cycle patterns, which are shown in Table II.

The relationship between the SM capacitor voltages and the duty-cycle pattern can be determined as follows. At a certain duty-cycle pattern under steady-state operating conditions, the volt–second product across the arm inductors L_{ju} and L_{jl} in a phase leg must be zero. Therefore, this yields

$$V_{\mathrm{DC}} - \overline{v_{ju}} - \overline{v_{jl}} = V_{\mathrm{DC}} - V_{C\mathrm{avg}}$$
$$(a \cdot 100\% + b \cdot 0\% + c \cdot 50\%) = 0. \tag{13}$$

By rearranging (13), the average of the SM capacitor voltages can be written as

$$\overline{V_C} = V_{C\mathrm{avg}} = \frac{V_{\mathrm{DC}}}{a + 0.5c}. \tag{14}$$

Note that, when operating under steady-state conditions, the voltages across all SMs are kept at $V_{C\mathrm{avg}}$. This is achieved through a capacitor voltage balancing algorithm, which will be discussed in the next section.

To understand the relationship between the output voltage of the MMC and the duty-cycle pattern applied, consider the example circuit shown in Fig. 1. Using phase-leg 1 upper arm SMs as the reference, according to (8), the phase-leg 2 lower arm SMs are in phase, while phase-leg 1 lower arm SMs and phase-leg 2 upper arm SMs are 180° out of phase. As such, the resultant output voltage v_{pi} is guaranteed to be a symmetrical waveform, and v_{pi} can be expressed by a, b, and c in a piecewise periodic function

$$v_{pi}(t) = v_{pi}(t + T_{\mathrm{sw}}) = \begin{cases} \dfrac{c}{2a + c} V_{\mathrm{DC}}, & 0 \le t < 0.5T_{\mathrm{sw}} \\ \dfrac{-c}{2a + c} V_{\mathrm{DC}}, & 0.5T_{\mathrm{sw}} \le t < T_{\mathrm{sw}}. \end{cases} \tag{15}$$

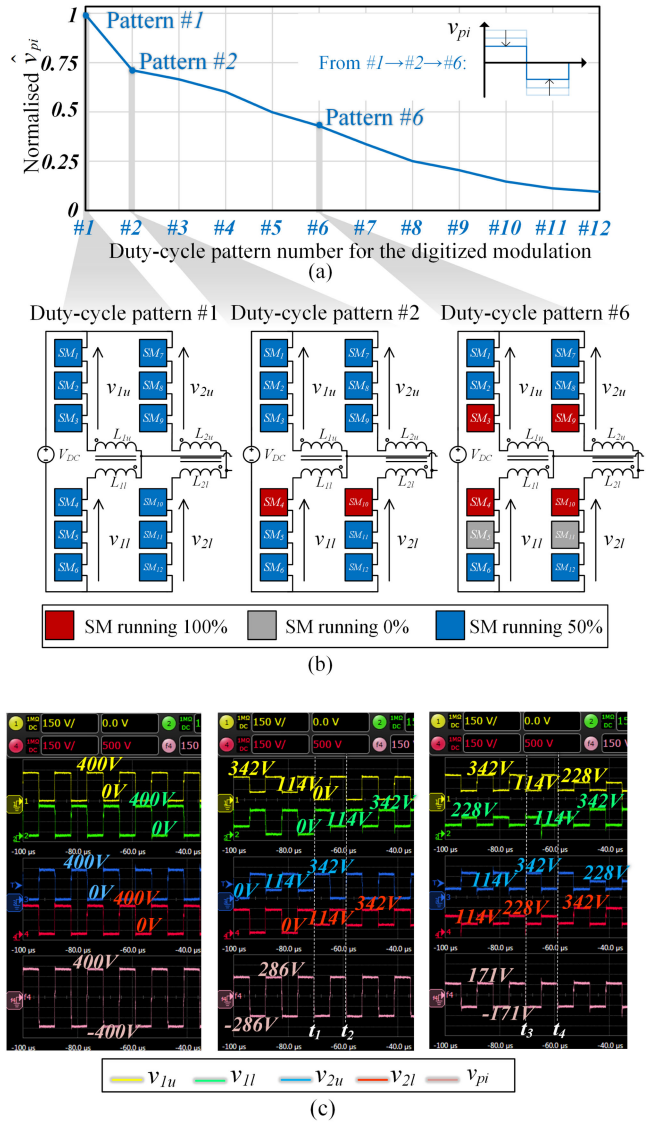

Fig. 7. Digitized modulation operations. (a) Duty-cycle pattern number versus output voltage amplitude. (b) Visualization for different duty-cycle patterns. (c) Experimental waveforms when running duty-cycle patterns #1, #2, and #6.

The amplitude of v_{pi} is

$$\hat{v_{pi}} = \frac{c}{2a + c} V_{\mathrm{DC}}. \tag{16}$$

An example of the proposed MMC regulating $\hat{v_{pi}}$ by applying different duty-cycle patterns is shown in Fig. 7 to highlight the operation of the digitized modulation. As visualized in Fig. 7(b), when running duty-cycle pattern #1, all SMs are at 50% during any switching cycle. At duty-cycle pattern #2, there are five SMs operating at 50% D and one SM operating at 100% D in each phase leg during a switching cycle. During time $t_1 - t_2$ in Fig. 7(c), the SMs with 100% D are within the lower arms in both phase legs 1 and 2. This is demonstrated by the voltage level 114 V in v_{1l} and v_{2l}, which is contributed by the SMs at 100% D. However, before t_1, the SMs at 100% D were in the upper arms in each phase leg. The reason for the variation of which SMs are operated at 100% D is due to the capacitor voltage balancing

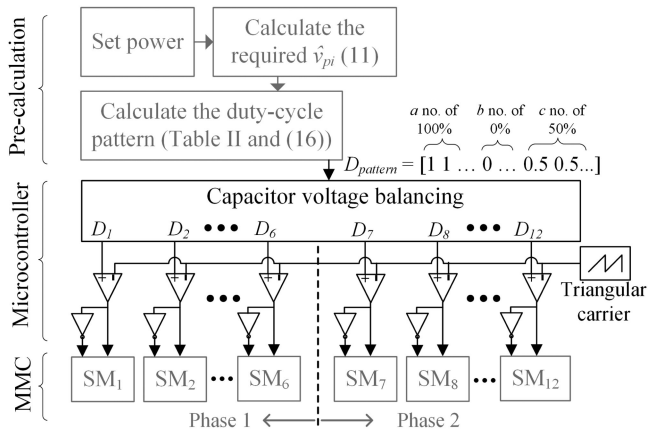

Fig. 8. Open-loop controller for an MMC-based IPT system.

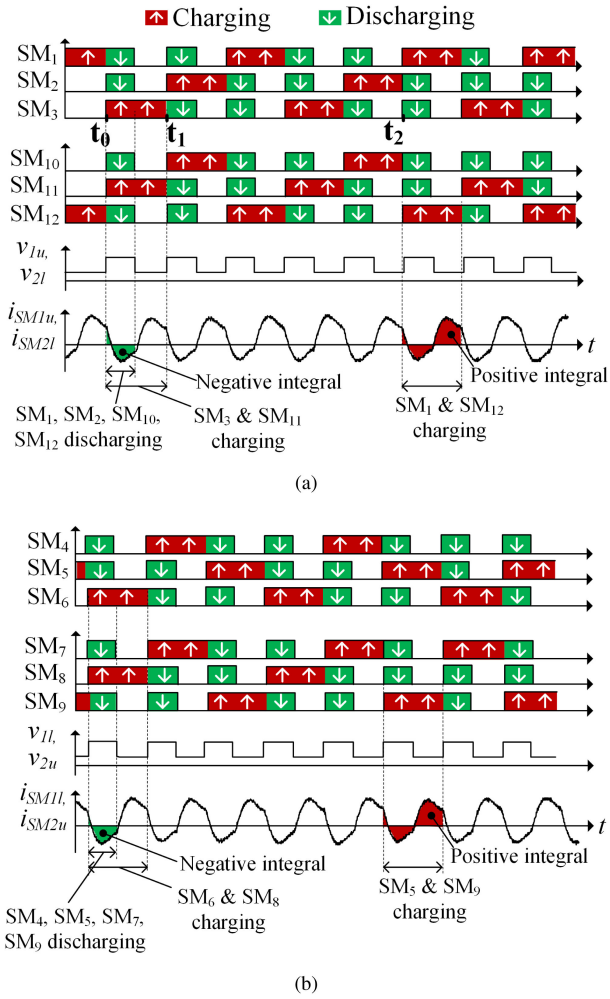

Fig. 9. Example of SMs capacitor charging/discharging for (a) phase leg 1 and (b) phase leg 2.

algorithm. It adjusts which SM will be operated at 100% D during the next switching cycle to ensure that the voltages across all SMs are approximately 114 V. At duty-cycle pattern #6, there are three SMs operating at 50% D, two SMs operating at 100% D, and one SM operating at 0% D in each phase leg. During time $t_3 - t_4$ in Fig. 7(c), the 0% D SMs are in the lower arms in each phase leg. After t_4, the 0% D SMs are changed to the upper arms. This is again a result of the capacitor voltage balancing algorithm. The experimental waveforms in Fig. 7(c) match well with the voltage levels shown in Table II, which verifies the validity of controlling the MMC with the proposed digitized modulation.

The digitized modulation allows for the MMC to generate a controllable v_{pi} amplitude at its output while ensuring it is a perfect square wave. This scheme, therefore, ensures that all the switching instances are always at the same point in each switching period, which, in turn, allows all switches to always operate under ZVS. This will be experimentally proved in Section V.

B. Primary-Side Control

The previous section showed that $\hat{v_{pi}}$ could be adjusted by operating the MMC in different duty-cycle patterns. Therefore, according to (11), the power transfer can be regulated using only the primary-side control, which changes $\hat{v_{pi}}$ accordingly. At each operating point, the required $\hat{v_{pi}}$ is calculated using (11), and the corresponding duty-cycle pattern that is needed to achieve this $\hat{v_{pi}}$ is determined using either Table II or (16). Once the duty-cycle pattern is determined, the controller is programmed to operate the SMs in this pattern using the open-loop control shown in Fig. 8. The intention of this article is to propose a new converter topology and a modulation scheme that can be used to regulate the power flow and to maintain ZVS operation. Therefore, the prototype employs an open-loop controller.

C. Capacitor Voltage Balancing

As is required for any MMC, the SM capacitor voltages need to be controlled to be at the same or similar value. This is referred to as capacitor voltage balancing. To further understand how different duty-cycles patterns will affect the charging and discharging of the SM capacitors, an example of the SM capacitor charging/discharging while using duty-cycle pattern #2 is shown in Fig. 9.

The charging and discharging of the capacitor in an SM is proportional to the integral of the SM current. Fig. 9 shows that the SMs with 100% D will see a positive integral of the SM current so that the capacitor will charge during this period. This is indicated in red. On the other hand, the SMs with 50% D will see a negative integral of the SM current, resulting in the discharging of their capacitors, and is indicated in green. Since the average current going through each SM is equal to the dc source current divided by the number of phase legs, in this particular design, the average SM current can be expressed by

$$\bar{I}_{\mathrm{SM}} = I_{\mathrm{DC}} = \frac{P}{2V_{\mathrm{DC}}}. \tag{17}$$

Therefore, during one switching period, the SM capacitor voltage variation will be

$$\Delta V_C = \frac{1}{C_{\mathrm{SM}}} \int_0^{T_{\mathrm{sw}}} i_{\mathrm{SM}}(t)dt = \frac{P}{2V_{\mathrm{DC}} f_{\mathrm{sw}} C_{\mathrm{SM}}}. \tag{18}$$

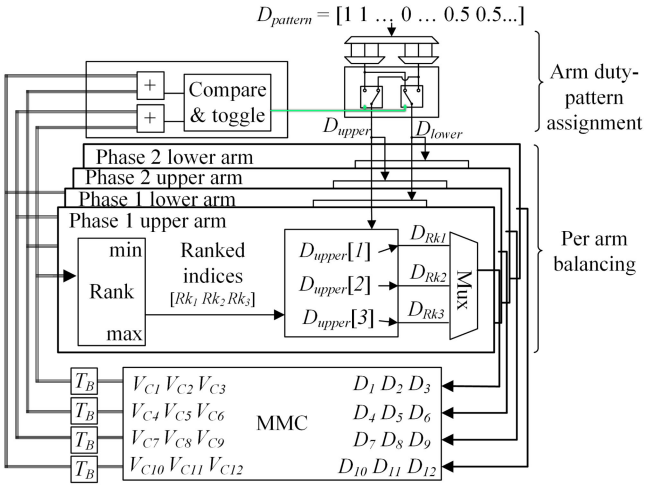

Fig. 10. Capacitor voltage balancing block diagram.

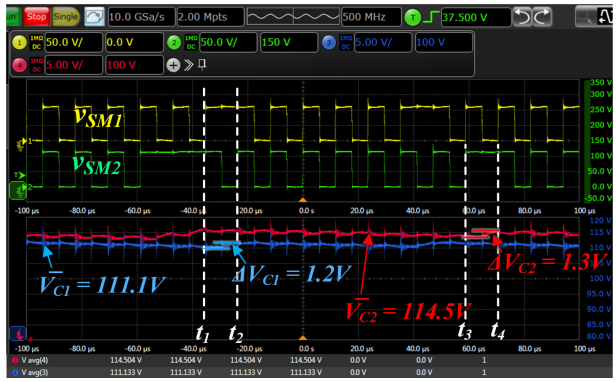

Fig. 11. Experimental results showing capacitor voltage balancing (capacitors in SM1 and SM2 are probed).

As explained previously, the SMs operating at 100% D will eventually be charged to full dc bus voltage, while the rest of the SMs will be discharged to 0 V. Therefore, a capacitor voltage balancing algorithm is employed, and a block diagram of this is shown in Fig. 10.

The balancing algorithm executes at a frequency, f_B, which is lower than or equal to the switching frequency ($f_B \leq f_{\text{sw}}$). Within each T_B ($T_B = 1/f_B$), the voltage across each SM capacitor is sensed by an isolated voltage-sensing circuit, and the ADC values are passed to the microcontroller. These ADC values will be divided into four groups, phase-leg 1 upper arm, phase-leg 1 lower arm, phase-leg 2 upper arm, and phase-leg 2 lower arm, to be processed by the algorithm. The algorithm contains two parts, duty-cycle pattern assignment and per-arm balancing, as depicted in Fig. 10.

In order to assign a duty-cycle pattern to each arm, the main duty-cycle pattern will be divided as equally as possible into two duty-cycle patterns: one for the upper arms and one for the lower arms. The upper and lower arm duty-cycle patterns can be interchanged according to the sum of their SM capacitor voltages. For example, when #2 is selected as the main duty-cycle pattern, the upper and lower arm duty-cycle patterns will initially be [100% 50% 50%] and [50% 50% 50%]. As expected, the upper arm voltages will increase because the 100% D SMs are now in the upper arms. During the next balancing cycle, the algorithm will swap the upper and lower arm duty-cycle patterns, giving the lower arms a chance to charge their SM capacitors.

The second part of the balancing algorithm dictates per-arm balancing. For an example shown in Fig. 10, [100% 50% 50%] are assigned to the phase-leg 1 upper arm. The isolated ADC sensing circuit would sense the capacitor voltage every T_B period, and the values will be ranked from low to high. Within these three SMs, the SM with the lowest voltage level (its ranked index would be "1") would get assigned the 100% duty cycle from the allowable duty-cycle values (in this case, the allowable duty-cycle values are [100% 50% 50%]). The SMs with higher voltages would get assigned to 50%. In Fig. 10(a), at t_0, SM3 capacitor has the lowest voltage. Therefore, it would be assigned 100% D during $t_0 - t_1$ period because the SM with 100% D will see a positive integral of the SM current in one switching cycle, which means that SM3 capacitor will be charging in this period. On the other hand, SM1 and SM2 capacitors have higher voltages. Therefore, they are assigned with 50% D, which means that they will see a negative integral of the SM current. Thus, their capacitors will be discharging. At t_1, SM1–3 capacitors' voltages are sensed again and ranked again; this time, SM2 has the lowest voltage. Thus, it will be assigned with 100% duty cycle, while SM1 and SM3 will be assigned with 50% D. Overall, the resultant waveform for the phase-leg 1 upper arm will remain the same, and SM1-3 capacitor voltages will be balanced.

By using the proposed balancing algorithm, the capacitor voltage variations between all SMs can be maintained as

$$\Delta V_C = \frac{P}{2V_{\text{DC}} f_B C_{\text{SM}}}. \tag{19}$$

In the MMC prototype, the balancing algorithm execution frequency is the same as the switching frequency. This ensures the lowest possible voltage variation in the SM capacitor voltages. Fig. 11 shows an example of the capacitor voltage balancing in the experimental setup. During $t_1 - t_2$, SM1 is at 100% D, which is shown in the yellow trace. As a result, C_1 voltage increases, indicated by the blue trace. During $t_3 - t_4$, SM2 is at 100% D, which is shown in the green trace. As a result, C_2 voltage increases, indicated by the red trace. The capacitor voltage ripples are measured at approximately 1.2–1.3 V, which match closely with (19). The slight difference in their average voltage values is due to the tolerances in the voltage-sensing circuitry.

D. Circulating Current Control

In traditional MMCs, the fundamental frequency of the output current is usually 50 Hz/60 Hz for grid systems or a few hundred hertz for drive systems [20], [21]. Because of the low fundamental frequency components, the ac part of the circulating current in (5) can become very large if v_{diff} is not maintained at a minimum. v_{diff} is typically minimized by ensuring that there is the same number of SMs inserted in any one phase leg at any given time.

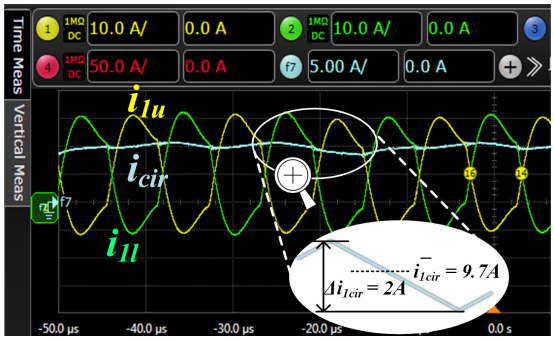

Fig. 12. Experimental circulating current for phase leg 1 when running duty-cycle pattern #2 while transferring 7.7 kW.

As stated above, the fundamental frequency is kept typically at 85 kHz in MMC-based IPT systems used for wireless EV charging. The switching frequency is also kept at 85 kHz to minimize the switching loss. As such, at this frequency, the ac part of the circulating current will naturally be quite small, even when there is no control to minimize v_{diff}. Under the proposed digitized modulation scheme, at any time during one switching period, $v_{ju} + v_{jl}$ will be equal to V_{DC}, except for a few duty-cycle patterns, such as #2, #4, #6, #7, #10, #11, and #12, where v_{diff} will be one SM capacitor voltage V_C (14). In such cases, the amplitude of the ac circulating current can be expressed by

$$\hat{i}_{j\text{cir}_{\text{AC}}} = \frac{1}{L_{ju} + L_{jl} + 2M_{jul}} \frac{1}{2 \times 85\,\text{kHz}} V_C. \tag{20}$$

Given the parameters of the system used in this article, the worst possible circulating current occurs under duty-cycle pattern #2 and is equal to 2 A (i.e., 1/340 μH/2/85 kHz $\times$ 114 V). The experimental results for this scenario are shown in Fig. 12, which verifies the accuracy of the mathematical expression.

V. Experimental Results

A. Experimental Setup and Waveforms

A prototype of the MMC-based primary-side-controlled IPT system shown in Fig. 1 was designed and built. The experimental setup is shown in Fig. 13, and the system parameters are shown in Table III. This design employs DD magnetic couplers on both the primary and secondary sides, which were built according to the SAE J2954 WPT2/Z2 recommended practice [2]. A demonstration video of the prototype system is available in the online supplementary material.

To comply with the SAE J2954 WPT2/Z2 specifications, the prototype is designed to maintain power transfer at 7.7 kW under a vertical (Z) misalignment of 140–210 mm, a longitudinal (X) misalignment of 75 mm, and a lateral (Y) misalignment of 100 mm. The misalignment between the couplers in X, Y, and Z directions is measured between the center of the secondary DD coupler and the center of the stationary primary DD coupler. The misalignment leads to variations in the coupling factor, k. When the center of the secondary coupler is at (75,100,210) with respect to the center of the primary coupler, the lowest k is measured at 0.138, and this position is shown in Fig. 13. When the secondary coupler is perfectly aligned with the primary and

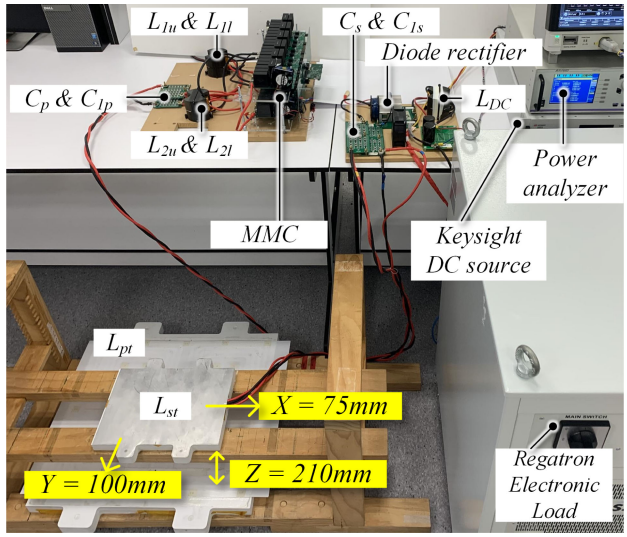

Fig. 13. SAE J2954 WPT2/Z2 compliant experimental setup.

TABLE III
Parameters of the MMC-Based IPT System

Description	Symbol	Value
MMC AC equivalent inductor	L_{pi} & R_{ac}	14.2 μH & 43 mΩ
MMC DC equivalent inductor	L_{armDC} & R_{DC}	340 μH & 16 mΩ
Primary parallel capacitor	C_p & ESR	258 nF & 6 mΩ
Primary series capacitor	C_{1p} & ESR	70.9 nF & 22 mΩ
Primary magnetic coupler	L_{pt} & R_{ac}	64.0 μH & 93 mΩ
Secondary magnetic coupler	L_{st} & R_{ac}	18.3 μH & 24 mΩ
Secondary series capacitor	C_{1s} & ESR	423 nF & 3.6 mΩ
Secondary parallel capacitor	C_s & ESR	348 nF & 4.5 mΩ
Per sub-module capacitor	C_{SM} & ESR	90 μF & 1.4 mΩ
Output DC inductor	L_{DC} & R_{DC}	480 μH & 40 mΩ
Switching frequency	f_{sw}	85 kHz
Coupling factor	k	0.138 - 0.31
DC input voltage	V_{DC}	350 - 450 V
Battery voltage	V_{batt}	280 - 420 V
Power level	P	7.7 kW
200V MOSFET part number	$S_1 - S_{12}$	IPP110N20N3
Diode part number	-	DSEI30-10A

is at its lowest Z position, i.e., (0,0,140), k reaches its highest value, which is 0.31.

In this experimental setup, two Keysight oscilloscopes with high-voltage differential probes and Hall-effect current probes are used to capture critical waveforms. A Zimmer power analyzer is used to measure input power, output power, and dc–dc efficiency. A Keysight power supply is used on the primary side as the dc bus voltage source, and a Regatron electronic load is used on the secondary side as the load battery.

The key waveforms of the MMC-based IPT system operating at the most extreme loading conditions when transferring 7.7-kW rated power are shown in Fig. 14. Fig. 14(a) depicts the operation of the MMC when the secondary magnetic coupler is at the most misaligned position ($X = 75, Y = 100, Z = 210$) and the load battery voltage is the lowest at 280 V. At this operating point, the MMC needs to generate v_{pi} with the highest amplitude

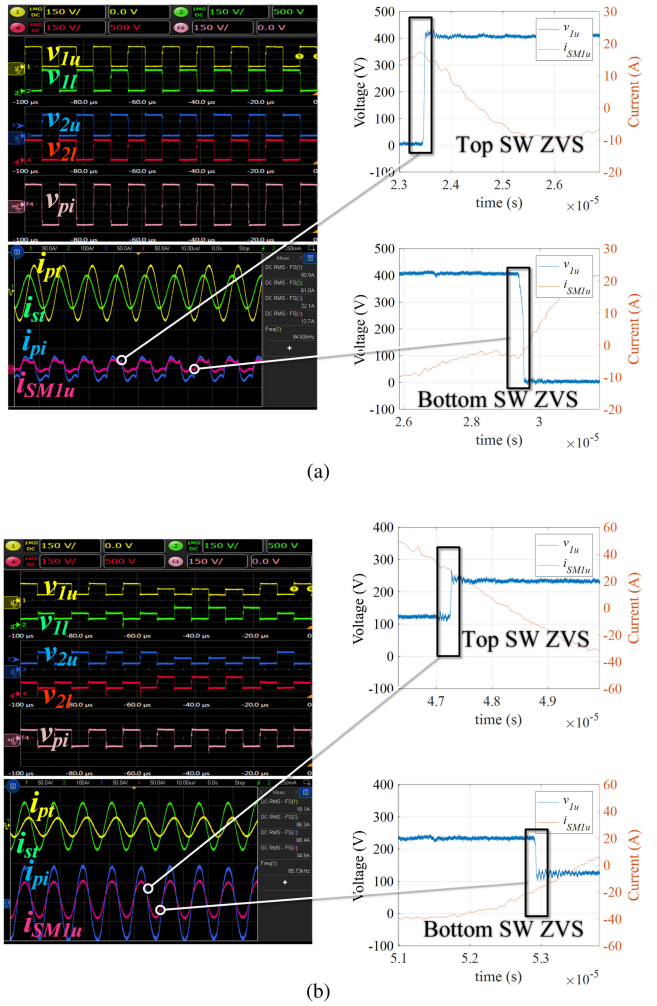

Fig. 14. Waveforms at two extreme cases when transferring 7.7 kW. (a) Most misaligned position $k = 0.138$, 280 VV_{batt}, highest $\hat{v_{pi}}$ required, and duty-cycle pattern #1. (a) Most aligned position $k = 0.31$, 420 VV_{batt}, lowest $\hat{v_{pi}}$ required, and duty-cycle pattern #6.

($\hat{v_{pi}} = 400$ V) to ensure sufficient current in the primary magnetic coupler. Therefore, the duty-cycle pattern applied in this case is #1. Fig. 14(b) depicts the operation of the MMC when the secondary magnetic coupler is perfectly aligned ($X = 0$, $Y = 0$, $Z = 140$) and the load battery voltage is the highest at 420 V. At this operating point, the MMC needs to generate v_{pi} with the lowest amplitude ($\hat{v_{pi}} = 171$ V) to reduce the current in the primary magnetic coupler. Therefore, the duty-cycle pattern applied in this case is #6.

B. ZVS Operations

ZVS is an important feature of the proposed MMC-based IPT system. In these two extreme cases shown in Fig. 14, when the top switch in an SM is turning ON, i_{SM} is negative. This means that during the deadtime for this switching transition, the SM current starts charging and discharging the output capacitance C_{oss} of the bottom switch and the top switch (consisting of drain–source capacitor and gate–drain capacitor where $C_{\text{oss}} = C_{\text{ds}} + C_{\text{gd}}$), respectively. Therefore, only the remaining current

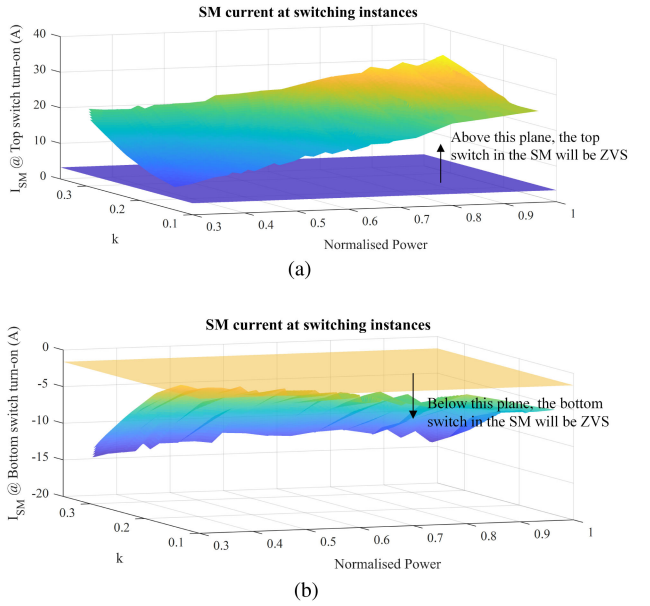

Fig. 15. 3-D plot to show the SM current at the switching instances and to demonstrate the ZVS operating region for (a) top switches and (b) bottom switches.

is passing through the bottom-switch channel, which would only result in a small turn-OFF loss because the majority of the SM current flows through the C_{oss}, in part because the Si MOSFET has a relatively large C_{oss} [24]. The bottom-switch channel current decays to 0 A as the gate–source voltage decreases below the threshold Vth, and now SM current i_{SM} starts to flow through the body diode of the top switch. The turn-ON gate signal is applied to the top switch after its body diode starts conducting, resulting in approximately 0 V across the top-switch drain–source at the instance of turn-ON. Therefore, zero-voltage turn-ON for the top switch is achieved.

Similarly, when the bottom switch is turning ON, i_{SM} is positive, indicating that the SM current flows through the bottom-switch body diode, resulting in a ZVS turn-ON for the bottom switch. Therefore, whether or not a switch is ZVS is determined by the SM current direction and amplitude at the instance of switching. For top-switch ZVS, the SM current needs to be positive (current entering the SM storage capacitor) at the transition as the bottom switch turns OFF and the top switch turns ON. The reciprocal is required for the bottom-switch ZVS, where the SM needs to be negative (current leaving the SM storage capacitor) at the transition as the top switch turns OFF and the bottom switch turns ON. The amplitude of the SM current at the switching instance to guarantee ZVS operation can be expressed as

$$|I_{\text{SM(ZVS)}}| = Q_{\text{oss}} * (a + c)/T_{\text{deadtime}} \tag{21}$$

where the deadtime implemented in the experiment is 200 ns, and the Q_{oss} of the MOSFET used (Infineon 200 V IPP110N20N3) is 160 nC, and the $(a + c)$ represents the number of inserted SMs in a phase leg.

Using (21), a 3-D plot is generated in Fig. 15 to show the operating region over which ZVS operation is guaranteed. The

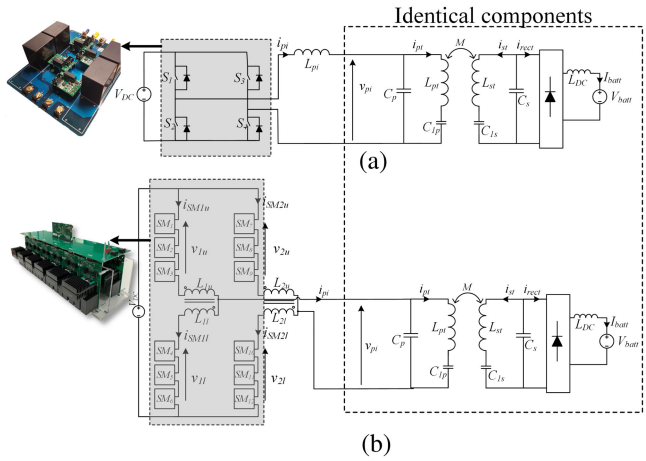

Fig. 16. Circuit diagrams for (a) proposed MMC-based and (b) typical FB-based IPT systems.

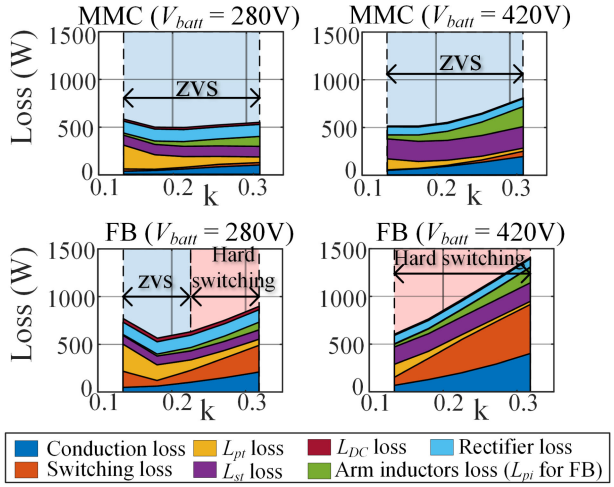

Fig. 17. Loss breakdown of the MMC-based IPT system and the FB-based IPT system.

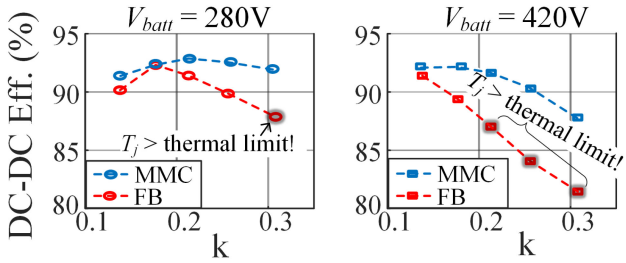

Fig. 18. Experimental dc–dc efficiency of the proposed MMC-based IPT system and a typical FB-based IPT system.

threshold plane for the SM current amplitude needed to guarantee ZVS is also displayed. For the top switch, if the SM current at the switching instance is above the threshold plane, the top switch will achieve ZVS. Similarly, for the bottom switch, if the SM current at the switching instance is below the threshold plane, the bottom switch will achieve ZVS. Although the bottom switches should theoretically have a smaller ZVS operation range due to the per-phase dc current [25], the proposed system has a rather large converter ac current (at least 22 A rms) compared to the per-phase dc current (9.6 A); therefore, the bottom switches still have a wide ZVS operation range. In Fig. 15, we can see that from 3 to 7.7 kW, and from $k = 0.1$ to 0.3, the proposed MMC will have all switches operating under ZVS condition. Because of this, low-cost 200-V Si MOSFETs can be utilized to build the MMC prototype.

C. Loss Breakdown and Comparison to Existing Solutions

To demonstrate the advantages of the proposed MMC-based IPT system, a comparison is made against a typical FB-based IPT system. To make a fair comparison, the MMC and the FB-based IPT systems had the exact same magnetics and compensation networks, and the circuit diagrams are shown in Fig. 16. To fairly consider the capabilities of the FB, the switches used in the FB are state-of-the-art discrete SiC MOSFETs from Wolfspeed, namely, C2M0025120D.

For each coupling position, the losses in each component of the systems are detailed in Fig. 17. For the MMC-based system, as the coupling increases, the MMC should adjust the duty-cycle pattern to lower the output voltage and the primary coupler current to regulate the power; thus, the primary coupler loss reduces. However, as the MMC output voltage decreases, the converter current increases to maintain the same power transfer, resulting in higher losses in the switches and the arm inductors. At 420-V battery voltage, the secondary magnetic coupler loss increases due to a higher volt-amp in the secondary compensation network. The primary coupler loss reduces due to the lower primary coupler volt-amp required, but the MMC losses increase further due to the higher converter current. As both the coupling and the battery voltage vary, there is an optimal operating point, where the sum of the magnetic losses and the converter losses will be minimal. This point is at $k = 0.21$ and $V_{\text{batt}} = 280$ V. Note that since the proposed MMC is a primary-side-controlled system, maximum efficiency tracking cannot be implemented.

For the FB-based system, since the compensation networks and the secondary-side circuits are identical to the MMC-based system, and the key waveforms such as i_{pi}, i_{pt}, and i_{st} are also identical, the losses in these parts are considered to be the same too. The only loss difference is the inverter loss. As the modulation depth increases for the FB system, the duty-cycle control results in the hard switching events for the SiC MOSFETs, which significantly increases the switching loss. This extra switching loss is indicated in the loss breakdown comparison in Fig. 17.

The experimental dc–dc efficiency of the proposed MMC-based IPT system was measured using a Zimmer power analyzer and is shown in blue in Fig. 18. The efficiency stays between 88% and 93% over the entire operating region specified in SAE J2954 WPT2/Z2 standard, which is high considering only primary-side control is utilized, and the semiconductor devices used are low-voltage low-cost Si MOSFETs rather than expensive SiC modules. On the other hand, the FB-based system suffers from higher switching loss; for the high coupling

TABLE IV
COMPARISON BETWEEN THE PROPOSED MMC-BASED IPT SYSTEM WITH SIMILAR EXISTING IPT SYSTEMS

Company / University	Year	Frequency	Air-gap	Power	Efficiency
Korea Advanced Institute of Science [26]	2010	20 kHz	120 mm	15 kW	83%
HEVO Power [27]	2014	85 kHz	∼304.8 mm	1-10 kW	>85%
Oak Ridge National Lab (ORNL) [28]	2015	22 kHz	N/A	6.6kW	85.1%
RWTH Aachen University [11]	2015	35 kHz	100-170 mm	3 kW	92-96%
Southwest Jiaotong University [29]	2017	85 kHz	200 mm	10 kW	94%
University of Auckland (UoA) [30]	2017	85 kHz	100-140 mm	3.3 kW	91.8%
Brusa [31]	2020	N/A	N/A	11 kW	>90%
Witricity [32]	2021	85 kHz	up to 210 mm	11 kW	>90%
This paper	2021	85 kHz	140-210 mm	7.7 kW	90-93%

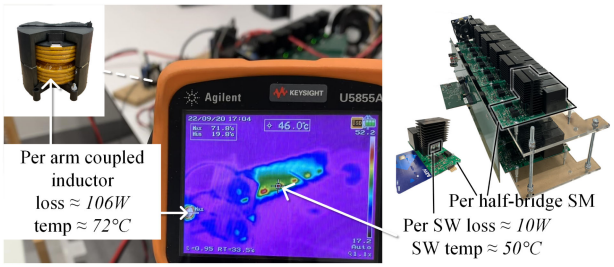

Fig. 19. Component temperatures at the worst operating point, highest inductor, and MOSFET current stress.

positions and high battery voltages, the FB will be incapable of transferring the rated 7.7 kW due to the thermal limit of the devices (each device would experience >100 W loss). Note that the conduction losses and switching losses of the 200-V Si MOSFET IPP110N20N3 used in the MMC and the 1200-V SiC MOSFET C2M0025120D used in the FB are derived from the manufacturer's spice models.

In the extreme case where the coupling is the highest ($k = 0.31$) and the battery voltage is the highest (420 V), the MOSFET loss and arm inductor loss reach a maximum. The thermal performance at this operating point is captured in Fig. 19. It can be seen that both the MOSFET and the inductor are operating well within their thermal safe operating area.

A list of existing IPT systems at a similar power level is compared with the proposed MMC-based IPT system, as shown in Table IV. Key matrices for the IPT system, such as the operating frequency, the air-gap of the system, the power level, and the power transfer efficiency, are listed out. It can be seen that the proposed system provides one of the widest operation ranges while achieving good efficiency. It is also believed to be the only system that utilizes Si MOSFETs. Note that some commercial IPT systems do not reveal all the specifications, some product-related information cannot be obtained, and they are indicated by "N/A."

VI. CONCLUSION

This article proposes an MMC-based IPT system suitable for high-power wireless EV charging applications. The key advantages of the proposed MMC include the integration technique between the arm inductors and the compensation network inductors, and ZVS operation over a large operating range. The operations of the proposed system, including the digitized modulation scheme, are discussed in detail. A primary-side controller is proposed, along with a capacitor voltage balancing algorithm. Several other issues associated with MMCs, such as arm inductor design and circulating current suppression, are also discussed. An SAE J2954 WPT2/Z2 compliant prototype has been built to verify the validity of the proposed system and the digitized modulation scheme. The MMC-based IPT prototype system is able to transfer 7.7-kW rated power with a coupling variation over 220% (from 0.138 to 0.31) and a load battery voltage variation over 150% (from 280 to 420 V) while maintaining 88%–93% efficiency, making it suitable for high-power wireless EV charging applications.

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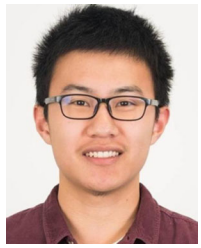

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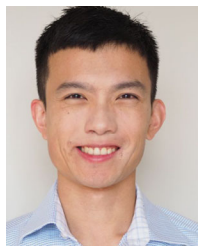

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