An *LLC*-Based Battery Equalizer With Inherent Current Limitation

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***Abstract*—Automatic battery equalizers require no sensing circuits, which reduces their cost, size, and complexity. However, among existing methods, additional resistors or diodes are used in the balancing paths to ensure safe operation, which degrades the conversion efficiency and balancing speed. To overcome this problem, this article proposes an equalizer architecture based on the half-bridge *LLC* converter. The inherent current limitation characteristic of the proposed equalizer improves the balancing speed. High conversion efficiency is achieved due to the soft-switching operations of the switches. The circuit topology and working modes are presented first, then the features of voltage equalization, inherent current limitation, and soft-switching conditions are analyzed in detail. Finally, the proposed equalizer is validated by simulation and experiment.**

***Index Terms*—Automatic equalizers, batteries, current limitation, *LLC* converter, multiwinding transformer.**

I. Introduction

LITHIUM-ION batteries are widely used in high-power applications, such as electric vehicles, energy storage systems, and telecom energy systems [1]. To meet their requirements, large numbers of lithium-ion cells may be connected in series and/or parallel to increase the battery's terminal voltage and capacity [2]. However, series-connected cells may have mismatched voltages, the degree of which may increase with repeated charging and discharging. Voltage mismatch can greatly reduce the battery's capacity and lifetime [3]. In the worst case, battery explosions or/and fires can occur. Therefore, an equalizer is usually used to balance the cell energies and create better battery packs.

In the last few years, many balancing methods have been proposed and can be generally classified into passive and active types [4]. Passive methods utilize resistors and transistors to dissipate the excess energy of high-voltage cells and are low-cost and compact. However, passive methods reduce the available capacity as the excess energy is dissipated. Furthermore, the heat dissipation accelerates the aging of cells.

In active balancing methods, the excess energy of higher voltage cells is transferred to lower voltage cells by an equalizer. The equalizer consists of active switches and passive elements such as capacitors [5]–[19], inductors [9]–[26], or transformers [24]–[34]. Active methods provide more efficient and rapid energy equalization. Usually, sensing circuits are required to obtain cell voltages to estimate the state-of-charge (SOC). However, the usage of a large number of sensing circuits increases the cost, size, and control complexity.

To remove the sensing circuits, automatic equalizers have been developed [6]–[13], [26]–[29]. Baughman *et al.* [6] propose a double-tiered switched-capacitor (SC) equalizer. Capacitors are alternately connected to the adjacent cells and states are switched back and forth between cells at a fixed frequency without consideration of the SOC. No sensing or closed-loop control is needed, and the process is self-limiting. To improve the energy transfer of chain structures, Shang *et al.* design a series of high-efficiency simplified SC equalizers [7], [8]. Due to the star structure of SCs, these equalizers allow more flexible balancing paths between cells. Alternatively, some equalizers use *LC* resonant tanks to balance cells [9]–[11]. These *LC*-based equalizers eliminate inrush current, which is a problem in the traditional SC equalizers. To reduce the number of switches and improve the balancing paths, Shang *et al.* [27] propose a balancing method based on a multiwinding transformer. Energy can be directly delivered from high-voltage cells to low-voltage cells. To further reduce the circuit size, an improved equalizer is proposed in [28], in which adjacent cell pairs share a transformer winding. The number of windings is cut in half in comparison to the number of cells. For the aforementioned automatic equalizers, the energy transfer is driven by voltage differences between cells. The overall balancing speed is slow, especially under small voltage differences (the balancing current is positively related to the voltage difference) [14]. In addition, some system constraints, such as maximum current and maximum voltage, have to be considered to ensure safe operation. The usual method is to add series resistors, which, in turn, increases conduction losses and heat.

In addition to the aforementioned automatic equalizers, another method is to build a current source to balance the cells [12], [13], [26]. Uno and Kukita propose a series of voltage equalizers based on the current source [12], [26]. Only one or two switches are used, which greatly reduces the cost and size. Balancing currents can be limited to desired levels without

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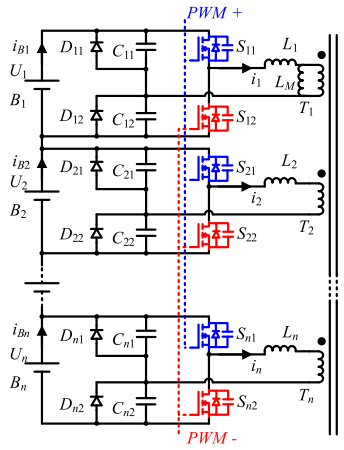

Fig. 1. Circuit structure of the proposed equalizer.

sensors and feedback control. When the voltage difference is low, the equalizers can benefit from using the quasi-constant current mode to maintain a relatively constant balancing current. This characteristic greatly improves the balancing speed under low-voltage-difference conditions. To serve more cells, a modularized architecture is proposed in [13]. Several capacitors are used to transfer energy between modules. In comparison with traditional modular systems, the required switch count can be halved. However, for equalizers based on the current source, many diodes are placed in the balancing paths, increasing conduction losses. Moreover, the ripple current under a voltage-balanced condition is identical to that under a voltage-imbalanced condition, increasing no-load losses.

To overcome these drawbacks, this article develops a voltage equalizer based on the half-bridge *LLC* converter. All MOSFETs are driven by a pair of complementary control signals with a fixed dead time. Energy can be directly transferred from higher voltage cells to lower voltage ones to achieve voltage equalization. Low switching losses are achieved by means of introducing the soft-switching operation. The parallel diodes of resonant capacitors impose restrictions on the maximum power to achieve a balancing current limitation. In this way, extra resistors and diodes are not required in the balancing paths. Therefore, the balancing speed is greatly improved, even with small voltage differences between cells.

The rest of this article is organized as follows. Section II introduces the equalizer and its working modes. Balancing principles, current limitations, soft-switching conditions, and the impacts of parameter mismatch are analyzed in Section III. Section IV presents a design example of an eight-cell equalizer. To grasp the equalization behaviors and validate the proposed circuit, simulation equalization results are performed in Section V. Section VI demonstrates a prototype and its experimental results. A comparison with existing methods is provided in Section VII, and finally, Section VIII concludes this article.

II. Proposed Equalizer and Working Modes

The structure of the proposed equalizer is shown in Fig. 1 and is inspired by the work in [35]. There are n cells in the battery string and each cell requires a winding of the multiwinding transformer, two MOSFETs, and a resonant tank. The resonant tank is built of a resonant inductor (L_i, $i = 1, 2, \ldots,$ and n), two resonant capacitors (C_{ij}, $j = 1,$ and 2), and two clamping diodes (D_{ij}). The frequency of the resonant tank f_r is calculated as

$$f_r = \frac{1}{2\pi\sqrt{2LC}} \tag{1}$$

where L is the inductance of the resonant inductor L_i and C is the capacitance of the resonant capacitors C_{ij}.

A detailed analysis of the proposed equalizer with three cells ($n = 3$) is used as an example to explain the operating principles. For the convenience of analysis, the following definitions and assumptions are given.

1) All windings have the same number of turns. L_M represents the magnetizing inductor. L_i contains the leakage inductance of the transformer winding.
2) The upper MOSFETs, S_{i1}, are driven by PWM+, and the others, S_{i2}, are driven by PWM−. The turn-ON time of the driving signals is controlled to be half of the resonant period.
3) Variables U_i, u_{cij}, u_{sij}, and U_M represent the voltages of cell B_i and resonant capacitor C_{ij}, the voltage across MOSFET S_{ij}, and the magnetizing voltage, respectively. During a switching period, U_i is supposed to be constant. During a dead time period, u_{cij} is supposed to be constant. Variables i_{Bi}, i_i, i_{Dij}, and i_M represent the currents of cell B_i, resonant inductor L_i, clamping diodes D_{ij}, and magnetizing inductor L_M.

There are three working modes: Power transmission mode (Mode 1), discharging limitation mode (Mode 2), and charging limitation mode (Mode 3). They are introduced as follows.

A. Power Transmission Mode (Mode 1)

Fig. 2 shows the operating stages of this mode, and the key waveforms are shown in Fig. 3. In this mode, all resonant capacitor voltages u_{Cij} vary from zero to U_i. No clamping diodes conduct and current limitation will not be triggered. It is assumed that the initial voltages of the battery cells satisfy $U_1 > U_2 > U_3$, and the energy is delivered from B_1 to B_2 and B_3.

Stage 1 $(t_0 - t_1)$*:* Before $t = t_0$, all switches are turned off. The magnetizing current L_M is negative and flows into low-voltage cells B_2 and B_3. The flowing current makes antiparallel diodes of S_{21} and S_{31} conduct, which provides zero-voltage-switching (ZVS) conditions for S_{21} and S_{31}. After $t = t_0$, switch S_{i1} is turned on. For cell B_1, resonance occurs among C_{11}, C_{12}, and L_1. The resonant current i_1 increases sinusoidally from zero. The current i_{B1} is $i_1/2$ due to the half-bridge structure. Since the impedance of paths is symmetrical and similar, the voltage U_M is clamped to $(U_1 + U_2 + U_3)/6$ and the current i_M increases linearly. This stage ends when the current i_1 drops back to zero.

Stage 2 $(t_1 - t_2)$*:* In this stage, all switches are turned off. At $t = t_1$, the current i_1 continues decreasing and the antiparallel diode of S_{11} starts conducting. i_2 and i_3 are positive due to the magnetizing current i_M ($i_M = i_1 + i_2 + i_3$). The resonant inductors L_i and the junction capacitors of S_{2j} and S_{3j} start resonating

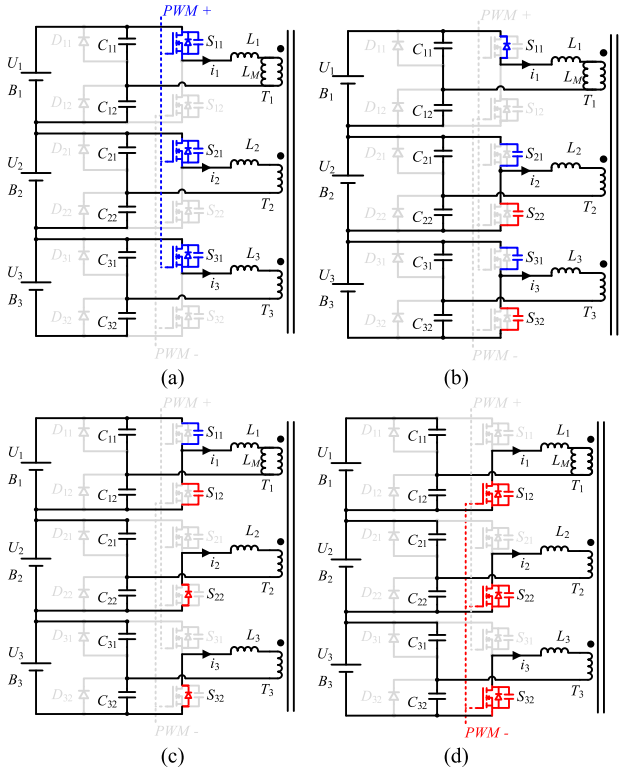

Fig. 2. Operation stages of the proposed equalizer in mode 1. (a) Stage 1(t_0–t_1). (b) Stage 2(t_1–t_2). (c) Stage 3(t_2–t_3). (d) Stage 4(t_3–t_4).

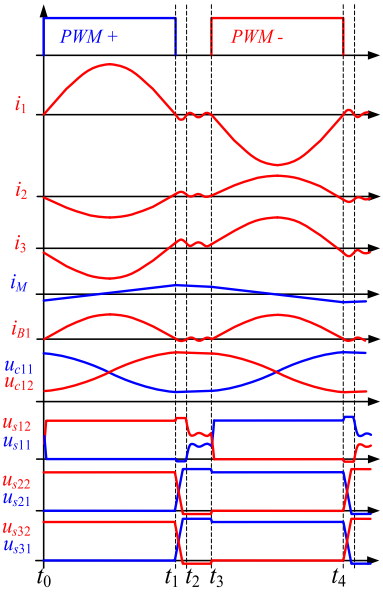

Fig. 3. Key waveforms of the proposed equalizer in mode 1.

until u_{s22} and u_{s32} decrease to zero. Then, the antiparallel diodes of S_{22} and S_{32} start conducting. This stage ends when the current i_1 increases back to zero.

Stage 3 $(t_2 - t_3)$*:* In this stage, all switches are still turned off. Since the energy is delivered from B_1 to B_2 and B_3 in this mode, the capacitor voltages u_{c22} and u_{c32} are lower than u_{c12}. So, the current i_M will continue flowing into B_2 and B_3. At $t = t_2$, the

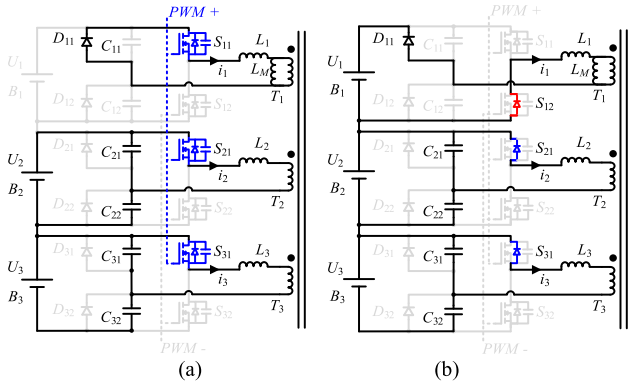

Fig. 4. Operation stages of the proposed equalizer in mode 2. (a) Stage 1(t_1–t_2). (b) Stage 2(t_2–t_3).

antiparallel diode of S_{11} stops conducting. The resonant inductor L_i and the junction capacitor of S_{1j} start resonating until a new steady-state appears. The voltage relation between capacitors can be obtained by shorting inductors and conducting diodes

$$u_{c12} - u_{s12} = \frac{u_{c22} + u_{c32}}{2}. \tag{2}$$

So, the voltage u_{s12} will trend to a bias value $u_{s12} = u_{c12} - (u_{c22} + u_{c32})/2$ with a slight resonance. The magnetizing current continues decreasing but is always positive, which guarantees that the antiparallel diodes of S_{22} and S_{32} keep conducting.

Stage 4 $(t_3 - t_4)$*:* In this stage, switch S_{i2} is turned on, and switch S_{i1} is turned off. Switches S_{22} and S_{32} achieve ZVS because their antiparallel diodes are conducting. Switch S_{12} achieves improved hard switching because the voltage across S_{12} is higher than zero and lower than U_1. The development of this stage is similar to that of Stage 1.

B. Discharging Limitation Mode (Mode 2)

Fig. 4 shows the operating stages of this mode, and the key waveforms are shown in Fig. 5. When the discharging current of high-voltage cells is relatively large, the relevant resonant capacitor voltages will decrease to zero and the clamping diodes start conducting. Then, the high-voltage cells will be bypassed, which means that current limitation will be triggered. Since the stages (t_0–t_1) and (t_3–t_5) are the same as those of (t_0–t_1) and (t_2–t_4) in Mode 1, their analysis is omitted here.

Stage 1 $(t_1 - t_2)$*:* In this stage, switch S_{i1} is turned ON, and switch S_{i2} is turned OFF. Before $t = t_1$, all the resonant tanks work normally and voltage u_{c11} decreases from U_1. At $t = t_1$, voltage u_{c11} decreases to zero and D_{11} starts conducting. The resonant tank stops working and cell B_1 is bypassed. Then, no energy is released from B_1. In addition, the voltages across resonant inductors change and the resonant current i_1 cannot decrease to zero at the end of this stage.

Stage 2 $(t_2 - t_3)$*:* In this stage, all switches are turned OFF. The parallel diode of S_{12} conducts until current i_1 decreases to zero. The currents i_2 and i_3 change from negative to positive and the relevant antiparallel diodes of S_{2j} and S_{3j} will automatically conduct. This stage ends when current i_1 decreases to zero.

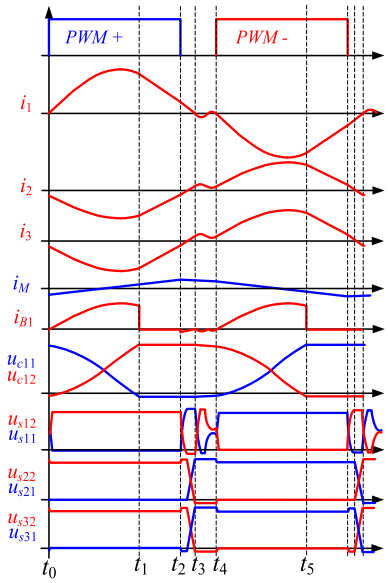

Fig. 5. Key waveforms of the proposed equalizer in mode 2.

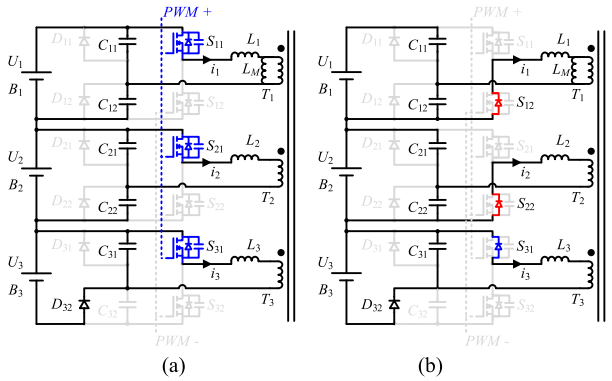

Fig. 6. Operation stages of the proposed equalizer in mode 3. (a) Stage 1(t_1–t_2). (b) Stage 2(t_2–t_3).

C. Charging Limitation Mode (Mode 3)

Fig. 6 shows the operating stages of this mode, and the key waveforms are shown in Fig. 7. When the charging current of low-voltage cells is relatively high, the relevant resonant capacitor voltages will also be clamped and current limitation will be triggered. Energy will continue flowing into low-voltage cells after the clamping diodes conduct. However, current limitation can be achieved by limiting the initial conditions and resonant amplitude. Since the stages (t_0–t_1) and (t_2–t_5) are the same as those of (t_0–t_1) and (t_2–t_5) in Mode 2, their analysis is omitted here.

Stage 1 ($t_1 - t_2$)*:* In this stage, switch S_{i1} is turned ON, and switch S_{i2} is turned OFF. At $t = t_1$, voltage u_{c32} decreases to zero from U_3, and D_{32} starts conducting. The resonant tank stops working and current i_3 flows directly into B_3. The energy transfer will not be stopped immediately in this stage. For later resonance, the initial conditions of the resonant tanks are clamped and the amplitude of resonance will not be increased. Then, current limitation is indirectly realized.

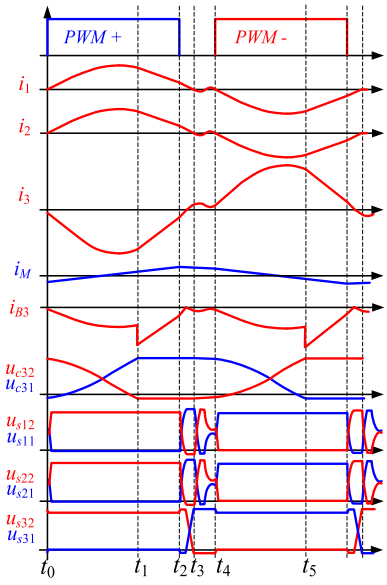

Fig. 7. Key waveforms of the proposed equalizer in mode 3.

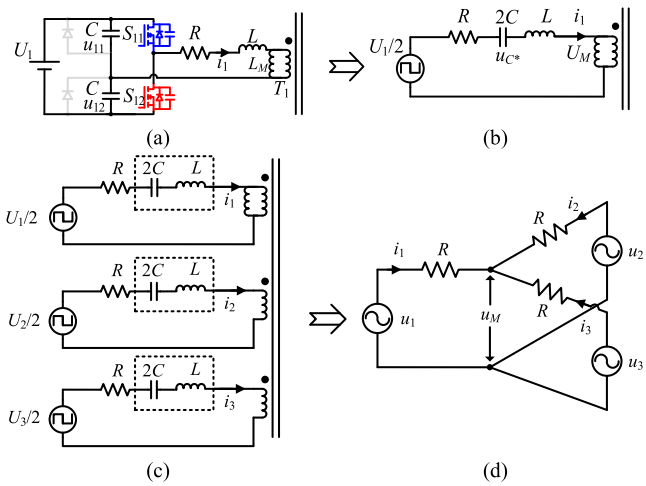

Fig. 8. Equivalent circuits of the proposed equalizer.

III. Feasibility and Characteristic Analysis

In this section, the features of voltage equalization and inherent current limitation, the ZVS condition, and the impact of parameter mismatch are analyzed based on the mathematic model.

A. Voltage Equalization

Before explaining the balancing principles of the proposed equalizer, the equivalent circuit is built first. Without loss of generality, cell B_1 is taken as an example to introduce the derivation process of the equivalent circuit. As shown in Fig. 8(a), when switch S_{11} is turned ON and S_{12} is turned OFF, the following differential equations are obtained:

$$\begin{cases} C\dfrac{du_{11}(t)}{dt} + i_1(t) = C\dfrac{du_{12}(t)}{dt} \\ L\dfrac{di_1(t)}{dt} = u_{11}(t) - U_M - Ri_1(t). \end{cases} \tag{3}$$

The aforementioned equation can be further rewritten as

$$\begin{cases} 2C\dfrac{du_{C*}(t)}{dt} = i_1(t) \\ L\dfrac{di_1(t)}{dt} + U_M + Ri_1(t) + u_{C*}(t) = \dfrac{U_1}{2} \end{cases} \tag{4}$$

where $u_{C*}(t) = (u_{12}(t) - u_{11}(t))/2$ and $U_1 = u_{11}(t) + u_{12}(t)$.

When switch S_{11} is turned OFF and S_{12} is turned ON, by similar calculations, the following differential equations are obtained:

$$\begin{cases} 2C\dfrac{du_{C*}(t)}{dt} = i_1(t) \\ L\dfrac{di_1(t)}{dt} + U_M + Ri_1(t) + u_{C*}(t) = -\dfrac{U_1}{2}. \end{cases} \tag{5}$$

It can be seen that the only difference between (4) and (5) is the polarity of the equivalent output voltage. According to (4) and (5), an equivalent circuit can be obtained, as shown in Fig. 8(b). Then, an equivalent circuit with three cells is built as shown in Fig. 8(c). By adopting the first harmonic approximation (FHA) method [35], the transformer and resonant tanks are removed. The equivalent model is further simplified in Fig. 8(d). According to the FHA method, the ac voltages u_1, u_2, and u_3 can be expressed as

$$\begin{cases} u_1(t) = \dfrac{2}{\pi}U_1 \sin(\omega(t - t_0)) \\ u_2(t) = \dfrac{2}{\pi}U_2 \sin(\omega(t - t_0)) \\ u_3(t) = \dfrac{2}{\pi}U_3 \sin(\omega(t - t_0)) \end{cases} \tag{6}$$

where $\omega = 2\pi f_r$. The voltage of the neutral point is expressed as

$$u_M = \frac{1}{3}(u_1(t) + u_2(t) + u_3(t)). \tag{7}$$

According to Fig. 8(d), currents i_1, i_2, and i_3 are expressed as

$$\begin{cases} i_1(t) = \dfrac{u_1(t) - u_M}{R} = \frac{2}{3\pi R}(2U_1 - U_2 - U_3)\sin(\omega(t - t_0)) \\ i_2(t) = \dfrac{u_2(t) - u_M}{R} = \frac{2}{3\pi R}(2U_2 - U_1 - U_3)\sin(\omega(t - t_0)) \\ i_3(t) = \dfrac{u_3(t) - u_M}{R} = \frac{2}{3\pi R}(2U_3 - U_1 - U_2)\sin(\omega(t - t_0)). \end{cases} \tag{8}$$

From (8), it can be found that the current of the cell with the maximum terminal voltage is positive and that of the cell with the minimum terminal voltage is negative. This indicates that the energy is transferred from the cell with higher voltage to the one with lower voltage. Cells with moderate voltage could absorb energy from high-voltage cells and release energy to low-voltage cells.

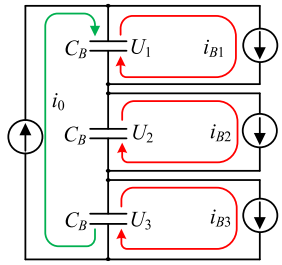

Fig. 9. Simplified model of the battery string.

Next, the average transmission power of the three cells is analyzed. From (6) and (8), the following expressions are obtained:

$$\begin{cases} P_1 = \dfrac{1}{T_S}\int_{t_0}^{t_0+T_r} u_1(t)i_1(t)dt = \dfrac{2T_rU_1(2U_1 - U_2 - U_3)}{3\pi^2 RT_S} \\ P_2 = \dfrac{1}{T_S}\int_{t_0}^{t_0+T_r} u_2(t)i_2(t)dt = \dfrac{2T_rU_2(2U_2 - U_1 - U_3)}{3\pi^2 RT_S} \\ P_3 = \dfrac{1}{T_S}\int_{t_0}^{t_0+T_r} u_3(t)i_3(t)dt = \dfrac{2T_rU_3(2U_3 - U_2 - U_1)}{3\pi^2 RT_S} \end{cases} \tag{9}$$

where T_S is the switching period and T_r is the resonant period. If $P_i > 0$ ($i = 1, 23$), cell B_i releases energy; otherwise, it absorbs energy.

To explain how the cell voltages become balanced, each cell is simplified as an internal resistor R_o and an ideal capacitor C_B [20]. The internal resistor is combined with the equivalent resistance R, and C_B represents the A-H capacity of the cells.

Then, the battery string can be simplified as shown in Fig. 9. Variables i_0 and i_{Bi} represent the load current of the battery string and the balancing current of cells, respectively.

If the voltage differences between the capacitors converge to zero, voltage equalization will be achieved. By using the state-space averaging method, the model of the circuit is formulated as follows:

$$C_B\frac{dU_1}{dt} = i_0 - \frac{P_1}{U_1} = i_0 - \frac{2T_r(2U_1 - U_2 - U_3)}{3T_SR\pi^2} \tag{10a}$$

$$C_B\frac{dU_2}{dt} = i_0 - \frac{P_2}{U_2} = i_0 - \frac{2T_r(2U_2 - U_1 - U_3)}{3T_SR\pi^2} \tag{10b}$$

$$C_B\frac{dU_3}{dt} = i_0 - \frac{P_3}{U_3} = i_0 - \frac{2T_r(2U_3 - U_2 - U_1)}{3T_SR\pi^2}. \tag{10c}$$

Subtracting (10b) from (10a) leads to

$$C_B\frac{d\hat{U}_{12}}{dt} = -k\hat{U}_{12} \tag{11}$$

where $\hat{U}_{12} = U_1 - U_2$ and $k = 2T_r/(T_sR\pi^2)$. As $-k < 0$, $\hat{U}_{12}$ will converge to zero. Therefore, voltage equalization of B_1 and B_2 is achieved. The voltage equalization of B_2 and B_3 and of B_1 and B_3 can be similarly proven.

Note that the equivalent resistance R is a critical parameter in controlling the convergence speed of the voltage difference. A lower equivalent resistance leads to a faster equalization.

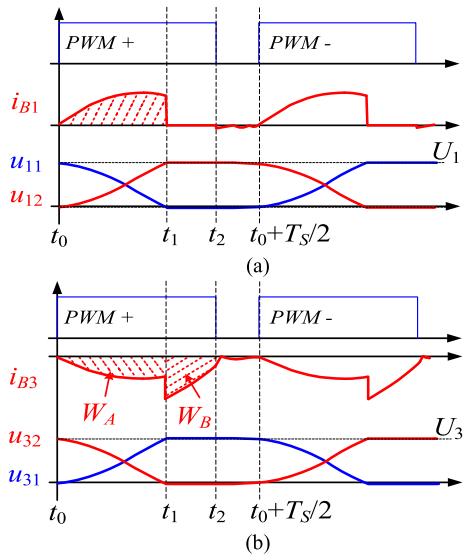

Fig. 10. Key current waveforms in different modes. (a) Discharging limitation mode. (b) Charging limitation mode.

B. Current Limitation Characteristic

Balancing current limitation is achieved during discharging and charging limitation modes.

For high-voltage cells, the discharging current is limited. According to the aforementioned analysis, the maximum current output happens when the voltage of the resonant capacitor is decreased to zero and its parallel diode conducts. According to Figs. 4 and 10(a), when switch S_{11} is turned ON, the following differential equations are obtained:

$$\begin{cases} C\frac{du_{11}(t)}{dt} + i_1(t) = C\frac{du_{12}(t)}{dt} = i_{B1}(t) \\ L\frac{di_1(t)}{dt} = u_{11}(t) - U_M \\ U_1 = u_{11}(t) + u_{12}(t). \end{cases} \tag{12}$$

When the resonant tank begins to work, i_1 increases from zero. At $t = t_0$, $u_{c11}(t_0) = U_1$ and $u_{c12}(t_0) = 0$. So, the initial conditions are

$$\begin{cases} u_{c11}(t)\,|_{t=t_0} = U_1 \\ i_1(t)\,|_{t=t_0} = 0. \end{cases} \tag{13}$$

Then, the solutions of (12) are expressed as

$$\begin{cases} u_{11}(t) = U_M + (U_1 - U_M)\cos(\omega(t-t_0)) \\ i_1(t) = 2C\omega(U_1 - U_M)\sin(\omega(t-t_0)). \end{cases} \tag{14}$$

Before $t = t_1$, the current flowing from B_1 is deduced by

$$i_{B1}(t) = C\frac{du_{11}(t)}{dt} + i_1(t) = -i_{B1}(t) + i_1(t) = \frac{i_1(t)}{2}. \tag{15}$$

This stage ends when the voltage across C_{11} decreases to zero and D_{11} begins to conduct. The current flowing from B_1 becomes zero. Therefore, the duration of this stage (t_0–t_1) can be expressed as

$$\Delta t = t_1 - t_0 = \frac{1}{\omega}\arccos\left(\frac{U_M}{U_1 - U_M}\right). \tag{16}$$

So, the maximum discharging current can be deduced by

$$I_{\max\_\text{disc}} = \frac{P_{\max\_\text{disc}}}{U_1} = \frac{2}{T_S}\int_{t_0}^{t_1} i_{B1}(t)dt = \frac{2CU_1}{T_S}. \tag{17}$$

For low-voltage cells, the charging current is limited. Without loss of generality, cell B_3 is taken as an example for analysis. As shown in Fig. 10(b), the energy flowing into B_3 consists of W_A and W_B during half a switching period. Next, the current $i_3(t)$ will be solved to obtain W_A and W_B.

Before switch S_{31} is turned ON, current i_3 is zero. At $t = t_0$, $u_{c31}(t_0) = 0$ and $u_{c32}(t_0) = U_3$. So, the initial conditions are

$$\begin{cases} u_{c31}(t)\,|_{t=t_0} = 0 \\ i_3(t)\,|_{t=t_0} = 0. \end{cases} \tag{18}$$

According to (12) and (18), the voltage and currents can be expressed as

$$\begin{cases} u_{c31}(t) = U_M - U_M\cos(\omega(t-t_0)) \\ i_3(t) = -2C\omega U_M\sin(\omega(t-t_0)) = 2i_{B3}(t). \end{cases} \tag{19}$$

Therefore, W_A can be expressed as

$$W_A = \int_{t_0}^{t_1} U_3\frac{i_3(t)}{2}dt = -CU_3^2. \tag{20}$$

After $t = t_1$, voltage u_{c32} decreases to zero. D_{32} starts conducting and capacitor C_{31} is in parallel with B_3. From (15) and $u_{c31}(t) = U_3$, current $i_{B3}(t)$ is changed to

$$i_{B3}(t) = C\frac{du_{c31}(t)}{dt} + i_3(t) = i_3(t). \tag{21}$$

Since the voltage across L_3 changes from $(2u_{c31}(t) - u_{c11}(t) - u_{c21}(t))/3$ to $(2U_3 - u_{c11}(t) - u_{c21}(t))/3$, current $i_3(t)$ should be expressed as

$$i_3(t) = i_3(t_1) + \int_{t_1}^{t}\frac{2U_3 - u_{c11}(t) - u_{c21}(t)}{3L} \tag{22}$$

W_B can be expressed as

$$W_B = \int_{t_1}^{t_0+T_S/2} U_3 i_3(t)dt. \tag{23}$$

From (20) and (23), the maximum charging current can be deduced by

$$I_{\max\_c} = \frac{P_{\max\_c}}{U_3} = \frac{2\,|W_A| + 2\,|W_B|}{T_S U_3}. \tag{24}$$

Then, the maximum balancing currents are obtained. It means that the balancing current is indirectly limited by inherent current limitation. In this section, energy transfer during dead time is not considered because the resonant current drops to a low level when the switches are turned OFF. Moreover, the dead time is relatively small and its effect is negligible.

Note that the maximum balancing current mainly depends on the cell voltages and the values of R, C, and L. R affects the voltage difference threshold that triggers current limitation. Thus, R should be set as low as possible to improve the performance of the proposed equalizer. C and L affect the maximum balancing current, with the effect of C being much greater. Thus,

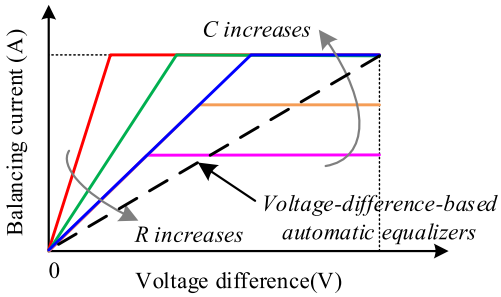

Fig. 11. Ideal relation curves of the balancing current versus voltage difference.

C is a critical parameter in controlling the balancing current. The effects of R and C are shown by the solid lines in Fig. 11, while the black dotted line shows the ideal current curve of the voltage-difference-based automatic equalizers. Whatever the voltage difference, the balancing current of the proposed method is higher than that of the voltage-difference-based automatic equalizers, which means that faster equalization is achieved.

C. ZVS Condition

Before switches are turned ON, the junction capacitors should be discharged by the magnetizing current. However, under a voltage-imbalanced condition, the magnetizing current automatically flows into the low-voltage cells during dead time. So, the switches of the low-voltage cells more easily achieve ZVS. According to the analysis in Section II, the switching voltages of other switches will trend to a bias value that is higher than zero and lower than the cell voltages. This switching mode, called improved hard switching, can provide lower switching losses than hard switching. Under a voltage-balanced condition, the magnetizing current will flow into each cell on average. All switches can achieve ZVS, so all junction capacitors should be discharged or charged by the magnetizing current. Taking a three-cell case as an example, the energy stored in the magnetizing inductor should be higher than that in the junction capacitors, that is

$$\frac{L_M}{2} i_{M\_\text{peak}}^2 \geq 3 C_S U_{\max}^2 \tag{25}$$

where C_s is the junction capacitor of the switches, $U_{\max}$ is the maximum cell voltage, and i_{M_peak} is the peak magnetizing current, which can be expressed as

$$i_{M\_\text{peak}} = \frac{U_{\max}}{8 L_M f_r}. \tag{26}$$

After discharging the junction capacitors, the magnetizing current $i_{M\_\text{peak}}{}^*$ can be rewritten as

$$i_{M\_\text{peak}^*} = \sqrt{i_{M\_\text{peak}}^2 - \frac{6 C_S}{L_M} U_{\max}^2}. \tag{27}$$

The magnetizing current $i_{M\_\text{peak}}{}^*$ starts decreasing after the switches are turned OFF, and the voltage U_M is less than $-U_{\max}/2$. Meanwhile, the magnetizing current should be greater than zero to guarantee the ZVS condition during dead time, that is,

$$i_{M\_\text{peak}^*} - \frac{U_{\max}}{2 L_M} T_{dt} \geq 0 \tag{28}$$

where T_{dt} is the dead time.

The dead time and magnetizing inductance can be obtained by (28). Note that these parameters can be used to design the transformer and driving signals to achieve ZVS of switches.

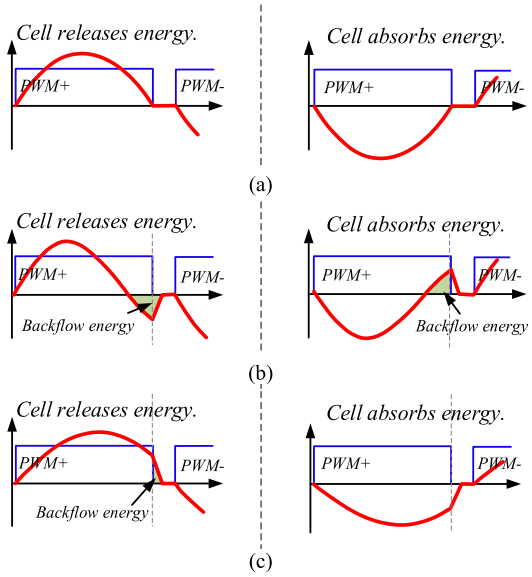

Fig. 12. Resonant current waveforms of three cases with matched or mismatched resonant inductances. (a) Case 1: $L = L_{\text{set}}$ ($f_r = f_{r\_\text{set}}$). (b) Case 2: $L < L_{\text{set}}$ ($f_r > f_{r\_\text{set}}$). (c) Case 3: $L > L_{\text{set}}$ ($f_r < f_{r\_\text{set}}$).

D. Impact of Parameter Mismatch

In the proposed equalizer, resonant tanks are important for energy transfer. The mismatched component parameters (L and C) will adversely affect the equalization performance. In particular, for resonant inductors that rely on the leakage inductors of the multiwinding transformer, it is difficult to guarantee consistency. To clarify the impact of parameter mismatch, cases with matched and mismatched inductances are analyzed as follows.

The resonant current waveforms of three cases with matched or mismatched resonant inductances are shown in Fig. 12. When the resonant parameters match, the resonant current will drop to zero when the switches are turned OFF. When the resonant parameters are lower than the set value, the resonant frequency increases. The resonant current will reverse before the switches are turned OFF and will reset during dead time. Whether the cell releases or absorbs energy, case 2 will result in backflow energy, as shown in Fig. 12(b). When the resonant parameters are higher than the set value, the resonant frequency decreases. The resonant current will not drop to zero before the switches are turned OFF. Similarly, backflow energy will occur. Compared with case 2, the backflow energy in case 3 is much lower, as shown in Fig. 12(c). The backflow energy will affect the initial conditions of the next half-resonant period, which reduces the resonant amplitude. Therefore, the balancing speed of cells with mismatched parameters decreases. In addition, backflow

TABLE I
EXPERIMENTAL PARAMETERS

Parameters		Value
Battery	Model	INR18650-15M
	Nominal capacity	1500 mAh
	Nominal voltage	3.7 V
	Internal resistance	<20m Ω
MOSFET	Model	IPA041N04NGXKSA1
	On-resistance	4.1 mΩ
	Junction capacitor	1200 pF
Transformer	$NP_1 : NP_2 : \ldots : NP_8$	1:1:…:1
	L_M	91 μH
	$R_{winding}$(100kHz)	≈30 mΩ
Inductor	L	≈1.12 μH
Capacitor	C	0.99 μF

energy causes unnecessary conduction losses, which reduces the conversion efficiency.

To sum up, when parameter mismatch is unavoidable, the turn-ON time of switches can be appropriately reduced to ensure that all resonant tanks work in case 1 or case 3.

IV. DESIGN EXAMPLE

In this section, as an example, a 15-W prototype of the proposed equalizer is designed for eight cells. Table I lists the main parameters.

The voltage range considered is 2.8–4.2 V. Due to the symmetry of the topology, the turn ratio of the transformer is 1:1:⋯:1. The switching frequency is set to 95 kHz and the desired duty cycle is 47%.

The maximum discharging current of each cell is limited to 0.8 A. From (17), the constraint of the capacitor C is expressed as

$$C \le \frac{T_S I_{\max\_\text{disc}}}{2U_{\max}} \approx 1\,\mu\text{F}. \tag{29}$$

According to (1), the resonant inductance is calculated by

$$L = \frac{1}{8\pi^2 C f_r^2} \approx 1.24\,\mu\text{H}. \tag{30}$$

The multiwinding transformer is made from a twisted multistrand magnet copper wire. The twisting process provides high spatial symmetry [19]. This coiling method helps to achieve consistent windings. The actual leakage inductance is approximately 0.45 μH. An additional inductance of 0.68 μH is added in each winding. The final value of L is around 1.12 μH. Then, the resonant frequency f_r is calculated to be 106 kHz and the duty cycle is revised to be 44%. The selected turn-ON time of the driving signals is slightly less than half of the resonant period.

Considering the different cell voltages, the balancing current of the lowest voltage cell could reach the maximum value. The feasibility of the calculated capacitor and inductor can be further verified by (24). The verified maximum discharging/charging currents (RMS values) are around 0.8/1.1 A, respectively.

To achieve ZVS, the magnetizing inductor L_M should meet the limitation of (28). Meanwhile, the magnetizing inductor L_M should be set much larger than the resonant inductance to eliminate its impact on the resonant tank. To compromise, L_M is set as 91 μH.

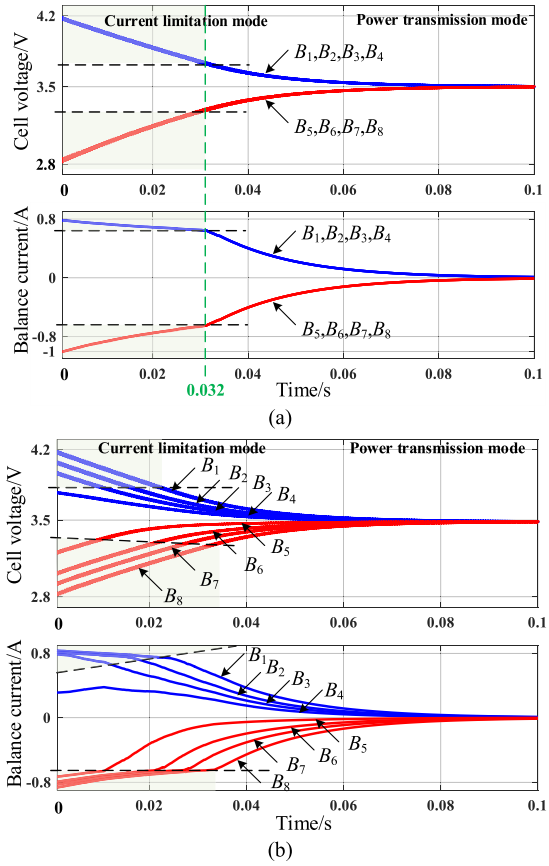

Fig. 13. Simulation equalization results with different initial states.

To improve the balancing speed and efficiency, the equivalent resistance R only uses the parasitic resistance of the circuit, which includes the internal resistors of the cells, the MOSFET turn-ON resistors, winding resistors, etc.

V. SIMULATION-BASED EQUALIZATION

To grasp the equalization behaviors and validate the proposed equalizer, equalization is simulated for eight cells. The values of the circuit parameters are taken from Section IV and Table I. A capacitor with a 20-mΩ internal resistor and a 50-mF ideal capacitance is used as each battery cell.

With different initial cell voltages ($U_1 = U_2 = U_3 = U_4 = 4.2$ V, $U_5 = U_6 = U_7 = U_8 = 2.8$ V), the simulation result and balancing current curve are as shown in Fig. 13(a). Before $t = 0.032$ s, the balancing current can keep a high value, meaning that current limitation is achieved. After $t = 0.032$ s, the balancing current starts to be related linearly to the voltage difference. Similarly, another simulation result is shown in Fig. 13(b). Current limitation is achieved when the cell voltage is significantly different from the average voltage. As the voltage difference decreases, related cells gradually change from the limitation mode to power transmission mode. The simulation results validate the current-limiting characteristics of the proposed equalizer.

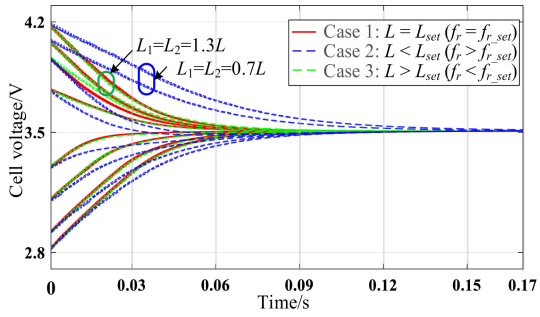

Fig. 14. Equalization results of three cases with matched or mismatched resonant inductances.

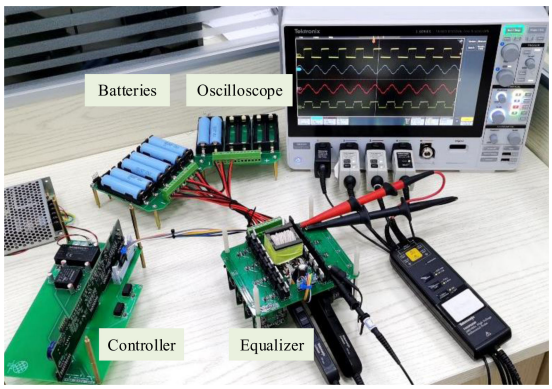

Fig. 15. Experimental prototype for eight battery cells.

To confirm the impact of parameter mismatch, three simulation-based equalization results with matched or mismatched inductances are shown and compared in Fig. 14. The equalization results show that all cell voltages eventually converge, whether the inductances are matched or mismatched. In case 1, all inductances are consistent ($L_i = L$, $i = 1, 2,\ldots,8$) and the resonant frequencies are matched. In case 2, some inductances are set lower than the set value ($L_1 = L_2 = 0.7L$, $L_i = L$, $i = 3,\ldots,8$). As shown by the blue dotted line, the balancing speed of the cells with mismatched parameters is significantly lower than that of the others. In case 3, some inductances are set higher than the set value ($L_1 = L_2 = 1.3L$, $L_i = L$, $i = 3,\ldots,8$). As shown by the green dotted line, the convergence speed of the cell voltages is virtually the same as that in case 1. Hence, the simulation results are consistent with the theoretical analysis. To reduce the impact of parameter mismatch, the turn-ON time of the driving signals should be set to be slightly less than half of the resonant period to ensure that all resonant tanks work in case 1 or 3.

VI. Experimental Results

A. Experimental Waveforms

As shown in Fig. 15, a prototype with eight lithium-ion cells is built to verify the feasibility of the proposed equalizer. The achievement of current limitation mode and soft switching is proven through the experimental waveforms.

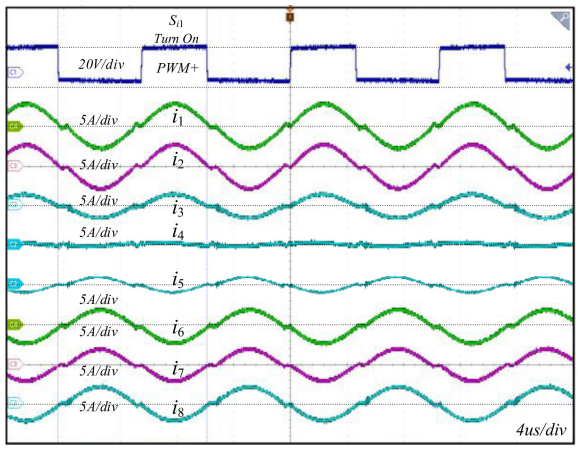

Fig. 16. Resonant current waveforms of the resonant inductors.

Fig. 16 shows the resonant current waveforms of eight resonant tanks. According to the amplitude and direction of the resonant currents, it can be seen that the energy is automatically and directly delivered from high-voltage cells ($U_1 = 3.9$ V, $U_2 = 3.9$ V, $U_3 = 3.6$ V, and $U_4 = 3.4$ V) to low-voltage cells ($U_5 = 3.2$ V, $U_6 = 3.0$ V, $U_7 = 3.0$ V, and $U_8 = 2.9$ V). When the MOSFETs are turned ON/OFF, the currents are close to zero, which decreases switching losses.

The steady-state waveforms of the proposed equalizer are shown in Fig. 17. Fig. 17(a) shows the waveform of the power transmission mode for cell B_1. In this mode, energy is automatically transferred from B_1 to other cells. The balancing current relies entirely on the voltage difference between cells. The voltage of the resonant capacitors is not clamped and the currents of the clamping diodes are zero.

Fig. 17(b) shows the waveform of the discharging limitation mode for cell B_1. In this mode, the current flowing from B_1 reaches the rated value. Before the switches are turned OFF, the voltage of the resonant capacitor C_{11} or C_{12} decreases to zero. Then, clamping diode D_{11} or D_{12} starts conducting and cell B_1 is bypassed. The energy transfer of B_1 is interrupted, which means that current limitation occurs. From the current waveform of i_{B1}, the average balancing current flowing from B_1 is approximately 0.8 A, which agrees well with the design considerations and theoretical analysis.

Fig. 17(c) shows the waveform of the charging limitation mode for cell B_8. In this mode, the current flowing into B_8 reaches the rated value. The voltage of resonant capacitor C_{81} or C_{82} decreases to zero and clamping diode D_{82} or D_{81} starts conducting. After that, the energy continues transferring to B_3 in this resonant period. However, the energy transferred in the later resonant period will stop increasing because of the limited initial conditions and resonant amplitude. Then, charging limitation is indirectly realized. From the current waveform of i_{B8}, the average balancing current flowing into B_8 is approximately 0.9 A.

Fig. 18 shows the switching stress waveforms under different voltage conditions. With different cell voltages ($U_1 = 3.7$ V, $U_2 = 3.5$ V, $U_3 = 3.4$ V, $U_4 = 3.4$ V, $U_5 = 3.3$ V, $U_6 = 3.2$ V,

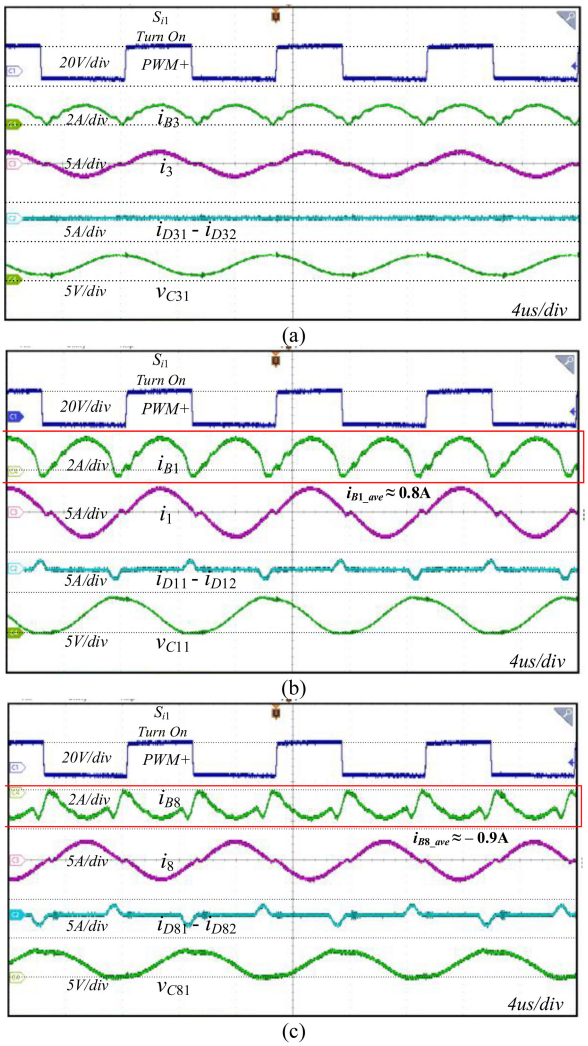

Fig. 17. Steady-state waveforms in different modes. (a) Power transmission mode. (b) Discharging limitation mode. (c) Charging limitation mode.

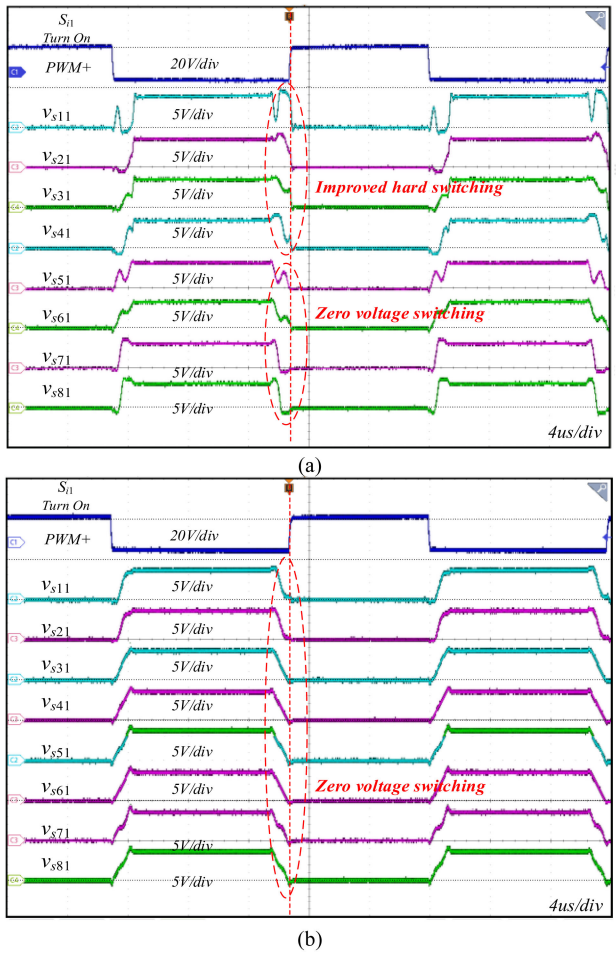

Fig. 18. Switching stress waveforms under different conditions. (a) Voltage-imbalanced condition. (b) Voltage-balanced conditions.

$U_7 = 3$ V, $U_8 = 2.9$ V), the switching stresses of S_{i1} are measured as shown in Fig. 18(a). Cell B_1 is running in the discharging limitation mode, while B_7 and B_8 are in the charging limitation mode. The other cells are running in power transmission mode. Before the MOSFETs are turned ON, the voltages of S_{51}, S_{61}, S_{71}, and S_{81} decrease to zero. Therefore, complete ZVS of these MOSFETs is achieved. The terminal voltages also drop for the other MOSFETs. Improved hard switching is achieved, which is consistent with the previous analysis. At the same cell voltage ($U_i = 3.4$ V), the switching stresses of S_{i1} are measured as shown in Fig. 18(b). All the switches can achieve ZVS, which means that the switching loss under a voltage-balanced condition can be reduced to a very low value.

B. Equalization Results

Fig. 19 shows the equalization results for the eight cells. The initial cell voltages are set to be different to simulate imbalanced conditions. As shown in Fig. 19(a), the maximum voltage difference is reduced from 1 V (2.95–3.95 V) to 25 mV (3.591–3.616 V). As with other voltage-difference-based automatic equalizers, the proposed equalizer can merge all cell voltages to a very small range. The voltage range, which is named the bandgap, can be improved by reducing the resistance of the circuit. This result proves that the proposed equalizer can be applied to the resting battery strings.

As shown in Fig. 19(b), the battery string is charged with a constant current ($i_0 \approx 0.3$A) and the maximum voltage difference is reduced from 1 V (2.93–3.93V) to 30 mV (3.811–3.841V). As shown in Fig. 19(c), the battery string is discharged with a constant load ($i_0 \approx -0.3$A) and the maximum voltage difference is reduced from 0.99 V (2.96–3.95 V) to 38 mV (3.111–3.149 V). It can be observed that the proposed equalizer achieves voltage equalization regardless of the state of the battery string (charging, discharging, or at rest).

Finally, the balancing efficiency is measured through experiments. The efficiency with respect to the discharging power P_{out} is shown in Fig. 20. P_{out} is the total power of the cells that are releasing energy. The efficiency is the ratio of the total power of the cells receiving energy to P_{out}. The power used for the calculation is obtained from the average cell current and voltage. The data are randomly selected from five experiments with different initial conditions. These results show that the proposed equalizer

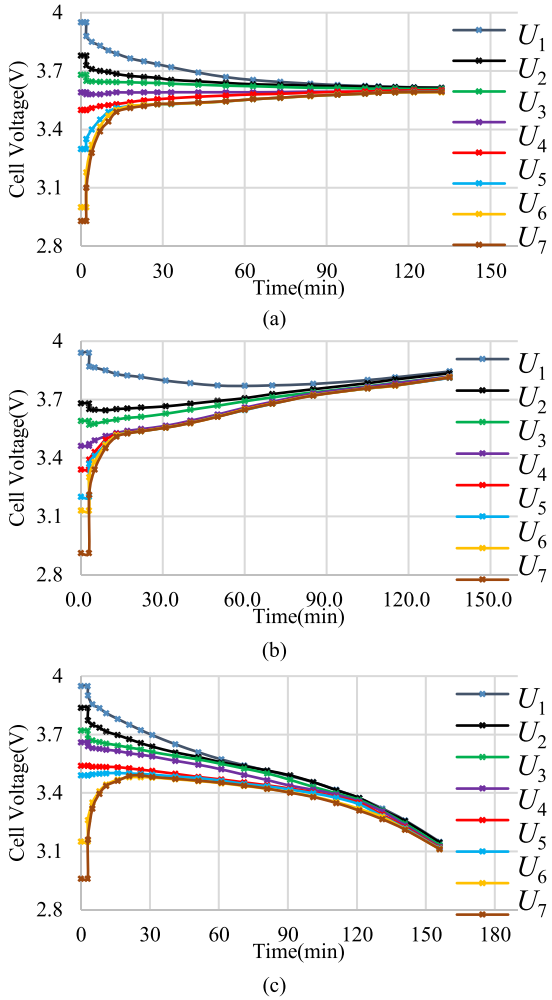

Fig. 19. Equalization results for eight cells in different situations. (a) At rest. (b) Charging. (c) Discharging.

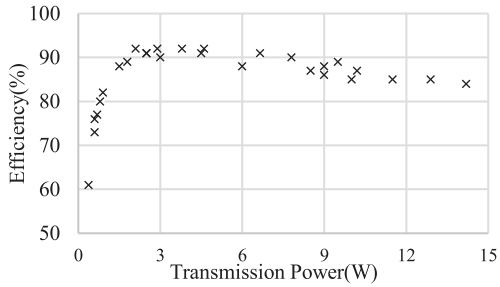

Fig. 20. Measured balancing efficiency with respect to the transmission power P_{out}.

can work with high efficiency under different conditions and achieved the highest efficiency of 92%. In addition, since the conduction loss is the main component of the power loss, the efficiency can be further improved by reducing the parasitic resistance of the circuit.

VII. Comparative Study

To show the features of the proposed equalizer, Table II presents a comparison between different methods in terms of sensor requirements, the balancing criterion, bandgap, balancing mode, soft switching, and number of components. The balancing criterion is evaluated according to the equalizer operating principle. The bandgap reflects the convergence of the final voltage difference. Balancing mode is evaluated according to the balancing paths; i.e., adjacent cell-to-cell (AC2C), cell-to-string (C2S), string-to-cell (S2C), any-cells-to-any-cells (AC2AC), etc. Soft switching is evaluated based on whether ZVS or ZCS is carried out. The cost is calculated in terms of the number and price of components required. The size is indirectly evaluated according to the number of large components, such as active switches and transformers. However, the balancing speed and efficiency cannot be accurately compared because they are dependent on various factors, such as number of cells, initial voltage, rated power, and cell capacity. Hence, they are fuzzified into five fuzzy scales [19], [27], [28]. Balancing speed is evaluated according to the balancing criterion and balancing mode. In general, a balancing criterion based on the current source is better than one based on the voltage difference. In addition, AC2AC is the most ideal mode and can achieve flexible energy transfer. The efficiency is evaluated in accordance with the conduction loss, switching loss, no-load loss, and magnetic loss. Rectifier diodes, additional resistors, hard-switching operations, and transformers will degrade the final scores.

Conventional active balancing methods can achieve energy equalization in a rapid and efficient manner. They can operate at the rated current regardless of the cell voltage. However, large numbers of sensors, bidirectional switches, and passive components are needed to control the balancing current or power, which greatly increases the system cost, size, and complexity.

The automatic equalizers described in [6]–[13] and [26]–[29] remove sensors, achieving smaller size and lower cost. The advantages of pure SC equalizers [6]–[8] lie in their simple structure. However, large inrush currents and slow balancing speeds are suffered. The resonant SC equalizers [9], [10] utilize resonant tanks to eliminate the inrush current. To improve the balancing mode, a parallel resonant SC equalizer [11] is proposed, which improves the balancing speed at the expense of high cost. The equalizers proposed in [27]–[29] use multiwinding transformers and symmetrical structures to achieve an AC2AC balancing mode. In [27] and [28], only one transformer and n switches (in the case of n cells) are used, resulting in low cost and small size. However, the balancing current of the aforementioned equalizers relies solely on the voltage difference between cells. This operating mode means that the voltage difference between cells only decreases to a small range rather than zero. On the other hand, these equalizers cannot operate at the rated current all the time, which limits the balancing speed.

To overcome this drawback, equalizers based on a constant current source are proposed in [12] and [26]. These methods build a quasi-constant current source, and the current flows into the lowest voltage cells. The balancing current is almost constant even when the voltage difference is low and all cells can completely converge to the same voltage. However, a large number of diodes are used to achieve uncontrolled rectification of the cell side. The diodes of the balancing paths increase the conduction loss. Meanwhile, these methods still have a high ripple current under voltage-balanced conditions, which increases the no-load loss.

TABLE II
COMPARISON BETWEEN DIFFERENT EQUALIZERS

Equalizers	Sensors	Balancing criterion	Bandgap	Balancing mode	Soft switching	Count of the components					Cost (n=10)	Size	Speed	Efficiency
						S*	D	T	C	L				
Conventional active methods	Need	Voltage or SOC	0	-	-	-	-	-	-	-	-	Large	5****	5
Double-Tiered SC equalizer [6]	Not need	Voltage difference	≈0	AC2C	×	2*n***	0	0	*n*	0	52***	Medium	2	2
Star-Structured SC equalizer [8]				AC2C	×	2*n*	0	0	*n*-1	0	51.8	Medium	2	2
Resonant SC equalizer [10]				AC2C	✓	2*n*	0	0	*n*-1	*n*-1	53.6	Medium	2	3
Parallel resonant SC equalizer [11]				AC2AC	✓	4*n*	0	0	*n*	*n*	104	Medium	3	4
Forward-flyback equalizer [27]				AC2AC	×	*n*	0	1	0	0	31	Small	3	2
Single-magnetic equalizer [28]				AC2AC	×	*n*	0	1	0	0	31	Small	3	3
Single-Switch equalizer [12]		Constant current source	0	P2C	×	1	*n*	0	*n*+1	*n*+1	11.9	Small	3	2
MSCD equalizer [26]				P2C	×	2	2n	1	2*n*+2	2*n*	29.4	Small	4	2
Proposed equalizer		Current limitation and voltage difference	≈0	AC2AC	✓	2*n*	2n	1	2*n*	*n*	74	Medium	4	4

* S, D, T, C, and L represent switches, diodes, transformers, capacitors, and inductors, respectively.
** *n* is the number of cells in the battery string.
*** Component cost per unit ($):MOSFET (1), gate driver (1.5), transformer (6), inductor (0.2), capacitor (0.2), diode (0.5) [18], [19], [25].
**** Each parameter is fuzzified into five fuzzy scales, where 1, 2, 3, 4, and 5 represent the lowest, low, medium, high, and highest scales, respectively.

Compared with other automatic equalizers, the proposed method has the following improved features.

1) The characteristic of current limitation improves the relationship between the balancing current and voltage difference. The balancing current is high over a wide voltage range. In combination with the AC2AC mode, the balancing speed of the proposed method is greatly improved.
2) All the switches can be turned ON/OFF at a near-zero current. The switches of the low-voltage cells achieve ZVS, while the others can achieve improved hard switching. Therefore, switching losses are reduced. Moreover, no diodes or additional resistors are used in the balancing paths, resulting in low conduction losses. Consequently, the method can theoretically achieve a higher balancing efficiency.
3) Under a voltage-balanced condition, all switches of the proposed equalizer can achieve ZVS and the ripple currents of the balancing paths are near-zero. This means that the no-load loss is very low.

In short, the proposed equalizer is effective, especially in battery strings with many cells and/or with a large voltage difference between cells.

VIII. CONCLUSION

An *LLC*-based equalizer is proposed in this article. Its highlights are inherent current limitations and soft-switching operations. The inherent current limitation characteristic improves the relationship between the balancing current and voltage differences, which increases the balancing speed. Under a voltage-imbalanced condition, the switches of low-voltage cells can achieve ZVS, while others can achieve an improved hard switching. The maximum conversion efficiency can reach 92%. Consequently, rapid balancing speed and high efficiency are achieved. In addition, no sensing circuit is required, which reduces the system complexity, cost, and size. Although a multiwinding transformer is used in the equalizer, the impact of parameter mismatch can be mitigated by designing appropriate driving signals. The theoretical analysis is verified by simulations and experiments. The experimental results demonstrate that rapid and effective voltage equalization is achieved.

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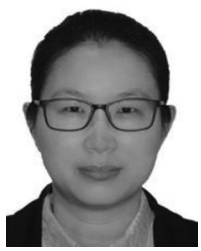

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