An Improved Adaptive Synchronous Rectification Method With the Enhanced Capacity to Eliminate Reverse Current

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***Abstract*—Adaptive synchronous rectification (SR) is a good solution to solve duty cycle loss for *LLC* resonant converter. Usually, whether the synchronous rectifier is turned OFF prematurely or late can be detected by whether the body diode is conducted on or not. However, when the switching frequency is below the resonant frequency, both SR turning-OFF prematurely and late may generate body diode conduction (BDC), which will cause logic errors in the conventional adaptive SR strategy. Then, a large reverse current from load to source will occur, which damages the efficiency. To solve the problem, the time-domain modeling of the SR drain-to-source voltage is established to analyze the mechanism of BDC caused by SR turning-OFF late. Moreover, an improved adaptive SR driving scheme is proposed, which can identify the two different types of BDC and tune SR to be turned OFF exactly. Finally, a 280 W *LLC* prototype is built to verify the established model and the proposed SR method. The prototype proves that both the duty cycle loss and the reverse current are eliminated and efficiency improvement of 0.54% is achieved.**

***Index Terms*—Adaptive synchronous rectification, body diode conduction (BDC), efficiency optimization, high frequency, *LLC* resonant converter, reverse current, ZCS.**

I. Introduction

RECENTLY, the rapid development of information technology has increased the demand for high-power-density power supplies. Thus, the requirement for both the switching frequency and efficiency are becoming higher and higher. As shown in Fig. 1, *LLC* resonant converter with synchronous rectification is an excellent candidate for high-frequency and high-efficiency applications due to the features of achieving zero voltage switching (ZVS) for primary switches and zero current switching (ZCS) for secondary switches [1]–[4]. The performance of synchronous rectification is one of the keys to improving efficiency. However, as the switching frequency increases, the duty cycle loss caused by stray inductance is more and more serious [5]. The conventional $V_{\rm ds}$ sensing based scheme is no longer suitable for high-frequency applications. Research on high-frequency SR strategies is becoming more and more important.

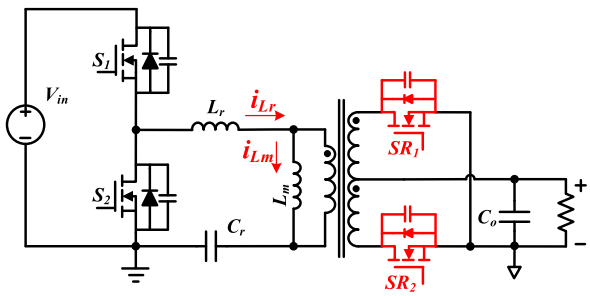

Fig. 1. *LLC* resonant converter with synchronous rectification.

Over the last few years, the synchronous rectification of *LLC* resonant converter can be classified into: current sensing based method [6]–[11]; $V_{\rm ds}$ sensing based method [12]–[19]; primary-side voltage sensing-based method [20], [21]; and the adaptive driving method [5], [22]–[30].

A. Current Sensing-Based Method

Sampling the zero-crossing point of $I_{\rm sr}$ (the current through the synchronous rectifier) to generate the driving signals is the most direct SR solution [6]–[9]. However, sensing the secondary-side current will result in large sampling loss and volume, which is unacceptable. As shown in Fig. 2, the improved method is the indirect current sensing-based scheme. By sensing the resonant inductor current and magnetizing inductor current and comparing between two current signals, the driving signal for SR can be generated. In the literature [10], the resonant current i_{Lr} is sampled by a current transformer, and the magnetizing current is obtained by the integration of the voltage across the transformer. In the literature [11], an external inductor L_p is paralleled with the magnetizing inductance L_m and L_p

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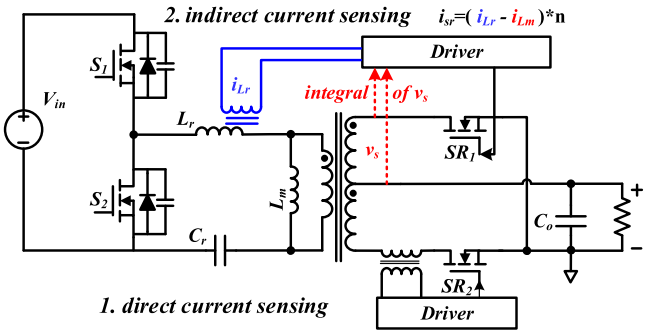


Fig. 2. Current sensing-based SR strategy.

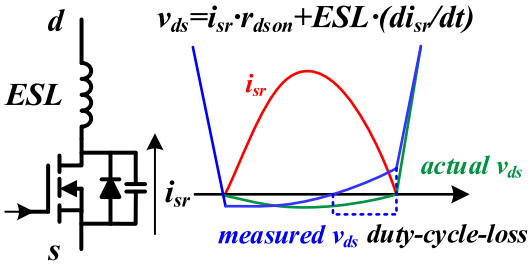


Fig. 3. Stray inductance leads to duty cycle loss.

is much smaller than L_m. Thus, the magnetizing current flows through the external inductor, which can be sampled to drive SR. The drawbacks of these indirect strategies are that the sensing loss is still considerable; the current transformer introduces the additional volume; the isolation performance is degraded; and the parameter deviation will seriously affect the performance of synchronous rectification.

B. VDS Sensing-Based Method

In the literature [12], $v_{\rm ds}$ is sampled and converted to the $v_{\rm gs}$ signal through a well-designed impedance network. The method owns the ultralow-cost but is sensitive to the switching frequency. $V_{\rm ds}$ sensing based method is widely applied in the smart driver integrated circuits(ICs) [13], [14] due to the feature of low sensing loss. While for the high-frequency *LLC* resonant converter, *di/dt* of the secondary-side current increases drastically, which enlarges the duty cycle loss (see Fig. 3) caused by the stray inductance [15]. The compensation scheme [13], [15]–[19] is especially important for high-frequency applications.

In the literature [15], an active RC compensation network is designed to sense the actual voltage on $R_{\rm ds(on)}$. In the literature [16], two switches are simplified in the compensation network with no change of performance. In the literature [13], [17], a well-designed inductor is in series at the source terminal to balance the phase leading generated by the equivalent series inductance(ESL). In the literature [18], the gate drive voltage is deliberately reduced before SR turning-OFF to increase $R_{\rm ds(on)}$. Then, the early turning-OFF problem caused by ESL can be relieved. In the literature [19], the same effect is achieved through different drive timings for parallel MOSFET to relieve duty cycle loss. These methods can compensate for the influence

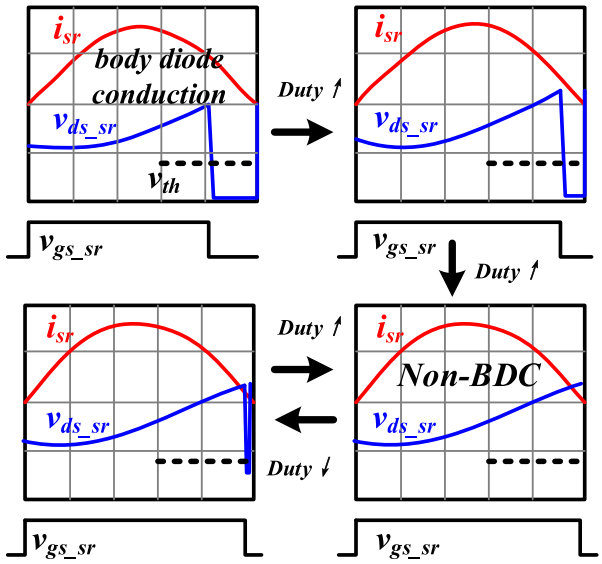


Fig. 4. Adaptive SR strategy proposed in [5].

of stray inductance to reduce duty cycle loss at the cost of circuit complexity. However, the parameters such as the stray inductance and $R_{\rm ds(on)}$ should be extracted and the performance of compensation depends sensitively on the accuracy of these extracted parameters. Moreover, it is difficult to design a compensator suitable for all working conditions, since $R_{ds(on)}$ varies at different temperatures.

C. Primary-Side Voltage Sensing-Based Method

Based on the operation principles of the *LLC* resonant converter, SR only conducts during *P* operation stage. Therefore, the SR driving signal can be generated by the recognition of *P* operation stage [31], which can be obtained by sampling the primary-side voltage. In the literature [20], the polarities of the half-bridge midpoint voltage and the voltage of the transformer are sampled and compared to determine P operation stage. In the literature [21], the sampled resonant capacitor voltage $v_{\rm cr}$ is integrated and compared with both input and output voltage to determine *P* operation stage. The two methods can significantly reduce the sampling loss and immune to the high-frequency noise.

D. Adaptive SR Driving Method

The adaptive SR driving scheme introduces the concept of closed-loop to thoroughly eliminate duty cycle loss. The gate driver signal of the current cycle is tuned by the sensed turning-OFF status of the previous cycle.

The features of the body diode conduction (BDC) are used to identify whether SR is turned OFF prematurely or late. As shown in Fig. 4, a universal adaptive driving scheme is proposed in the literature [5], where the turning-OFF point lags when BDC is detected and leads when BDC does not occur. In the literature [22], the adaptive driving scheme is applied to the low-cost microcontroller through multi-cycle adjustment. In the

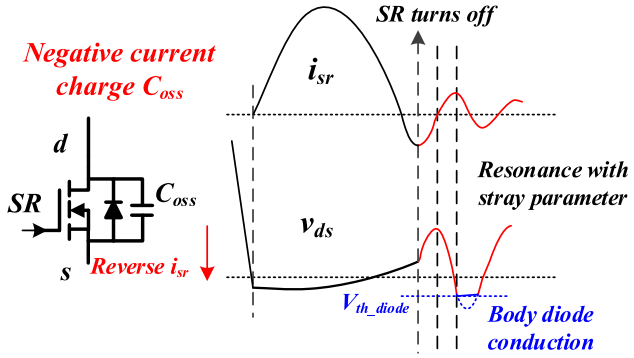


Fig. 5. BDC caused by SR turning-OFF late.

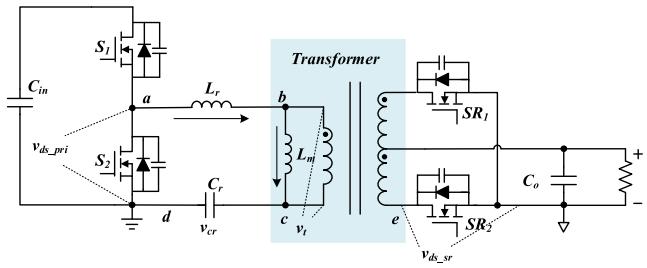


Fig. 6. Definition of the symbol of the related voltage and current.

literature [23], the body diode information is sensed to add delay to eliminate the duty cycle loss. In the literature [25], the regulation of turning-OFF point is achieved by the regulation of the turning-OFF voltage threshold and multilevel thresholds are set to ensure fast and accurate regulation. In the literature [26], an analytic-adaptive SR strategy is proposed for improving the transient-state performance. The dual verification strategy for SR turning-OFF is proposed in [27] to regulate the proper turning-OFF point of SR.

With the development of these years, adaptive SR strategy has gradually been accepted by the industry. Several IC products [28]–[30] have adopted the concept to solve the duty cycle loss. Meanwhile, with the development of the performance of the low-cost microcontrollers, it will become more and more popular to use adaptive SR strategies to solve the high-frequency SR problems.

The similarity of these adaptive schemes is that sensing BDC to identify the turning-OFF information of the current cycle and BDC represents that SR turns OFF prematurely. As shown in Fig. 5, when the SR turns OFF late, the reverse current will charge the junction capacitance, and the subsequent resonance process will also cause BDC [24]. In other words, both turning-OFF prematurely and late will lead to the conduction of the body diode. If the detected BDC is caused by SR turning-OFF late, the control logic in [5] and [22] will be reversed, causing a large reverse current from the load to the source.

In this article, the issue of BDC caused by turning-OFF late is analyzed quantitatively through the model for $v_{\mathrm{ds\_sr}}$ during the dead-time. Moreover, an improved adaptive SR strategy is proposed to distinguish the two different types of BDC and to take the corresponding measures to regulate the turning-OFF point. The proposed method can solve the problems of the reverse current from load to the source caused by SR turning-OFF late. Meanwhile, the proposed method is fully compatible with the conventional adaptive SR strategy.

This article is structured as follows. The time-domain model between the drain-source voltage $v_{\mathrm{ds\_sr}}$ of SR and the reverse current (i_{Lm}-i_{Lr}) is established in Section II. Then, the generation mechanism and the condition of BDC caused by turning-OFF late are discussed quantitatively. In Section III, the sampling circuits and the control logic of the proposed adaptive SR strategy are described. The sampling circuits are simple and low-loss, while the control logic is compatible with the conventional adaptive SR strategy. A comparison of different SR driving schemes is presented in Section IV. Finally, the experimental results and the conclusion are given in Sections V and VI, respectively.

II. Issue of BDC Caused by SR Turning-OFF Late

In this section, the principle of the BDC after turning OFF late will be analyzed. Since this type of BDC only occurs at the condition of $f_s<f_r$, the other two conditions are not discussed in this section, but will be covered in the following section. For the convenience of the effective presentation, the symbol of the related voltage and current are defined as follows.

1) Resonant current i_{Lr}.
2) Magnetic current i_{lm}.
3) Midpoint voltage of the half bridge $v_{\mathrm{ds\_pri}}$.
4) Drain-source voltage of the synchronous rectifier $v_{\mathrm{ds\_sr}}$.
5) Voltage across the transformer v_t.
6) Voltage across the resonant capacitor v_{cr}.

As shown in Fig. 6, the positive directions of i_{Lr} and i_{Lm} are from a to b and from b to c, respectively. The positive directions of v_t, v_{cr}, *and* $v_{\mathrm{ds\_pri}}$ are from b to c, from c to d, and from a to d.

Fig. 7 shows the main voltage and current waveform during the dead-time when $f_s<f_r$. There are three stages before the BDC. The equivalent circuits of these stages are shown in Fig. 8.

1) *Stage 1[t_0 - t_1]*: At t_0, the resonant current i_{Lr} equals the magnetic current i_{Lm} and the current through SR_2 decreases to 0. Since SR_2 is still ON, i_{sr} keeps falling to the negative. The current is transferring from the load to the source. During this stage, $v_{\mathrm{ds\_sr}}$ is slightly larger than 0 and v_t is clamped to be $n*V_o$. At t_1, this stage ends when SR_2 is turned OFF.
2) *Stage 2[t_1 - t_2]*: After SR_2 is turned OFF, the reversed i_{sr} charges the junction capacitance of SR_2, causing $v_{\mathrm{ds\_sr}}$ to rise. The amplitude of i_{sr} gradually decreases as $v_{\mathrm{ds\_sr}}$ increases. When $i_{\mathrm{ds\_sr}}$ returns 0, $v_{\mathrm{ds\_sr}}$ reaches the peak value of this stage. At this time, i_{Lr} equals to i_{Lm}. This is a multiresonance process composed of the four energy storage devices L_r, C_r, L_m, and $C_{\mathrm{oss\_sr}}$. Then, $v_{\mathrm{ds\_sr}}$ will continue to decrease and may cause the BDC of SR_2 at the lowest point (shown as the red dashed circle in Fig. 7). As shown in Fig.9, the simplified equivalent circuits of stage

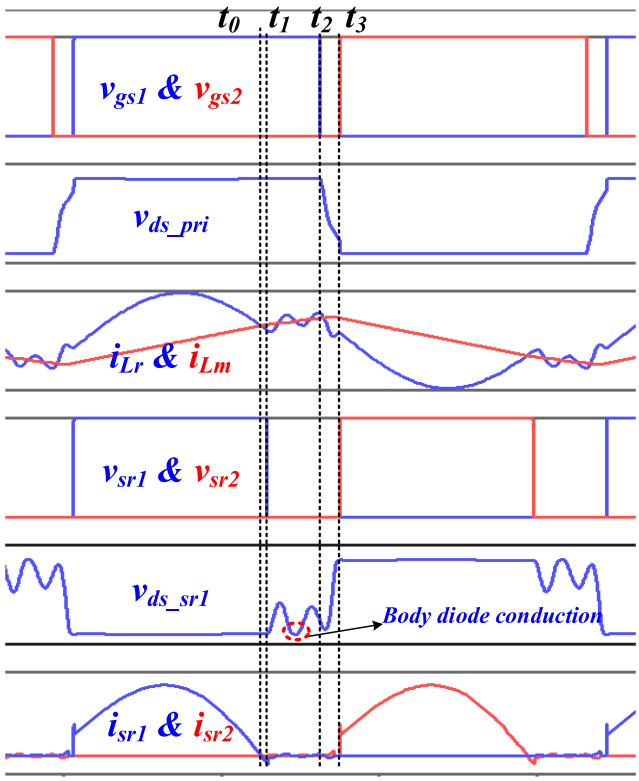


Fig. 7. Main waveforms during the dead-time when f_s<f_r.

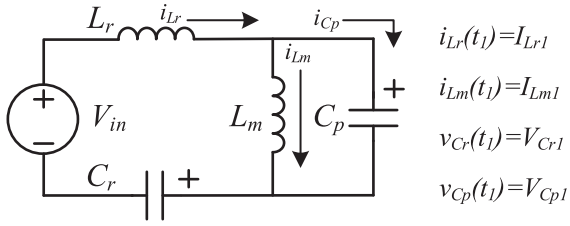


Fig. 8. Simplified equivalent circuits of stage 2.

2 can be obtained by converting the junction capacitance of the synchronous rectifier to the primary side.

Based on Kirchhoff's law, the Time-Domain Equations of this stage can be obtained that

$$\begin{cases} V_{in} = L_r \cdot {di_{\mathrm{Lr}}(t)}/{dt} + v_{\mathrm{cp}}(t) + v_{\mathrm{cr}}(t) \\ i_{\mathrm{Lr}}(t) = C_r \cdot {dv_{\mathrm{cr}}(t)}/{dt} \\ v_{\mathrm{cp}}(t) = L_m \cdot {di_{Lm}(t)}/{dt} \\ i_{\mathrm{Lm}}(t) = i_{\mathrm{Lr}}(t) - i_{\mathrm{cp}}(t) \\ i_{\mathrm{cp}}(t) = C_p \cdot {dv_{\mathrm{cp}}(t)}/{dt} \end{cases} \tag{1}$$

where C_p is the sum of the primary-side parasitic capacitance of the transformer and the equivalent junction capacitance converted from the synchronous rectifier. The voltage of $v_{\mathrm{ds\_sr}}$ can be represented by the voltage across C_p.

$$v_{ds\_sr1}(t) = v_o - \frac{v_{\mathrm{cp}}(t)}{n} \tag{2}$$

Through Laplace transformation, (1) can be transformed into

$$\begin{cases} V_{in}/s = Lr \cdot [s \cdot i_{Lr}(s) - I_{Lr1}] + v_{cp}(s) + v_{cr}(s) \\ i_{Lr}(s) = C_r \cdot [s \cdot v_{cr}(s) - V_{cr1}] \\ v_{cp}(s) = L_m \cdot [s \cdot i_{Lm}(s) - I_{Lm1}] \\ i_{Lm}(s) = i_{Lr}(s) - i_{cp}(s) \\ i_{cp}(s) = C_p \cdot [s \cdot v_{cp}(s) - V_{cp1}] \end{cases} . \tag{3}$$

Then, $v_{\mathrm{cp}}(s)$ can be represented that

$$v_{\mathrm{cp}}(s) = \frac{A \cdot s^3 + B \cdot s^2 + C \cdot s + D}{X \cdot s^4 + Y \cdot s^2 + 1} \tag{4}$$

where *A*, *B*, *C*, and *D* are the coefficients related to the initial values of the voltage and current and can be represented that

$$\begin{aligned} A &= L_m L_r C_r C_p V_{cp1} \\ B &= -L_m L_r C_r \cdot (I_{\mathrm{Lm1}} - I_{Lr1}) \ldots\ldots turn\_off\_current \\ C &= L_m C_r \cdot (V_{in} - V_{cr1}) + L_m C_p V_{cp1} \\ D &= -L_m \cdot I_{Lm1} \end{aligned} \tag{5}$$

where *X* and *Y* are the constant related to the resonant parameters and can be represented that

$$\begin{aligned} X &= L_m L_r C_r C_p \\ Y &= L_r C_r + L_m C_r + L_m C_p. \end{aligned} \tag{6}$$

The time-domain equation of V_{cp} can be obtained by inverse Laplace transformation

$$\begin{aligned} V_{\mathrm{cp}}(t) = {} & \frac{-A \cdot {\omega_{d1}}^2 + C}{Y - 2X \cdot {\omega_{d1}}^2} \cos(\omega_{d1} \cdot t) \\ & + \frac{-B \cdot \omega_{d1} + {D}/{\omega_{d1}}}{Y - 2X \cdot {\omega_{d1}}^2} \sin(\omega_{d1} \cdot t) \\ & + \frac{-A \cdot {\omega_{d2}}^2 + C}{Y - 2X \cdot {\omega_{d2}}^2} \cos(\omega_{d2} \cdot t) \\ & + \frac{-B \cdot \omega_{d2} + {D}/{\omega_{d2}}}{Y - 2X \cdot {\omega_{d2}}^2} \sin(\omega_{d2} \cdot t) \end{aligned} \tag{7}$$

where ω_{d1} and ω_{d2} are the angular frequency resonated by L_m, L_r, C_r, and C_p and can be represented that

$$\begin{aligned} \omega_{d1} &= \sqrt{\frac{L_r C_r + L_m C_p + L_m C_r + \sqrt{(L_r C_r + L_m C_p + L_m C_r)^2 - 4 L_m L_r C_r C_p}}{2 L_m L_r C_r C_p}} \\ \omega_{d2} &= \sqrt{\frac{L_r C_r + L_m C_p + L_m C_r - \sqrt{(L_r C_r + L_m C_p + L_m C_r)^2 - 4 L_m L_r C_r C_p}}{2 L_m L_r C_r C_p}}. \end{aligned} \tag{8}$$

According to the actual parameters of several hundred kHz *LLC* resonant converters, ω_{d1} is a relatively large value, the order of magnitudes is about 10MHz, which represents the oscillation frequency of v_{cp}. ω_{d2} is a relatively small value, the order of magnitudes is about 100 kHz, which represents the envelope frequency of the v_{cp} during the dead-time.

The relationship between v_{cp} and the initial voltage and current value of this stage can be obtained by simplifying (7).

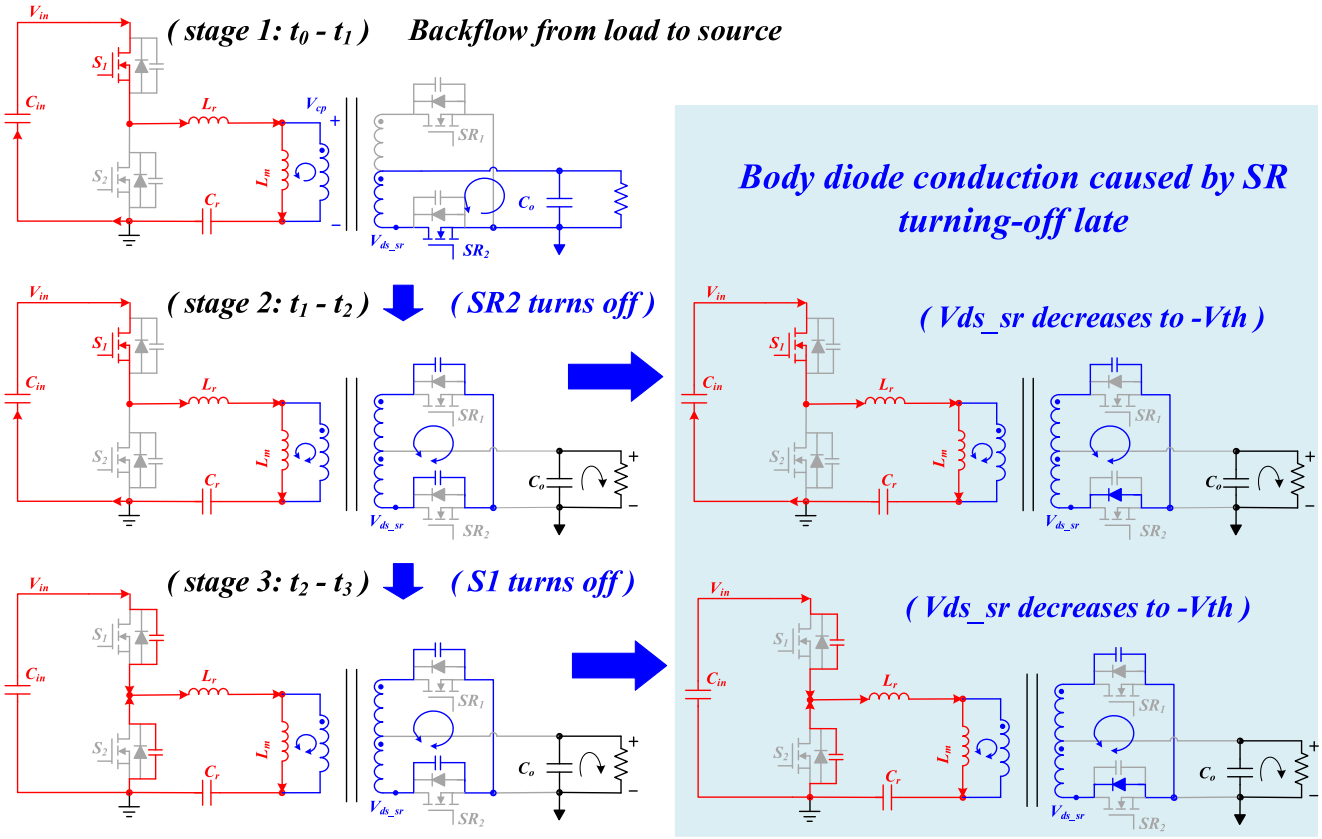


Fig. 9. Equivalent circuits of each stage before BDC.

Eq. (9) shown at the bottom of this page, where k_1, k_2, k_3, k_4, k_5, k_6, k_7, and k_8 are the constant only related to L_m, L_r, C_r, and C_p and can be represented that

$$\begin{cases} k_1 = \frac{-L_m C_r}{\sqrt{Y^2-4X}} \\ k_2 = \frac{L_m C_p \cdot (L_r C_r \omega_{d1}{}^2 - 1)}{\sqrt{Y^2-4X}} \\ k_3 = \frac{L_m}{\sqrt{Y^2-4X}\cdot\omega_{d1}} \\ k_4 = \frac{-L_m \cdot (L_r C_r \omega_{d1}{}^2 - 1)}{\sqrt{Y^2-4X}\cdot\omega_{d1}} \end{cases} \quad \begin{cases} k5 = \frac{L_m C_r}{\sqrt{Y^2-4X}} \\ k6 = \frac{-L_m C_p \cdot (L_r C_r \omega_{d2}{}^2 - 1)}{\sqrt{Y^2-4X}} \\ k7 = \frac{-L_m}{\sqrt{Y^2-4X}\cdot\omega_{d2}} \\ k8 = \frac{L_m \cdot (L_r C_r \omega_{d2}{}^2 - 1)}{\sqrt{Y^2-4X}\cdot\omega_{d2}} \end{cases}. \tag{10}$$

The condition for the BDC of SR_2 Is That $V_{ds\text{·}Sr}$ resonates to below -$V_{th\text{·}diode}$. Equivalently, V_{cp} Should Meet the requirement that

$$v_{cp} \geq n \cdot (V_o + V_{th\_diode}). \tag{11}$$

Fig. 10 shows the waveform of $v_{ds\text{·}sr}$ at different reverse current. The black line represents the condition of no reverse current, the blue line represents little reverse current and the boundary condition of BDC, and the black line represents the condition of large reverse current and BDC. It can be deduced from Fig. 10 that

a) Since ω_{d2} is much smaller than ω_{d1}, the influence of ω_{d2} component on $v_{ds\text{·}sr}$ is much smaller than the ω_{d1} component within one or two oscillation periods.
b) The ω_{d2} component makes $v_{ds\text{·}sr}$ gradually increase. If the first valley value of $v_{ds\text{·}sr}$ cannot satisfy the condition of BDC, the body diode will not be conducted.
c) Increasing the reverse current (i_{Lm}-i_{Lr}) will enlarge the magnitude of $v_{ds\text{·}sr}$. If the reverse current is large enough, the effect of ω_{d2} component on increasing $v_{ds\text{·}sr}$ can be balanced, and then the first valley value of $v_{ds\text{·}sr}$ may satisfy the condition of BDC (red line).
d) This type of BDC cannot be generated from SR turning-OFF early or exactly. Therefore, the two types of BDC are mutually exclusive, which is one of the bases for the proposed SR control strategy.

3) Stage 3[t_2 - t_3]: If S_1 is turned OFF before $v_{ds\text{·}sr}$ reaches the valley value, stage 3 will occur. Stage 3 is a special case, which usually occurs when the switching frequency is slightly smaller than the resonant frequency. Under this circumstance, there is not enough time for $v_{ds\text{·}sr}$ to

$$V_{cp}(t) = \left\{ \begin{array}{l} ((V_{in} - V_{cr1}) \cdot k_1 + V_{cp1} \cdot k_2) \cdot \cos(\omega_{d1} \cdot t) \\ +(I_{Lr1} \cdot k_3 + (I_{Lm1} - I_{Lr1}) \cdot k_4) \cdot \sin(\omega_{d1} \cdot t) \\ +((V_{in} - V_{cr1}) \cdot k_5 + V_{cp1} \cdot k_6) \cdot \cos(\omega_{d2} \cdot t) \\ +(I_{Lr1} \cdot k_7 + (I_{Lm1} - I_{Lr1}) \cdot k_8) \cdot \sin(\omega_{d2} \cdot t) \end{array} \right\} \begin{array}{l} \text{highfrequency} \\ \\ \text{lowfrequency} \end{array} \tag{9}$$

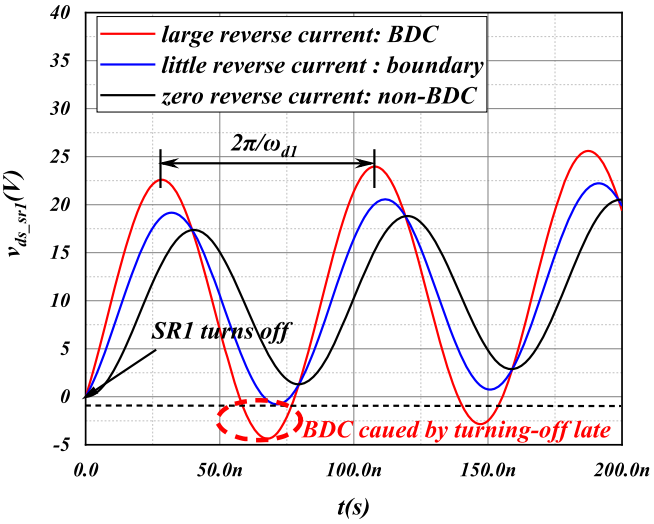


Fig. 10. $V_{\mathrm{ds\_sr}}$ waveform versus different reverse currents (i_{Lm}-i_{Lr}).

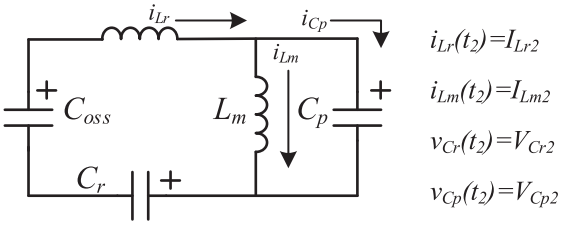


Fig. 11. Equivalent circuit of stage 3.

complete one oscillation cycle, and the primary-side S_1 is turned OFF.

When S_1 is turned OFF, $V_{\mathrm{ds\_pri}}$ drops rapidly, and the equivalent circuit of this stage is shown in Fig. 11. Based on Kirchhoff's law, the time-domain equations of stage 3 can be obtained that

$$\begin{cases} v_{\mathrm{coss}}(t) = L_r \cdot \frac{di_{Lr}(t)}{dt} + v_{\mathrm{cp}}(t) + v_{\mathrm{cr}}(t) \\ i_{Lr}(t) = C_r \cdot \frac{dv_{\mathrm{cr}}(t)}{dt} = -C_{\mathrm{oss}} \cdot \frac{dv_{\mathrm{coss}}(t)}{dt} \\ v_{\mathrm{cp}}(t) = L_m \cdot \frac{di_{Lm}(t)}{dt} \\ i_{Lm}(t) = i_{Lr}(t) - i_{\mathrm{cp}}(t) \\ i_{\mathrm{cp}}(t) = C_p \cdot \frac{dv_{\mathrm{cp}}(t)}{dt} \end{cases} . \quad (12)$$

The differences between (12) and (1) are that V_{in} is replaced with $V_{\mathrm{coss}}(t)$. Similar to the derivation process of stage 2, the time-domain equation of $V_{\mathrm{cp}}(t)$ for stage 3 can be obtained that (13) shown at the bottom of this page, where ω_{d3} and ω_{d4} are the angular frequency resonated by L_m, L_r, C_r, C_{oss}, and C_p and can be represented that (14) shown at the bottom of this page.

The differences between (14) and (8) are that C_r is replaced with C_{oss}'. Based on the numeral calculation, both ω_{d3} and ω_{d4} are the relatively large values when compared with the switching frequency and will change the value of $v_{\mathrm{ds\_sr}}$ rapidly during stage 3.

Where k_9, k_{10}, k_{11}, k_{12}, k_{13}, k_{14}, k_{15}, and k_{16} are the constant that is similar to (10) (the only difference is that C_r is replaced with C_{oss}') and can be represented that

$$\begin{cases} k_9 = \frac{-L_m C_{oss}'}{\sqrt{Y'^2 - 4X'}} \\ k_{10} = \frac{L_m C_p \cdot (L_r C_{oss}' \omega_{d3}^2 - 1)}{\sqrt{Y'^2 - 4X'}} \\ k_{11} = \frac{L_m}{\sqrt{Y'^2 - 4X'} \cdot \omega_{d3}} \\ k_{12} = \frac{-L_m \cdot (L_r C_{oss}' \omega_{d3}^2 - 1)}{\sqrt{Y'^2 - 4X'} \cdot \omega_{d3}} \end{cases} \quad \begin{cases} k_{13} = \frac{L_m C_{oss}'}{\sqrt{Y'^2 - 4X'}} \\ k_{14} = \frac{-L_m C_p \cdot (L_r C_r \omega_{d4}^2 - 1)}{\sqrt{Y'^2 - 4X'}} \\ k_{15} = \frac{-L_m}{\sqrt{Y'^2 - 4X'} \cdot \omega_{d4}} \\ k_{16} = \frac{L_m \cdot (L_r C_{oss}' \omega_{d4}^2 - 1)}{\sqrt{Y'^2 - 4X'} \cdot \omega_{d4}} \end{cases} .$$

$$X' = L_m L_r C_{oss}' C_p$$

$$Y' = L_r C_{oss}' + L_m C_{oss}' + L_m C_p \quad (15)$$

Fig. 12 shows the comparison of $v_{\mathrm{ds\_sr}}$ between stages 2 and 3. The waveforms of the different $v_{\mathrm{ds\_sr}}$ separate when S_1 is turned OFF. The effect of stage 3 is to enlarge the resonant frequency of $v_{\mathrm{ds\_sr}}$.

Based on the established model and the numerical calculation verification, if S_1 turns OFF during the fall of $v_{\mathrm{ds\_sr}}$, the possibility of BDC will be strengthened [see Fig. 12(a)]; if S_1 turns OFF during the rise of $v_{\mathrm{ds\_sr}}$, the trend of BDC will be reduced [see Fig. 12(b)]. In any case, the later the SR is turned OFF, the larger the reverse current and the more possible reverse BDC will occur.

Based on the analysis above, one of the necessary conditions for reverse BDC is $f_s < f_r$, because sufficient time is required to make $v_{\mathrm{ds\_sr}}$ drop below $-V_{\mathrm{th\_diode}}$ after SR turning-OFF. Another necessary condition is that SR is turned OFF late and reverse current (i_{Lm}-i_{Lr}) should have sufficient value. As shown in Fig. 13, the status of *LLC* with SR can be divided into the following four situations.

$$V_{\mathrm{cp}}(t) = \left\{ \begin{array}{l} ((V_{\mathrm{in}} - V_{\mathrm{cr2}}) \cdot k_9 + V_{\mathrm{cp2}} \cdot k_{10}) \cdot \cos(\omega_{d3} \cdot t) \\ +(I_{Lr2} \cdot k_{11} + (I_{Lm2} - I_{Lr2}) \cdot k_{12}) \cdot \sin(\omega_{d3} \cdot t) \\ +((V_{\mathrm{in}} - V_{\mathrm{cr2}}) \cdot k_{13} + V_{\mathrm{cp2}} \cdot k_{14}) \cdot \cos(\omega_{d4} \cdot t) \\ +(I_{Lr2} \cdot k_{15} + (I_{Lm2} - I_{Lr2}) \cdot k_{16}) \cdot \sin(\omega_{d4} \cdot t) \end{array} \right\} \begin{array}{l} \text{highfrequency} \\ \\ \text{lowfrequency} \end{array} \quad (13)$$

$$C_{\mathrm{oss}}' = \frac{C_{\mathrm{oss}} \cdot C_r}{C_{\mathrm{oss}} + C_r} \approx C_{\mathrm{oss}}$$

$$\omega_{d3} = \sqrt{\frac{L_r C_{\mathrm{oss}}' + L_m C_p + L_m C_{\mathrm{oss}}' + \sqrt{(L_r C_{\mathrm{oss}}' + L_m C_p + L_m C_{\mathrm{oss}}')^2 - 4 L_m L_r C_{\mathrm{oss}}' C_p}}{2 L_m L_r C_{\mathrm{oss}}' C_p}} \quad (14)$$

$$\omega_{d4} = \sqrt{\frac{L_r C_{\mathrm{oss}}' + L_m C_p + L_m C_{\mathrm{oss}}' - \sqrt{(L_r C_{\mathrm{oss}}' + L_m C_p + L_m C_{\mathrm{oss}}')^2 - 4 L_m L_r C_{\mathrm{oss}}' C_p}}{2 L_m L_r C_{\mathrm{oss}}' C_p}}$$

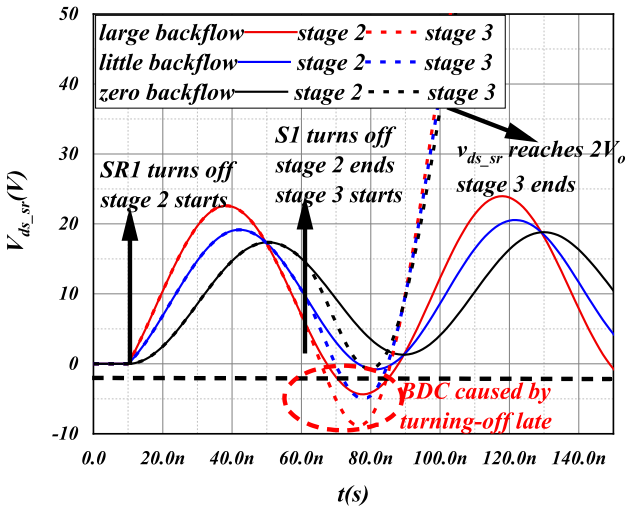


Fig. 12. Effect of stage 3 (a) strengthening and (b) weakening the trend of BDC.

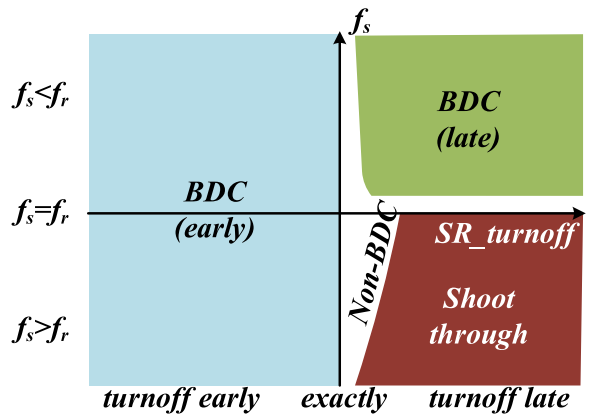


Fig. 13. Status of *LLC* with SR.

1) *BDC*(*Early*): As long as SR is turned OFF early, BDC will occur (blue area).
2) *BDC*(*Late*): When f_s<f_r and SR turns OFF late, reverse BDC may occur (green area).

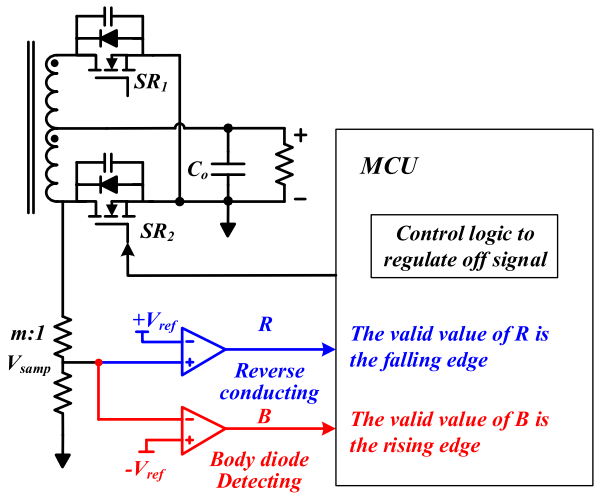


Fig. 14. Sampling circuits of the proposed adaptive SR driving scheme.

3) *Shoot Through*: When $f_s \geq f_r$ and SR turning-OFF is turned too late, shoot through will occur, which must be prohibited (red area).
4) *Non-BDC*: In the remaining area, BDC cannot be detected. At this time, SR may be turned OFF exactly or slightly later. This interval owns enough fault tolerance. If *LLC* works in this area, both high efficiency and safety can be guaranteed.

To improve the robustness of the conventional adaptive SR strategy, it is necessary to determine whether BDC is caused by turning-OFF early or late. In Section III, the improved adaptive SR strategy is proposed, which can determine the types of BDC and perform the corresponding strategy.

III. Proposed Adaptive Synchronous Rectification Driving Strategy

To identify whether the sampled BDC is caused by turning-OFF early or late, an additional comparator is required. Fig. 14 shows the sampling circuit of the proposed adaptive SR driving scheme. The specification of the comparator is LT1715, which contains two comparators inside. The input voltage range of LT1715 is from −5 V to +5 V. Therefore, the sampling signal should be scaled down to adapt to the input voltage range. The negative reference voltage $-V_{\rm ref}$ is set to be higher than $-V_{\rm diode}/10$, while $+V_{\rm ref}$ is set to be slightly greater than 0V. The signal *B* represents BDC and the rising edge is the valid signal. Meanwhile, the signal *R* represents the possibility of BDC caused by SR turning-OFF late, and the falling edge is the valid signal.

One of the comparators is used to detect BDC. Signal *B* rises when the sampled drain-source voltage $V_{\rm samp}$ is lower than $-V_{\rm ref}$, which indicates that the body diode is conducted on. Signal *B* can be applied to regulate both the turn-ON point and the turning-OFF point. As shown in Fig. 15, $-V_{\rm ref}$ should be smaller than the valley value of $v_{\rm ds}$ during the conduction and be larger than the threshold voltage of the body diode. Therefore, $-V_{\rm ref}$ meets the

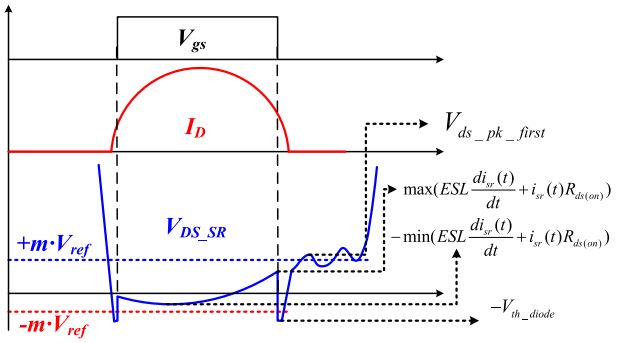


Fig. 15. Range of the reference voltage.

requirement that

$$-V_{\text{th\_diode}} \le m\cdot(-V_{\text{ref}}) \le -\min(\text{ESL}\times\frac{di_{\text{sr}}(t)}{dt}+i_{\text{sr}}(t)\cdot R_{\text{ds(on)}}). \quad (16)$$

Another comparator is used to distinguish the type of BDC. Signal R is available when V_{samp} decreases from higher than $+V_{\text{ref}}$ to lower than $+V_{\text{ref}}$, which indicates the possibility to generate BDC caused by SR turning-OFF late. Moreover, the signal R can also be used to reset the driving signal for another synchronous rectifier. As shown in Fig. 15, $+V_{\text{ref}}$ should be larger than the peak value of v_{ds} during the conduction and be smaller than the first peak value during the resonant period. Therefore, $+V_{\text{ref}}$ meets the requirement that

$$\max(L\frac{di_{\text{sr}}(t)}{dt}+i_{\text{sr}}(t)\cdot R_{\text{ds(on)}}) \le m\cdot(+V_{ref}) \le V_{\text{ds\_pk\_first}}$$

$$V_{\text{ds\_pk\_first}} \approx \frac{((V_{\text{in}}-V_{\text{cr1}})\cdot k_1+V_{\text{cp1}}\cdot k_2)}{n} + \frac{\sqrt{((V_{\text{in}}-V_{\text{cr1}})\cdot k_1+V_{\text{cp1}}\cdot k_2)^2+(I_{Lr1}\cdot k_3+(I_{Lm1}-I_{Lr1})\cdot k_4)^2}}{n}. \quad (17)$$

By detecting whether the R signal exists or not, the proposed SR strategy can be divided into two conditions. As shown in Fig. 16, when f_s (the switching frequency) is larger than f_r (the resonant frequency) or f_s is slightly smaller than f_r, there is not enough time for V_{ds} to resonate half of the high-frequency (ω_{d1}) oscillation cycle after SR is turned OFF. It means that there will be no falling edge of the R signal, and BDC will not occur when turning-OFF late. Then, the conventional adaptive SR driving scheme can work normally under this condition. The turning-OFF point lags when BDC is detected and leads when BDC does not occur.

As shown in Fig. 17, when f_s is smaller than f_r, $V_{\text{ds'sr}}$ will resonate for enough time and a falling edge of signal R will appear after SR is turned OFF. Therefore, both turning-OFF early and late can lead to BDC. In this condition, the conventional adaptive SR driving scheme cannot work normally. It is necessary to determine the type of BDC (turning-OFF early or late). Fig. 17(a) shows the condition of SR turning-OFF prematurely, where BDC occurs before signal R. Fig. 17(b) shows the condition of SR turning-OFF late, where the signal R appears before BDC is detected. The two different types of BDC can be distinguished by the order of the R signal and the B signal. Fig. 17(c) represents the circumstance of turning-OFF slightly late or exactly.

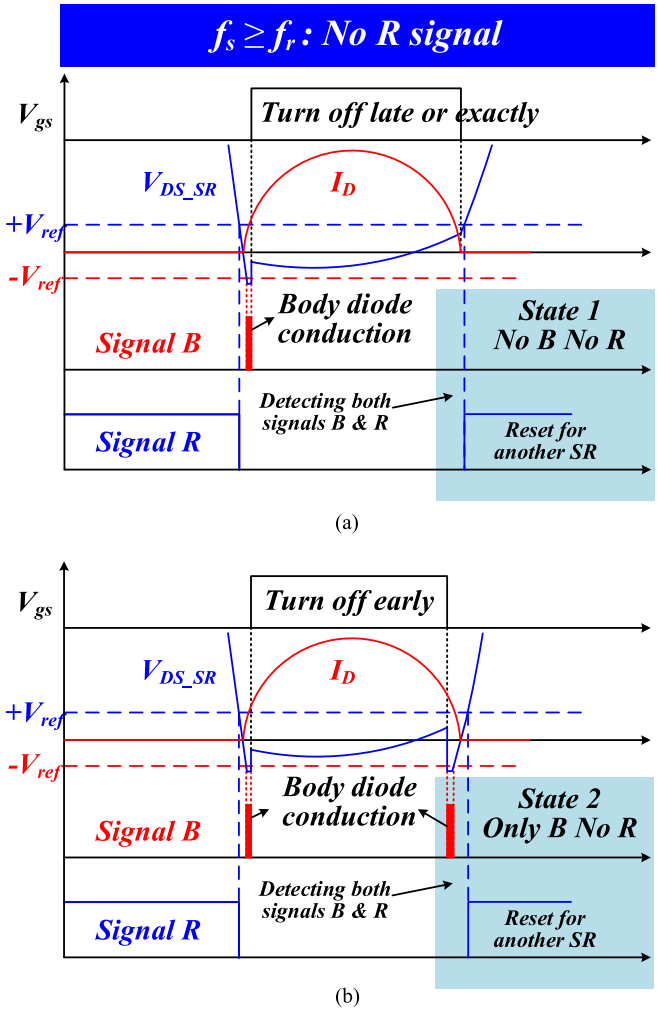


Fig. 16. Timing sequential of the sampling circuits when no valid R signal is detected ($f_s \ge f_r$ or f_s is slightly smaller than f_r).

TABLE I
STATES OF THE SYNCHRONOUS RECTIFICATION

State	Coding	Situation
State 1	$\overline{B}$	Turning-off exactly or turning-off late
State 2	$B\overline{R}$	Turning-off early $f_s \ge f_r$
State 3	BR	Turning-off early $f_s < f_r$
State 4	RB	Turning-off late $f_s < f_r$

For the convenience of digital implementation, the states of SR are classified and coded by the sampled signal. As given in Table I, the state of SR can be divided into the following four states according to the combination of the sampled signals R and B. Fig. 18 shows the detecting process and the control strategy for the four states of SR. First, check whether signal B

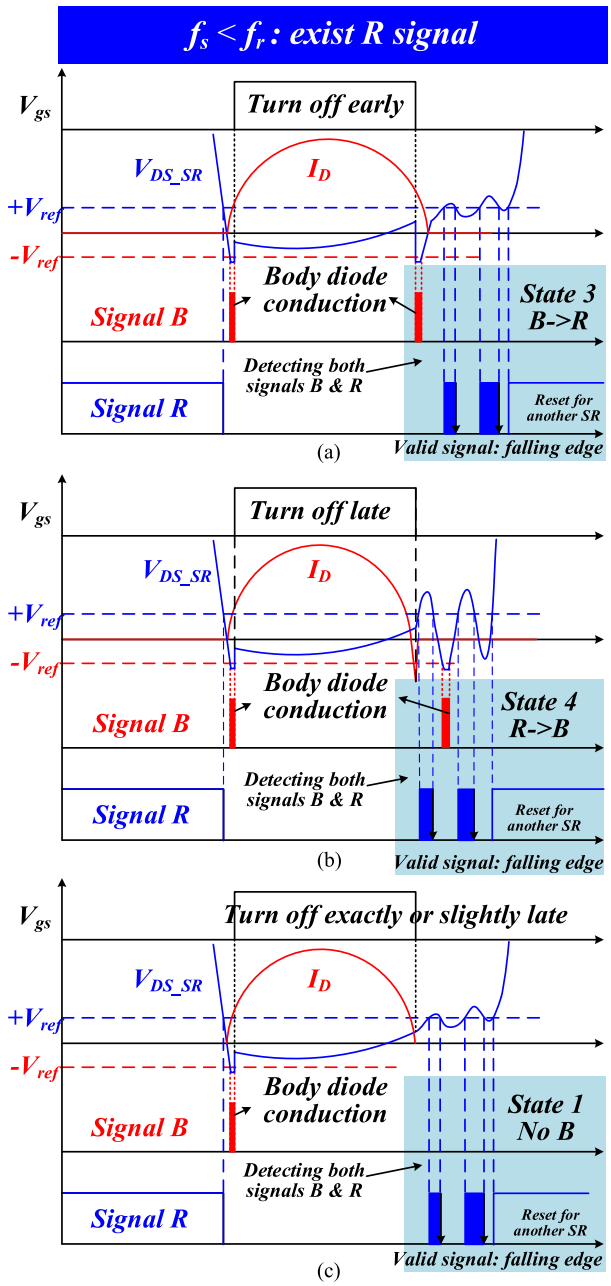


Fig. 17. Timing sequential of the sampling circuits when *R* signal is detected ($f_s < f_r$).

is available. If signal *B* is invalid, SR is at state. 1) If signal *B* is valid, then identify whether signal *R* is valid. If the R signal is invalid, SR is at State. 2) If both signal B and signal *R* are valid, the order between *R* and *B* should be determined. If *B* is before *R*, SR is at state 3. Otherwise, it is state 4.

State 0 is the initial state, which indicates that the current status of SR is unknown and needs to be identified first.

State 1 is coded as /B, which represents no BDC is detected. No matter state 1 occurs at the circumstances of $f_s \geq f_r$ or $f_s < f_r$, state 1 always represents that SR is turned OFF slightly late or exactly. The strategy for state 1 is leading the turning-OFF point until the BDC is detected. Then, lagging the turning-OFF point until BDC disappears again.

State 2 is coded as *B* /*R*, which represents that BDC can only be caused by turning-OFF prematurely. State 2 usually occurs when $f_s \geq f_r$ or f_s is slightly smaller than f_r. The strategy for state 2 is lagging the turning-OFF point until the BDC cannot be detected.

States 3 and 4 are coded as BR and RB, respectively. Both of the states occur when f_s is smaller than f_r and have the potential to achieve BDC caused by turning-OFF late. For state 3, BDC occurs before the falling edge of signal *R*, which represents that the BDC is caused by SR turning-OFF early. The strategy for state 3 is the same as state 2. For state 4, BDC occurs after the falling edge of signal *R*, which represents that BDC is caused by SR turning-OFF late. The strategy for state 4 is leading the turning-OFF point until BDC cannot be detected. Then, continue to lead the turning-OFF point until BDC appears again. Finally, lagging the turning-OFF point until no BDC is detected.

State 5 is the steady state, which means the turning-OFF point is regulated to the optimal point. Then, the SR control strategy enters the dormant state and detects whether BDC occurs again. If BDC is detected, the SR strategy restarts to state 0.

The strategy for states 1–4 can regulate the turning-OFF point to achieve ZCS of SR and enter the steady state.

IV. Comparison With Other Adaptive SR Driving Scheme

A comparison of different SR control strategies is illustrated in Table II. Different types of SR methods are compared for their performance of the target items, and set as strong, medium, and weak according to the order of their performance.

Theoretically, the current sensing based scheme is the most direct SR driving scheme [6], [7]. The benefits of the current sensing-based scheme are the elimination of duty cycle loss and prevention of reverse conduction. Moreover, the sampling circuit is the simplest and the cost is the lowest among other SR schemes. However, the extra loss introduced by the sampling circuits prevents it from being used directly. In the literature [10], [11], the indirect current sensing schemes are proposed. The core of these methods is to determine the secondary-side SR current by the subtraction between the sampled resonant current i_{Lr} (integrated by the voltage across resonant capacitor $v_{\rm cr}$) and the sampled magnetic current i_{Lm} (integrated by the voltage across the transformer). Then, the loss from the sampling circuits is significantly reduced. However, the performance is greatly affected by the deviation of circuit parameters such as the resonant capacitor C_r, the magnetic inductor L_m and turn ratios n. It is difficult to eliminate the duty cycle loss or to prevent reverse conduction when the circuit parameters deviate. The cost for this type of SR method depends on the complexity of the implementation.

The $V_{\rm ds}$ sensing based schemes introduce the lowest sampling loss and are widely applied in smart drivers [13], [14]. The cost for this type of SR method is low due to the implementation of IC. However, the performance of $V_{\rm ds}$ sensing based schemes is greatly influenced by ESL and owns the worst duty cycle loss. Moreover, for high-frequency applications, the duty cycle loss will become more and more serious due to the sharp increase

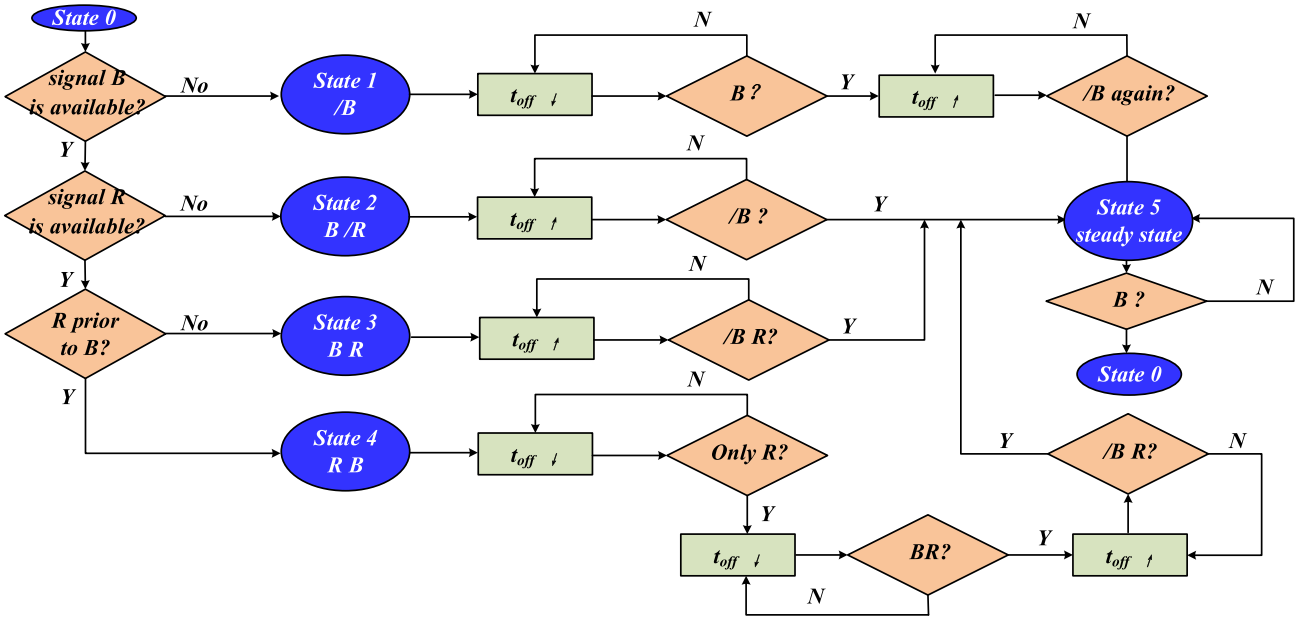


Fig. 18. Control flowchart of the proposed SR tuning process.

TABLE II
COMPARISON OF *LLC* SR CONTROL STRATEGIES

Control category	Current sensing based		V_{ds} sensing based		Adaptive based	
Sub-category	direct	Indirect	Without compensation	With compensation	Conventional adaptive	The proposed method
Reference	[6, 7]	[10, 11]	[13, 14]	[15-17]	[5, 22]	
Low loss of the sampling circuits	weak	medium	strong	medium	medium	medium
Low complexity of the sampling circuits	strong	weak	strong	medium	strong	medium
Low duty-cycle-loss	strong	medium	weak	medium	strong	strong
Ability to prevent reverse conduction	strong	medium	strong	medium	weak	strong
Robust to the circuit parameter drift	strong	weak	medium	weak	strong	strong
Easy to be realized by IC/MCU	strong	weak	strong	medium	strong	strong
Fit for high switching frequency	strong	medium	weak	medium	medium (calculation speed)	medium (calculation speed)
Fast regulating speed	strong	strong	strong	strong	weak	weak
Low cost	strong	medium	strong	medium	weak	weak

in *di/dt*. The compensation schemes [15]–[17] for $V_{\rm ds}$ sensing based method are introduced to reduce the duty cycle loss. The core of the compensation schemes is to balance the voltage caused by ESL through the Wheatstone bridge and to determine the actual voltage across $R_{\rm ds(on)}$. However, the complexity of the sampling circuit is increased. Moreover, the main drawback is that the compensation parameters are sensitive to the values of parasitic parameters, which are greatly affected by temperature. Therefore, the steady-state performance (duty cycle loss and reverse conduction) depends on the accuracy of stray inductance and $R_{\rm ds(on)}$.

The adaptive SR driving strategy [5], [22] can theoretically eliminate duty cycle loss through the simple sampling circuits and the simple control logic. Moreover, the method is insensitive to the stray parameters. The core of this method is to determine whether the turning-OFF point is premature by detecting BDC. Since BDC can also be caused by SR turning-OFF late, the conventional adaptive SR driving strategy may result in reverse

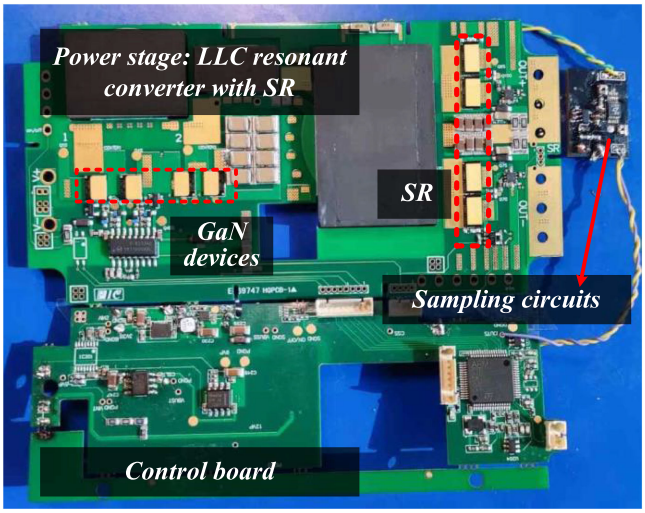


Fig. 19. Designed prototype for *LLC* with SR.

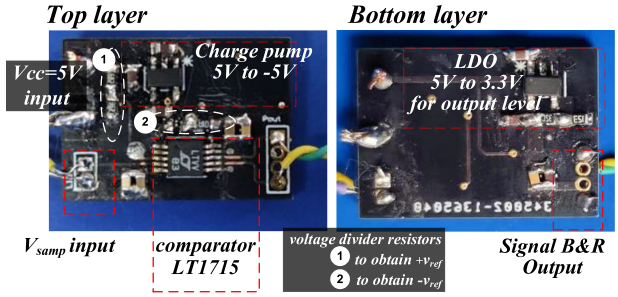


Fig. 20. PCB of the sampling circuits.

conduction under the working condition of $f_s<f_r$. The main drawback of this method is the regulating speed, which costs a relatively long time to regulate the turning-OFF point to the optimal position.

In this article, the proposed SR driving scheme inherits the advantages and disadvantages of the conventional adaptive SR scheme. Moreover, the problem of reverse conduction is solved at the cost of slightly increasing sampling complexity. The cost for this method is higher than other SR methods due to the additional comparator and micro-controller unit(MCU). However, if the proposed method could be implemented by the integrated circuits, the cost would approach the $V_{\rm ds}$ sensing-based method. The proposed scheme owns the features of simple and low-loss sampling circuits, good performance (both duty cycle loss and reverse conduction are eliminated), and insensitive to stray parameters. Therefore, the proposed SR driving scheme can be a good candidate for *LLC* synchronous rectification.

V. Experimental Results

A 280-W prototype of *LLC* resonant converter with synchronous rectification, as shown in Fig. 19, has been built to verify the established model and the proposed adaptive SR method above. The specifications of the prototype are as follows: input voltage $V_{\rm in}$ = 140-180V, output voltage V_o = 14V, maximum output current I_o = 20A, switching frequency f_s varies from 330 to 600 kHz. Fig. 19 shows the *LLC* power stage, the control stage, and the comparator board. Fig. 20 shows the enlarged view of the printed circuit board(PCB) of the comparator board, which is plugged on the secondary side of the *LLC* resonant converter, comparing $V_{\rm ds\cdot sr}$ with the two threshold voltages $+V_{\rm ref}$ and $-V_{\rm ref}$ to determine the features of BDC and reverse current. The sampled signals *B* and *R* are transferred to the microcontroller to regulate the turning-OFF point.

Table III gives the specific parameter of the designed prototype. Both the primary and secondary switches are chosen to be gallium nitride(GaN) devices for high-frequency switching.

TABLE III
Design Specification of the *LLC* Prototype.

Components	Parameters
Primary Switches S_1-S_2	GaN System GS66506T 650V, 22.5A. $R_{ds(on)}$=67mΩ,
Secondary Switches SR_1 and SR_2	GaN System GS61008T 100V, 90A. $R_{ds(on)}$=7mΩ
Transformer *T*	EQ38-3F46 ferrite core; Primary side series; n_p=6; Secondary side parallel; n_s=1*3; L_m= 20μH 8mm*2Oz;
Resonant inductor L_r	EQ18-3F46 ferrite core; 2.8μH, 4mm* 2Oz
Resonant capacitor C_r	2.2nF*16 500V, multiplayer ceramic capacitors (MLCC)
Input Capacitor C_{in}	22μF 500V, electrolytic capacitor
Output Capacitor C_o	4.7μF*80 50V, MLCC
Microcontroller	STM32F334R8
SR comparator	LT1715

Si8273 from Silicon Lab and UCC27611 from Texas Instruments are chosen to drive the primary and secondary GaN devices, respectively. Ferrite core material 3F46 from Ferroxcube is selected for transformer and inductor due to its performance for high-frequency applications. Planar cores are selected for the consideration of high power density. STM32F334R8 from STMicroelectronics is selected as the microcontroller due to its integrated high-resolution pulsewidth modulation generator. Thus, the time resolution ΔD is 0.868 ns. LT1715 from Linear Technology is chosen as the comparator for sampling the status of SR due to 4 ns propagation delay and TTL/CMOS compatible output. The charge pump IC TPS60402 (with the voltage divider resistors) is chosen to generate the negative reference voltage $-V_{\rm ref}$.

Figs. 21 and 22 show the results of the sampling circuits. The SR gate-to-source voltage $v_{\rm gs\cdot sr}$ (dark red line), resonant current i_{Lr} (green line), and magnetizing current i_{Lm} (pink line) are shown in the upper part of the figures. In fact, i_{Lm} is not measurable and is obtained by integrating the primary-side voltage across the transformer. i_{Lm} here is used to mark the appropriate SR turning-OFF point. The SR drain-to-source voltage $v_{\rm ds\cdot sr}$ (blue line), the sampled *R* signal (red line), and the sampled *B* signal (yellow line) are also listed in the figures. The red shaded area is the detecting window for the sampled

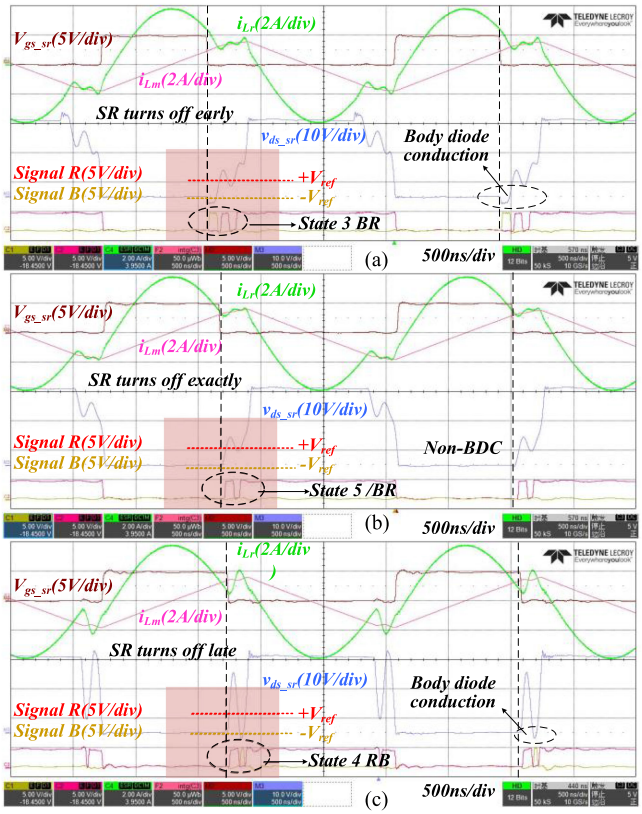


Fig. 21. Results of the sampling circuits when f_s<f_r. (a) SR turning OFF premature. (b) SR turning OFF exactly. (c) SR turning OFF late.

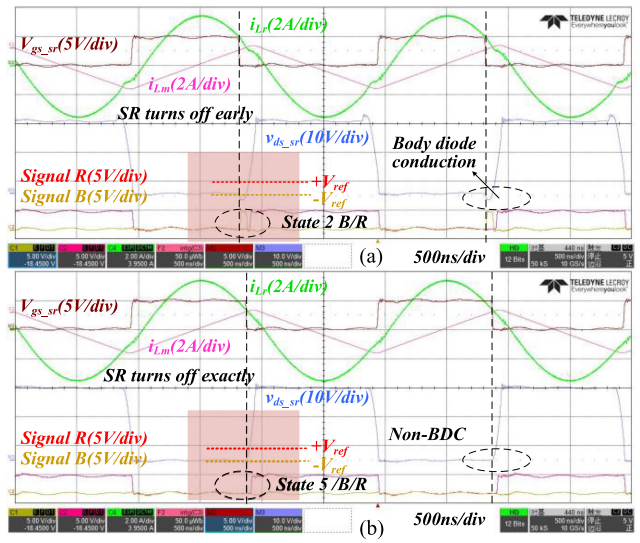


Fig. 22. Results of the sampling circuits when f_s≥f_r. (a) SR turning OFF early and (b) SR turning OFF exactly.

signals *R* and *B*. The falling edge of the *R* signal is valid, which represents that f_s is low enough for v_{ds_sr} to perform the resonance process mentioned in Section II. The rising edge of the *B* signal is valid, which means that the body diode of SR is conducted on. Fig. 21 shows the circumstance of f_s<f_r, the valid *R* signal can be detected in the detecting window. When SR is turned OFF prematurely [shown in Fig. 21(a)], the

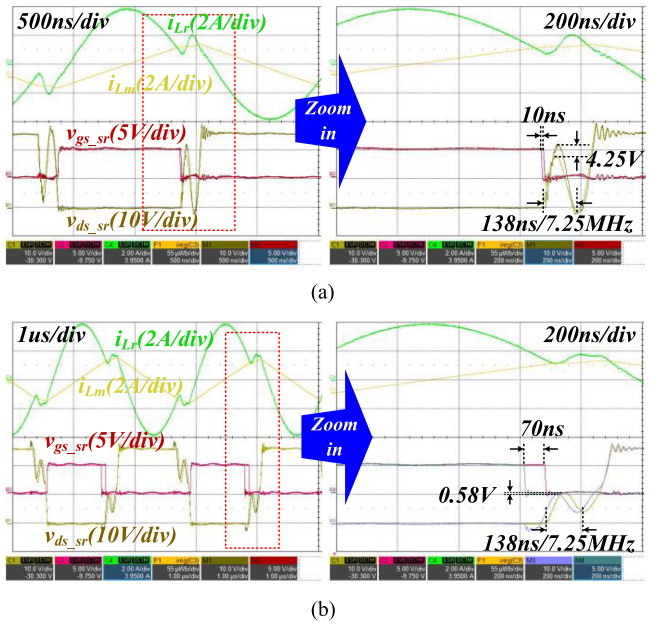


Fig. 23. Verification of the established model in Section II.

state BR can be sampled; when SR is turned OFF exactly [see Fig. 21(b)], the state/*BR* can be sampled; when SR is turned OFF too late, the state *RB* can be sampled. Fig. 22 shows the circumstance of f_s≥f_r, the valid *R* signal cannot be detected in the detecting window. When SR is turned OFF prematurely [see Fig. 22(a)], the state *B/R* can be sampled; when SR is turned OFF exactly or too late [see Fig. 22(b)], the state /*B*/*R* can be sampled. In the digital implementation, the range of f_s can be identified through the existence of the valid R signal, and then the different SR strategies can be implemented. In the case of f_s≥f_r, the conventional adaptive SR scheme can be used; while for the circumstance of f_s<f_r, the issue of BDC caused by SR turning-OFF late should be considered.

To verify the proposed model in Section II, the waveforms for different turning-OFF points are compared in Fig. 23. The adopted L_m, L_r, and C_r of the prototype are 20, 2.8, and 35.2 nF, respectively. Meanwhile, C_p is extracted to be 196.2 pF through the finite-element software. According to the model proposed in Section II, the angular frequency of oscillation during the dead time ω_{d1} = 4.56e7 rad/s. It can be seen from Fig. 23 that the oscillation frequency is 7.25 MHz(4.56e7 rad/2π), which is consistent with the model. According to the model, the larger the reverse current (i_{Lm}-i_{Lr}) at the turning-OFF point, the larger the oscillation amplitude. In Fig. 23(a), the two SR turning-OFF points only differ by 10ns, but the amplitudes of v_{ds_sr} differ by 4.25 V. In Fig. 23(b), the two SR turning-OFF points differ 70ns, but the amplitudes of v_{ds_sr} only differ by 0.58 V. The phenomenon can be well explained by the proposed model. Both the two comparison objects in Fig. 23(a) are in the case of SR turning-OFF late.

Although the difference of the turning-OFF points is only 10 ns, the difference for the reverse current in the two cases is relatively large. The comparison objects in Fig. 23(b) are that SR turns OFF early and exactly. Although the SR turning-OFF

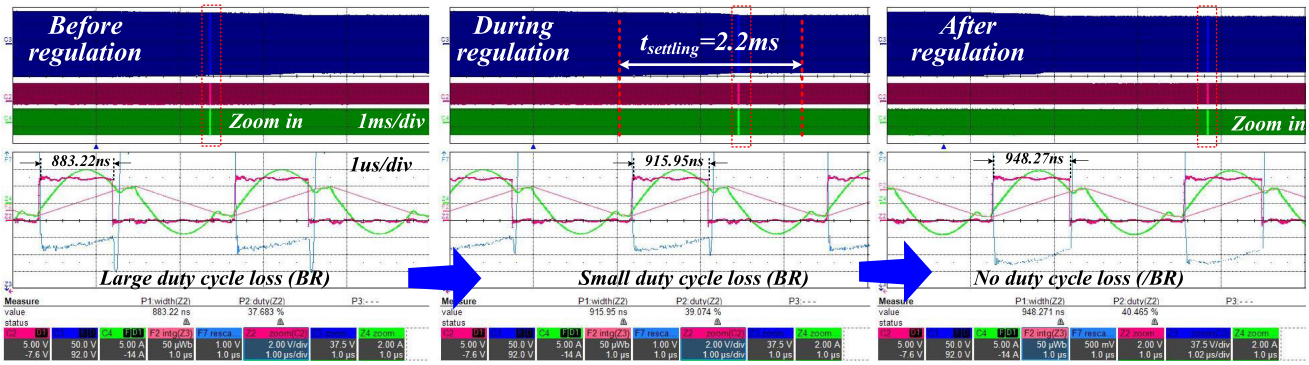


Fig. 24. Tuning process when $f_s < f_r$ and SR turning OFF early.

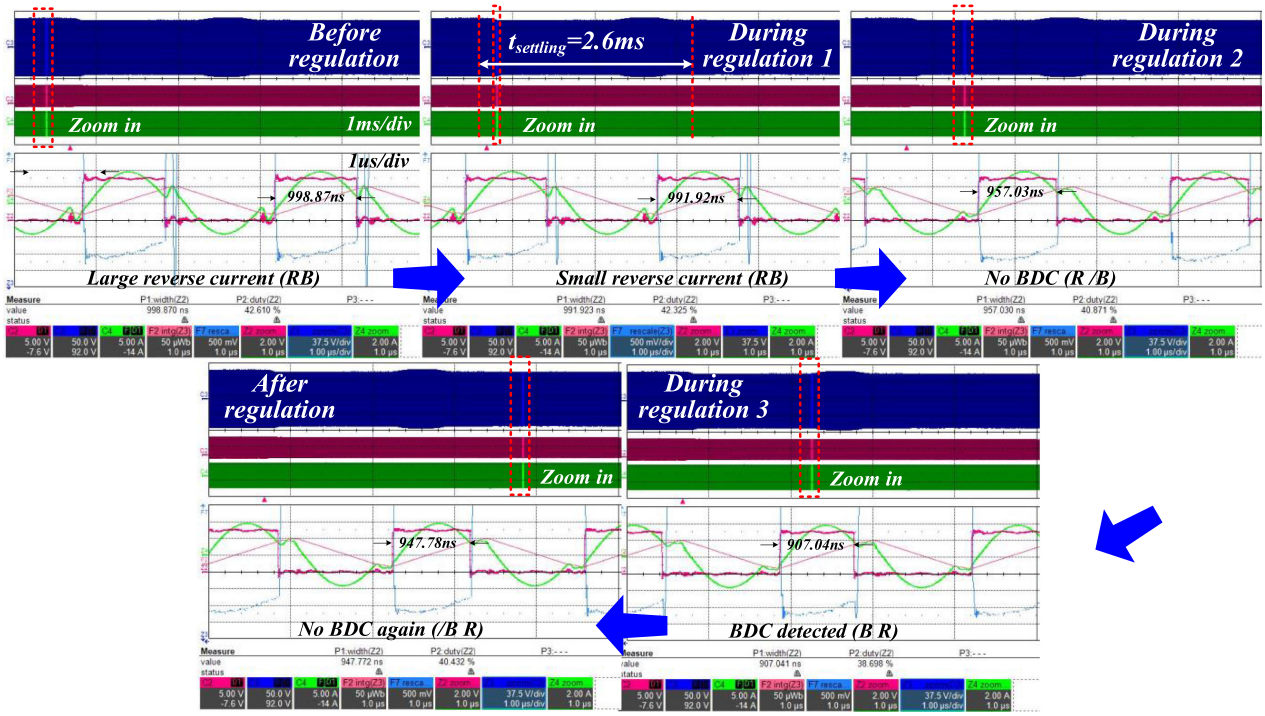


Fig. 25. Tuning process when $f_s < f_r$ and SR turning OFF late.

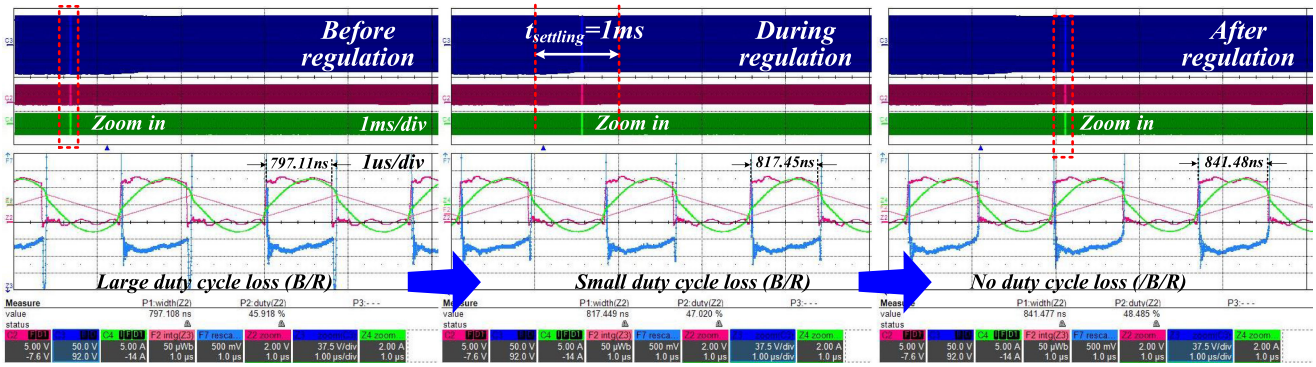


Fig. 26. Tuning process when $f_s \geq f_r$.

points differ by 70 ns, the reverse current of the two conditions is the same. Therefore, the oscillation amplitudes are similar.

Fig. 24 shows the dynamic regulating process when $f_s<f_r$ and SR is turned OFF prematurely. The test conditions for Fig. 24 are $f_{\rm sw}$ = 425 kHz, $V_{\rm in}$ = 160 V, and I_o = 10A, while the settling time is 2ms. The left-side figure is the waveforms before regulating. The current SR pulsewidth is smaller than the required SR pulsewidth, and the body diode is conducted on due to SR turning-OFF early. According to the sampled status, the SR control strategy gradually increases the SR pulsewidth. The middle figure is the waveforms during regulation. The duty of SR increases from 37.7% to 39.1%. The right-side figure is the waveforms after regulating. It can be seen that the current SR pulsewidth equals the required SR pulsewidth, and BDC is eliminated.

Fig. 25 shows the dynamic regulating process when $f_s<f_r$ and SR is turned OFF late. The test conditions for Fig. 25 are $f_{\rm sw}$ = 425 kHz, $V_{\rm in}$ = 160 V, and I_o = 10 A, while the settling time is 2.6 ms. Before regulating, the current SR pulsewidth has been larger than the required SR pulsewidth, and there is BDC caused by SR turning-OFF late. The proposed SR control strategy can effectively identify this type of BDC and gradually reduce the SR pulsewidth. During the regulation, the duty of SR continues to decrease until BDC (another type) is detected. As shown in the middle figure, three states *RB*, *R/B*, and *BR* will go through one by one. Then, BDC can be detected and the SR pulsewidth continues to increase and will end until BDC cannot be detected again. The last figure is the waveforms when the regulating process has been finished. It can be seen that the current SR pulsewidth equals the required SR pulsewidth, and BDC is eliminated.

Fig. 26 shows the dynamic regulating process of SR when $f_s>f_r$. The test conditions for Fig. 26 are $f_{\rm sw}$ = 577 kHz, $V_{\rm in}$ = 180 V, and I_o = 10 A, while the settling time is 1ms. Before regulating, the SR pulsewidth is smaller than the required SR pulsewidth, and there is BDC caused by SR turning-OFF early. The SR control strategy starts to increase the SR pulsewidth when detecting the SR status. The right-side figure shows the waveforms after regulating. The current SR pulsewidth has been regulated to the required SR pulsewidth, and BDC cannot be detected. Therefore, within all switching frequency regions and the circumstance of SR status, the SR gate driving signal could be tuned to be the optimal turning-OFF point using the proposed adaptive SR driving scheme.

To verify the dynamic performance of the *LLC* resonant converter with the proposed SR method, Fig. 27(a) shows the transient process for the start-up conditions. To reduce the overshoot current during the start-up process and to prevent i_{Lr} from entering the capacitive region, a high-frequency soft starting method is adopted, where the *LLC* resonant converter works in the $f_s>f_r$ condition. The SR turning-OFF points are synchronized with the ones of the primary switches. Fig. 27(b) and (c) shows the transient processes at the nominal input when load steps up and down between full load and 25% load. When a step load variation occurs, the proportion integral derivative(PID) tuning module responds and the output voltage V_o can be regulated to 14 V. The proposed SR method can regulate

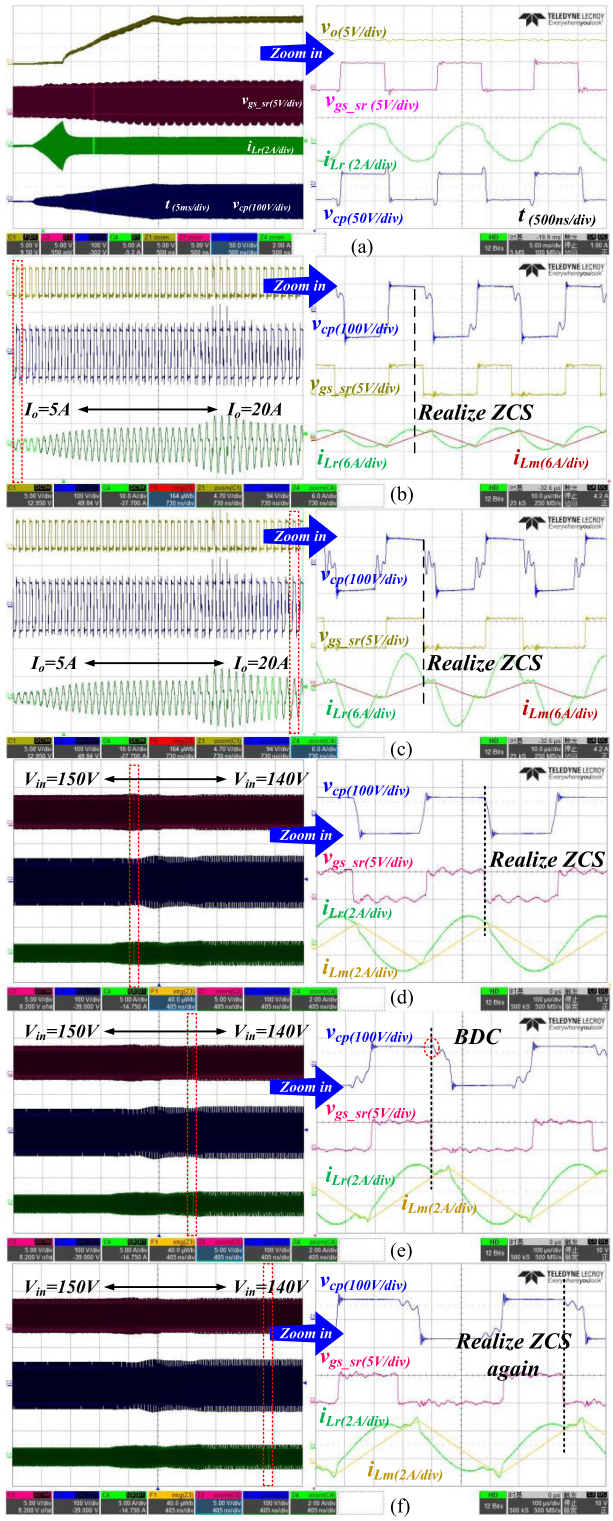


Fig. 27. Transient processes for (a) start-up, (b) and (c) load steps, (d)–(f) input voltage steps of the *LLC* converter with the proposed SR method.

the turning-OFF point based on the sampled $v_{\rm ds\_sr}$ signal. The SR for both the 25% and 100% load conditions can realize ZCS at the steady state. Fig. 27(d)–(f), respectively, show the SR waveforms before, during, and after regulation when the

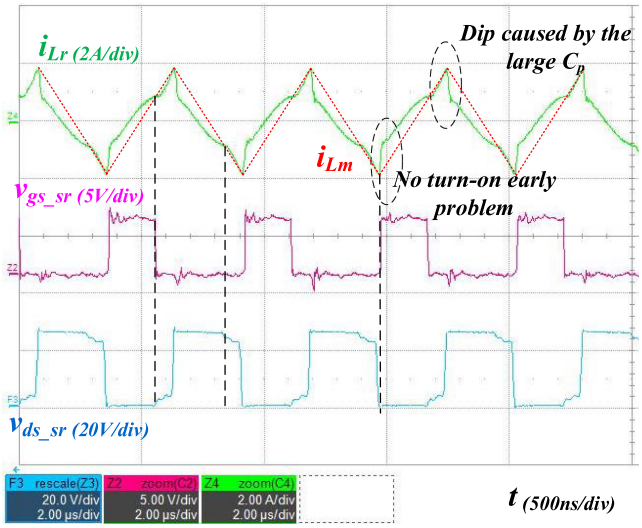
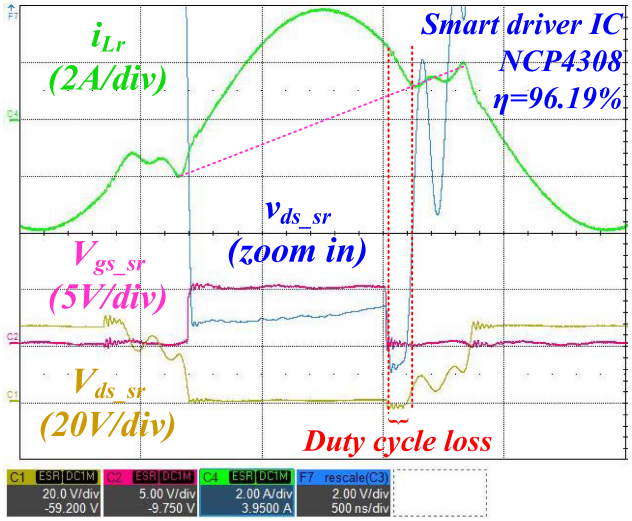


Fig. 28. SR waveform at 10% load.

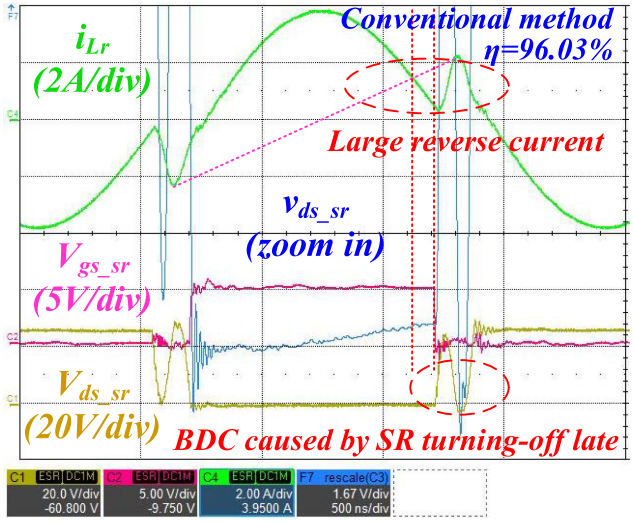
input voltage steps from 150 to 140 V. When the input variation occurs, the PID tuning module works and the switching frequency is regulated to make the output voltage to be 14 V. Meanwhile, the proposed SR method regulates the turning-OFF point based on the sampled $v_{\mathrm{ds\_sr}}$ signal. The SR for both the 150 and 140 V input conditions can realize ZCS at the steady state.

In the adaptive SR method, the turning-ON points of SRs are synchronized with the ones of the primary switches. Thus, the issue of capacitive current spike always occurs in the light load condition to decrease efficiency [30]. Fig. 28 shows the main waveforms of the designed *LLC* resonant at 10% load. Due to the small junction capacitance of the primary switches and the large junction capacitance of the secondary switches, the resonant current i_{Lr} will generate a large dip [32], which can lead the phase of the energy transferring period at light load. Then, the efficiency degradation caused by premature turn-ON in the adaptive SR method can be suppressed.

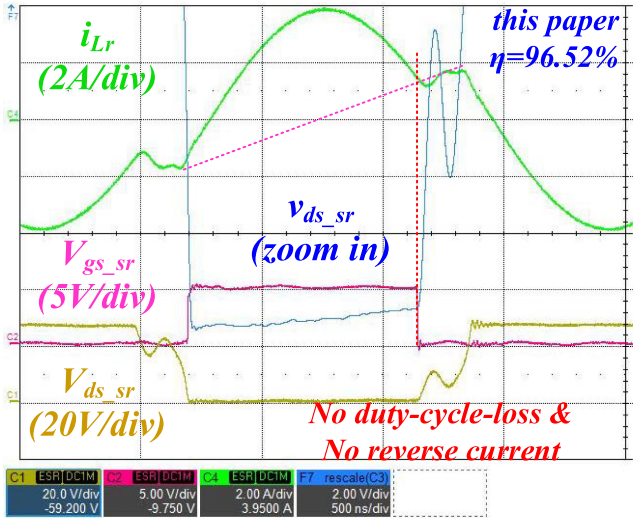
To verify the actual effect of the proposed adaptive SR strategy, the commercial smart driver IC and the conventional adaptive SR method are simultaneously compared in Fig. 29 under the same working condition of $V_{\mathrm{in}} = 160$ V and $I_o = 10$ A (half load). Fig. 29(a) shows the SR effect using the commercial smart driver IC NCP4308 from on semiconductor. Due to the optimization of the layout and the selected low inductance GaN devices, the ESLs introduced by PCB and devices have been reduced as much as possible. Therefore, only 96 ns duty cycle loss is obtained when f_s is around 400 kHz. However, since GaN devices have no parasitic body diodes, the voltage drop during reverse conduction is relatively large, which still generates the considerable duty cycle loss. When $f_s < f_r$ and load switches from heavy to light, the required SR pulsewidth is smaller than the current one, which may cause reverse BDC. If adopting the conventional adaptive SR scheme, the SR pulsewidth will continue to increase after detecting the BDC. The operation is opposite to the required operation (reducing the SR pulsewidth), which will result in a large reverse current from load to source. Fig. 29(b)



(a)



(b)



(c)

Fig. 29. Effect comparison with half-load condition among (a) commercial smart driver IC, (b) conventional SR adaptive method, and (c) the proposed adaptive SR strategy.

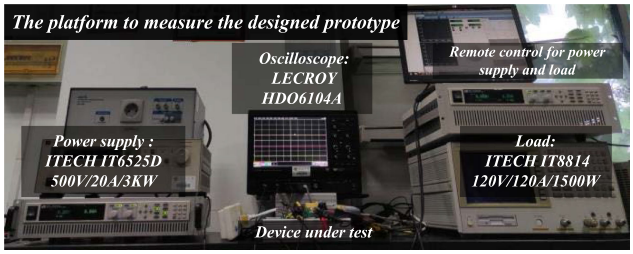


Fig. 30. Efficiency comparison with the commercial SR controllers.

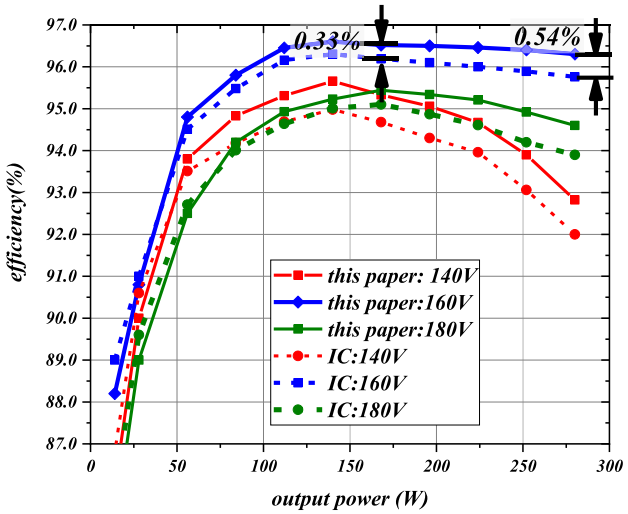


Fig. 31. Platform to measure the efficiency curve.

shows the situation described above. After load stepping down, the SR pulsewidth is limited to the maximum value (if not limited, shoot through will occur), resulting in the larger loss. Fig. 29(c) shows the SR effect of the proposed method, which can tune SR to be the optimal turning-OFF point, avoiding both issues of duty cycle loss and reverse current from load to source. Then, the efficiency can be improved from 96.19% (using smart diver IC) and 96.03% (using conventional adaptive SR method) to 96.52%.

Fig. 30 shows the efficiency comparison between the commercial SR smart driver NCP4308 and the proposed adaptive SR driving scheme. The platform to measure the efficiency curve is shown in Fig. 31. When the switching frequency is higher, the efficiency improvement is higher. Meanwhile, the efficiency is improved more significantly at the heavy load. The reasons for the phenomenon are that the smart driver IC will produce larger duty-cycle-loss when the *di/dt* is higher and the proposed SR method can eliminate duty-cycle-loss. In light-load conditions, the efficiency of the proposed SR method is worse than the one of the smart driver IC due to the larger switching loss (the green mode in the smart driver IC). Meanwhile, the loss of the introduced high-precision comparator and MCU in the proposed SR method is gradually not negligible. Finally, the efficiency is improved by 0.33% at the half load (waveforms shown in Fig. 29) and 0.54% at the full load.

In fact, GaN devices can operate at several MHz switching frequencies. If adopting the commercial smart drivers in high-frequency GaN-based applications, the duty cycle loss caused by parasitic inductance will be larger. The efficiency improvement of the proposed SR driving strategy will be much more significant.

VI. Conclusion

In this article, the issue of BDC caused by SR turning-OFF late is modelled and analyzed quantitatively. Then, the generation mechanism and conditions for this type of BDC are obtained. Moreover, an improved adaptive SR driving scheme is proposed to distinguish the two different types of BDC and to take the corresponding measures to regulate the turning-OFF point. Finally, the established model is verified that can explain the actual phenomenon. Besides, the proposed SR control strategy is verified to eliminate both duty cycle loss and reverse current effectively.

References

[1] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Using LLC resonant converter for designing wide-range voltage source," *IEEE Trans. Ind. Electron.,* vol. 58, no. 5, pp. 1746–1756, May 2011.

[2] C. Fei, F. C. Lee, and Q. Li, "High-Efficiency high-power-density LLC converter with an integrated planar matrix transformer for high-output current applications," *IEEE Trans. Ind. Electron.,* vol. 64, no. 11, pp. 9072–9082, Nov. 2017.

[3] Q. Liu, Q. Qian, B. Ren, S. Xu, W. Sun, and L. Yang, "A Two-stage buck-boost integrated LLC converter with extended ZVS range and reduced conduction loss for high-frequency and high-efficiency applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 727–743, Feb. 2021.

[4] W. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, and B. J. Blalock, "Investigation of gallium nitride devices in high-frequency LLC resonant converters," *IEEE Trans. Power Electron.,* vol. 32, no. 1, pp. 571–583, Jan. 2017.

[5] W. Feng, F. C. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Trans. Power Electron.,* vol. 27, no. 8, pp. 3775–3781, 2012.

[6] X. Xie, J. C. P. Liu, F. N. K. Poon, and M. H. Pong, "A novel high frequency current-driven synchronous rectifier applicable to most switching topologies," *IEEE Trans. Power Electron.,* vol. 16, no. 5, pp. 635–648, May 2001.

[7] Z. Liu, R. Yu, T. Chen, Q. Huang, and A. Q. Huang, "Real-time adaptive timing control of synchronous rectifiers in high frequency GaN LLC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 2214–2220.

[8] J. Zhang, J. Wang, G. Zhang, and Z. Qian, "A hybrid driving scheme for full-bridge synchronous rectifier in LLC resonant converter," *IEEE Trans. Power Electron.,* vol. 27, no. 11, pp. 4549–4561, Nov. 2012.

[9] G. K. Y. Ho, R. Yu, and B. M. H. Pong, "Current driven synchronous rectifier with saturable current transformer and dynamice gate voltage control for LLC resonant converter," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 2345–2351.

[10] X. Wu, G. Hua, J. Zhang, and Z. Qian, "A new current-driven synchronous rectifier for series–parallel resonant (LLC) DC–DC converter," *IEEE Trans. Ind. Electron.,* vol. 58, no. 1, pp. 289–297, Jan. 2011.

[11] D. Huang, D. Fu, F. C. Lee, and P. Kong, "High-Frequency high-efficiency CLL resonant converters with synchronous rectifiers," *IEEE Trans. Ind. Electron.,* vol. 58, no. 8, pp. 3461–3470, Aug. 2011.

[12] M. Li, Z. Ouyang, M. A. E. Andersen, and B. Zhao, "Self-Driven gate driver for LLC synchronous rectification," *IEEE Trans. Power Electron.,* vol. 36, no. 1, pp. 56–60, Jan. 2021.

[13] "NCP4303A, NCP4303B secondary side synchronous rectification driver for high efficiency SMPS topologies," OnSemiconductor, Denver, CO, USA, Apr. 2015.

[14] "UCC24610 GREEN rectifier^{TM} controller device," TexasInstruments , Dallas, Texas, USA, 2015. [Online]. Available: https://www.ti.com/lit/gpn/ucc24610

[15] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.,* vol. 24, no. 5, pp. 1321–1329, May 2009.

[16] D. Wang and Y. Liu, "A zero-crossing noise filter for driving synchronous rectifiers of LLC resonant converter," *IEEE Trans. Power Electron.,* vol. 29, no. 4, pp. 1953–1965, Apr. 2014.

[17] L. He and J. Chen, B. Cheng, and H. Zhou, "Duty cycle loss compensation method based on magnetic flux cancelation in high-current High-frequency synchronous rectifier of LCLC converter," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 103–113, Jan. 2021.

[18] O. Yu, C. Chen, C. Yeh, and J. Lai, "Cyclically adaptive multilevel gate driving for drain-source synchronous rectifier efficiency improvement and range extension," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 1582–1587.

[19] O. Yu, C. W. Chen, C. S. Yeh, and J. S. Lai, "Sequential parallel switching for drain-source synchronous rectification efficiency boost in parallel switch rectifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 67, no. 11, pp. 2637–2641, Nov. 2020.

[20] M. Mohammadi and M. Ordonez, "Synchronous rectification of LLC resonant converters using homopolarity cycle modulation," *IEEE Trans. Ind. Electron.,* vol. 66, no. 3, pp. 1781–1790, Mar. 2019.

[21] J. Hsu, M. Ordonez, W. Eberle, M. Craciun, and C. Botting, "LLC synchronous rectification using resonant capacitor voltage," *IEEE Trans. Power Electron.,* vol. 34, no. 11, pp. 10970–10987, Nov. 2019.

[22] C. Fei, Q. Li, and F. C. Lee, "Digital implementation of adaptive synchronous rectifier (SR) driving scheme for high-frequency LLC converters with microcontroller," *IEEE Trans. Power Electron.,* vol. 33, no. 6, pp. 5351–5361, Jun. 2018.

[23] A. Iorio, A. Bianco, M. Foresta, G. Scappatura, C. Adragna, and S. DeSimone, "Predictive adaptive method for synchronous rectification," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 1986–1992.

[24] F. Wang, B. A. McDonald, J. Langham, and B. Fan, "A novel adaptive synchronous rectification method for digitally controlled LLC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 334–338.

[25] S. C. Moon, C. S. Chen, and D. J. Park, "Adaptive dead time synchronous rectification control for high efficiency LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 2939–2946.

[26] P. Amiri, C. Botting, M. Craciun, W. Eberle, and L. Wang, "Analytic-Adaptive LLC resonant converter synchronous rectifier control," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5941–5953, May 2021.

[27] Q. Qian, S. Xu, J. Yu, W. Sun, and H. Li, "A digital detecting method for synchronous rectification based on dual-verification for LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 2091–2097.

[28] "UCD7138 4-A and 6-A single-channel synchronous-rectifier driver with body-diode conduction sensing and reporting datasheet (Rev. B)," Texas-Instruments, Dallas, TX, USA, 2015. [Online]. Available: https://www.ti.com/lit/gpn/ucd7138

[29] "SRK2001: Adaptive synchronous rectification controller for LLC resonant converter," STMicroelectronics, Geneva, Switzerland, 2015. [Online]. Available: https://www.st.com/resource/en/datasheet/srk2001.pdf

[30] "FAN6248XC /XD: Advanced synchronous rectifier controller for LLC resonant converter," OnSemiconductor, Phoenix, AZ, USA, 2017, [Online]. Available: https://www.onsemi.cn/pub/Collateral/FAN6248HC-D.PDF

[31] Y. Wei, Q. Luo, and H. A. Mantooth, "Synchronous rectification for LLC resonant converter: An overview," *IEEE Trans. Power Electron.,* vol. 36, no. 6, pp. 7264–7280, Jun. 2021.

[32] L. Xue and J. Zhang, "Highly efficient secondary-resonant active clamp flyback converter," *IEEE Trans. Ind. Electron.,* vol. 65, no. 2, pp. 1235–1243, Feb. 2018.