A Hysteresis Current Controller PWM Scheme Applied to Three-Level NPC Inverter for Distributed Generation Interface

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***Abstract*—In this article, a novel pulsewidth modulation (PWM) technique is proposed for an existing space vector hysteresis current controller (SVHCC) scheme. A three-level neutral-point-clamped (NPC) inverter is used for dual purpose of shunt active power filtering and solar photovoltaic (PV) power integration to a distribution grid. This dual-purpose NPC inverter utilizes the proposed PWM technique for solving the neutral-point voltage-balancing issue in a unique way. Due to the inherent advantages of the SVHCC, the current control is characterized by fast action and optimal switching. A single reference current required for both filtering and maximum PV power integration is generated using instantaneous power theory, where a diode bridge rectifier load is considered to demonstrate the controller performance while compensating nonlinear current components. Thus, not only a unique space-vector-based PWM technique is adopted for fast-tracking of currents, but also a sliding current error boundary is used for the first time. This sliding technique tackles the dc-link balance issue of the NPC inverter while controlling the output currents simultaneously. The simulation and hardware results prove the aforementioned performance and demonstrate the efficacy of the proposed PWM current controller.**

***Index Terms*—Distributed generation (DG), neutral-point-clamped (NPC) inverter, neutral-point (NP) voltage balancing, shunt active power filter (SAPF), space vector hysteresis current controller (SVHCC).**

I. Introduction

In DISTRIBUTED generation (DG) systems powered by solar photovoltaic (PV) arrays, current-controlled voltage-source inverters (VSIs) are normally used. The VSI, which is mainly used for integrating solar dc power into ac grid, is underutilized in terms of its current capacity during the low irradiation period. During those time periods, the unused inverter capacity can be used to support the grid through reactive and harmonic current compensation at the point of common coupling (PCC) [1], [6]. These harmonic currents (to be compensated) are generated by the nonlinear electrical devices present in the distribution system, which, in turn, cause undesired power losses in the grid, voltage waveform distortion, etc. [7]. Thus, reactive power and harmonic current compensation are two significant concerns for proper distribution system operation [1].

The reference signal given to the VSI employed for renewable energy integration as well as shunt active power filtering is a current signal [1], [8], and thus, current control of the VSI is a natural choice. The reference current to the inverter consists of three components: first, sum of load harmonic currents; second, reactive current of the load; and third, required line current to transfer PV power to the grid. This reference current can be accurately generated using instantaneous power theory or *pq* theory [9], [10]. In recent times, model-predictive control (MPC) has gained popularity as an effective control technique for multilevel inverters (MLIs) [11]–[13]. In [11], two strategies based on the multiobjective cost function and the single-objective cost function were proposed to control inverter currents and balance the dc-link capacitor voltages, but the total dc-link voltage was not held constant with the variation of power demand. In [12], the MPC algorithm is relatively complex for practical implementation, whereas, in [13], an intelligent neural-network-based MPC was used for grid current control. The effectiveness of the MPC scheme of [13] was demonstrated through simulation studies.

Apart from MPC, several classical hysteresis-control-based approaches [14]–[16] for current control of three-level neutral-point-clamped (NPC) inverters have also been reported in the literature. In [14], three individual current controllers for three phases were suggested. However, the neutral-point (NP) voltage-balancing issue was not discussed in this article. An improved digital hysteresis current controller for a grid-tied three-level NPC converter is proposed in [15] for single-phase application. This technique has the capability of reactive power compensation, but the output current contains relatively more amount of harmonic components. A direct current control method was proposed in [16] for grid-connected NPC inverters, where "the best inverter voltage vector" is applied, which opposes the current error vector for superior current control, and symmetric switching frequencies within the three phases are observed. However, the switching frequency achieved in this article may widely vary with the modulation index, and capacitor voltage-imbalance issues may get aggravated if no redundant vector is available for reducing the deviation in dc-link capacitor voltages.

Among different hysteresis controllers, a space vector hysteresis current controller (SVHCC) has the inherent advantage of optimal switching pattern, good dynamic behavior, superior

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transient performance, and nearly constant switching frequency for the inverter [17], [23]. Among various three-phase inverters used for dual purpose of active power injection and shunt compensation, most of the power converters utilize a two-level structure [4], [6]. However, in medium-voltage and high-power applications, MLIs are more suitable [24], [26]. Out of various MLI structures, a three-level NPC inverter has gained maximum popularity in industry. The SVHCC technique employed for the three-level NPC inverter needs to maintain the dc-link capacitor voltages at half the total dc-link voltage apart from appropriately tracking the reference output current. In the literature so far, the SVHCC technique is mainly demonstrated either for the two-level inverter [17], [19], [21] or for the MLI structures without any NP [18], [22], [23]. It is established in the literature that the power factor angle, load imbalances, and nonlinear loads cause oscillations and deviations in the NP voltage of a three-level NPC inverter [27], [28]. In very few publications, researchers have discussed about hysteresis current control implemented for three-level NPC inverters and the associated NP voltage-balancing issue. However, these works require either a lookup table approach or a complex algorithm and exhibit nonoptimal switching [29], [31]. Although Chauhan and Tekwani [32] and Sezen *et al.* [33] presented the three-level NPC inverter for DG or shunt active power filter (SAPF) applications, the dc-link NP voltage-balancing issue was not discussed at all. The SVHCC-based technique is also studied for various grid-connected applications in the literature [34], [35]. A circular hysteresis strategy was studied for active power filter application in [34]. The SVHCC with a fractal approach for sector detection was implemented for the three-level front-end converters in [35]. However, these works do not either ensure an optimal switching pattern or use the NPC inverter.

In this article, a comprehensive classical SVHCC-based pulsewidth modulation (PWM) current control scheme is proposed with an NP balancing method for the three-level NPC VSI. The symmetric modulation as in [36] is maintained in this work, where the distribution of duty cycle among the redundant vectors is calculated at the beginning of every modulation period with an objective to achieve NP voltage balance by the end of the modulation period. Similar to the existing SVHCC operation, this controller calculates (in real time) the length of the boundary of the current error space vector and also the required changes related to boundary construction for balancing NP voltage in the dual-purpose inverter. Also, compensation of harmonic currents of nonlinear loads by the standard SVHCC results in higher distortion in compensated grid current [37]. To address this, in this article, a method for identifying the appropriate switching vectors for improved tracking of the reference current is proposed and experimentally verified.

To summarize, the contributions of this article are as follows.

1) For the first time, the SVHCC is modified for the three-level NPC converter, where, along with optimal output current control, balancing of internal dc capacitor voltage is also achieved. Although a model-based approach may be an alternative, the proposed PWM method uses the classical space vector current control philosophy as a baseline. The proposed sliding-type space vector boundary is also realized in the space vector plane to achieve balancing of neutral voltage.
2) The proposed space vector approach achieves an improved tracking of the rapidly changing reference current (using "Big-vectors" shown later) and, thereby, reduces the distortion in the compensated grid current at the PCC.

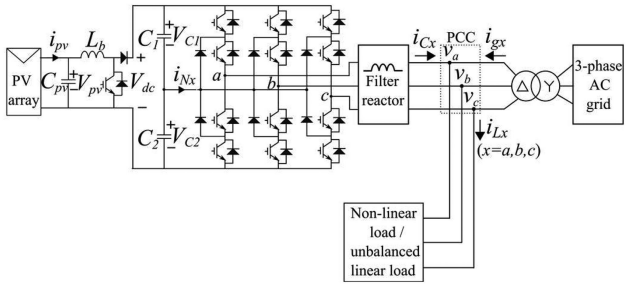

Fig. 1. System configuration.

II. System Description

Fig. 1 shows the power circuit of the dual-purpose inverter, which integrates the solar PV to the grid as well as operates as an SAPF simultaneously. Henceforth, for brevity, this dual operation (application) of the inverter would be termed as "DG + SAPF operation (application)" in this article. The dc link of the three-level VSI is powered by a PV-array-fed boost converter. Thus, the power from solar PV can be fed to the PCC, which also connects local nonlinear loads. At the PCC, the net real power supplied into the grid is equal to that of the solar PV power minus real power drawn by the load at the PCC. To make the grid voltage more realistic in simulation, 3% fifth harmonic component and 1% seventh harmonic component have been considered in the grid voltage. Furthermore, the line impedance between the PCC and the source grid is considered to be consisting of 200 mΩ resistance and 300 μH inductance.

The reference current to the VSI for DG + SAPF application is generated through instantaneous power theory (*pq* theory), and the corresponding block diagram is shown in Fig. 2. From PCC fundamental voltages and load currents (calculated from grid currents and converter currents at the PCC by using Kirchhoff's current law), instantaneous real power (p) and instantaneous imaginary power (q) of the nonlinear load are derived. Both p and q have an average $(\bar{p}\ \text{and}\ \bar{q})$ and an oscillating $(\tilde{p}\ \text{and}\ \tilde{q})$ part. $\bar{p}$ represents the average real power drawn by the load, and therefore, except this, other powers $(\tilde{p}\ \text{and}\ q)$ need to be supplied through the VSI to compensate for harmonic and reactive components of the nonlinear load current. For this, a converter current reference is generated through the calculation of compensating powers $(p^*_{\text{conv}}\ \text{and}\ q^*_{\text{conv}})$. In this article, p_{pv} is obtained by the maximum power point tracking controller (using the conventional perturb and observe method) after considering the efficiency of the boost converter (i.e., p_{pv} is the output of the boost converter). The power loss in the converter results in dc-link voltage drop, and to compensate for that, p_{loss} is found by a proportional–integral (PI) based voltage controller for maintaining the dc-link voltage at a constant value. It can

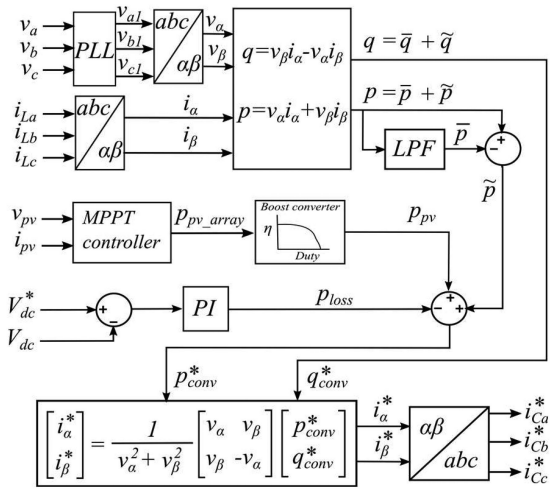

Fig. 2. Reference current generation based on instantaneous power theory or *pq* theory.

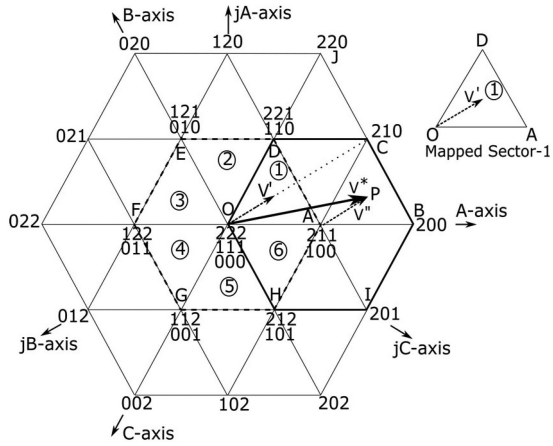

Fig. 3. Reference voltage vector upon three-level space vector structure.

also be observed that in the case of solar power integration to the grid and in the absence of any nonlinear/linear load at the PCC, (p and q) will be zero, and hence, in this case, $p^*_{\rm conv}$ consists of only $p_{\rm pv}$ and $p_{\rm loss}$.

III. Space Vector Hysteresis Current Control

From Fig. 1, one can write

$$V^* = R_f I^* + L_f \frac{dI^*}{dt} + V_{\rm pcc} \tag{1}$$

where $V_{\rm pcc}$ is the PCC phase voltage vector, I^* is the VSI reference current vector (current direction is toward the PCC), R_f and L_f are the resistance and the inductance of the filter reactor, respectively, and V^* is the VSI reference voltage vector. In the SVHCC, on the space vector plane, in every switching cycle period $(2T_s)$, V^* is synthesized by the nearest three stationary vectors V_k, and respective vector timings T_k are decided indirectly by setting up an appropriate space vector current error boundary. This results in the actual converter current vector I to be equal to I^* in average sense, but, instantaneously, I would be different from I^*. The applied inverter voltage vector V_k and actual current vector I are related by the following dynamic equation:

$$V_k = R_f\ I + L_f \frac{dI}{dt} + V_{\rm pcc}. \tag{2}$$

The current error vector is defined as

$$\Delta I_k = I - I^*. \tag{3}$$

From (1) and (2), after neglecting R_f (due to its insignificant value/effect as compared to L_f), the voltage error vector is defined as

$$\Delta V_k = V_k\ -\ V^* = L_f\ \frac{d\,(I - I^*)}{dt}. \tag{4}$$

From (3) and (4), we have

$$\Delta I_k = \frac{\Delta V_k}{L_f}\ T_k. \tag{5}$$

The calculated value of ΔI_k in (5) is used to compute the boundary of the current error for the SVHCC. The actual current error vector is made to remain within the current error boundary (calculated online) with the help of boundary check tables as well as by applying a proper vector V_k (for corrective action at the onset of every violation of this boundary) [22].

Fig. 3 shows the derived reference voltage vector V^* on the three- level space vector plane at some particular instant, where the tip of V^* lies in triangle ACB. The boundary calculation [in (5)] requires estimated values of approximate vector application times T_k of vectors of triangle ACB. These timings T_k are similar to those of a voltage-controlled conventional space vector pulsewidth modulation (SVPWM) scheme, where an optimal vector sequence is maintained. For each triangular region of the three-level space vector plane in Fig. 3, there will be different formulas for finding these application times as per SVPWM [38]. Calculation of T_k with these formulas may turn out to be a complex process for implementation using a microprocessor if a generalized approach is not followed. It can be observed from Fig. 3 that the set of nearest three vectors of V^* along with their timings is the same as that for V'' in an imaginary two-level space vector plane contained by hexagon ODCBIH. Furthermore, the combination of V'' and hexagon ODCBIH is similar in geometry to that of V' and inner hexagon FEDAHG. Thus, for easy calculation of T_k during a complete switching cycle period $(2T_s)$ in triangle ACB, the outer hexagon ODCBIH containing the tip of the vector V^* is mapped into the inner hexagon FEDAHG. This makes triangle ACB to be mapped into triangle ODA. By this process, V^* in the original space vector plane (or V'' in hexagon ODCBIH) is mapped into V' inside the hexagon FEDAHG for the example shown here. Similarly, every outer hexagon and outer triangle of Fig. 3 can be mapped into the inner hexagon and respective triangle to compute T_k easily [22]. As these timings (equivalent to a voltage controlled space vector strategy) are used further to calculate the current error boundary, the proposed current controller in the steady-state condition is also able to exhibit optimal switching sequence and maintain the switching frequency in and around $1/2T_s$.

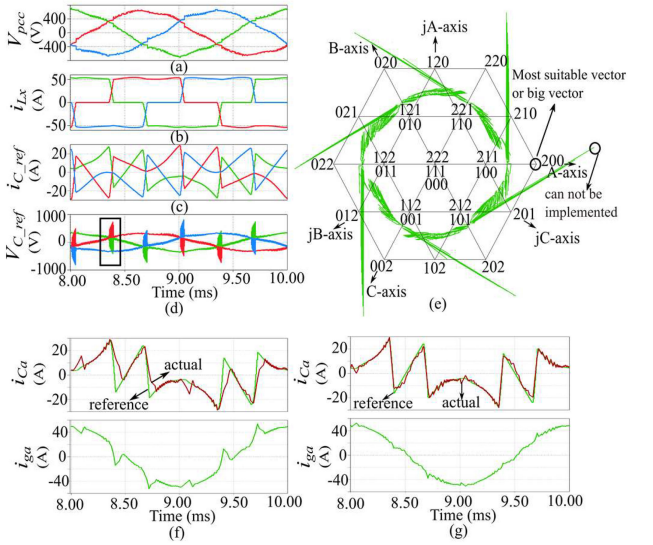

Fig. 4. Compensation of a DBR along with DG. (a) PCC phase voltages, $V_{\rm pcc}$. (b) DBR load currents, i_{Lx}. (c) Reference current to transmit PV power and to simultaneously compensate reactive and harmonic current components of DBR, $i_{C\_\rm ref}$. (d) Inverter reference voltage to produce reference current, $V_{C\_\rm ref}$. (e) Space vector of inverter reference voltage upon space vector structure. (f) Current tracking without applying big vectors (i.e., with limit on (dI*/dt)). (g) Current tracking with application of big vectors.

IV. Compensation of Nonlinear Load By Using "Big Vectors"

In the implementation of the SVHCC, if V^* is inside the space vector structure, then for every switching cycle period, proper vectors for switching can be chosen, and the appropriate current error boundary can be constructed. However, sometimes, the vector V^* in (1) can go out of space vector structure during the instants when the rate of change of reference current is high. This situation is illustrated in Fig. 4 through simulated waveforms. Under a certain load condition, Fig. 4(a) shows the PCC phase voltages (having a total harmonic distortion (THD) of 4.5%), and Fig. 4(b) shows the current drawn by the non-linear load [diode bridge rectifier (DBR)] at the PCC. Fig. 4(c) shows the reference current generated by the *pq* theory, as described in Fig. 2. For supplying this reference current, the required reference voltage for the inverter is calculated using (1) and is shown in Fig. 4(d). From Fig. 4(d), the corresponding locus of the tip of the reference voltage vector V^* on space vector plane is determined and shown in Fig. 4(e). From this figure, it can be observed that in a fundamental cycle, on six occasions [during commutation intervals of DBR], the vector V^* moves out of the space vector structure and enters into the deep overmodulation zone. Hence, in Fig. 4(e), during commutation intervals, V^* cannot be adequately mapped into an inner triangle of the standard SVHCC technique. In order to solve this problem, the rate of change of current reference needs to be limited such that V^* remains in the same triangle during the entire commutation interval. However, it causes ineffective tracking of reference current [as shown in Fig. 4(f)]. Hence, to improve the tracking, six particular vectors are applied during every commutation period and let those six particular vectors be termed as "big vectors." For example,

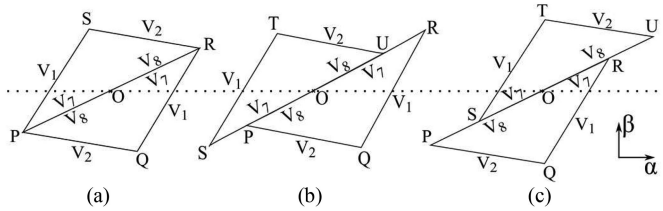

Fig. 5. Movement of current error space vector on the $\alpha\beta$ plane when V′ is at centroid of mapped sector 1. (a) No NP voltage balance of earlier reported SVHCC (equal boundaries for redundant vectors) [17], [22]. (b) Proposed SVHCC with NP voltage balance and $x < 0.5$. (c) Proposed SVHCC with NP voltage balance and $x > 0.5$.

during the commutation period highlighted in Fig. 4(d) and associated trajectory in Fig. 4(e), V^* enters into the triangle formed by the vectors 101, 212, 201, and 202 and then goes out of the space vector structure. One option to avoid such deep overmodulation is to set an appropriate limit on dI^*/dt term in (1) such that V^* is synthesized by the same vectors (101, 212, 201, and 202) of the present triangle. However, this leads to ineffective tracking of the reference current, which further results in higher distortion in the compensated grid current, as shown in Fig. 4(f). From Fig. 4(e), it is worth noticing that the nearest vector during commutation is 200 (one of the six big vectors), and application of that vector during the commutation interval results in improved tracking of the reference current. Similarly, during other commutation intervals, corresponding nearest big vector can be identified and applied to improve the tracking of the reference current for SAPF operation of the inverter. After the completion of the commutation period, the current controller switches back to the steady-state SVHCC technique (that maintains optimal switching sequence similar to that of a conventional voltage controlled SVPWM). The overall improved reference current tracking performance (both in steady-state and transient conditions) is shown in Fig. 4(g).

V. Proposed NP Balancing Method

In the existing SVHCC [22], the application sequence of the vectors is V_8, V_2 , V_1, and V_7 for half the PWM switching cycle (T_s), and for the remaining half cycle, the sequence is reversed, i.e., V_7, V_1, V_2, and V_8. Here, the vectors V_7 and V_8 are redundant vectors with equal application time, i.e., $T_7 = T_8 = 0.5T_z$, where T_z represents the total application duration of the redundant vectors in T_s [22]. With this equal application time for redundant vectors, the trajectory of ΔI is shown in Fig. 5(a). For the case when the tip of the vector V′ is located at the centroid of the mapped sector 1 (as shown in Fig. 3), the trajectory segments are given in Table I. However, with this conventional modulation, in an NPC structure, the balancing of NP voltage cannot be ensured (due to the presence of power circuit nonidealities, control delays, dead-time effect, unequal equivalent series resistances of capacitors, etc.), and thus, asymmetry in the output voltage waveforms creeps in.

To maintain NP voltage at the desired value (i.e., half the dc-link voltage), the estimated application durations of the redundant vectors (T_7 and T_8) are adjusted online in a unique

TABLE I
TRAJECTORY OF CURRENT ERROR VECTOR

Applied vector V_k	Time	SVHCC of [22] Vector timing T_k	SVHCC of [22] ΔI trajectory	Proposed SVHCC Vector timing T_k	Proposed SVHCC ΔI trajectory
V_8	T_s	$T_8 = 0.5T_z$	OP	$T_8 = xT_z$	OP
V_2		T_2	PQ	T_2	PQ
V_1		T_1	QR	T_1	QR
V_7		$T_7 = 0.5T_z$	RO	$T_7 = (1-x)T_z$	RO
V_7	T_s	$T_7 = 0.5T_z$	OP	$T_7 = (1-x)T_z$	OS
V_1		T_1	PS	T_1	ST
V_2		T_2	SR	T_2	TU
V_8		$T_8 = 0.5T_z$	RO	$T_8 = xT_z$	UO

TABLE II
VOLTAGE VECTOR SELECTION LOGIC IN MAPPED SECTOR 1

Present Vector	Previous Vector	Next Vector: SVHCC of [22] (Boundaries defined along jA, jB and jC axes) if $(ji_A - ji_A^*) \geq 0.5$ $\Delta i_{1(jA)}$	if $(ji_C - ji_C^*) \geq 0.5$ $\Delta i_{2(jC)}$	if $(ji_B - ji_B^*) \geq 0.5$ $\Delta i_{z(jB)}$	Proposed SVHCC (changes in jB axis only) if $(ji_B - ji_B^*) \geq 0.5$ $x\Delta i_{z(jB)}$	if $(ji_B - ji_B^*) \geq 0.5$ $(1-x)\Delta i_{z(jB)}$
V_1	V_7	V_2	-	-	-	-
	V_2	V_7	-	-	-	-
V_2	V_8	-	V_1	-	-	-
	V_1	-	V_8	-	-	-
V_7	-	-	-	V_1	-	V_1
V_8	-	-	-	V_2	V_2	-

way for modifying the current error boundary. For this purpose, T_7 and T_8 are calculated at the beginning of every switching cycle with an objective of achieving zero average NP current in the least possible time. However, total application duration of the redundant vectors should remain unchanged (i.e., $T_7 + T_8 = T_z$) in this process. Considering x to be the fraction of duration during which the vector V_8 is applied, new timings are $T_8 = xT_z$ and $T_7 = (1-x)\,T_z$ with

$$0 \leq x \leq 1. \tag{6}$$

Also, at the starting of every PWM switching cycle, the mapped sector and actual vectors (along with their indices as shown in the space vector structure) to be applied can be easily identified [22]. With these known switching vectors and sensed load current, the NP currents associated with the switching vectors can be calculated. Now, let i_{N1}, i_{N2}, i_{N7}, and i_{N8} be the NP current for vectors V_1, V_2, V_7, and V_8, respectively. It is worth noting that $i_{N7} = -i_{N8}$. Hence, the average neutral current in a duration of $2T_s$ can be calculated as

$$i_{N\_\text{avg}} = \frac{i_{N8}x2T_z + i_{N2}2T_2 + i_{N1}2T_1 + i_{N7}\,(1-x)\,2T_z}{2T_s}. \tag{7}$$

Now, the average NP current is

$$i_{N\_\text{ref}} = \frac{-C\,(V_{C1} - V_{C2})}{2T_s} \tag{8}$$

where $C = C_1 = C_2$ (in Fig. 1). By equating i_{N_avg} to i_{N_ref} (i.e., nullification of NP voltage deviation is targeted in next $2T_s$ time), the following relationship can be written:

$$x = 0.5 - \frac{(i_{N1}T_1 + i_{N2}T_2) + 0.5C\,(V_{C1} - V_{C2})}{2i_{N8}T_z}. \tag{9}$$

The value of x is calculated once for every $2T_s$ time period and is kept under limits as given in (6). Upon using $T_8 = xT_z$ and $T_7 = (1-x)\,T_z$, the new shape of the current error trajectory as achieved by the modified SVHCC is shown in Fig. 5(b) and (c) for $x < 0.5$ and $x > 0.5$, respectively. The sequence of vectors, their approximate timings, and the trajectory of ΔI for the case shown in Fig. 5 are shown in Table I, which highlights the required changes during the application of vectors contributing to NP voltage balancing as compared to that of the earlier SVHCC (without NP voltage-balancing feature). Although the sequence of applied vectors remains unchanged, the difference lies in the distribution of T_7 and T_8 in T_s. As a result, the current error space vector structure may become a little skewed, as shown in Fig. 5(b) and (c). However, in all steady-state cases, the current error vector comes back almost to zero position ("O") at the end of every PWM switching cycle. Hence, the proposed modified SVHCC method achieves tracking of the reference current along with NP voltage balance. Table II presents the difference in the logic for selecting the voltage vectors between the existing SVHCC and the modified SVHCC. As observed from this table, the main difference lies in the length of the current error boundary along the orthogonal axis, pointing toward redundant vectors on the space vector plane. For mapped sector 1 in Table II, the *jB* axis is in the direction of the redundant vectors.

VI. RESULTS AND DISCUSSION

A. Simulation Results

The inverter system, as shown in Figs. 1 and 2, has been simulated for both DG and DG + SAPF operation using MATLAB/Simulink 2019b environment using the parameters given in Table III.

Fig. 6 shows few waveforms obtained by simulation studies when the inverter is acting as a DG only. Fig. 6(a) and (b) shows the *a*-phase grid current and inverter output line-to-line voltage, respectively. Fig. 6(c) shows the index of applied voltage vectors [22], which indicates an optimal and controlled way of switching. It is worth noting that the sequence of the applied vectors is similar to that of a conventional SVPWM technique. The fast Fourier transform (FFT) of the line-to-line voltage in Fig. 6(b) indicates a concentration of switching harmonics in and around the designed 10-kHz frequency.

The simulation results for a combined DG + SAPF operation of the system, with the application of big vectors for compensating DBR load, are shown in Fig. 7(a). As can be seen from this figure, up to 0.1 s, the NPC inverter supplies all the harmonic components of the current of the nonlinear load. Simultaneously, it also injects the harvested solar PV power into the PCC. As this

TABLE III
SYSTEM PARAMETERS

Symbol	Description	Simulation parameters	Hardware parameters
V_{pcc}	Supply voltage at PCC (line-line)	400 V rms	100 V rms
f_s	Supply frequency	50 Hz	50 Hz
C_1, C_2	dc-link capacitance	1000 μF	2200 μF
V_{dc}	dc-link nominal voltage	800 V	200 V
L_f	Filter inductance	4 mH	3.85 mH
L_b	Boost converter inductance	4 mH	5 mH
C_{pv}	PV array filter capacitance	70 μF	220 μF
f_b	Boost converter switching frequency	20 kHz	5 kHz
$2T_s$ $(1/2T_s)$	PWM modulation period (designed switching frequency)	100 μs (10kHz)	100 μs (10kHz)

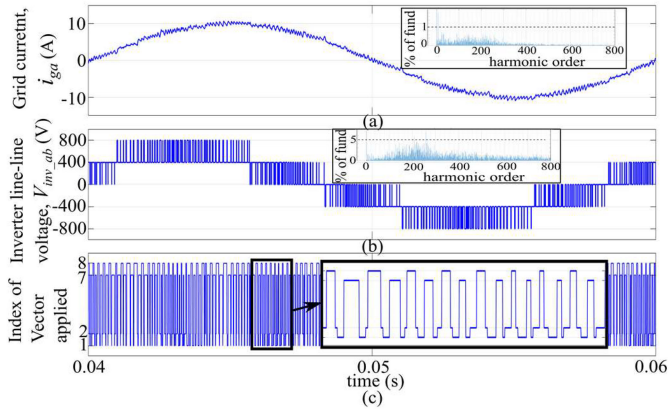

Fig. 6. Simulation results when the system is acting as DG only. (a) Grid current i_{ga}. (b) Inverter line–line voltage $V_{\mathrm{inv\_}ab}$. (c) Index of the vector applied.

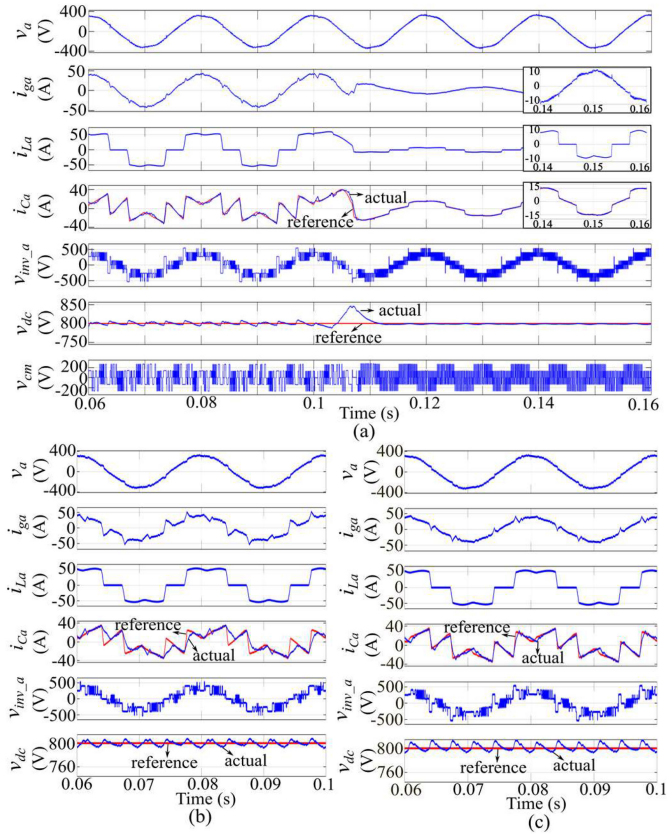

Fig. 7. Simulation results obtained for DG + SAPF operation of the system (PCC phase voltage v_a , grid current i_{ga}, load current i_{La}, reference and actual converter currents i_{Ca}, inverter phase voltage $V_{\mathrm{inv\_}a}$, reference and actual dc-link voltage V_{dc}, and inverter common-mode voltage V_{cm}) for (a) DBR load while applying big vectors and (b) TBR load (firing angle 10°) without applying big vectors and (c) with applying big vectors.

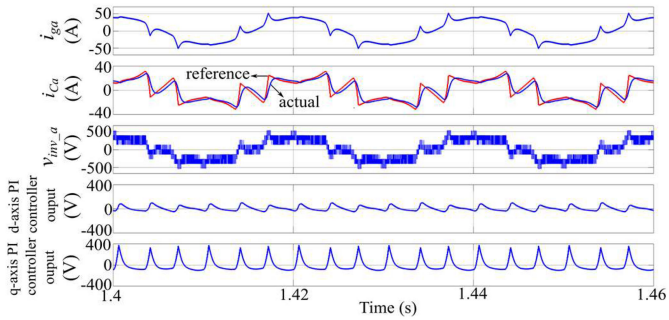

Fig. 8. Simulation results obtained for DG + SAPF operation of the system with DBR load for VOC (where the PI controller is used with an antiwindup strategy): grid current i_{ga}, reference and actual converter currents i_{Ca}, inverter phase voltage $V_{\mathrm{inv\_}a}$, and output of the d- and q-axis PI controllers.

PV power is less than the power requirement of the nonlinear load, net power flows from the grid to the PCC with a nearly sinusoidal waveform at unity power factor. At 0.1 s, there is a sudden drop in the nonlinear load current, and as a result, the flow of power reverses, i.e., from the PCC to the grid. In both of these cases, the grid current is maintaining unity power factor with a nearly sinusoidal waveform because of the successful operation of the active power filter. It is worth noting that the application of the big vectors ensured the successful operation of the active power filter, as shown in Fig. 7(a). A combined DG + SAPF operation of the system, while compensating Thyristor bridge rectifier (TBR) load (with 10° firing angle), is shown in Fig. 7(b) and (c) for the cases of without and with application of big vectors. As can be observed from these figures, distortion in compensated grid current is improved with the application of big vectors. For comparison purpose, a simulation study has been carried out by applying conventional voltage-oriented control (VOC) (where the PI controller is used with an antiwindup strategy), and corresponding results are shown in Fig. 8. For determining the optimal values of proportional and integral gains of the PI controllers, software simulation studies have been carried out with a wide range of controller parameters. It can be observed from Figs. 7(a) and 8 that even though PI controllers are not saturated, the current tracking is inferior in VOC with respect to the SVHCC. This is due to the inherent slower behavior of PI controllers in tracking a fast changing reference signal. In fact, the THD of the compensated grid current is found to be 25.2%, and thus, it will be very difficult to maintain the THD below 5% using the lower size filter used in the proposed article.

Fig. 9. Experimental setup for implementing the SVHCC technique for the three-level NPC inverter for DG and SAPF application.

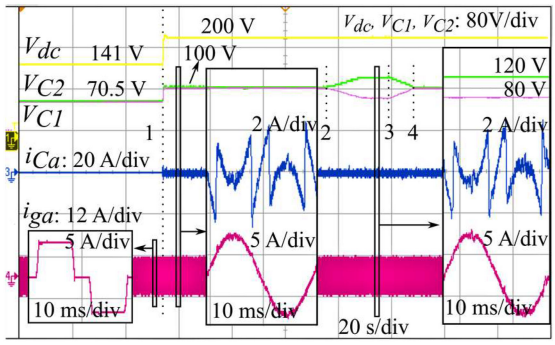

Fig. 10. Experimental results for SAPF operation along with dc-link NP balancing while compensating DBR load: [Instant 1: Turn-ON of converter modulation with the NP voltage-balancing method enabled; Instant 2: NP voltage-balancing method disabled (Now, $V_{C1}$and V_{C2} start deviating and settle at unequal values); Instant 3: Re-enabling of the NP voltage-balancing method; Instant 4: $V_{C1}$and V_{C2} settle back at half the dc-link voltage].

As it may be difficult to perceive the effect of the NP voltage-balancing issue properly in a simulation environment, the study on the proposed NP voltage-balancing technique is demonstrated only through hardware results. Although available zero-sequence voltage addition techniques are helpful for voltage-controlled PWM methods, the proposed NP balancing technique may be recommended strongly for the grid-connected systems, where current control is a mandatory requirement.

B. Experimental Results

Fig. 9 shows the experimental setup implementing the system considered in Fig. 1. The parameters of the experimental setup are shown in Table III. Semikron-make power semiconductor switches (insulated-gate bipolar transistor modules), diodes, DBR, and gate drivers have been used in the experimental setup. The switching signals for the converter are generated using the DSP microcontroller TMS320F28379D from Texas Instruments. PV array characteristic is emulated using a PV emulator (Chroma model 62100H-600S). A DBR is considered as the typical nonlinear load. The current error boundaries are calculated at every 50 μs, and boundary crossings are checked at every 6 μs. As would be demonstrated, the proposed SVHCC technique not only is able to contain the wide variation of switching frequency but also ensures optimal switching pattern of vectors.

An overview of experimental results is presented here. Fig. 10 and Fig. 11 demonstrate the successful implementation of the proposed NP voltage-balancing technique while the inverter is acting as the SAPF and DG+SAPF, respectively. Fig. 12 demonstrates the dual operation as DG + SAPF when the net power is supplied from the grid to the PCC without applying big vectors, and the THD is not within acceptable limits. Fig. 13 compares the current tracking capability between two cases: first, when no big vector is applied, and second, when big vectors are applied. The improved tracking results with better THD performance are shown in Fig. 14. Finally, Fig. 15 demonstrates the dual operation as DG + SAPF, where the net power flows

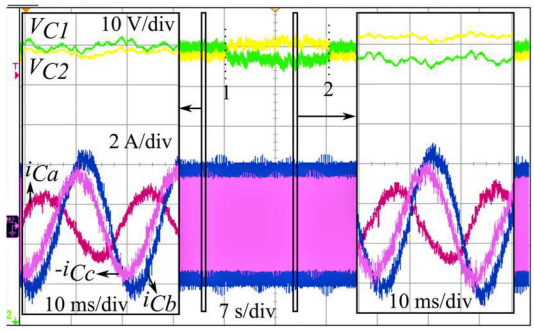

Fig. 11. Experimental results for DG + SAPF operation along with dc-link NP voltage balancing while compensating unbalanced linear load: [Instant 1: NP voltage-balancing method disabled (V_{C1} and V_{C2} start deviating and settle at unequal values); Instant 2: Re-enabling of the NP voltage-balancing method (V_{C1} and V_{C2} settle back at half the dc-link voltage).

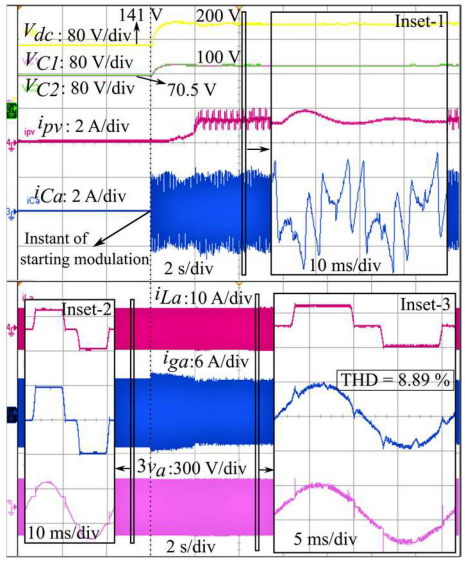

Fig. 12. Experimental results for DG + SAPF operation without applying big vectors: dc-link voltage $V_{\rm dc}$, dc-link capacitor voltages V_{C1} and V_{C2}, PV array current $i_{\rm pv}$, and system's a-phase converter current i_{Ca}, load current i_{La}, grid current i_{ga}, and thrice the PCC phase voltage v_a.

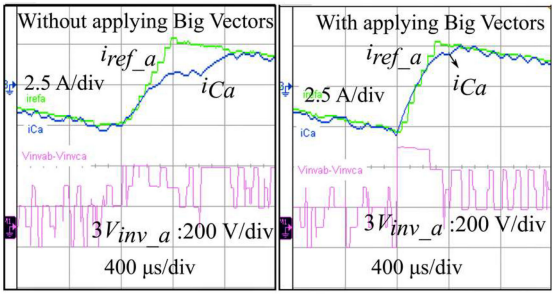

Fig. 13. Experimental results: Comparison of current tracking during same commutation interval for without and with applying big vector.

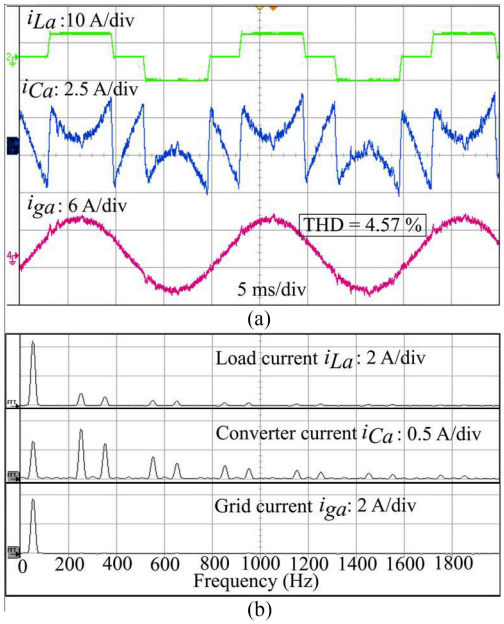

Fig. 14. Experimental results with applying big vectors. (a) a-phase's load current i_{La}, converter current i_{Ca}, and grid current i_{ga}. (b) Harmonic spectrum of currents.

from the PCC to the grid (grid current is out of phase with PCC voltage).

The NP voltage balancing achieved by the proposed technique in addition to SAPF operation of the inverter while compensating a DBR load is shown in Fig. 10 (with an indication of four time instants). Before instant 1 in this figure, the NPC inverter remained unoperational and the dc-link voltage $(V_{\rm dc})$ is settled at 141 V (peak value of the PCC line-to-line voltage) with equal voltage sharing between the top and bottom capacitors, whereas grid current (i_{ga}) is equal to DBR load current. At instant 1, the converter modulation incorporating the proposed NP balancing technique is started, and this raises $V_{\rm dc}$ to its reference value of 200 V. Furthermore, V_{C1} and V_{C2} are also maintained at 100 V approximately. Also, i_{Ca} follows its reference and, thus, makes i_{ga} sinusoidal in shape. To illustrate the effectiveness of the proposed technique further, the NP balancing algorithm is disabled at instant 2, and this results in a deviation of V_{C1} and V_{C2} (which subsequently settles at 80 and 120 V, respectively, as shown in this figure). It is worth noting that even when dc-link

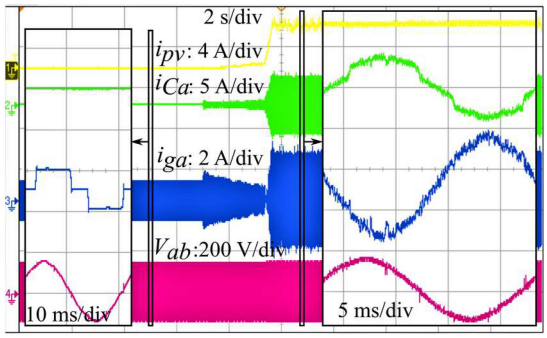

Fig. 15. Experimental results with applying big vectors and for the case of net power being supplied from the PCC to the grid: PV array current $i_{\rm pv}$, converter current i_{Ca}, grid current i_{ga}, and PCC line voltage v_{ab}.

capacitor voltages are unequal, i_{Ca} and i_{ga} do not deviate from their desired wave shape. However, at instant 3, the NP voltage-balancing algorithm is again enabled, and thus, V_{C1} and V_{C2} are made equal before instant 4.

The NP voltage balancing is also achieved for DG + SAPF operation while compensating an unbalanced linear load, and the inverter currents are shown in Fig. 11. Before instant 1 in this figure, the proposed NP voltage-balancing technique was activated, and V_{C1} and V_{C2} are maintained almost at 100 V with a maximum difference of 2 V due to voltage ripple. At instant 1, the NP voltage-balancing technique is disabled, and hence, a higher voltage deviation of maximum 8 V is observed (expanded view is shown in Inset 2). At instant 2, the NP voltage-balancing technique is enabled again.

Fig. 12 shows waveforms for DG + SAPF operation without the application of big vectors. It shows the transient and steady-state behavior of the dc-link voltages, PV array current, a-phase system currents, and a-phase PCC voltage when net real power is supplied from the grid to the PCC. As observed in this figure, the converter operation is started at the third vertical grid line of the scope display. Before this instant, the converter current i_{Ca} as well as the PV array output current $i_{\rm pv}$ remains at zero, and the DBR load is supplied by the grid only. Thus, the grid current i_{ga} is equal to the load current i_{La} as shown in Inset 2 of this figure. When both the NPC inverter and the boost converter are activated, PV power starts getting harvested, and also, the converter current starts following its reference. The dc-link voltage $V_{\rm dc}$ attains its reference value of 200 V (with NP voltage control). Zoomed view of the steady-state operation is shown in insets 1 and 3 of Fig. 12. It is also seen that i_{ga} became almost sinusoidal and is in phase with the a-phase PCC voltage v_a (derived as $v_{ab} - v_{ca} = 3v_a$ as the NP is not accessible). This indicates that the dual-purpose inverter successfully transfers real power from the PV array to the PCC as well as supplies the required reactive and harmonic components of the nonlinear load current to the PCC. However, the current i_{ga} in Fig. 12 has a THD of 8.89%, which is quite high. The reason for this high THD is the inability of the line current to follow the corresponding reference waveform faithfully in the absence of big vectors, as shown on the left side of Fig. 13. However, with the application of big vectors, the line current

TABLE IV
COMPARISON OF FREQUENCY COMPONENTS IN GRID CURRENT

i_{ga} Harmonic order	Without applying big vectors	With applying big vectors
1	100 %	100 %
5	5.17 %	1.27 %
7	5.47 %	1.25 %
11	3.25 %	1.00 %
13	4.00 %	1.50 %
17	2.05 %	1.05 %
19	3.72 %	1.32 %

follows the corresponding reference waveform quite faithfully (as shown on the right side of Fig. 13), which, in turn, reduces the THD substantially. Fig. 14, which shows some representative waveforms in the presence of big vectors, corroborates this.

As shown in Fig. 14(a), with the application of big vectors, the THD reduced to 4.57% from 8.89% in Fig. 12. Fig. 14(b) shows the FFT spectrum of system currents. The low-order harmonics present in grid current for both the cases (without and with the application of big vectors) are compared in Table IV. This comparison highlights the reduction of specific harmonic components due to the fast-tracking ability of the proposed controller. In a different scenario, Fig. 15 demonstrates the steady-state waveforms for DG + SAPF operation when the generated PV power is higher than the real power drawn by DBR load. The excess power is seen feeding the grid at unity power factor because the grid current (i_{ga}) lags the PCC line voltage (v_{ab}) by 210°.

VII. CONCLUSION

In this article, a popularly used three-level NPC inverter is employed as a dual-purpose inverter for integrating DG to the grid as well as for shunt active power filtering. Although several zero-sequence voltage addition techniques are being used in voltage-controlled PWM methods for different applications, this work uses a new current-controlled PWM scheme, which is equipped with unique NP balancing technique and a fast-acting current tracking ability (by utilizing the "big vectors"). The inherent advantages of the existing SVHCC are also retained. In order to maintain the neutral voltage balancing in the dc link, a simple technique is also proposed by skewing the computed boundary in an innovative way. The performance of the current controller has been investigated extensively under different operating conditions in the presence of nonlinear loads. The issue of ineffective compensation of nonlinear load is solved effectively by the proposed fast-acting SVHCC. The proposed improved current controller with a dual-purpose inverter can provide a smart solution in an ac microgrid application.

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