A High Step-Up/Step-Down LVS-Parallel HVS-Series ZVS Bidirectional Converter With Coupled Inductors

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***Abstract*—This article introduces a nonisolated bidirectional converter with high-voltage conversion ratio. In the proposed converter, by integrating the two-phase low-voltage-side (LVS)-parallel high-voltage-side (HVS)-series bidirectional converter with the coupled inductors, features, such as high voltage gain, low voltage stresses, current sharing, and current ripple cancelation, are achieved. Due to the proposed converter's operation in triangular conduction mode, the desirable benefits of zero voltage switching, diode reverse recovery elimination, and reduction of converter filter inductors and, consequently, leakage inductors are obtained. To recycle the leakage inductors' energy and to solve the related difficulties for both operation modes, a simple passive clamp with the minimum number of elements is utilized. Also, to improve the light-loads' efficiency, the variable frequency control is developed. The proposed converter is comprehensively analyzed, and to verify the analysis, the experimental results are provided.**

***Index Terms*—High step-up/step-down converter, low-voltage-side (LVS)-parallel high-voltage-side (HVS)-series converter, nonisolated bidirectional converter (BDC), zero voltage switching (ZVS).**

I. Introduction

In THE past decades, the development of renewable energy systems, hybrid/electric vehicles (EVs/HEVs), and uninterruptible power supplies (UPSs) is among the most attractive topics in power electronics. The dc–dc bidirectional converters (BDCs) are one of the key components in such applications [1]–[3] with the important functions of managing the charge and discharge of batteries and handling the voltage difference between batteries and the dc bus. Applying the battery cells in series connection is usually avoided due to the difficulties, such as charge imbalance between the series battery cells and the need for additional battery voltage-balancing circuits [4]. As a solution, the high step-up/step-down BDCs are utilized to match the low-voltage battery with the high-voltage dc bus.

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Compared with unidirectional high step-up or high step-down converters, the design of high step-up/step-down BDCs faces more challenges, due to two operation modes in opposite directions. Since the low-voltage-side (LVS) source is commonly batteries, providing the continuous-nonpulsating LVS current with a low ripple to maintain the battery lifetime is necessary [5]. Furthermore, the current level of LVS is high, and important issues, such as conduction losses and thermal management, should be taken into consideration.

The LVS-parallel high-voltage-side (HVS) series structures are among the most favorable circuit structures to address the aforementioned challenges [6]. In these structures, the converter is normally based on parallel-interleaved converters to obtain excellent features, such as current sharing and current ripple cancelation. Moreover, each phase's HVS terminals are electrically placed in series to increase the voltage gain and reduce the components' voltage stress.

In a general classification, the BDCs can be divided into isolated BDCs and nonisolated BDCs. In isolated converters, the converter transformer processes all the output power, which causes increased transformer volume and losses. Moreover, many of the isolated topologies, such as dual-active-bridge converters, as the most common structure of isolated BDCs, require high number of active switches [7], [8]. Hence, when isolation is not a requirement, nonisolated BDCs are usually preferred.

Utilizing the coupled inductor with the converter filter inductor (i.e., coupled filter inductor) is the most common method to increase the voltage gain in nonisolated BDCs [9]–[20], and is also common in nonisolated unidirectional structures [21]. This method is also integrated with other switched-capacitor circuits to increase the voltage gain and recycle the leakage inductor energy [9]–[18]. In these converters, unlike the isolated BDCs, only a portion of output power is processed through the coupled inductors. Besides, as the magnetizing inductor of the coupled inductors plays the filter inductor's role, the core reset is not an issue. In the BDCs with coupled filter inductor, by properly controlling the converter, the leakage inductor energy could be utilized to achieve zero voltage switching (ZVS) [10]–[18].

The general drawback of BDCs with coupled filter inductor is the large current ripple and/or pulsating state of LVS current due to the coupled inductor on the converter filter inductor [10]–[19]. As a solution, it is necessary to utilize the bulky low-pass filter on

the converter's high-current LVS, which increases the converter volume and conduction losses [9]. Shaneh *et al.* [20] introduce a two-phase interleaved structure with current ripple cancelation featuring the continuous-low-ripple current on LVS. However, recycling the leakage inductors' energy is the main issue in this converter, which is solved with many auxiliary components, including four separate clamp circuits without achieving ZVS condition. In [22] and [23], the single-phase BDCs with coupled filter inductor are introduced, featuring low LVS current ripple. However, these converters suffer from limited voltage gain since the coupled inductors are merely utilized to obtain current ripple cancelation, and the voltage gain is independent of the coupled inductors' wingdings turn ratio.

In high step-up/step-down BDCs with coupled inductors proposed in [24]–[29], the coupled inductors are implemented separately from the converter filter inductor (i.e., built-in transformer). Therefore, the LVS current benefits from continuous state and low ripple. Besides, in [24]–[26], this method is utilized with the parallel-interleaved structure. However, in [29], the voltage stress of all switches are more than the voltage level of HVS, and BDCs in [27] and [28] suffer from limited voltage gain. Moreover, despite the benefits of proposed converters in [24]–[26], they utilize high number of components, including eight [24], [25] and six [26] active switches.

In BDCs [30]–[42], the high voltage gain is obtained without using the coupled inductors, and thus, the related mentioned issues with the coupled inductors do not exist in these converters. These converters are based on integrating the basic BDCs with the switched-capacitor or quasi-Z-source circuits [31]–[42]. Generally, the voltage gains of these converters are limited, and to increase the voltage gain, additional circuit cells are required [32], [33], which increases the converter's volume. This is in contrast with the coupled inductors BDCs, where the voltage gain could be increased by increasing the windings turns ratio, considering the value of the leakage inductor and the associated issues. Besides, the pulsed current related to parallel unbalanced voltage capacitors in switched-capacitor circuits should be addressed as it requires the large value capacitors to alleviate this issue [33]–[42]. The other drawback of these converters is that most of them are hard switched [31]–[42]. This issue limits the converter switching frequency, especially when the conventional silicon MOSFETs are utilized as their body diodes commonly suffer from the large reverse recovery time [43], [44]. It is worth mentioning that in BDCs, the antiparallel diodes of switches mostly operate as the converter main diodes.

The triangular conduction mode (TCM) operation is among the simplest methods to obtain soft switching in BDCs [22], [45], [46]. In this method, the main inductor of the converter is designed small enough such that its current flows in both directions. This way, ZVS condition, elimination of diodes-reverse-recovery losses, and reduction of main inductances can be obtained [22]. However, due to the large current ripple of main inductors, both the converter's conduction losses and core losses are increased. These losses are almost constant regardless of the output power in fixed-frequency operation; hence, the value of these losses would be dominant in light loads, results in dropped efficiency in this region [22]. Moreover, the regular BDCs with single-phase structure in TCM suffer from a large current ripple on the LVS source [45].

This article introduces a two-phase LVS-parallel HVS-series TCM BDC with coupled inductors to address the existing solutions' issues. Thanks to the LVS-parallel HVS-series structure, the current sharing is achieved, voltage gain is increased, and the voltage stresses are reduced. Furthermore, the coupled inductors' secondary windings are jointly implemented on the common path of two phases in the form of winding-cross-coupled inductors (WCCIs) [47]. As a result, excellent voltage gain and current ripple cancelation are achieved utilizing a minimum number of windings. Due to TCM operation and current ripple cancelation, ZVS and elimination of the diodes-reverse-recovery losses are obtained without a large current ripple on the LVS side. Moreover, the converter inductors' values, including the leakage inductors' values and the associated issues, are reduced. To completely solve the leakage inductors' difficulties in two phases and both boost and buck operation modes, a simple passive clamp circuit with the minimum number of elements is applied. Furthermore, to reduce losses related to TCM operation in light loads, variable frequency control (VFC) is adopted in the proposed converter.

The rest of this article is organized as follows. Section II describes the circuit configuration and operation principles of the proposed converter. The proposed converter specifications are discussed in Section III. Section IV provides the design considerations. In Section V, the experimental results, loss analysis, and comparison are presented. Finally, Section VI concludes this article.

II. Circuit Configuration and Operation

Fig. 1(a) shows the circuit configuration of the proposed converter. The converter circuit comprises two phases in which the LVSs of phases are parallel, and the HVSs (V_{H1} and V_{H2}) are series. The upper phase comprises of the inductor L_1, the LVS switch S_1, HVS switch S_3, and the HVS capacitor C_{H1}. The lower phase includes the inductor L_2, the LVS switch S_2, HVS switch S_4, and the HVS capacitor C_{H2}. Besides, the capacitors C_{S1}–C_{S4} are the snubber capacitors of switches. To increase the voltage gain and obtain the current ripple cancelation, the secondary windings of coupled inductors (L_3 and L_4) are inserted in the common path of two phases, in the crossed form. The secondary windings of coupled inductors L_3 and L_4 contribute to increasing the voltage gain of both phases. This leads to a reduced number of coupled inductor windings compared to other existing converters with WCCIs [47].

The proposed converter also includes a simple passive clamp circuit, which composes a single clamp capacitor C_C and three diodes D_{C1}, D_{C2}, and D_{C3}. The passive clamp has the role of limiting the voltage of the switches S_1 and S_2 at both the boost and buck operation modes. Otherwise, during the turn-OFF instants of S_1 and S_2, the stored energy in the leakage inductors is depleted through a resonance with switch output capacitors, causing an undesirable voltage spike on S_1 and S_2.

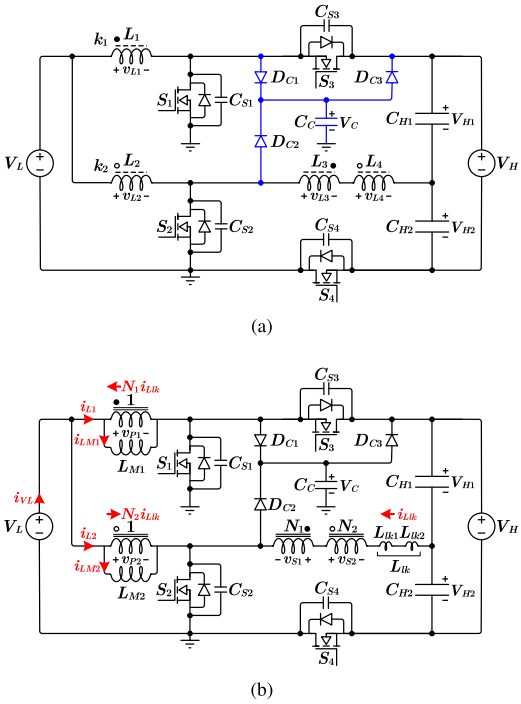


Fig. 1. (a) Circuit structure of the proposed converter. (b) Equivalent circuit of the proposed converter.

A pair of coupled inductors L_1 and L_2 with coupling coefficient k, as shown in the Appendix, can be modeled with an ideal transformer with turn ratio N ($N = k\sqrt{L_2/L_1}$), a magnetizing inductor (L_M) on the primary side ($L_M = L_1$), and a leakage inductor (L_{lk}) on the secondary side ($L_{lk} = (1-k^2)L_2$). Fig. 1(b) illustrates the equivalent circuit of the proposed converter using the model. It is worth mentioning that, in the equivalent circuit of the proposed converter, the magnetizing inductors L_{M1} and L_{M2} act as the converter filter inductor. Also, the series leakage inductors (L_{lk1} and L_{lk2}) can be replaced with an equivalent leakage inductor L_{lk} ($L_{lk} = L_{lk1} + L_{lk2}$).

The proposed converter has two overall operation modes of boost and buck modes, based on whether the power flow direction is from V_L to V_H or vice versa. Also, each operation mode includes 12 operating intervals, which are discussed below comprehensively. In the analysis, the following assumptions are considered.

1) The converter is in the steady-state condition.
2) The values of the windings turn ratios are equal ($N_1 = N_2 = N$).
3) The converter operates in TCM (the values of magnetizing inductors L_{M1} and L_{M2} are small enough such that their currents flow in both directions).
4) The values of the HVS capacitors C_{H1} and C_{H2} and also the clamp capacitor C_C are large enough that their voltages are constant in a switching cycle.
5) The voltage drop of the diodes D_{C1}, D_{C2}, and D_{C3} during the forward biased condition are equal and defined as $V_{D,\mathrm{ON}}$.

A. Boost Mode

In the boost mode, S_1 and S_2 are the main switches, and S_3 and S_4 act as the synchronous switches complementary to S_1 and S_2 with a proper deadtime. Also, two phases operate with interleaved pattern and there is a phase shift of 180° between them. The equivalent circuits of 12 operating intervals in boost mode and the theoretical key waveforms are illustrated in Figs. 2 and 3, respectively.

At the beginning of interval 1, it is assumed that the value of i_{LM1} is I_0, and i_{LM2} has a negative value of $-I_0'$. Also, it is assumed that S_1 is ON and the body diode of S_2 is conducting.

Interval 1 [t_0–t_1]*:* In this interval and by conducting the S_2 body diode, S_2 turns ON under ZVS. During this interval, the voltage of V_L is placed across L_{M1} and L_{M2}. Hence, i_{LM1} increases linearly and i_{LM2} reduces linearly in the negative direction as follows:

$$i_{LM1}(t) = I_0 + \frac{V_L}{L_{M1}}(t - t_0) \tag{1}$$

$$i_{LM2}(t) = -I_0' + \frac{V_L}{L_{M2}}(t - t_0). \tag{2}$$

In this interval, the currents of i_{LM1} and i_{LM2} conduct through S_1 and S_2, respectively, and there are no currents in the windings of the ideal transformers.

Interval 2 [t_1–t_2]*:* At t_1, S_1 turns OFF, and the snubber capacitors C_{S1} and C_{S3} start to charge and discharge, respectively, by means of i_{LM1}. Meanwhile, a resonance starts between L_{lk} and C_{S4} causes C_{S4} charging.

Interval 3 [t_2–t_3]*:* At t_2, C_{S1} is charged to V_C, D_{C1} is forward biased, and the voltage of C_{S1} is clamped on V_C. Hence, the resonance between L_{lk} and C_{S4} in interval 2 continues in this interval between L_{lk}, C_{S4}, and C_{S3}. During this resonance, C_{S3} is discharged from V_{H1} to zero and C_{S4} is charged from V_{H2} to $V_H - V_C$. At the end of this interval, the values of i_{LM1}, i_{LM2}, and i_{Llk} are defined I_1, $-I_1'$, and I_{K0}, respectively.

Interval 4 [t_3–t_4]*:* At t_3, S_3 body diode is forward biased. By conducting S_3 body diode, the synchronous switch S_3 turns ON under ZVS, and thus, the current of S_3 body diode conducts through S_3. In this interval, the voltage of $-(V_C + V_{D,\mathrm{ON}} - V_L)$ is placed across L_{M1}, and the voltage of L_{M2} is V_L as yet. Hence, the equations of i_{LM1} and i_{LM2} would be

$$i_{LM1}(t) = I_1 - \frac{V_C + V_{D,\mathrm{ON}} - V_L}{L_{M1}}(t - t_3) \tag{3}$$

$$i_{LM2}(t) = -I_1' + \frac{V_L}{L_{M2}}(t - t_3). \tag{4}$$

Also, the voltage of $(N+1)(V_C + V_{D,\mathrm{ON}}) - V_{H1}$ is placed across L_{lk}; hence, the equation of i_{Llk} is given by

$$i_{Llk}(t) = I_{K0} + \frac{(N+1)(V_C + V_{D,\mathrm{ON}}) - V_{H1}}{L_{lk}}(t - t_3). \tag{5}$$

At the end of this interval, the value of i_{Llk} is defined I_{K1}.

Interval 5 [t_4–t_5]*:* At t_4, the current of C_C reaches zero, and so, D_{C1} turns OFF. Then, the current of C_C increases in the negative direction through D_{C3}. In this interval, the voltages of L_{M1} and L_{M2} are $-(V_C - V_{D,\mathrm{ON}} - V_L)$ and V_L, respectively.

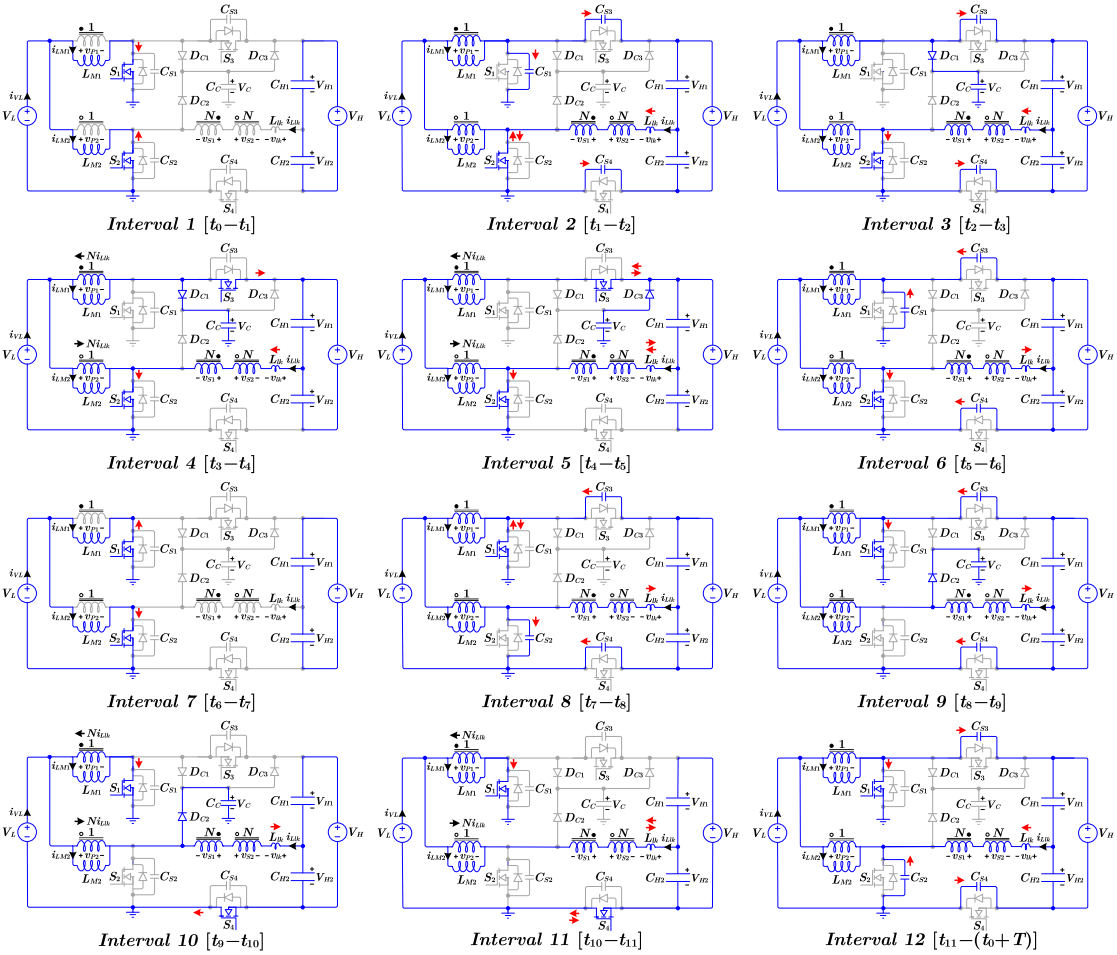


Fig. 2. Equivalent circuits of 12 operating intervals in boost mode.

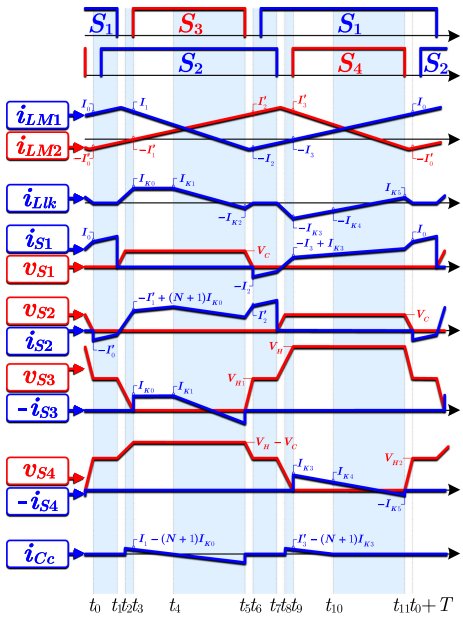


Fig. 3. Theoretical key waveforms in boost mode.

Hence, i_{LM1} and i_{LM2} continues to reduce and increase, respectively, at almost the same current rates in interval 4. Besides, the voltage of $-(V_{H1}-(N+1)(V_C-V_{D,\mathrm{ON}}))$ is placed across L_{lk}. Hence, the equation of i_{Llk} is given by

$$i_{Llk}(t)=I_{K1}-\frac{V_{H1}-(N+1)(V_C-V_{D,\mathrm{ON}})}{L_{lk}}(t-t_4). \quad (6)$$

At the end of this interval, the value of i_{Llk} is defined $-I_{K2}$.

Interval 6 [t_5–t_6]*:* At t_5, the synchronous switch S_3 turns OFF, and the snubber capacitors C_{S1} and C_{S3} start to discharge and charge, respectively, by means of i_{LM1}. Meanwhile, a resonance starts between L_{lk} and C_{S4} causes C_{S4} discharging. During this interval, C_{S1} discharges completely, C_{S3} charges until V_{H1}, and C_{S4} discharges from V_H-V_C to V_{H2}. At the end of this interval, the values of i_{LM1} and i_{LM2} are defined $-I_2$ and I_2', respectively.

Interval 7 [t_6–t_7]*:* At t_6, C_{S1} is discharges, and its body diode turns ON. By conducting the S_1 body diode, S_1 turns ON under ZVS. During this interval, the voltage of V_L is placed across L_{M1} and L_{M2}. Hence, i_{LM1} reduces linearly in the negative direction, and i_{LM2} increases linearly. In this interval, the currents of i_{LM1}

and i_{LM2} conduct through S_1 and S_2, respectively, and there are no currents in the windings of the ideal transformers.

Interval 8 [t_7–t_8]*:* At t_7, S_2 turns OFF, and the snubber capacitors C_{S2} and C_{S4} start to charge and discharge, respectively, by means of i_{LM2}. Meanwhile, a resonance starts between L_{lk} and C_{S3} causes C_{S3} charging.

Interval 9 [t_8–t_9]*:* At t_8, C_{S2} is charged to V_C, and thus, D_{C2} is forward biased. In this interval, resonance continues between L_{lk}, C_{S3}, and C_{S4}. During this resonance, C_{S4} discharges completely, and C_{S3} charges from V_{H1} to V_H. At the end of this interval, the values of i_{LM1}, i_{LM2}, and i_{Llk} are defined $-I_3$, I_3', and $-I_{K3}$, respectively.

Interval 10 [t_9–t_{10}]*:* At t_9, S_4 body diode is forward biased and starts to conduct. By conducting S_4 body diode, the synchronous switch S_4 turns ON under ZVS, and so, S_4 body diode current conducts through S_4. In this interval, the voltage of $-(V_C + V_{D,\text{ON}} - V_L)$ is placed across L_{M2}, and the voltage of L_{M1} is V_L as yet. Hence, the equations of i_{LM1} and i_{LM2} would be

$$i_{LM1}(t) = -I_3 - \frac{V_L}{L_{M1}}(t - t_9) \tag{7}$$

$$i_{LM2}(t) = I_3' + \frac{V_C + V_{D,\text{ON}} - V_L}{L_{M2}}(t - t_9). \tag{8}$$

Also, the voltage of $V_{H2} - (N+1)(V_C + V_{D,\text{ON}})$ is placed across L_{lk}, hence, the equation of i_{Llk} is obtained as follows:

$$i_{Llk}(t) = -I_{K3} + \frac{V_{H2} - (N+1)(V_C + V_{D,\text{ON}})}{L_{lk}}(t - t_9). \tag{9}$$

At the end of this interval, the value of i_{Llk} is defined $-I_{K4}$.

Interval 11 [t_{10}–t_{11}]*:* At t_{10}, the current of C_C reaches zero, and so, D_{C2} turns OFF. In this interval, the voltages of L_{M1}, L_{M2}, and L_{lk} are V_L, $-(V_C + V_{D,\text{ON}} - V_L)$, and $V_{H2} - (N+1)(V_C + V_{D,\text{ON}})$, respectively. Hence, i_{LM1} increases linearly, i_{LM2} reduces linearly, and i_{Llk} reduces linearly in the negative direction, at the same current rates in interval 10. At the end of this interval, the value of i_{Llk} is defined I_{K5}.

Interval 12 [t_{11}–$(t_0 + T)$]*:* At t_{11}, the synchronous switch S_4 turns OFF, and the snubber capacitors C_{S2} and C_{S4} start to discharge and charge, respectively, by means of i_{LM2}. Meanwhile, a resonance starts between L_{lk} and C_{S3} causes C_{S3} discharging. During this interval, C_{S2} discharges completely, C_{S4} charges until V_{H2}, and C_{S3} discharges from V_H to V_{H1}. At the end of this interval, the values of i_{LM1} and i_{LM2} are defined I_0 and $-I_0'$, respectively, and the next switching cycle begins.

B. Buck Mode

In the buck mode, S_3 and S_4 are the main switches, and the switches S_1 and S_2 act as the synchronous switches in the complementary with S_3 and S_4, considering a sufficient deadtime. Also, two phases operate with interleaved pattern and there is a phase shift of 180° between them. The equivalent circuits of 12 operating intervals in buck mode and the theoretical key waveforms are illustrated in Figs. 4 and 5, respectively.

At the beginning of interval 1, it is assumed that i_{LM1} has a negative value of $-I_0$, and the value of i_{LM2} is I_0'. Also, it is assumed that S_1 is ON, and the body diode of S_2 is conducting.

Interval 1 [t_0–t_1]*:* In this interval and by conducting the S_2 body diode, the synchronous switch S_2 turns ON under ZVS, and so, S_2 body diode current conducts through S_2. During this interval, the voltage of $-V_L$ is placed across L_{M1} and L_{M2}. Hence, i_{LM1} increases linearly in the negative direction and i_{LM2} reduces linearly as follows:

$$-i_{LM1}(t) = -I_0 - \frac{V_L}{L_{M1}}(t - t_0) \tag{10}$$

$$-i_{LM2}(t) = I_0' - \frac{V_L}{L_{M2}}(t - t_0). \tag{11}$$

In this interval, the currents of $-i_{LM1}$ and $-i_{LM2}$ conduct through S_1 and S_2, respectively, and there are no currents in the windings of the ideal transformers.

Interval 2 [t_1–t_2]*:* At t_1, the synchronous switch S_1 turns OFF, and the snubber capacitors C_{S1} and C_{S3} start to charge and discharge, respectively, by means of i_{LM1}. Meanwhile, a resonance starts between L_{lk} and C_{S4} causes C_{S4} charging.

Interval 3 [t_2–t_3]*:* At t_2, C_{S4} is charged to $V_H - V_C$, and thus, D_{C3} is forward biased. In this interval, resonance continues between L_{lk}, C_{S1}, and C_{S3}. During this resonance, C_{S3} discharges completely, and C_{S1} charges to V_C. At the end of this interval, the values of $-i_{LM1}$, $-i_{LM2}$, and i_{Llk} are defined $-I_1$, I_1', and I_{K0}, respectively.

Interval 4 [t_3–t_4]*:* At t_3, S_3 body diode is forward biased. By conducting S_3 body diode, S_3 turns ON under ZVS. In this interval, the voltage of $V_C - V_{D,\text{ON}} - V_L$ is placed across L_{M1}, and the voltage of L_{M2} is $-V_L$ as yet. Hence, the equations of $-i_{LM1}$ and $-i_{LM2}$ would be

$$-i_{LM1}(t) = -I_1 + \frac{V_C - V_{D,\text{ON}} - V_L}{L_{M1}}(t - t_3) \tag{12}$$

$$-i_{LM2}(t) = I_1' - \frac{V_L}{L_{M2}}(t - t_3). \tag{13}$$

Also, the voltage of $-(V_{H1} - (N+1)(V_C - V_{D,\text{ON}}))$ is placed across L_{lk}, and i_{Llk} reduces linearly from I_{K0}. Hence, the equation of i_{Llk} is given by

$$i_{Llk}(t) = I_{K0} - \frac{V_{H1} - (N+1)(V_C - V_{D,\text{ON}})}{L_{lk}}(t - t_3). \tag{14}$$

At the end of this interval, the value of i_{Llk} is defined I_{K1}.

Interval 5 [t_4–t_5]*:* At t_4, the current of C_C reaches zero, and so, D_{C3} turns OFF. In this interval, similar to interval 4, the voltages of L_{M1}, L_{M2}, and L_{lk} are $V_C - V_{D,\text{ON}} - V_L$, $-V_L$, and $-(V_{H1} - (N+1)(V_C - V_{D,\text{ON}}))$, respectively. Hence, $-i_{LM1}$ increases linearly, $-i_{LM2}$ reduces linearly, and i_{Llk} reduces linearly, at the same current rates in interval 4. At the end of this interval, the value of i_{Llk} is defined $-I_{K2}$.

Interval 6 [t_5–t_6]*:* At t_5, S_3 turns OFF, and the snubber capacitors C_{S1} and C_{S3} start to discharge and charge, respectively, by means of $-i_{LM1}$. Meanwhile, a resonance starts between L_{lk} and C_{S4} causes C_{S4} discharging. During this interval, C_{S1} discharges completely, C_{S3} charges until V_{H1}, and C_{S4} discharges

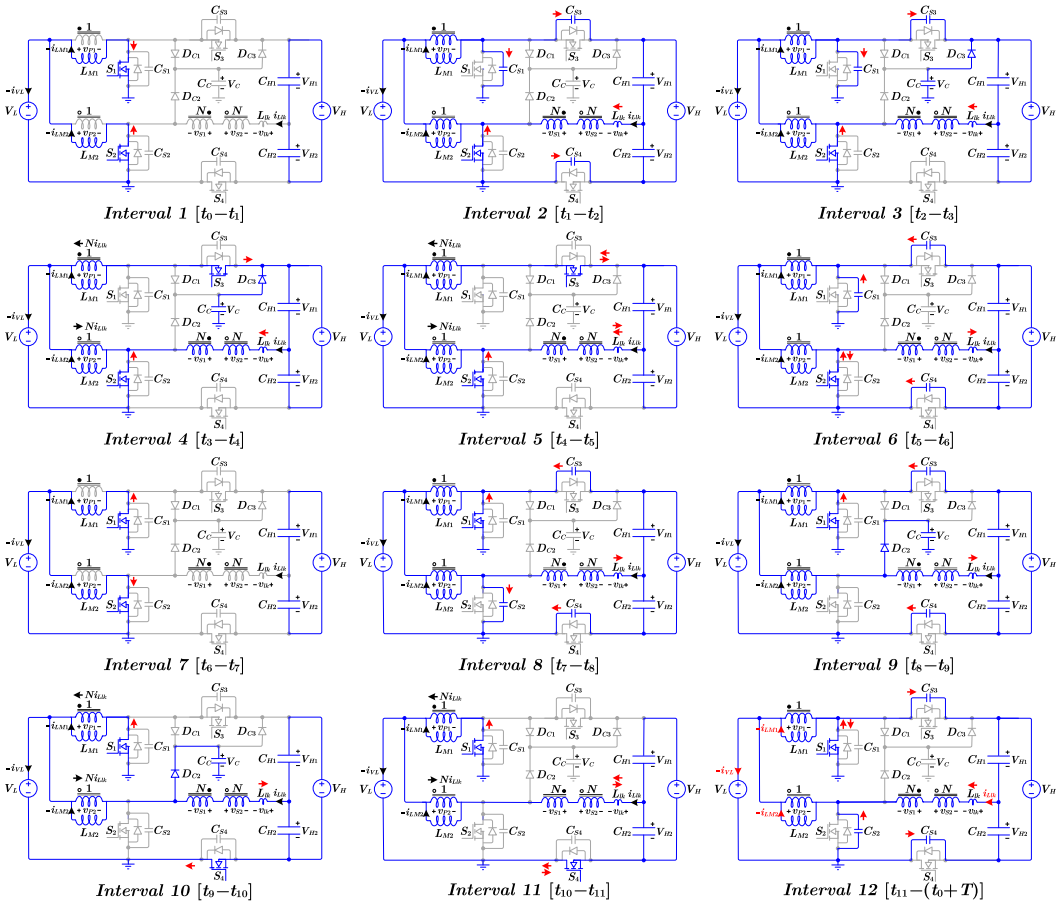


Fig. 4. Equivalent circuits of 12 operating intervals in buck mode.

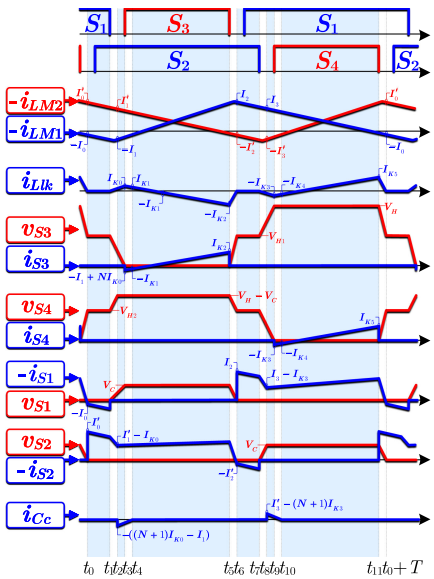


Fig. 5. Theoretical key waveforms in buck mode.

from $V_H - V_C$ to V_{H2}. At the end of this interval, the values of $-i_{LM1}$ and $-i_{LM2}$ are defined I_2 and $-I_2'$, respectively.

Interval 7 [t_6–t_7]*:* At t_6, S_1 body diode is forward biased and starts to conduct. By conducting S_1 body diode, the synchronous switch S_1 turns ON under ZVS, and so, S_1 body diode current conducts through S_1. During this interval, the voltage of $-V_L$ is placed across L_{M1} and L_{M2}. Hence, $-i_{LM1}$ reduces linearly, and $-i_{LM2}$ increases linearly in the negative direction. In this interval, the currents of $-i_{LM1}$ and $-i_{LM2}$ conducts through S_1 and S_2, respectively, and there are no currents in the windings of the ideal transformers.

Interval 8 [t_7–t_8]*:* At t_7, S_2 turns OFF, and the snubber capacitors C_{S2} and C_{S4} start to charge and discharge, respectively, by means of $-i_{LM2}$. Meanwhile, a resonance starts between L_{lk} and C_{S3} causes C_{S3} charging.

Interval 9 [t_8–t_9]*:* At t_8, C_{S2} is charged to V_C, and thus, D_{C2} is forward biased. In this interval, resonance continues between L_{lk}, C_{S3}, and C_{S4}. During this resonance, C_{S4} discharges completely, and C_{S3} charges to V_H. At the end of this interval, the values of $-i_{LM1}$, $-i_{LM2}$, and i_{Llk} are defined I_3, $-I_3'$, and $-I_{K3}$, respectively.

Interval 10 [t_9–t_{10}]*:* At t_9, S_4 body diode and D_{C2} are forward biased and starts to conduct. By conducting S_4 body diode, S_4 turns ON under ZVS. In this interval, the voltage of $V_C + V_{D,\mathrm{ON}} - V_L$ is placed across L_{M2}, and the voltage of L_{M1} is $-V_L$ as yet. Hence, the equations of $-i_{LM1}$ and $-i_{LM2}$

would be

$$-i_{LM1}(t) = I_3 - \frac{V_L}{L_{M1}}(t - t_9) \tag{15}$$

$$-i_{LM2}(t) = -I_3' + \frac{V_C + V_{D,\mathrm{ON}} - V_L}{L_{M2}}(t - t_9). \tag{16}$$

Also, the voltage of $V_{H2} - (N+1)(V_C + V_{D,\mathrm{ON}})$ is placed across L_{lk}; hence, the equation of i_{Llk} is obtained as follows:

$$i_{Llk}(t) = -I_{K3} + \frac{V_{H2} - (N+1)(V_C + V_{D,\mathrm{ON}})}{L_{lk}}(t - t_9). \tag{17}$$

At the end of this interval, the value of i_{Llk} is defined $-I_{K4}$.

Interval 11 $[t_{10}$–$t_{11}]$*:* At t_{10}, the current of C_C reaches zero, and so, D_{C2} turns OFF. In this interval, similar to interval 10, the voltages of L_{M1}, L_{M2}, and L_{lk} are $-V_L$, $V_C + V_{D,\mathrm{ON}} - V_L$, and $V_{H2} - (N+1)(V_C + V_{D,\mathrm{ON}})$, respectively. Hence, $-i_{LM1}$ reduces linearly, $-i_{LM2}$ increases linearly, and i_{Llk} increases linearly, at the same current rates in interval 10. At the end of this interval, the value of i_{Llk} is defined I_{K5}.

Interval 12 $[t_{11}$–$(t_0 + T)]$*:* At t_{11}, S_4 turns OFF, and the snubber capacitors C_{S2} and C_{S4} start to discharge and charge, respectively, by means of $-i_{LM2}$. Meanwhile, a resonance starts between L_{lk} and C_{S3} causes C_{S3} discharging. During this interval, C_{S2} discharges completely, C_{S4} charges until V_{H2}, and C_{S3} discharges from V_H to V_{H1}. At the end of this interval, the values of $-i_{LM1}$ and $-i_{LM2}$ are defined $-I_0$ and I_0', respectively, and the next switching cycle begins.

III. Converter Specifications

This section describes the key specifications of the proposed converter, including the voltage gain, stresses of the switches, and the current ripple cancelation. For this purpose, the following assumptions are considered in the analysis.

1) The operating duty cycle in boost mode (duty cycle of S_1 and S_2) and buck mode (duty cycle of S_3 and S_4) are D and D', respectively.
2) The resonance intervals (intervals 2, 3, 6, 8, 9, and 12) are very short, and these intervals are omitted in the analysis. Besides, the voltage drop of the diodes is omitted here ($V_{D,\mathrm{ON}} = 0$). Based on these simplifications, some of the required simplified waveforms of the proposed converter in boost mode are shown in Fig. 6.

A. Voltage Gain and Voltage Stress of Semiconductors

In the steady-state condition, the average voltage across each converter inductor is equal to zero (i.e., volt-second balance). Considering this fact, and from the simplified waveform of v_{LM1} (or v_{LM2}) in Fig. 6, the value of V_C is derived as

$$V_C = \frac{V_L}{1 - D}. \tag{18}$$

Also, due to the almost symmetrical operation of the proposed converter, we have $V_{H1} = V_{H2}$. Hence, considering that $V_{H1} + V_{H2} = V_H$, the following equation would be obtained:

$$V_{H1} = V_{H2} = \frac{V_H}{2}. \tag{19}$$

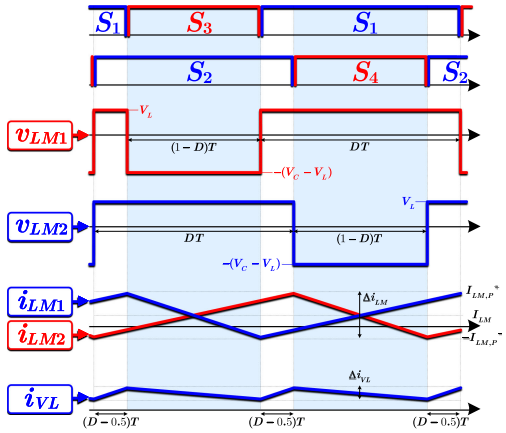


Fig. 6. Simplified waveforms of the proposed converter in boost mode.

From equivalent circuit of interval 11 in boost mode (see Fig. 2), and using the KVL and KCL laws, we have $-V_L + L_{M2}\frac{di_{LM2}}{dt} - NV_C - L_{lk}\frac{di_{Llk}}{dt} + V_{H2} = 0$ and $i_{LM2} = -(N+1)i_{Llk}$. Using these equations, and also from (18), (19), (42), (43), and (44), the voltage gain of the proposed converter in boost mode would be obtained as

$$\frac{V_H}{V_L} = \frac{2(1+N) - D\alpha}{1 - D} \tag{20}$$

where α is given by

$$\alpha = \frac{2N^2(1 - k^2)}{(N+1)k^2}. \tag{21}$$

Similarly, in the buck mode and considering the value of α given by (21), the voltage gain is derived as

$$\frac{V_L}{V_H} = \frac{D'}{2(N+1) - (1 - D')\alpha}. \tag{22}$$

Based on (20)–(22), the voltage gain of the proposed converter versus duty cycle for different values of k considering $N = 1$ are plotted in Fig. 7(a).

In an ideal case that coupling is complete ($k = 1$), from (21), the value of α would be equal to zero. Hence, from (20) and (22), the voltage gains in boost and buck modes when $k = 1$ are given by (23) and (24), respectively

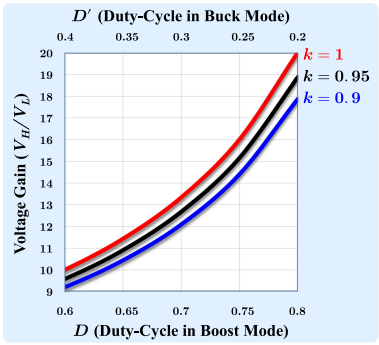
$$\frac{V_H}{V_L} = \frac{2(1+N)}{1 - D} \tag{23}$$

$$\frac{V_L}{V_H} = \frac{D'}{2(N+1)}. \tag{24}$$

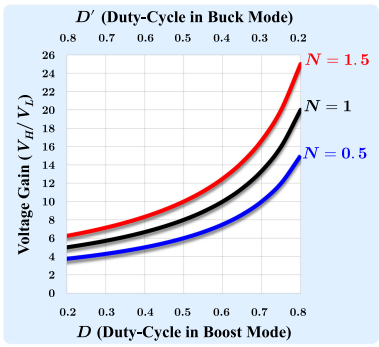
From (23) and (24), the voltage gain of the proposed converter for different values of N is plotted in Fig. 7(b).

Based on the analysis of the converter operation, the voltage stress of the switches S_1 and S_2, and diodes D_{C1} and D_{C2} is equal to V_C. From (18) and (23), the voltage of V_C, and so, the voltage stress of S_1, S_2, D_{C1}, and D_{C2} is derived as

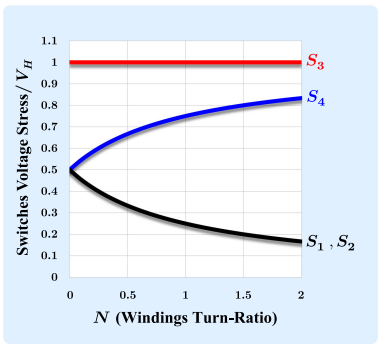
$$V_C = \frac{V_H}{2(N+1)}. \tag{25}$$



(a)



(b)



(c)

Fig. 7. (a) Voltage gain versus duty cycle for different values of k ($N = 1$). (b) Voltage gain versus duty cycle for different values of N ($k = 1$). (c) Voltage stress of switches versus N ($k = 1$).

Moreover, the voltage stress of switch S_4 and diode D_{C3} is $V_H - V_C$. By using (25), the voltage of $V_H - V_C$, and so, the voltage stress of S_4 and D_{C3} is obtained as

$$V_H - V_C = \frac{(2N+1)V_H}{2(N+1)}. \tag{26}$$

Finally, the voltage stress of S_3 is V_H. Based on the derived equations, the voltage stress of the converter switches versus N, considering $k = 1$, are plotted in Fig. 7(c).

B. Current Ripple Cancelation

In the proposed converter, similar to the converters with WCCIs [47], the current ripple cancelation is feasible. To illustrate this point, based on the defined currents in Fig. 1(b), the LVS currents of upper phase (i_{L1}) and lower phase (i_{L2}) are equal to $i_{LM1} - N_1 i_{Llk}$ and $i_{LM2} + N_2 i_{Llk}$, respectively. Since the current of LVS (i_{VL}) is equal to $i_{L1} + i_{L2}$, the value of i_{VL} would be obtained as

$$i_{VL} = i_{LM1} + i_{LM2} - N_1 i_{Llk} + N_2 i_{Llk}. \tag{27}$$

From (27), if the turn ratios of the ideal transformers in the model are equal ($N_1 = N_2$), regardless of i_{Llk} shape, we always have $i_{VL} = i_{LM1} + i_{LM2}$. On the other hand, if the shapes of i_{LM1} and i_{LM2} are the same with a phase shift of 180°, the LVS current ripple cancelation is feasible. For this purpose, the main switches in each operation mode should be driven with the interleaved pattern in which a phase shift of 180° is applied between them. Besides, in the ideal case, the operating duty cycles of both phases, the average values of phase current, and each phase's specifications should be the same. The simplified waveforms of i_{LM1}, i_{LM2}, and i_{VL} shown in Fig. 6 are clarified the mentioned points. Hence, if the mentioned conditions are satisfied, regardless of converter operation mode, output power, and the voltage levels of LVS or HVS, the current ripple cancelation would be obtained. From Fig. 6, the current ripple of the LVS current (Δi_{VL}) would be derived as

$$\Delta i_{VL} = \frac{2V_L(D-0.5)}{L_M f} \tag{28}$$

where f is the operating switching frequency of the converter. Also, the current-ripple ratio of LVS current (i_{VL}) to magnetizing inductor current (i_{LM}) is obtained as

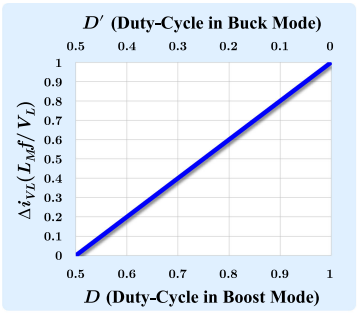
$$\frac{\Delta i_{VL}}{\Delta i_{LM}} = \frac{2(D-0.5)}{D}. \tag{29}$$

From (28) and (29), the normalized value of Δi_{VL} versus duty cycle and $\Delta i_{VL}/\Delta i_{LM}$ versus duty cycle are depicted in Fig. 8.

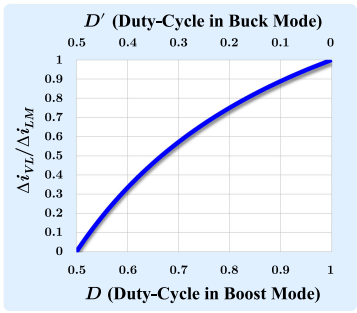
IV. Design Considerations

This section describes various design parameters of the proposed converter. For this purpose, the initial points that should be considered are as follows.

1) Since the voltage waveforms of L_{M1} and L_{M2} include two similar waveforms with a phase shift of 180°, to realize the current ripple cancelation, the values of the magnetizing inductors L_{M1} and L_{M2} should be equal ($L_{M1} = L_{M2} = L_M$).
2) The average values of i_{LM1} and i_{LM2} are equal (I_{LM}). In fact, the current balance between the two phases is established.
3) As discussed in the previous section, to realize the current ripple cancelation, the turn ratios of the ideal transformers in the model should be selected the same ($N_1 = N_2 = N$).
4) Due to similar condition of the LVS switches (S_1 and S_2), the values of their snubber capacitors can be selected the same ($C_{S1} = C_{S2} = C_{SL}$). Similarly, since the conditions of the HVS switches (S_3 and S_4) are almost the same, the values of their snubber capacitors are selected equally ($C_{S3} = C_{S4} = C_{SH}$).



(a)



(b)

Fig. 8. (a) Normalized value of LVS current ripple (Δi_{VL}) versus duty cycle. (b) Current-ripple ratio of LVS current (i_{VL}) to magnetizing inductor current (i_{LM}) versus duty cycle.

A. ZVS Condition

To guarantee the ZVS condition of the proposed converter in boost mode, at the beginning of intervals 6 and 12, the stored energy in L_{M1} and L_{M2} should be sufficient to discharge C_{S1} and C_{S3} from V_C to zero, and to charge C_{S2} and C_{S4} from zero to $V_H/2$. Similarly, in buck mode, at the beginning of intervals 2 and 8, the sufficient energy should be stored in L_{M1} and L_{M2} to discharge C_{S2} and C_{S4} from $V_H/2$ to zero, and charge C_{S1} and C_{S1} from zero to V_C. Considering the simplified waveforms of i_{LM1} and i_{LM2} in Fig. 6, the current values of L_{M1} and L_{M2} at the beginning of intervals 6 and 12 correspond with the negative peak value of i_{LM1} and i_{LM2} ($-I_{LM,P}{}^{-}$). Consequently, the ZVS condition in the proposed converter would be written as follows:

$$\frac{1}{2}L_M(-I_{LM,P}{}^{-})^2 > \frac{1}{2}C_{SL}{V_C}^2 + \frac{1}{2}C_{SH}\left(\frac{V_H}{2}\right)^2. \quad (30)$$

It is worth mentioning that the ZVS condition of (30) is also valid in buck mode since the current values of L_{M1} and L_{M2} at the beginning of intervals 2 and 8 of buck mode also correspond with the negative peak value of i_{LM1} and i_{LM2} ($-I_{LM,P}{}^{-}$).

By substituting V_C from (25) in (30), and by considering an additional 50% margin for the tolerances of the devices and losses of parasitic elements, the ZVS condition in both the boost and buck operation modes would be derived as

$$-I_{LM,P}{}^{-} < -\frac{1.5V_H}{2}\sqrt{\frac{1}{L_M}\left(C_{SH} + \frac{C_{SL}}{(N+1)^2}\right)}. \quad (31)$$

It is worth mentioning that the value of L_{M1} and L_{M2} (L_M) determines the value of $-I_{LM,P}{}^{-}$ based on the operating condition of the converter, which is discussed in Section IV-C.

B. Selection of Snubber Capacitors

The snubber capacitors are responsible for the reduction of switches turn-OFF losses. It should be noted that using the larger values for the snubber capacitors causes the reduction of the switches turn-OFF losses. However, as (31) shows, when the values of snubber capacitors (C_{SL} and C_{SH}) are selected large, the required value of $-I_{LM,P}{}^{-}$, and so, the current ripple of i_{LM1} and i_{LM2} would be increased. This issue causes increased conduction and core losses. Hence, in the proposed converter, selecting the minimum values for the snubber capacitors is desirable.

C. Design of L_{M1} and L_{M2} to Obtain ZVS Condition

The value of magnetizing inductors L_{M1} and L_{M2} (L_M) determines the current ripple of i_{LM}, and so the value of $-I_{LM,P}{}^{-}$. Hence, the value of L_M has an important role in providing ZVS condition in (31). To ensure the ZVS condition (31) in the entire operating range, the value of L_M should be selected at the worst-case operating point, when the average value of i_{LM1} and i_{LM2} (I_{LM}) has the maximum value ($I_{LM,\max}$). In this operating point, i_{LM1} and i_{LM2} have the maximum level and the value of $|-I_{LM,P}{}^{-}|$ is minimized. Hence, if the value of L_M is designed for this operating point, in the other operating points where the value of I_{LM} is reduced, the value of $|-I_{LM,P}{}^{-}|$ is increased, and the ZVS condition of (31) would be satisfied. As a result, the ZVS condition is obtained for the entire operating range of the converter.

In the proposed converter, since $i_{VL} = i_{LM1} + i_{LM2}$, $I_{VL} = P_o/V_L$, and $I_{LM1} = I_{LM2} = I_{LM}$, the average value of i_{LM} (I_{LM}) would be equal to $P_o/2V_L$. Hence, the value of I_{LM} is maximized when the converter operates in maximum output power ($P_{o,\max}$) and V_L has the minimum value ($V_{L,\min}$). Consequently, the maximum average value of i_{LM1} and i_{LM2} ($I_{LM,\max}$) would be obtained as

$$I_{LM,\max} = \frac{P_{o,\max}}{2V_{L,\min}}. \quad (32)$$

Fig. 9(a) illustrates the simplified waveform of i_{LM1} at operating point that the average value has the maximum value (worst-case condition). In Fig. 9(a), to simplify the analysis, the value of Δi_{LM} is considered $2(1+\beta)I_{LM,\max}$. Hence, the value of the negative peak would be $-\beta I_{LM,\max}$. From Fig. 9(a), the value of L_M is

$$L_M = \frac{V_{L,\min}D_{\max}}{2f_{\min}(1+\beta)I_{LM,\max}} \quad (33)$$

where $f_{\min}$ is the minimum switching frequency, and the value of $I_{LM,\max}$ is obtained from (32). It is worth mentioning that $f_{\min}$ is considered when the converter operates with VFC. The VFC is discussed in the next section. If the converter operates with the constant switching operation, the switching frequency should be considered for $f_{\min}$. Besides, $D_{\max}$ is the maximum

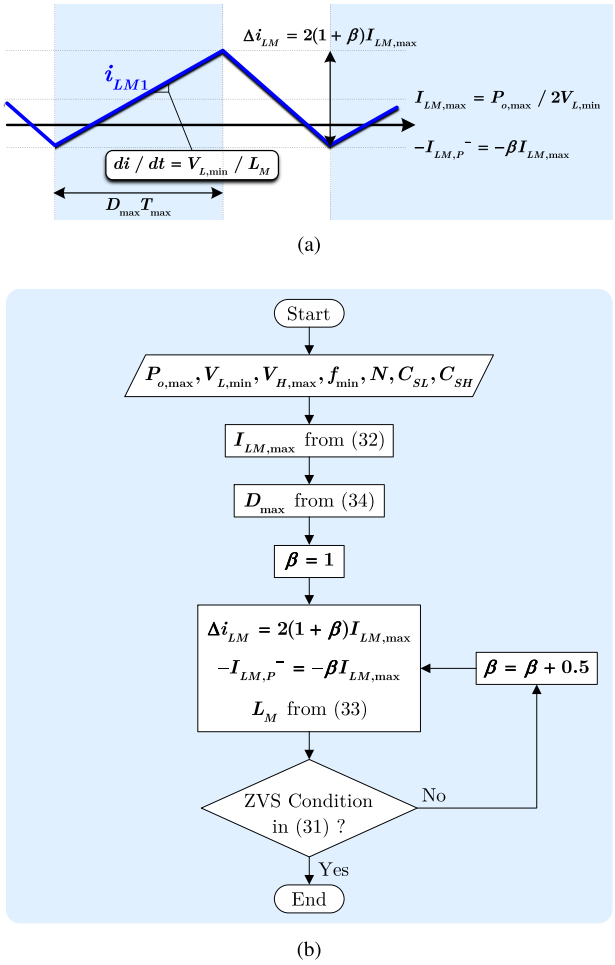


Fig. 9. (a) Simplified waveform of i_{LM1} when its average value (I_{LM}) has maximum value. (b) Design process of L_M value.

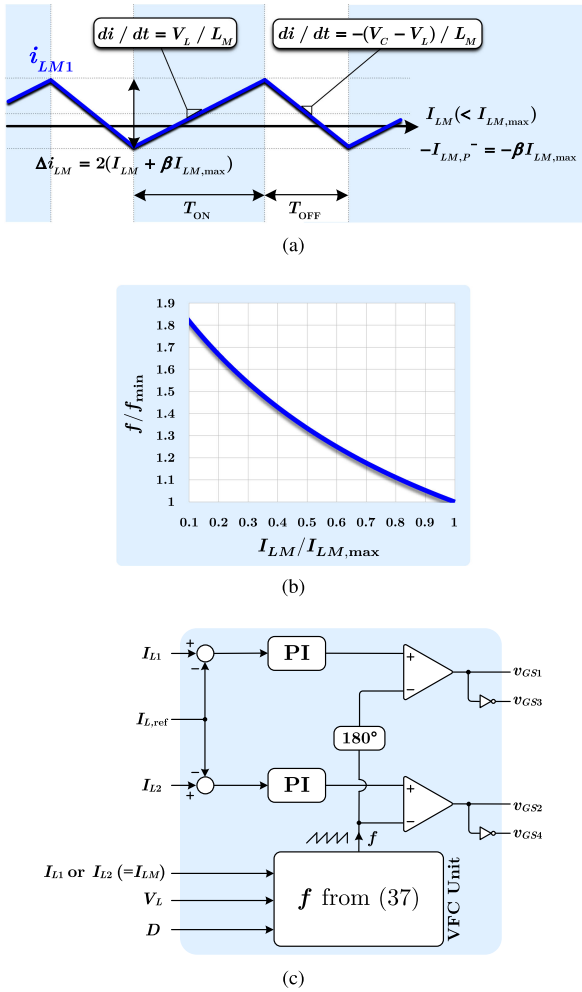


Fig. 10. (a) Waveform of i_{LM1} at the operating point that $I_{LM} < I_{LM,\max}$ and $-I_{LM,P}^{-} = -\beta I_{LM,\max}$. (b) Values of $f/f_{\min}$ versus $I_{LM}/I_{LM,\max}$ for specific values of V_L and V_H. (c) Overall block diagram of the control circuit.

value of duty cycle in boost mode. From (23), the value of $D_{\max}$ is derived as

$$D_{\max} = 1 - \frac{2V_{L,\min}(1+N)}{V_{H,\max}}. \tag{34}$$

Now, to design L_M from (33), it is important to select the value of β, such that the value of $-I_{LM,P}^{-}$ is large enough to satisfy ZVS condition in (31). Since $-I_{LM,P}^{-} = -\beta I_{LM,\max}$, if $\beta > 0$, the value of $-I_{LM,P}^{-}$ would be in the negative region. By a proper over design, the initial value of β can be selected equal to one, and so, the values of $-I_{LM,P}^{-}$ and Δi_{LM} would be $-I_{LM,\max}$ and $2I_{LM,\max}$, respectively. Based on these values and the converter specifications, the ZVS condition in (31) is checked. If the ZVS condition is satisfied, the design of L_M value is finished. Otherwise, the value of β should be selected larger ($\beta = \beta + 0.5$), and the design procedure of L_M value is repeated. Fig. 9(b) illustrates the design process of L_M value, as discussed earlier. Note that the discussed design procedure of L_M is valid in both boost and buck operation modes.

D. Variable Frequency Control

Generally, in TCM operation, to achieve the ZVS condition and reverse recovery cancelation, the main inductors are designed such that their currents flow in both directions. When the converter operates at a constant switching frequency, the current ripple of main inductors is almost constant for different operating conditions. This issue results in almost constant conduction and core losses, which drops the light loads' efficiency. To alleviate this problem, the VFC can be applied such that when the output power is reduced, the switching frequency is increased to reduce the current ripple of main inductors.

In the selection of the switching frequency in proportion to the output power, as discussed in Section IV-C, it should be noted that the negative value of i_{LM1} and i_{LM2} ($-I_{LM,P}^{-}$) must always be at the desired level to satisfy the ZVS condition ($-I_{LM,P}^{-} = -\beta I_{LM,\max}$).

Fig. 10(a) illustrates the waveform of i_{LM1} at the operating point that its average value is lower than maximum value ($I_{LM} < I_{LM,\max}$). Also, its negative value is at the level of $-\beta I_{LM,\max}$, which satisfies the ZVS condition. From Fig. 10(a),

considering that $f = 1/T = 1/(T_{\rm ON} + T_{\rm OFF})$, and from (25), the value of switching frequency f corresponds to this operating point would be

$$f = \frac{V_L(V_H - 2V_L(N+1))}{2L_M V_H(I_{LM} + \beta I_{LM,\rm max})}. \quad (35)$$

From (35), and based on the measured values of V_H, V_L, and I_{LM}, the value of switching frequency can be calculated. Based on (35), and for specific values of V_L and V_H, the values of $f/f_{\rm min}$ versus $I_{LM}/I_{LM,\rm max}$ are depicted in Fig. 10(b).

To reduce the variables that need to be measured from the converter, and by substituting V_L or V_H from (23) in (35), the value of switching frequency f can be calculated from

$$f = \frac{V_H(1-D)}{4L_M(1+N)(I_{LM} + \beta I_{LM,\rm max})} \quad (36)$$

or

$$f = \frac{V_L D}{2L_M(I_{LM} + \beta I_{LM,\rm max})} \quad (37)$$

where, in (36), the variables that need to be measured from the converter include I_{LM} and V_H. Also, (37) requires I_{LM} and V_L. It is worth mentioning that (35)–(37) are valid in both boost and buck operation modes.

Fig. 10(c) illustrates the overall block diagram of the control circuit based on the calculation of f from (37). The average current mode control can be utilized for each phase to control the current and obtain the current balancing between phases. The value of $I_{L,\rm ref}$ is determined from an outer control unit, based on the condition and requirements of the system.

In the proposed converter, the values of i_{L1} and i_{L2} are equal to $i_{LM1} - Ni_{Llk}$ and $i_{LM2} + Ni_{Llk}$, respectively [see Fig. 1(b)]. Since the average value of i_{Llk} is equal to zero ($I_{Llk} = 0$), the equations of $I_{L1} = I_{LM1}$ and $I_{L2} = I_{LM2}$ are established. Assuming that the current balancing between phases is established, we have $I_{L1} = I_{L2} = I_{LM}$. Hence, the measured value of I_{L1} (or I_{L2}) would be equal to I_{LM}.

It is worth mentioning that to implement the VFC unit, as illustrated in Fig. 10(c), an additional processor is required to calculate the corresponding switching frequency. This way, compared to constant switching operation, the switching losses at light loads are reduced, resulting in improved efficiency at light loads. On the other hand, to implement the control unit in constant switching frequency, the frequency calculation unit is eliminated, and only the sawtooth wave with constant switching can be applied. Hence, in constant frequency operation, the converter control would be more simple, albeit with the cost of reduced efficiency.

V. Experimental Results

To verify the theoretical analysis, a prototype of the proposed converter is implemented. Table I presents the prototype specifications and values/part numbers of the components.

A. Design Procedure

Based on the values of V_L and V_H, considering the operating duty cycle of 0.6 in the boost mode ($D = 0.6$), from (23), the value of turn ratio (N) is obtained 0.67. From (25), the voltage stress of S_1 and S_2 is 120 V. Also, the voltage stress of S_3 is 400 V (V_H), and from (26), the voltage stress of S_4 would be 280 V. For S_1 and S_2, IRF200P223 ($V_{\rm DS} = 200$ V, $R_{\rm DS(ON)} = 9.5$ mΩ, and $C_{\rm oss} = 628$ pF) is utilized. Also, IPW65R041CFD ($V_{\rm DS} = 650$ V, $R_{\rm DS(ON)} = 37$ mΩ, and $C_{\rm oss} = 400$ pF) is used for S_3 and S_4. The output capacitors of switches are utilized as the snubber capacitors. Hence, we have $C_{S1} = C_{S2} = C_{SL} = 628$ pF and $C_{S3} = C_{S4} = C_{SH} = 400$ pF.

To select the inductance value of L_M, based on the design process in Fig. 9(b), values of $I_{LM,\rm max}$ and $D_{\rm max}$ are obtained 4.17 A and 0.6, respectively. Moreover, from Fig. 9(b) and considering $\beta = 1$, the values of Δi_{LM}, $-I_{LM,P}{}^{-}$, and L_M would be obtained 16.7 A, –4.17 A, and 17.3 μH, respectively. Finally, from ZVS condition, the valid equation of -4.17 A < -1.80 A would be obtained. Hence, the design process is finished with the obtained values. For the magnetic cores, high flux toroid C058110A2 ($V_e = 20.7$ cm^3 and $A_e = 144$ mm^2) is utilized. The number of windings turns of the primary and secondary sides is 15 and 11, respectively.

TABLE I
Prototype Specifications and Values/Part Numbers of Utilized Components

Symbol	Parameter	Value/Part Number
P_o	Output Power	400 W
V_H	HVS Voltage	400 V
V_L	LVS Voltage	48 V
$f_{\rm min}$	Minimum Switching Frequency	100 kHz
S_1 , S_2	LVS Switches	IRF200P223 (200 V / 100 A)
S_3 , S_4	HVS Switches	IPW65R041CFD (650 V / 68.5 A)
-	Magnetic Cores	High Flux C058110A2
L_M	Magnetizing Inductance	17.3 µH
N	Turn Ratio	0.67
L_{lk}	Equivalent Leakage Inductance	2.8 µH
C_C	Clamp Capacitor	MKT1820547165 (4.7 µF / 160V)
C_{H1} , C_{H2}	HVS Capacitors	B32526R3686K000 (68 µF / 250V)

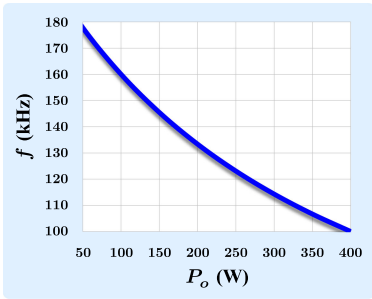


Fig. 11. Operating frequency (f) of the prototype converter versus output power (P_o) in the variable frequency operation.

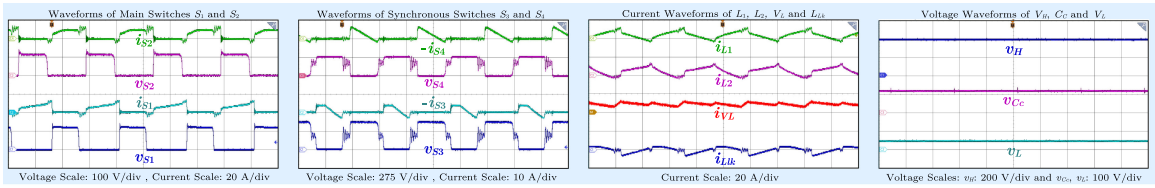


Fig. 12. Experimental waveforms (time scale is 4 μS/div) at full load (400 W) ($f = 100$ kHz) in (a) boost mode and (b) buck mode.

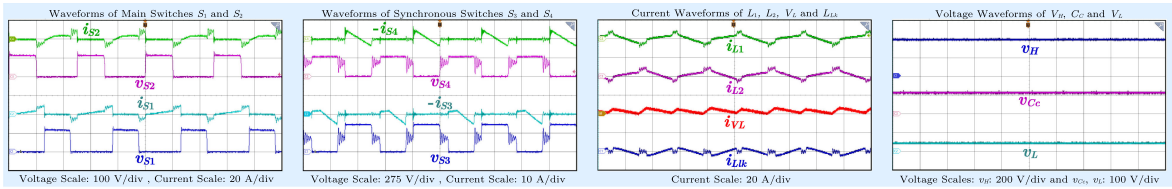


Fig. 13. Experimental waveforms (time scale is 4 μS/div) at 25% of full load (100 W) ($f = 100$ kHz) under constant frequency operation in (a) boost mode and (b) buck mode.

Based on the converter specifications, the voltage of capacitors C_{H1} and C_{H2} is 200 V ($V_H/2$), and the voltage of clamp capacitor (V_C) would be 120 V. For the capacitors C_{H1} and C_{H2}, Film Capacitor B32526R3686K000 (68 μF/250 V) is utilized. Also, Film Capacitor MKT1820547165 (4.7 μF/160 V) is applied for the clamp capacitor C_C.

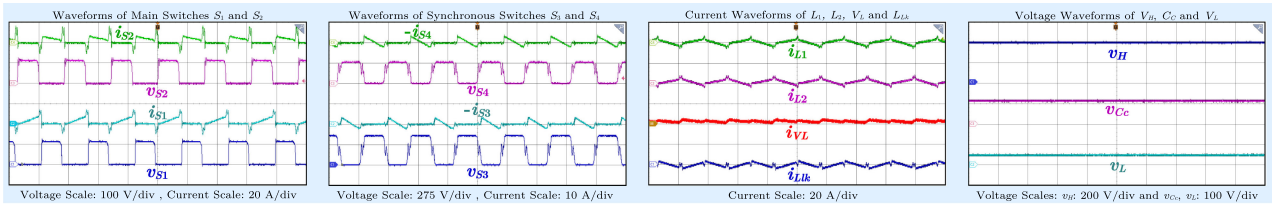
Finally, to implement the VFC for improving the efficiency at light loads, based on the operating condition and parameters of the converter, the operating switching frequency is calculated from (37). For the operating point of $V_L = 48$ V and $V_H = 400$ V, the operating frequency of the prototype converter versus output power (P_o) in the variable frequency operation is depicted in Fig. 11.

B. Experimental Waveforms

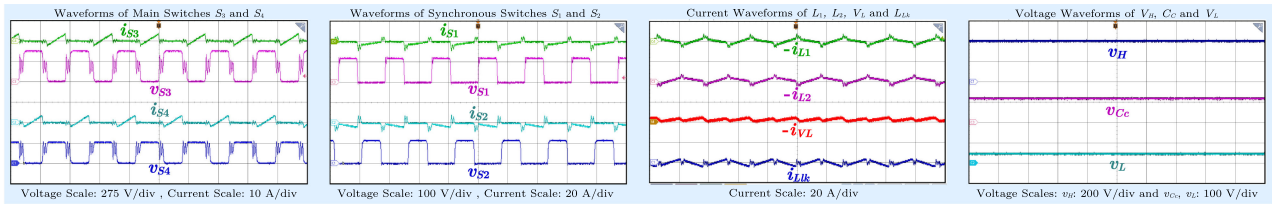
Here, the prototype converter's experimental waveforms are presented. Fig. 12 shows the proposed converter's experimental waveforms at full-load condition (400 W). Moreover, the experimental waveforms at 25% of full load (100 W) with constant frequency operation (100 kHz) are shown in Fig. 13. It is worth mentioning that in both constant frequency operation and VFC, the converter operates with the switching frequency of 100 kHz at the full-load condition.

As seen in Figs. 12 and 13, the experimental waveforms are in accordance with the theoretical analysis, including all the switches voltage stresses. The main switches' waveforms clearly show the ZVS condition as their voltages drop to zero completely before the main switches' turn-ON instants. As observed from the synchronous switches' current waveforms, the current direction is changed through the switch before the switch's turn-OFF instant. Hence, the synchronous switches' body diodes do not conduct in this region, and the reverse recovery losses of the synchronous switches body diodes are eliminated. According to current waveforms of LVS (i_{VL} in boost mode and $-i_{VL}$ in buck mode), the LVS current benefits from the continuous-nonpulsating state.

Fig. 14 shows the experimental waveforms of the proposed converter at 25% of full load (100 W) under VFC. According to Fig. 11, in the prototype converter, when the output power (P_o)



(a)



(b)

Fig. 14. Experimental waveforms (time scale is 4 μS/div) at 25% of full load (100 W) ($f = 160$ kHz) under VFC in (a) boost mode and (b) buck mode.

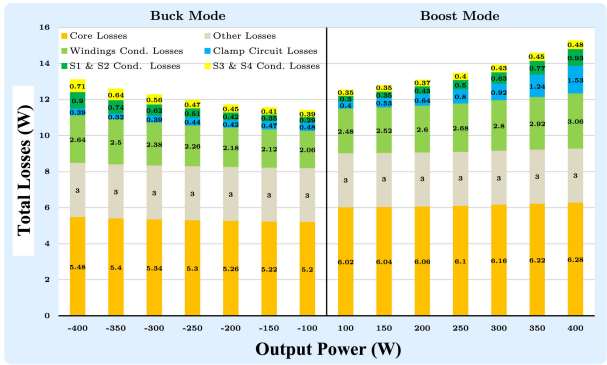
is 100 W, the switching frequency would be equal to 160 kHz. As seen in Fig. 14, the proposed converter features, including voltage stresses, ZVS, elimination of diode reverse recovery, and continuous-nonpulsating state of LVS current, are still well established. Besides, compared to the experimental waveforms of 100 W under the constant switching frequency of 100 kHz shown in Fig. 13, the current ripples of the magnetic elements as well as switches are reduced significantly. This feature causes reduced conduction losses and core losses, which is clarified in the next section.

C. Power Losses Analysis and Comparison

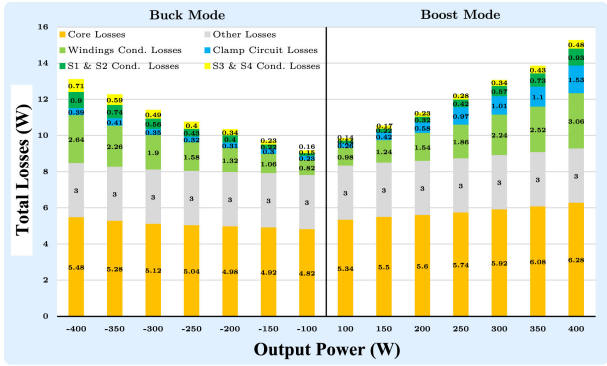
Fig. 15 presents the prototype's loss breakdown at different output power conditions under constant frequency operation and VFC.

The conduction losses of the switches and windings are calculated from $R_{\mathrm{DS(on)}}I^2_{\mathrm{RMS,Switch}}$ and $R_{\mathrm{DC,Coil}}I^2_{\mathrm{RMS,Coil}}$, respectively, where the currents' rms values have been measured from the experimental waveforms. Based on the specifications of the selected switches and at the junction temperature (T_j) of 75 °C, $R_{\mathrm{DS(ON)}}$ for the LVS switches S_1 and S_2 is 14 mΩ, and for the HVS switches S_3 and S_4 is 56 mΩ. Also, $R_{\mathrm{DC,Coil}}$ for the primary and secondary windings of the coupled inductors are 18 and 13 mΩ, respectively. It is worth mentioning that the conduction losses of the converter capacitors C_{H1}, C_{H2}, and C_C are calculated from $R_{\mathrm{ESR}}I^2_{\mathrm{RMS,Cap}}$, where R_{ESR} is the equivalent series resistance of the capacitors. Due to low values of R_{ESR} of the capacitors, the calculated values of capacitors' conduction losses are obtained below 50 mW. Hence, the capacitors' conduction losses are neglected in loss analysis.

The clamp circuit losses include the conduction losses of diodes D_{C1}, D_{C2}, and D_{C3} that is calculated from $V_{D,\mathrm{ON}}I_{\mathrm{avg},D}$. Based on the specifications of the selected diodes and at the junction temperature (T_j) of 75 °C, $V_{D,\mathrm{ON}}$ is considered equal to 1 V. Moreover, the currents' average values have been measured from the experimental waveforms.



(a)



(b)

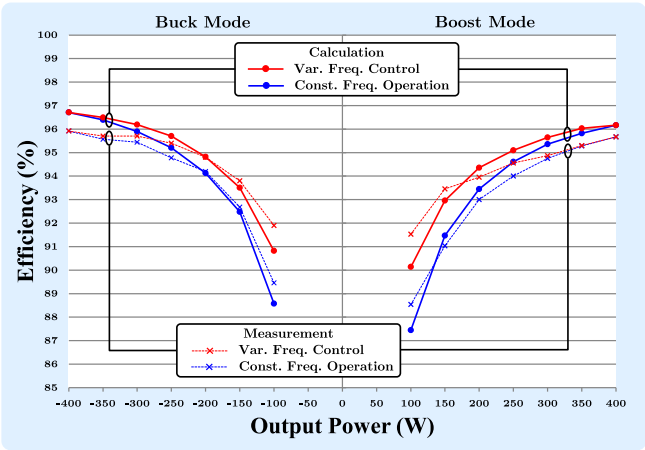
Fig. 15. Prototype's loss breakdown at different output power conditions under (a) constant frequency operation and (b) variable frequency control.

The core losses are obtained from the manufacturer's core loss density curves. According to the manufacture information, the curves of core loss density are theoretically obtained from Steinmetz equation $P_C = aB^b f^c$, where P_C is the core loss density in milliwatt per cubic centimeter (mW/cm^3), B is the peak flux density in tesla (T), and f is the switching frequency in kilohertz (kHz). Besides, a, b, and c are the Steinmetz coefficient

TABLE II
COMPARISON BETWEEN THE PROPOSED CONVERTER AND PREVIOUS COUNTERPART CONVERTERS

	Proposed BDC in [26]	Proposed BDC in [18]	Proposed BDC in [12]	Proposed BDC in [13]	Proposed BDC in [9]	Proposed BDC in [15]	Proposed BDC in [27]	Proposed BDC in [20]	Proposed BDC in [10]	Proposed Converter
No. of Switches	6	5	4	4	4	4	4	4	4	4
No. of Mag. Cores	3	1	1	1	3	1	2	3	1	2
No. of Capacitors	3	3	2	3	5	3	3	4	3	3
LVS Cur. Ripple	Very Low	Low	High	High	Very Low	High	Low	Very Low	High	Low
Continuous LVS Cur.	Yes	No	No	No	Yes	No	Yes	Yes	No	Yes
Switching Cond.	ZVS	ZVS	ZVS	ZVS	Hard	ZVS	ZVS	ZCS	ZVS	ZVS
Prototype Peak Power	500 W	200 W	300 W	200 W	400 W	1 kW	1 kW	600 W	400 W	400 W
Exp. Peak Eff.	97.1%	97.3%	96. 4%	96.8%	94.2%	96%	95.8%	Not Reported	96.5%	96.6%[1]
Design Scalability	No	No	No	No	No	No	No	No	Yes	No
Control Approach	Volt. Matching Control	Not Reported	Voltage-Mode Control	Not Reported	Voltage-Mode Control	Volt. Matching Control	PWM-PPS Control	Current-Mode Control	PWM-PPS Control	Current-Mode Control[2]
Volt. Stress of LVS Switches[3]	$\frac{V_H}{2N+1}$	$\frac{V_H}{1+N(2-D)}$	$\frac{V_H}{N+2}$	$\frac{V_H}{N+2}$	$\frac{V_H}{N+2}$	$\frac{V_H}{N+1}$	$\frac{V_H}{N+1}$	$\frac{V_H}{N(N+1)+1}$	$\frac{V_H}{N+2}$	$\frac{V_H}{2(1+N)}$
Volt. Stress of HVS Switches[3]	$\frac{NV_H}{2N+1}$	$\frac{NV_H}{1+N(2-D)}$	$\frac{(N+1)V_H}{N+2}$	$\frac{(N+1)V_H}{N+2}$	$\frac{(N+1)V_H}{N+2}$	$\frac{NV_H}{N+1}$	$\frac{NV_H}{N+1}$	$\frac{(1+2N(1+N))V_H}{N+1}$	$\frac{(N+1)V_H}{N+2}$	V_H , $\frac{(2N+1)V_H}{2(N+1)}$
Voltage Gain[3]	$\frac{2N+1}{1-D}$	$\frac{1+N(2-D)}{1-D}$	$\frac{N+2}{1-D}$	$\frac{N+2}{1-D}$	$\frac{N+2}{1-D}$	$\frac{N+1}{1-D}$	$\frac{N+1}{1-D}$	$\frac{N(N+1)+1}{1-D}$	$\frac{N+2}{1-D}$	$\frac{2(1+N)}{1-D}$

[1]The losses of utilized circuits for control and gate drive are ignored.
[2]In both constant frequency operation and variable frequency control.
[3]3 In boost mode (D is the converter duty-cycle in boost mode) and in the ideal case ($k = 1$).



Note: The losses of utilized laboratory circuits for control and gate drive are included.

Fig. 16. Calculated and measured efficiency curves of the prototype converter versus output power under constant frequency operation and VFC.

provided by the manufacturer. For the selected core, the Steinmetz coefficients are $a = 246.54$, $b = 2.218$, and $c = 1.311$. In the end, a constant loss of 3 W is considered as "other losses" for the losses of the control and gate drive circuits, based on the utilized laboratory circuits.

As seen in Fig. 15, in VFC, compared to constant frequency operation, the conduction losses of the converter have a significant reduction at light loads. The reason is that, in VFC, as the output power is reduced, the switching frequency is increased; hence, the current ripple of the switches and inductors is reduced. It is worth mentioning that, based on the theoretical Steinmetz equation $P_C = aB^b f^c$ for calculating the core loss density, when the output power is reduced, the current ripple and the peak flux density B are reduced, but on the other hand, the switching frequency f is increased. Hence, as shown in Fig. 15, the core losses in VFC compared to constant frequency operation do not significantly reduce.

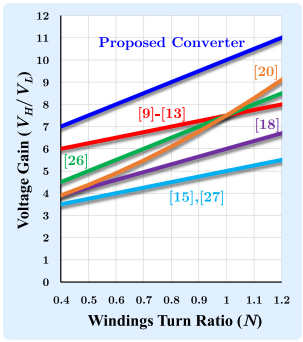
Based on the loss breakdown in Fig. 15, the calculated efficiency curves of the prototype converter are illustrated in Fig. 16. Besides, to confirm the validity of the loss analysis, the measured efficiency curves of the prototype converter are illustrated in Fig. 16. As seen, the experimental peak efficiencies of 95.6% and 95.9% are, respectively, obtained for boost and buck modes at full load (400 W) by considering the losses of utilized circuits for control and gate drive. Furthermore, regardless of control and gate drive circuit losses, the experimental peak efficiencies at full load in boost and buck modes are obtained 96.3% and 96.6%, respectively.

The key specifications comparison between the proposed converter and previous counterpart converters are presented in Table II. For better comparisons and based on Table II, the curves of the voltage gains and voltage stresses of the converters versus windings turn ratio (N) for the operating duty cycle of 0.6 in boost mode ($D = 0.6$) are plotted in Fig. 17.

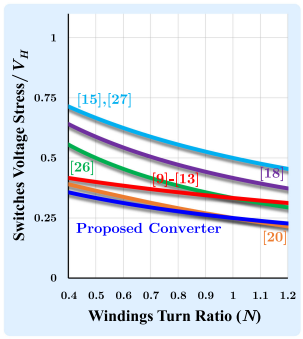
It can be seen that compared to other topologies, the HVS voltage stress of the proposed converter is higher. However, as seen in the loss analysis, despite using typical switches with high voltage rating for HVS switches, the overall conduction losses are small due to the low current levels of HVS switches. As a result, this drawback has no significant effect on the converter efficiency.

VI. CONCLUSION

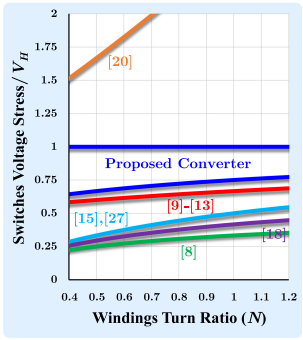
A high step-up/step-down converter is introduced, which provides features, such as bidirectional power-flow ability, excellent voltage gain, very low voltage stress of LVS switches, current sharing, current ripple cancelation, ZVS, elimination of diodes reverse recovery, reduced values of inductors and leakage inductors, and simple clamp circuit. The converter's operation in both boost and buck modes was comprehensively discussed. Besides, the converter specifications were presented, including the voltage gains in both the ideal and nonideal cases, the voltage stresses of switches in the ideal case, and current ripple cancelation feasibility. The design considerations were



(a)



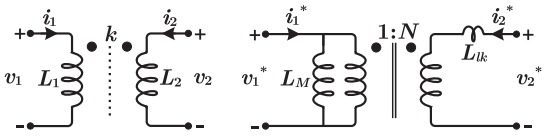
(b)



(c)

Fig. 17. Comparison between the proposed converter and previous counterpart converters in boost mode ($D = 0.6$). (a) Voltage gains. (b) Voltage stresses of LVS switches. (c) Voltage stresses of HVS switches.

presented considering ZVS in the converter's entire operating region. To improve the light-load efficiency, the VFC was investigated, including all the required equations. Finally, to verify the analysis, the experimental results of a 48–400 V, 400-W prototype converter were presented. Due to the proposed converter's superior voltage gain, the mentioned voltage conversion was obtained with reasonable duty cycle of 0.6 (in boost mode) and windings turn ratio of about 0.7. Moreover, the voltage stress of 120 V was achieved for LVS switches, and the voltage stresses of upper and lower HVS switches were, respectively, obtained 400 and 280 V. The prototype converter's experimental waveforms were all matched with the theoretical analysis. The experimental efficiencies of 95.6% and 95.9% were obtained for boost and buck modes at full load (400 W), respectively. Furthermore, regardless of control and gate drive



(a) (b)

Fig. 18. Equivalent circuit of coupled inductors. (a) Coupled inductors. (b) Equivalent circuit.

circuits losses, the experimental peak efficiencies at full load in boost and buck modes were, respectively, achieved 96.3% and 96.6%. Besides, the measured efficiencies of VFC compared to constant frequency operation at 25% of full load (100 W) show the improvement of 3% and 2.4% in boost and buck modes, respectively.

APPENDIX

Here, the parameters of the utilized model for coupled inductors are obtained. From Fig. 18(a), v_1 and v_2 are

$$v_1 = L_1\frac{di_1}{dt} + k\sqrt{L_1L_2}\frac{di_2}{dt} \tag{38}$$

$$v_2 = k\sqrt{L_1L_2}\frac{di_1}{dt} + L_2\frac{di_2}{dt}. \tag{39}$$

From the equivalent circuit of the coupled inductor in Fig. 18(b), v_1^* and v_2^* are

$$v_1^* = L_M\frac{di_1^*}{dt} + NL_M\frac{di_2^*}{dt} \tag{40}$$

$$v_2^* = NL_M\frac{di_1^*}{dt} + (L_{lk} + N^2L_M)\frac{di_2^*}{dt}. \tag{41}$$

From (38)–(41), considering $v_1 = v_1^*$, $v_2 = v_2^*$, $i_1 = i_1^*$, and $i_2 = i_2^*$, the parameters of the equivalent circuit would be

$$L_M = L_1 \tag{42}$$

$$L_{lk} = (1 - k^2)L_2 \tag{43}$$

$$N = k\sqrt{\frac{L_2}{L_1}}. \tag{44}$$

REFERENCES

[1] K. Jin, X. Ruan, M. Yang, and M. Xu, "A hybrid fuel cell power system," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1212–1222, Apr. 2009.
[2] A. Khaligh and Z. Li, "Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art," *IEEE Trans. Veh. Technol.*, vol. 59, no. 6, pp. 2806–2814, Jul. 2010.
[3] A. Nasiri, Z. Nie, S. B. Bekiarov, and A. Emadi, "An on-line UPS system with power factor correction and electric isolation using BIFRED converter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 722–730, Feb. 2008.
[4] A. Tavakoli, S. A. Khajehoddin, and J. Salmon, "A modular battery voltage-balancing system using a series-connected topology," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5952–5964, Jun. 2020.
[5] E. M. Krieger, "Effects of variability and rate on battery charge storage and lifespan," Ph.D. dissertation, Dept. Mech. Aerosp. Eng., Princeton Univ., Princeton, NJ, USA, Jan. 2013.
[6] N. Rana and S. Banerjee, "Development of an improved input-parallel output-series buck-boost converter and its closed-loop control," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6428–6438, Aug. 2020.

[7] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a non-resonant single-phase dual-active-bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148–3172, Mar. 2020.

[8] F. Zahin, A. Abasian, and S. A. Khajehoddin, "An alternative dual active bridge modulation to minimize RMS current and extend ZVS range," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 5952–5959.

[9] Y. Zhang, H. Liu, J. Li, and M. Sumner, "A low-current ripple and wide voltage-gain range bidirectional DC-DC converter with coupled inductor," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1525–1535, Feb. 2020.

[10] R. Hu, J. Zeng, J. Liu, and K. W. E. Cheng, "A nonisolated bidirectional DC-DC converter with high voltage conversion ratio based on coupled inductor and switched capacitor," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1155–1165, Feb. 2021.

[11] Z. Hosseinzadeh, N. Molavi, and H. Farzanehfard, "Soft-switching high step-up/down bidirectional DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4379–4386, Jun. 2019.

[12] W. Hassan, J. L. Soon, D. Dah-Chuan Lu, and W. Xiao, "A high conversion ratio and high-efficiency bidirectional DC-DC converter with reduced voltage stress," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11827–11842, Nov. 2020.

[13] N. Molavi, E. Adib, and H. Farzanehfard, "Soft-switching bidirectional DC-DC converter with high voltage conversion ratio," *IET Power Electron.*, vol. 1, no. 1, pp. 33–42, Jan. 2018.

[14] H. Liu, L. Wang, Y. Ji, and F. Li, "A novel reversal coupled inductor high-conversion-ratio bidirectional DC-DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4968–4979, Jun. 2018.

[15] H. Wu, K. Sun, L. Chen, L. Zhu, and Y. Xing, "High step-up/step-down soft-switching bidirectional DC-DC converter with coupled-inductor and voltage matching control for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2892–2903, May 2016.

[16] S. M. P., M. Das, and V. Agarwal, "Design and development of a novel high voltage gain, high-efficiency bidirectional DC-DC converter for storage interface," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4490–4501, Jun. 2019.

[17] Y. T. Yau, W. Z. Jiang, and K. I. Hwu, "Bidirectional operation of high step-down converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6829–6844, Dec. 2015.

[18] Y. Hsieh, J. Chen, L. Yang, C. Wu, and W. Liu, "High-conversion-ratio bidirectional DC-DC converter with coupled inductor," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 210–222, Jan. 2014.

[19] M. Packnezhad and H. Farzanehfard, "Soft switching high step up/down converter using coupled inductors with minimum number of components," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 7938–7945, Sep. 2021.

[20] M. Shaneh, M. Niroomand, and E. Adib, "Non-isolated interleaved bidirectional DC-DC converter with high step voltage ratio and minimum number of switches," *IET Power Electron.*, vol. 12, no. 6, pp. 1510–1520, May 2019.

[21] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of high-step-up coupled-inductor boost converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 689–704, Jun. 2016.

[22] M. R. Mohammadi, B. Poorali, S. Eren, and M. Pahlevani, "A non-isolated TCM bidirectional converter with low input-current-ripple for DC microgrids," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10845–10855, Nov. 2021.

[23] A. R. Naderi Akhormeh, K. Abbaszadeh, M. Moradzadeh, and A. Shahirinia, "High gain bidirectional quadratic DC-DC converter based on coupled inductor with current ripple reduction capability," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 7826–7837, Sep. 2021.

[24] Z. Yan, J. Zeng, W. Lin, and J. Liu, "A novel interleaved nonisolated bidirectional DC-DC converter with high voltage-gain and full-range ZVS," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7191–7203, Jul. 2020.

[25] Z. Yan, J. Zeng, Z. Guo, R. Hu, and J. Liu, "A soft-switching bidirectional DC-DC converter with high voltage-gain and low voltage stress for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 6871–6880, Aug. 2021.

[26] H. Bahrami, S. Farhangi, H. Iman-Eini, and E. Adib, "Analysis, design, and implementation of DC-DC IBBC-DAHB converter with voltage matching to improve efficiency," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5209–5219, Jul. 2019.

[27] H. Wu, Y. Lu, L. Chen, P. Xu, X. Xiao, and Y. Xing, "High step-up/step-down non-isolated BDC with built-in DC-transformer for energy storage systems," *IET Power Electron.*, vol. 9, no. 13, pp. 2571–2579, Oct. 2016.

[28] J. Yao, A. Abramovitz, and K. Ma Smedley, "Steep-gain bidirectional converter with a regenerative snubber," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6845–6856, Dec. 2015.

[29] M. Packnezhad and H. Farzanehfard, "Bidirectional soft switching converter with reduced current ripple at low voltage side," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4668–4675, Aug. 2021.

[30] N. A. Dung, H. Chiu, Y. Liu, and P. J. Huang, "Analysis and implementation of a high voltage gain 1 MHz bidirectional DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1415–1424, Feb. 2020.

[31] Y. Zhang, Q. Liu, J. Li, and M. Sumner, "A common ground switched-quasi-Z-source bidirectional DC-DC converter with wide-voltage-gain range for EVs with hybrid energy sources," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5188–5200, Jun. 2018.

[32] S. H. Hosseini, R. Ghazi, and H. Heydari-Doostabad, "An extendable quadratic bidirectional DC-DC converter for V2G and G2V applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4859–4869, Jun. 2021.

[33] S. M. Fardahar and M. Sabahi, "New expandable switched-capacitor/switched-inductor high-voltage conversion ratio bidirectional DC-DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2480–2487, Mar. 2020.

[34] Y. Zhang, W. Zhang, F. Gao, S. Gao, and D. J. Rogers, "A switched-capacitor interleaved bidirectional converter with wide voltage-gain range for super capacitors in EVs," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1536–1547, Feb. 2020.

[35] N. Elsayad, H. Moradisizkoohi, and O. A. Mohammed, "Design and implementation of a new transformerless bidirectional DC-DC converter with wide conversion ratios," *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 7067–7077, Sep. 2019.

[36] Y. Zhang, Y. Gao, L. Zhou, and M. Sumner, "A switched-capacitor bidirectional DC-DC converter with wide voltage gain range for electric vehicles with hybrid energy sources," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9459–9469, Nov. 2018.

[37] Y. Zhang, Y. Gao, J. Li, and M. Sumner, "Interleaved switched-capacitor bidirectional DC-DC converter with wide voltage-gain range for energy storage systems," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3852–3869, May 2018.

[38] N. Elsayad, H. Moradisizkoohi, and O. A. Mohammed, "A new hybrid structure of a bidirectional DC-DC converter with high conversion ratios for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 69, no. 1, pp. 194–206, Jan. 2020.

[39] D. Flores Cortez, G. Waltrich, J. Fraigneaud, H. Miranda, and I. Barbi, "DC-DC converter for dual-voltage automotive systems based on bidirectional hybrid switched-capacitor architectures," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3296–3304, May 2015.

[40] Y. Zhang, Q. Liu, Y. Gao, J. Li, and M. Sumner, "Hybrid switched-capacitor/switched-quasi-z-source bidirectional DC-DC converter with a wide voltage gain range for hybrid energy sources EVs," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2680–2690, Apr. 2019.

[41] A. Kumar, X. Xiong, X. Pan, M. Reza, A. R. Beig, and K. A. Jaafari, "A wide voltage gain bidirectional DC-DC converter based on quasi Z-source and switched capacitor network," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 68, no. 4, pp. 1353–1357, Apr. 2021.

[42] Z. Wang, P. Wang, B. Li, X. Ma, and P. Wang, "A bidirectional DC-DC converter with high voltage conversion ratio and zero ripple current for battery energy storage system," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8012–8027, Jul. 2021.

[43] M. R. Mohammadi, "A lossless turn-on snubber for reducing diode reverse recovery losses in bidirectional buck/boost converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 1396–1399, Feb. 2020.

[44] M. R. Mohammadi, "An active-clamping ZVS interleaved buck/boost bi-directional converter with one auxiliary switch," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7430–7438, Sep. 2010.

[45] A. Rodriguez, A. Vazquez, M. R. Rogina, and F. Briz, "Synchronous boost converter with high efficiency at light load using QSW-ZVS and SiC mosfets," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 386–393, Jan. 2018.

[46] J. Zhang, J. S. Lai, R. Y. Kim, and W. Yu, "High-power density design of a soft-switching high-power bidirectional dc-dc converter," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1145–1153, Jul. 2007.

[47] W. Li, Y. Zhao, J. Wu, and X. He, "Interleaved high step-up converter with winding-cross-coupled inductors and voltage multiplier cells," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 133–143, Jan. 2012.

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