Letters

A Fast Droop-Recovery Event-Driven Digital LDO With Adaptive Linear/Binary Two-Step Search for Voltage Regulation in Advanced Memory

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***Abstract*—This letter presents an event-driven digital low-dropout regulator (DLDO) with an adaptive linear/binary two-step search achieving a fast transient response. A two-dimensional (2-D) circular shifting register (CSR) offers an adaptive linear-search regulation. When a large voltage droop occurs, the CSR activates a fast-tracking mode that provides immediate recovery from the droop. Once the linear search by the CSR is completed, a subrange successive-approximation register (Sub-SAR) conducts the binary-search regulation. The full-scale current range of the Sub-SAR is adaptively scaled by referencing the CSR, which reduces the number of searching steps and improves undershoot or overshoot caused by the binary-search operation. Ring amplifier based 1.5b continuous-time (CT) comparators and the asynchronous controllers realize the event-driven operation that breaks a tradeoff between transient response and sampling clock frequency. The proposed DLDO was fabricated in a 40 nm CMOS process. The DLDO can operate in an input voltage $V_{\rm IN}$ range from 0.6 to 1.2 V. When a load current step of 104.2 mA/1 ns was applied at a $V_{\rm IN}$ of 1.0 V, a droop-recovery time and a settling time were measured as 6 and 15 ns, respectively.**

***Index Terms*—Advanced memory system, auto-zeroing inverter, binary search, circular shifting register (CSR), digital low-dropout regulator, event driven, fast transient response, linear search, low-dropout regulator (LDO), ring-amplifier based comparator (RA-CMP), subrange SAR.**

I. Introduction

RECENT technologies in memory systems, such as embedded DRAM (eDRAM), resistive RAM (Re-RAM), and phase-change RAM (PC-RAM), require a dedicated power management scheme because of their increased power density and data rate [1]. Sensing all bit-line data per word-line activation draws a large current, causing a significant voltage droop that should be recovered within tens of ns, which is the access period of each bank. However, sub-1V supply voltage makes it difficult to attain the fast recovery using analog low-dropout regulators. A digital low-dropout regulator (DLDO) can be applied to memory systems to realize low-voltage regulation with fast response [2]. Nevertheless, such memory systems impose several critical constraints on the DLDO. An operating clock frequency $f_{\rm CLK}$ is limited to tens of MHz, worsening the transient response. In addition, an on-chip output capacitor $C_{\rm OUT}$, which only have hundreds of pF, causes a large voltage droop by the steep load current variation.

In addressing performance degradation by the $f_{\rm CLK}$ and $C_{\rm OUT}$ constraints, several schemes have been reported to improve the transient response. While a linear search based on a barrel shift register [3]–[5] can improve the regulation speed, multistep control increases the structural complexity and requires a multibit analog-to-digital converter [5]. Another approach is a binary search based on a successive-approximation register (SAR) [6]. The binary-search regulation can provide a fast transient response, but trial-and-comparison procedure of the SAR operation can cause significant overshoot or undershoot.

This letter proposes an event-driven DLDO with an adaptive two-step search procedure that aims to achieve fast droop recovery with mitigation of the $f_{\rm CLK}$ and $C_{\rm OUT}$ constraints. Fig. 1

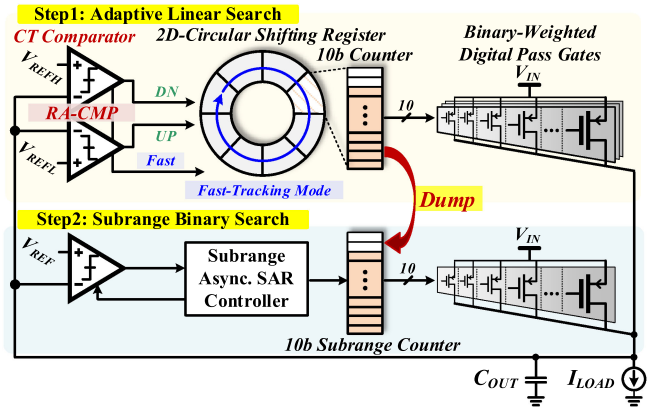

Fig. 1. Overall architecture of proposed DLDO.

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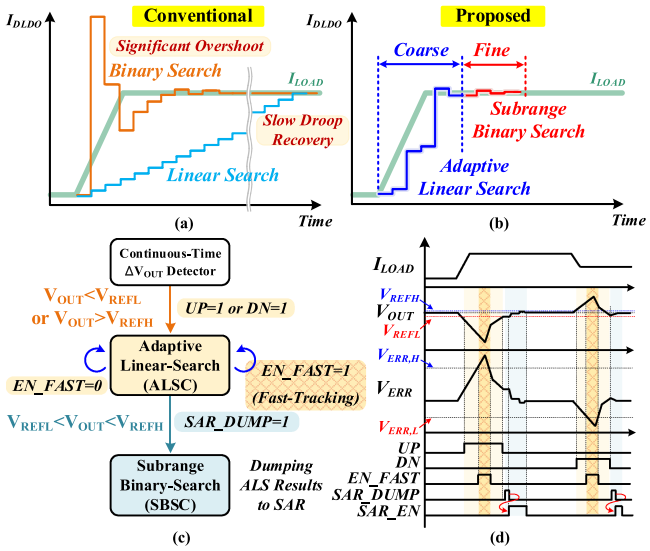


Fig. 2. Conceptual procedures. (a) Conventional linear/binary searches. (b) Proposed two-step adaptive search. (c) State diagram of proposed searching procedure. (d) Timing diagram of proposed DLDO operation.

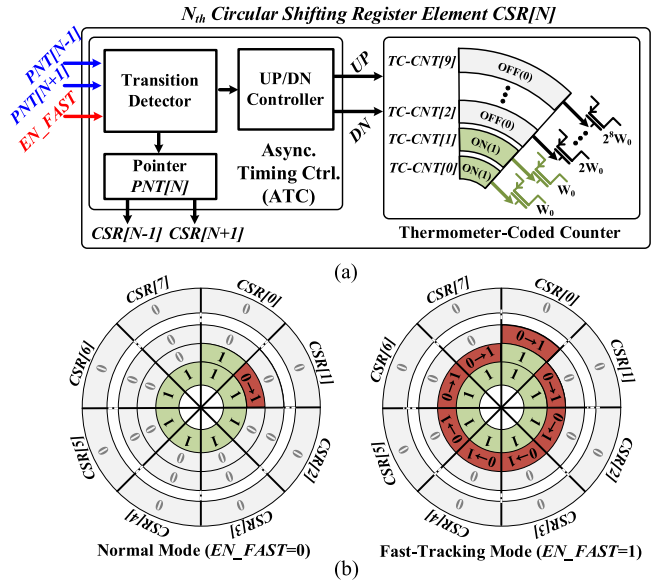


Fig. 3. (a) Block diagram of the CSR element. (b) Comparison between normal mode and fast-tacking mode.

shows the proposed architecture, which combines an adaptive linear search and a subrange binary search. A continuous-time (CT) ring amplifier based comparator (RA-CMP) realizes the event-driven operation overcoming the f_{CLK} constraint. A two-dimensional circular shifting register (2D-CSR) conducts the adaptive linear-search regulation by boosting recovery from the voltage droop. Then, a subrange SAR performs the binary-search regulation with an adaptive current range, thus reducing overshoot or undershoot.

This letter is organized as follows. Section II explains the operating principle and overall architecture of the proposed DLDO. Section III describes the circuit implementation in detail. The measurement results are presented in Section IV. Finnally, Section V concludes this letter.

II. Operating Principle and Architecture

Fig. 2(a) shows the conceptual searching procedures for conventional DLDOs. The linear-search DLDO has limitation of the slow transient response, while the binary-search DLDO shows large overshoot or undershoot during regulation. Conversely, the proposed searching procedure shown in Fig. 2(b) performs an adaptive linear search for coarse-step regulation and a subrange binary search for fine-step regulation, providing fast transient response without significant shootings. Fig. 2(c) and (d) shows the state diagram and the timing diagram of the proposed searching procedure, respectively. When V_{OUT} becomes lower than V_{REFL} or higher than V_{REFH}, the RA-CMP triggers an adaptive linear-search controller (ALSC) by activating *UP* or *DN* signal. The ALSC adjusts the searching steps adaptively based on an amplified output error V_{ERR}. When a large V_{ERR} is detected, a fast-tracking mode is enabled to increase the number of searching steps for fast V_{ERR} recovery. Otherwise, the ALSC updates the CSR sequentially.

After the linear-search regulation, a subrange binary-search controller (SBSC) triggers *SAR_DUMP* to set an adaptive binary-search range by referring to the turn-ON bits of the CSR. After that, *SAR_EN* is enabled to start the subrange successive-approximation register (Sub-SAR) for the fine-step regulation. The subrange operation can reduce not only the number of searching steps but also the undershoot or overshoot in V_{OUT} by eliminating overflow bits. In addition, the asynchronous operations of the ALSC and SBSC allow the DLDO to achieve fast transient response, despite the f_{CLK} limitation.

A. ALSC With 2-D Circular Shifting Register

The ALSC is implemented with the 2D-CSR and the corresponding binary-weighted pass gate arrays. Fig. 3(a) shows the block diagram of the 2D-CSR element. Each CSR element consists of an asynchronous timing controller (ATC), a 1b register as a pointer, and a 10b thermometer-coded counter (TC-CNT). The 2-D configuration of the 10b TC-CNT in each element allows the ALSC to realize the fast-tracking mode easily by updating either a single element or eight elements entirely. The ATC manages the asynchronous operations of the pointer and the TC-CNT in the same element. During the ALSC operation, the activated pointer moves clockwise or counter-clockwise, which corresponds to shifting up or down, respectively. At the CSR element where the pointer is activated, the TC-CNT increases or decreases its value according to *UP* or *DN* signal. If the RA-CMP triggers *EN_FAST* due to a large output variation, all elements in the 2D-CSR are updated at once in increment or decrement, as shown in Fig. 3(b). The fast-tracking mode can increase or decrease the current by double considering the previous regulation. Thus, the ALSC realizes a boosted recovery from the voltage droop without critical undershoot or overshoot. At this time, the regulation speed of the ALSC is mainly determined by the number of updated elements and logic delay per searching step. Considering stability of the

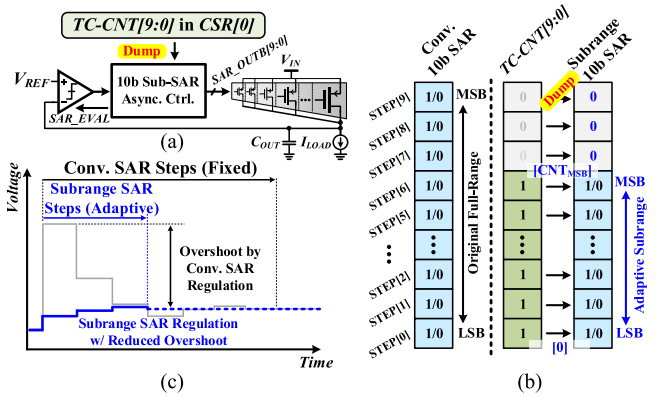


Fig. 4. (a) Block diagram of the SBSC. Operational principles of (b) subrange-decision procedure and (c) adaptive subrange SAR regulation.

DLDO, the maximum number of updated elements was designed as eight during the fast-tracking mode. The postlayout simulated logic delay per update was about 1 ns at $V_{\rm IN}$ of 1 V, realizing fast regulation speed without use of several GHz clock.

B. SBSC With Subrange Successive-Approximation Register

The SBSC is implemented by a 10b Sub-SAR, as shown in Fig. 4(a). At the start of the SBSC, *TC-CNT* [9 : 0] in *CSR*[*0*] is transferred to the Sub-SAR. As illustrated in Fig. 4(b), when *TC-CNT* [CNT_{MSB}*:0*] has turn-ON bits ("1"), the Sub-SAR conducts the binary search from CNT_{MSB} to 0 instead of a fixed number of steps. In this way, the Sub-SAR adaptively adjusts a full-range of the successive approximation according to the ALSC status. The subrange operation provides a faster binary search by eliminating the overflow bit, thus reducing undershoot or overshoot during the trial-and-comparison procedure, as shown in Fig. 4(c).

C. Stability Analysis

Fig. 5(a) shows the discrete-time DLDO model and open-loop transfer function. The DLDO control model is constructed with RA-CMP, ALSC, SBSC, zero-order hold (ZOH), and CT output stage. $F_{\rm CLK}$ and $F_{\rm OUT}$ are the equivalent operating frequency of the control model and output stage pole, respectively. The dc gain $K_{\rm DC}$ comes from current conversion ratio of the output stage. The RA-CMP is modeled with a comparator considering the detection delay which is the same range with logic delay in the following digital controller. The ALSC and SBSC are modeled with $K_{\rm SR}$ and $K_{\rm SAR}$, which represent gains of each control stages, respectively. Using the discrete-time model, stability of the DLDO was analyzed as shown in Fig. 5(b). With the load current $I_{\rm LOAD}$ of 10 and 100 mA conditions, pole analyses versus $K_{\rm SR}$ and $K_{\rm SAR}$ were conducted. According to the design of the ALSC and SBSC, $K_{\rm SR}$ and $K_{\rm SAR}$ are not larger than eight and two, respectively. In those $K_{\rm SR}$ and $K_{\rm SAR}$ ranges, the DLDO shows stable operation as shown in Fig. 5(b).

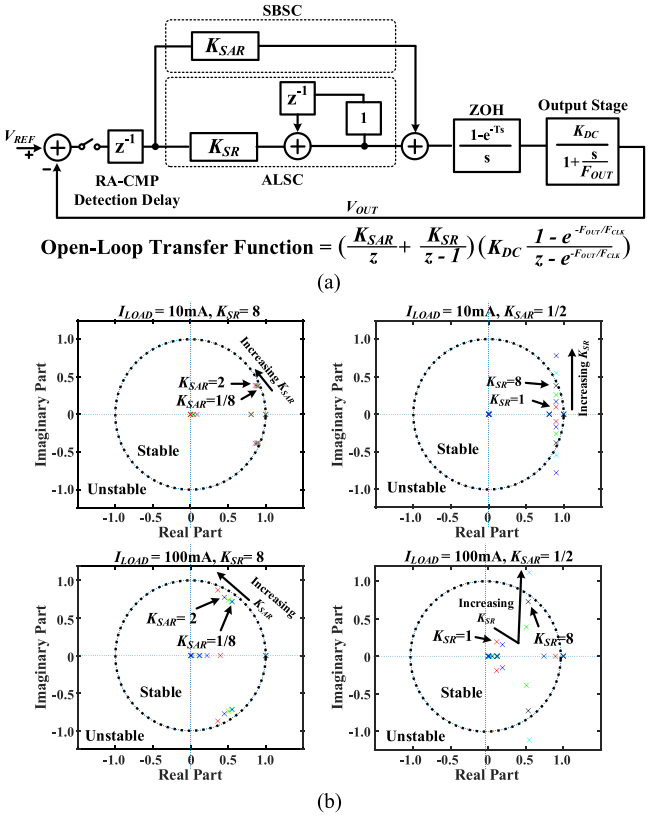


Fig. 5. (a) Discrete-time DLDO control model and (b) pole plots of the DLDO model at $I_{\rm LOAD}$ of 10 and 100 mA across $K_{\rm SR}$ and $K_{\rm SAR}$, respectively.

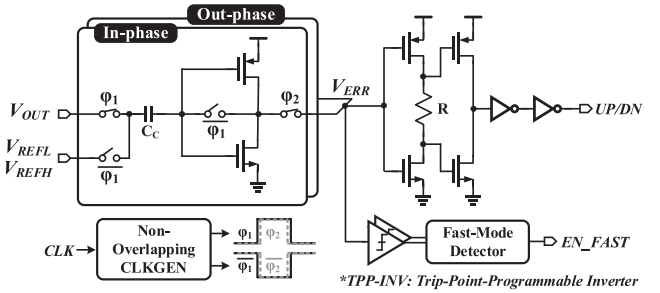


Fig. 6. Circuit implementation of the RA-CMP.

III. Circuit Implementations

A. Time-Interleaved Ring Amplifier Based Comparator

Fig. 6 shows the schematic of 1.5 b RA-CMP that compares $V_{\rm OUT}$ with $V_{\rm REFH}$ and $V_{\rm REFL}$. Each comparator is implemented with time-interleaved ring amplifiers to offer a seamless conversion [7]. When $V_{\rm ERR}$ exceeds a boundary range from $V_{\rm ERR,L}$ to $V_{\rm ERR,H}$, *EN_FAST* is activated, and the ALSC conducts fast-tracking regulation. Out-of-range detection of $V_{\rm ERR}$ is realized by trip-point programmable inverters (TPP-INV) [8] that provide CT detection.

The RA-CMP can operate with auto-zeroing frequency $F_{\rm AZ}$ ranging from 10 kHz to 100 MHz. The $F_{\rm AZ}$ can be determined depending on available clock frequency, power-supply rejection bandwidth, or $V_{\rm REF}$ tracking speed. Fig. 7 shows

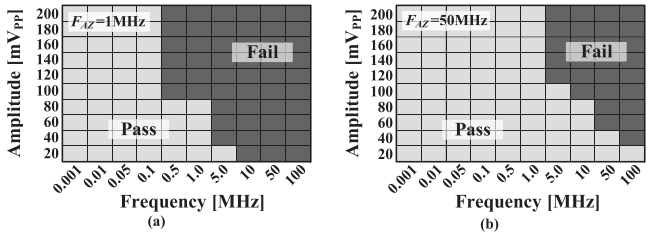


Fig. 7. Simulated Shmoo plots for supply-ripple sensitivity of the RA-CMP at (a) $F_{\mathrm{AZ}} = 1$ MHz and (b) $F_{\mathrm{AZ}} = 50$ MHz.

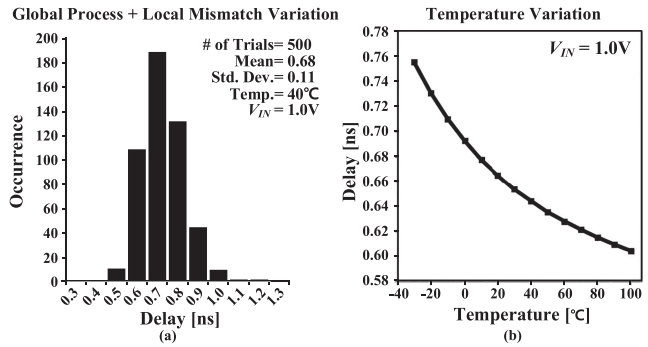


Fig. 8 (a) Monte Carlo simulation of the RA-CMP detection delay under global-local process variation with 500 trials. (b) Simulated detection delay of the RA-CMP versus temperature.

Shmoo plots indicating operation of the RA-CMP when supply ripple is injected with frequency range from 1 kHz to 100 MHz and amplitude range from 20 to 200 $\mathrm{mV_{PP}}$. If the RA-CMP generates *UP* or *DN* signals due to the power-supply ripple at the given amplitude and frequency, the corresponding ripple injection condition is marked as "Fail." Because of the auto-zeroing process in the RA-CMP, higher F_{AZ} offers more robustness to the power-supply ripple [7]. Therefore, the F_{AZ} can be chosen depending on the required power-supply rejection (PSR) performance of the DLDO. Fig. 8(a) shows the Monte Carlo simulations of the RA-CMP detection delay with 500 trials. Under the global process variation and local mismatch effect, the RA-CMP maintains fast detection delay below 1 ns, which ensures robustness to the process variation. To examine a sensitivity to temperature variation, the detection delays of the RA-CMP were simulated by varying operating temperature from -30 to 100°C as shown in Fig. 8(b). The simulated detection delay ranges from 0.6 to 0.76 ns, which guarantees the RA-CMP operation within the wide temperature range.

B. Asynchronous 2-D Circular Shifting Register

Fig. 9(a) shows the circuit implementation of the 2D-CSR element. The 1b pointer and 10b TC-CNT are implemented using a C-element that offers asynchronous operation. The ATC in *CSR* [*N*] updates their pointer and TC-CNT by detecting transitions in adjacent CSRs while *UP* or *DN* signal is activated. However, the fast-tracking mode can cause a limit-cycle oscillation (LCO) due to propagation delay in the ALSC. To prevent the LCO that alternates *UP* and *DN* signals, an LCO detector is realized with cascaded flip-flops triggered by *UP* or *DN* in sequence, as shown

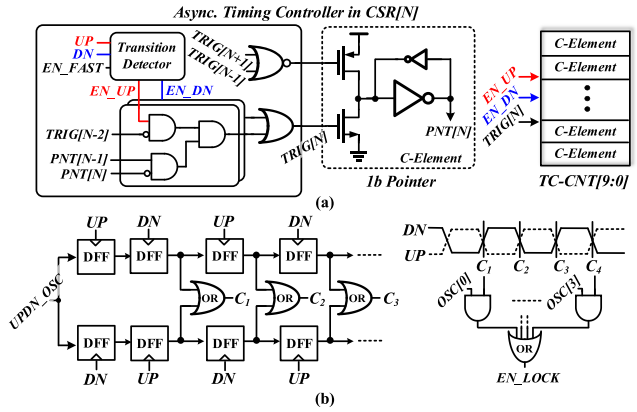


Fig. 9 Circuit implementations of (a) the 2D-CSR and (b) the limit-cycle-oscillation detector.

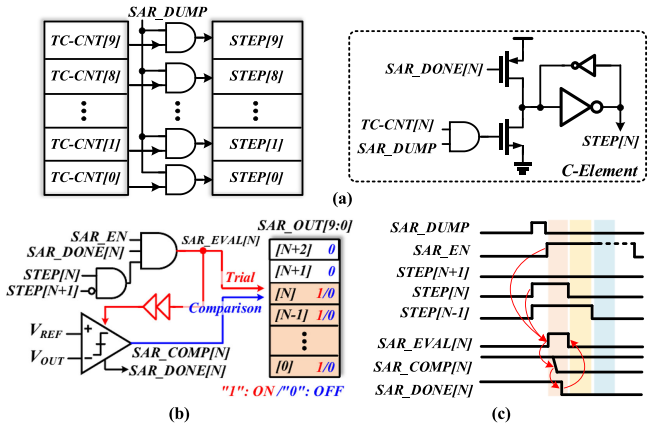
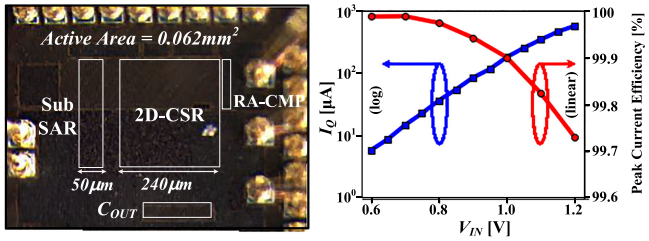


Fig. 10 Circuit implementations of (a) the adaptive subrange register and (b) the SAR control logic. (c) Timing diagram of the asynchronous Sub-SAR operation.

in Fig. 9(b). The number of allowed *UP/DN* oscillations can be programmable via *OSC* [*3:0*]. When the LCO detector activates *EN_LOCK*, the fast-tracking mode is forced to be turned OFF, and the ALSC can exit from the LCO.

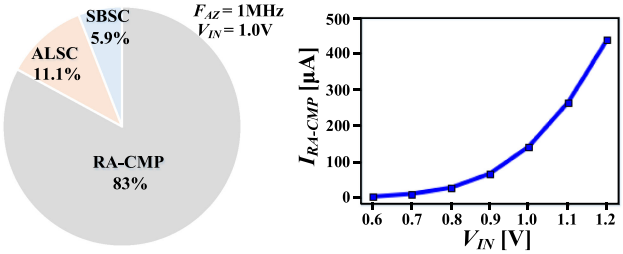
C. Subrange Successive Approximation Register

Fig. 10(a) shows the implementation of the asynchronous 10b Sub-SAR. The subrange operation is realized by dumping 10b *TC-CNT* [*9:0*] of *CSR* [*0*] into *STEP* [*9:0*], which is a 10b C-element register for indicating the binary-search step. The overflow bits are initiated to turn-OFF bit ("0") and the subrange bits are initiated to turn-ON bit ("1") for the following trial-and-comparison procedures. Fig. 10(b) and (c) show the SAR control logic and its timing diagram. If the boundary of turn-ON and turn-OFF bit in *STEP* [*9:0*] is *STEP* [*N*], the SAR controller performs the binary search by activating *SAR_EVAL* [*N*], which triggers a strong-arm latch comparator. After the trial-and-comparison procedures, the SAR output register *SAR_OUT* [*N*] is updated according to the comparator output *SAR_COMP* [*N*]. Then, *SAR_DONE* [*N*] and *STEP* [*N*] are disabled and the next searching step is conducted at *STEP* [$N-1$] stage. In this way, the Sub-SAR realizes the asynchronous operation and the adaptive number of search steps.



(a) (b)

Fig. 11 (a) Die photomicrograph of the fabricated DLDO. (b) Measured quiescent current and peak current efficiency versus input voltage V_{IN}.



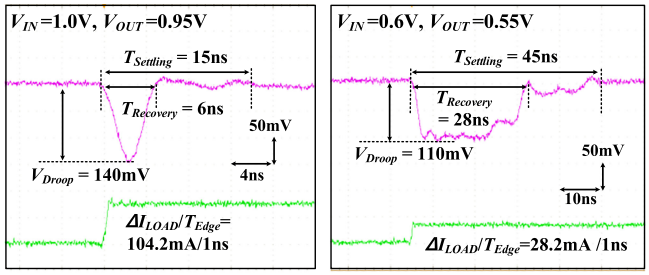
(a) (b)

Fig. 12 Simulated (a) power breakdown of the DLDO and (b) current consumption of the RA-CMP versus input voltage V_{IN}.

IV. Measurement Results

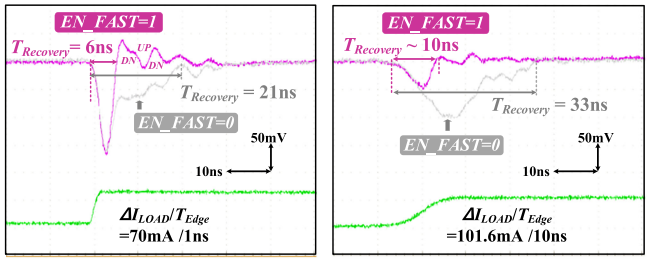
The prototype of the proposed DLDO was fabricated in a 40 nm CMOS process. Fig. 11(a) shows the die photomicrograph of the prototype. The fabricated DLDO occupies an active area of 0.062 mm^2 that includes an on-chip output capacitor of 150 pF. The DLDO supports input voltage V_{IN} ranging from 0.6 to 1.2 V at a dropout V_{DO} of 50 mV. The measured quiescent current and current efficiency versus V_{IN} are shown in Fig. 11(b). The DLDO achieves peak current efficiencies better than 99.7% across the entire V_{IN} range. In the measurements, a 1-MHz clock was applied to the RA-CMP for the time-interleaved operation, and other blocks did not use any clock source. Fig. 12(a) shows the power breakdown of the overall DLDO at V_{IN} of 1.0 V and F_{AZ} of 1 MHz. Owing to the asynchronous operation, the ALSC and SBSC consume only 11.1% and 5.9% of quiescent current. The RA-CMP occupies 83% of the entire quiescent current. Depending on the input voltage V_{IN}, the current consumption of the RA-CMP can be scaled efficiently as shown in Fig. 12(b).

Fig. 13 shows the measured load transient responses. At a V_{IN} of 1 V, a load current step of 104.2 mA was applied within an edge time T_{Edge} less than 1 ns. The DLDO achieves a droop-recovery time T_{Recovery} of 6 ns and a settling time T_{Settling} of 15 ns. The voltage droop V_{Droop} was measured as 140 mV. At a V_{IN} of 0.6 V with a load step of 28.2 mA, the DLDO achieves a T_{Recovery} of 28 ns and a T_{Settling} of 45 ns. Fig. 14 shows the comparison of load transient responses depending on the fast-tracking mode in the ALSC. At V_{IN} of 1.0 V, T_{Recovery} were significantly improved by the fast-tracking mode. Fig. 15(a) and (b) show the measured load regulation and line regulation across



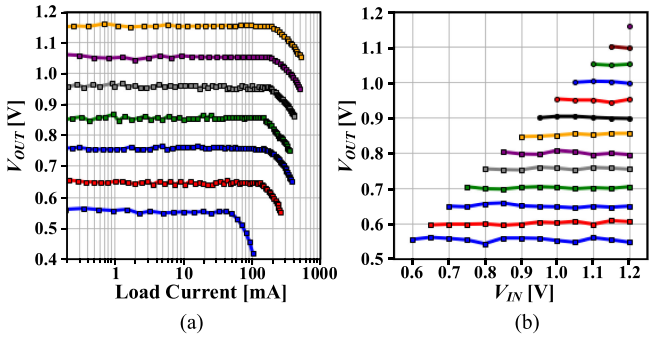
(a) (b)

Fig. 13 Measured load transient responses at V_{IN} of (a) 1.0 V and (b) 0.6 V.



(a) (b)

Fig. 14 Measured load transient improvements by fast-tracking mode with load steps of (a) 70 mA/1 ns and (b) 101.6 mA/10 ns at V_{IN} of 1.0 V.



(a) (b)

Fig. 15 Measured (a) load regulation and (b) line regulation.

the V_{IN} range, respectively. The two-step searching procedure achieves not only the fast droop recovery but also accurate regulation. Fig. 16 shows the postlayout simulation results of the PSR at F_{AZ} of 1, 10, and 50 MHz. The PSR can be improved by increasing F_{AZ}. The PSR is less sensitive to the load current I_{LOAD}, and the DLDO can maintain the PSR even if the load current is increased to full load condition. Table I shows the performance summary and comparison with other works [5], [6], [9], [10]. The proposed DLDO achieves highly improved transient responses of T_{Recovery} and T_{Settling}, providing a fast droop recovery for advanced memory systems.

V. Conclusion

This letter presented an event-driven DLDO with an adaptive two-step search for realizing a fast droop recovery in advanced

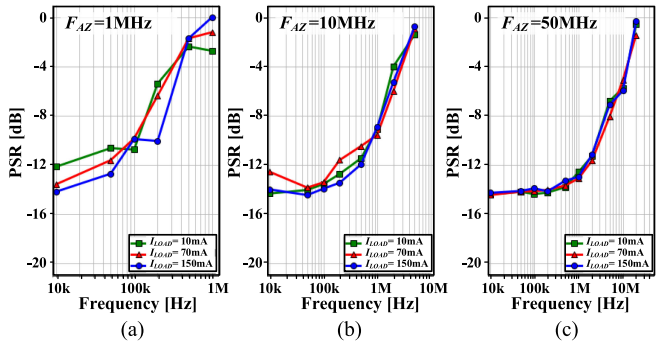


Fig. 16 Postlayout simulated PSRs at F_{AZ} of (a) 1 MHz, (b) 10 MHz, and (c) 50 MHz.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[5] ISSCC 2019	[6] JSSC 2018	[9] TPEL 2020	[10] TPEL 2021	This Work
Technology [nm]	65	65	130	110	**40**
Operating Type	Digital Time-Driven	Digital Time-Driven	Digital Time-Driven	Digital Time-Driven	**Digital Event-Driven**
f_{CLK} **[MHz]**	16-100	1-240	250	100	**1**
Search Type	Computational	Binary/ PD/PWM	Adaptive	Variable Step-Size	**Adaptive Linear-Binary**
V_{IN} **[V]**	0.65-1.15	0.5-1	0.5-1.22	0.8-1.2	**0.6-1.2**
V_{OUT} **[V]**	0.6-1.1	0.3-0.45	0.35-1.17	0.7-1.1	**0.55-1.15**
$I_{LOAD,MAX}$ **[mA]**	16.3	2	145	50	**200**
C_{LOAD} **[nF]**	0.25	0.4	1.5	0.04	**0.15**
I_Q **[µA]**	80-1200	14	3200	188.8-197.9	**6-550**
$T_{Recovery}$ **[ns]** @ V_{IN}, f_{CLK}	N/A	N/A	N/A	67 @ 1V, 100MHz	**6 @ 1V, 1MHz**
$T_{Settling}$ **[ns]** @ V_{IN}, f_{CLK}	27.9 @ 1.1V, 100MHz	100 @ 0.5V, 100MHz	55 @ 0.98V, 250MHz	N/A	**16 @ 1V, 1MHz**
ΔV_{Droop} **[mV]** @ $\Delta I_{LOAD}/T_{Edge}$	46 @ 5.6mA/0.1ns	40 @ 1.06mA/1ns	280 @ 40mA/0.1ns	360 @ 47.5mA/1ns	**140 @ 104.2mA/1ns**
Peak Current Efficiency [%]	99.7	99.8	97.8	92.98-99.61	**> 99.7**
FoM$_1$ [ps] *	29.3^{+}	199^{+}	63.9^{+}	1.26^{+}	**5.36**
FoM$_2$ [ps] **	N/A	N/A	N/A	107.2	**1.527**

*$\mathrm{FOM}_1 = T_R\,(I_Q/\Delta I_{LOAD})$, ${T_R}^{+} = C_{LOAD}\,(\Delta V_{Droop}/\Delta I_{LOAD})$ at $T_R >> T_{Edge}$, T_R = *Response time*.
$\mathrm{FOM}_2 = T_{Recovery}\,(\Delta V_{Droop}/V_{OUT})(I_Q/\Delta I_{LOAD})$ **[11].

memory systems. The time-interleaved RA-CMP and the asynchronous two-step regulation offer an immediate response to the load variation. The ALSC with 2D-CSR and the SBSC with 10b Sub-SAR provide fast regulation with mitigation of undesirable output shootings. The DLDO achieves a fast droop recovery within 6 ns and a settling time of 15 ns against a 104.2 mA/1 ns load current step at V_{IN} of 1 V.

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