# A Battery Charging Method With Natural Synchronous Rectification Features for Full-Bridge *CLLC* Converters

Huan Chen, *Student Member, IEEE*, Kai Sun, *Senior Member, IEEE*, Haixu Shi, *Member, IEEE*, Jung-Ik Ha, *Fellow, IEEE*, and Sangwon Lee, *Student Member, IEEE*

***Abstract*—The *CLLC* converter is a promising topology for bidirectional power conversation applications, such as vehicle-to-grid (V2G) systems and battery energy storage (BES) systems. Battery charging is one of the most important functions of the *CLLC* converter in V2G and BES applications. Synchronous rectification (SR) is of vital importance in these applications because it can increase efficiency. In this article, a battery charging method with natural SR features is proposed for the full-bridge *CLLC* converter. The proposed method consists of a parameter matching design procedure and SR control. A novel SR principle is adopted in this article. Different from the current SR methods, the parameter design process is taken into consideration for the SR realization. After the parameter matching design procedure, the required ON-state time of the secondary side switches for the SR is nearly fixed during the whole charging process. As a result, the SR drive signal can be generated directly according to the switching frequency. No sensor detection or software estimation is needed, allowing natural SR to be realized. A lab-level prototype was built to verify the proposed method. The experimental results show an obvious efficiency improvement (up to 2.11%) over the uncontrolled rectification, and the SR of the proposed method is nearly the same as complete SR (with maximum efficiency difference of 0.31%) during the whole battery charging process.**

***Index Terms*—Battery charging, *CLLC* converter, parameter matching design, synchronous rectification (SR).**

## I. Introduction

THE *CLLC* converter is a high-frequency and high-efficiency isolated bidirectional dc/dc converter, which has drawn attention from academia and industry in recent years. The *CLLC* converter has excellent soft-switching characteristics [1], [2]. As a result, it is regarded as a promising topology for bidirectional power transmission.

The application fields of the *CLLC* converter include uninterrupted power supply systems, dc distribution systems, vehicle-to-grid (V2G) systems, battery energy storage (BES) systems, more electric aircraft, and reversible solid oxide fuel cell systems [1]–[7]. One of the research questions of the *CLLC* converter in V2G and BES systems is topology improvement. Three-level *CLLC* topology and the three-phase *CLLC* topology are proposed for off-board bidirectional electric vehicle (EV) chargers in [8] and [9]. Several two-stage *CLLC* topologies are proposed for BES systems in [10]–[12]. In order to achieve higher frequency, higher efficiency, and higher power density, advanced wide band gap devices and magnetic technologies are introduced to the *CLLC* converter [9], [13]–[19]. Several works about gallium nitride (GaN) and silicon carbide (SiC) based *CLLC* converters for V2G and BES systems are reported in [13]–[17]. The power rate and switching frequency for such converters reach up to 22 kW and 1 MHz, respectively. In [9], [18], and [19], planar transformer designs and magnetic integration methods are proposed for the *CLLC* converter to improve the power density.

Another hot research topic relating to *CLLC* converters is synchronous rectification (SR). SR can significantly increase efficiency by reducing conduction loss on the secondary side body diodes, which is very important for V2G and BES applications.

The existing research on SR for the *CLLC* converter can be summarized into sensor detection-based methods [1], [20]–[24] and software estimation-based methods [25]–[28]. A common disadvantage of the sensor detection-based method is that an extra cost must be paid for sensors and corresponding analog circuits. In [20], an SR method using the third winding voltage and the drain–source voltage is proposed, but this method has complex implementation. To reduce the system complexity, two improved SR methods are proposed [21], [22]. The method in [21] only needs to sense the drain–source voltage of one switch, and the method in [22] measures the inductor voltage instead of the drain–source voltage. The methods in [20]–[22] are voltage-based methods. The application of voltage-based methods is limited by the withstand voltage (less than 200 sV) of sensor chips. In addition, both the drain-source voltage and inductor voltage will oscillate after the secondary side current reaches zero, which may cause incorrect SR drive signals. To

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overcome the limitations of voltage-based methods, researchers proposed several current-based methods [1], [23], [24]. The key of the current-based method is the detection of the zero current crossing point. The detection is realized by using a current transformer in [1] and a shunt resistor in [23] and [24]. However, due to the bandwidth limitation of the sensor and the performance limitation of the digital controller, the phase delay of detection is unavoidable. The higher the switching frequency is, the larger the phase delay will be. As a result, current-based SR methods are not suitable for high-frequency applications.

The largest advantage of software-estimation SR over sensor-detection SR is that the SR drive signal is generated by software calculation using the current and voltage information at the input and the output side. As a result, no extra sensors are needed, which means no extra costs need to be paid. In [25], a phase tracking method is proposed to estimate the phase difference between the primary and the secondary side current in the half-bridge *CLLC* converter. The phase difference can be calculated by an analytic formula so that the method is easy to implement. However, the method is based on the first harmonic approximation (FHA) model, so the estimation is inaccurate as the switching frequency changes. In addition, this method only applies to the half-bridge *CLLC* converter. For higher power-rate applications (e.g., V2G systems and BES systems), a full-bridge *CLLC* is necessary. In [26], an improved version of the phase tracking method based on the extended harmonic model (EHA) is proposed. The estimation accuracy is improved, but the calculation process is much more complex and relies on a look-up table. This method also cannot be adopted for the full-bridge topology. In [27], a simplified ON-state time estimation method for the secondary side switch is proposed. The calculation is simple and the method works for the full-bridge *CLLC* converter. However, as the method is based on the FHA model, its accuracy relies on tuning the ON-state time offset value, making the method inconvenient to implement. In order to solve accuracy problems, a digital sensorless SR method is proposed in [28]. The method is based on the time domain model [29] of the full-bridge *CLLC* converter, so estimation accuracy is guaranteed. However, the time-domain model of the *CLLC* converter does not have an analytic solution, so the calculation relies on numerical iteration, which is time consuming and impractical for real-time calculation. To simplify the calculation, 3-D polynomial fitting is used [28]. However, 3-D polynomial fitting is also very complex, and a large amount of predetermined data need to be calculated and stored in the controller. As a result, implementation of this method is also complex and inconvenient.

In this article, a battery charging method with natural SR features is proposed for the full-bridge *CLLC* converter. Our method focuses on the realization of SR in the battery charging process, which is one of the most important functions of the *CLLC* converter in V2G and BES applications.

The proposed battery charging method consists of a parameter matching design procedure and SR control. Different from the current SR principle, which generates the SR drive signal by sensor-detection or software-estimation, a novel SR principle is used in the proposed method. The parameter design process is taken into consideration in the SR realization.

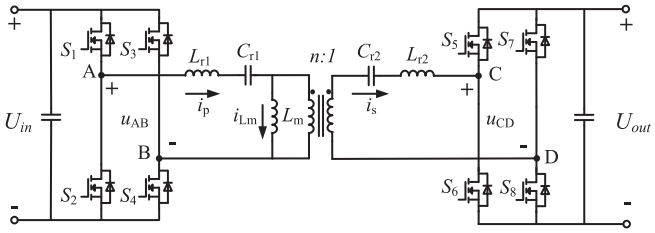


Fig. 1. Topology of the full-bridge *CLLC* converter.

The converter is designed to work under the PO Mode [29]. The key of SR in the PO Mode is to generate the SR drive signal according to the length of the P Mode stage. A special working condition where the length of the P Mode stage is fixed at $\pi$ is derived, and the analytic expression of output *U–I* characteristics is obtained under this condition. A parameter matching design procedure based on the analytic *U–I* characteristics is proposed for resonant tank design. The actual working condition of the *CLLC* converter based on the parameter matching is very close to the derived special working condition during the whole battery charging process. As a result, the actual length of the P Mode can be seen as fixed at $\pi$. Then, a simple SR control is proposed, and the SR drive signal is generated directly according to the switching frequency. No sensor-detection or software-estimation is needed. Because of this, the proposed battery charging method has natural SR features. The SR effect of the proposed method is also analyzed in detail and is verified by experimental results.

The rest of this article is organized as follows. In Section II, the SR problem of the full-bridge *CLLC* converter is introduced in detail, including the controlled variable $D_s$ (the duty cycle of the secondary side drive signal), as well as the time domain estimation method of $D_s$ and its difficulty in practical implementation. In Section III, the core ideal of the proposed battery charging method is explained. Then, the special working condition where the length of the P Mode stage is fixed at $\pi$ is derived, and the relationship between the length of the P Mode stage and the output current is analyzed. After that, the parameter matching design procedure and the SR control of the proposed battery charging method are discussed and analyzed. In Section IV, experimental results are provided to verify the natural SR of the proposed battery charging method. Finally, Section V concludes this article.

## II. Synchronous Rectification in Full-Bridge *CLLC* Converters

### A. *Controlled Variable in the Synchronous Rectification of Full-Bridge* CLLC *Converters*

Fig. 1 shows the topology of a full-bridge *CLLC* converter. $S_1$ to $S_4$ are the primary side switches, and $S_5$ to $S_8$ are the secondary side switches. The primary side, secondary side current, and magnetizing are indicated by $i_p$, $i_s$, and $i_{Lm}$, respectively. The positive directions of voltage and current used in the analysis are also given, and the transformer turns ratio is *n*.

Suppose the switching frequency $f_s$ of the *CLLC* converter is not larger than its resonant frequency $f_r$ ($f_s \leq f_r$). Under this

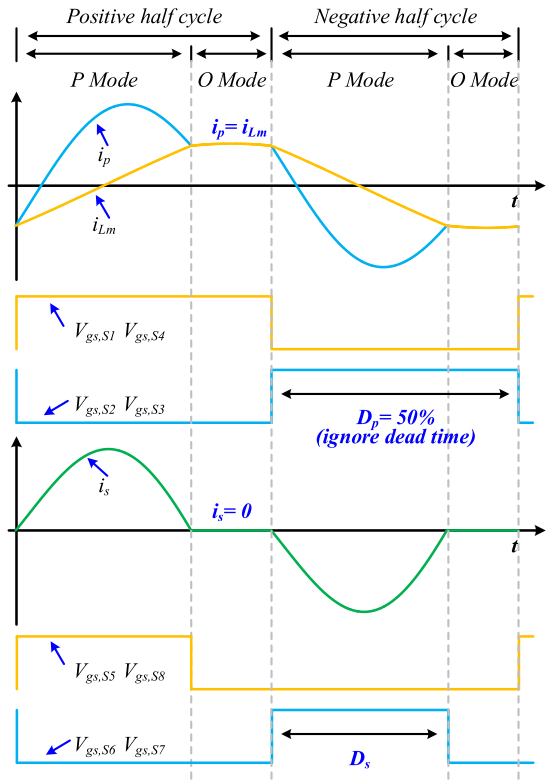


Fig. 2. Waveforms of the *CLLC* converter in PO Mode.

condition, the *CLLC* converter works under the PO mode. The PO Mode consists of a P Mode stage and an O Mode stage. The P Mode stage and the O Mode stage are defined as follows:

If the input voltage (i.e., $u_{AB}$ in Fig. 1) and output voltage (i.e., $u_{CD}$ in Fig. 1) of the resonant tank have the same polarity, the converter works in the P Mode stage. If the secondary side current (i.e., $i_s$ in Fig. 1) maintains at zero so that the secondary side part of the resonant tank does not participant the resonance process, the converter works in the O Mode stage. Waveforms of the *CLLC* converter under the PO Mode are illustrated in Fig. 2.

In Fig. 2, $D_p$ is the duty cycle of the primary side drive signals ($V_{gs,S1}$, $V_{gs,S2}$, $V_{gs,S3}$, and $V_{gs,S4}$), while $D_s$ is the duty cycle of the secondary side drive signals ($V_{gs,S5}$, $V_{gs,S6}$, $V_{gs,S7}$, and $V_{gs,S8}$). The operating process of the PO Mode in the positive half cycle is symmetrical to that in the negative half cycle. Take the positive half cycle for example. In P Mode stage, $i_p$ is larger than $i_{Lm}$ so that $i_s$ is positive. In O Mode stage, $i_p$ equals to $i_{Lm}$ so that $i_s$ is zero.

Since $i_p$ does not have a zero-value stage, $D_p$ is fixed at 50%. In this analysis, the dead time is quite small compared with the switching period; hence, the impacts of the dead time are ignored for simplicity. In practical implementation, the dead time is necessary for soft switching and safety. The actual value of $D_s$ is slightly less than 50%. From Fig. 2 it can be found that $i_s$ is zero in O Mode stage. On one hand, $V_{gs,S5}$ to $V_{gs,S8}$ must be zero in O Mode stage to ensure the converter operates correctly. On the other hand, in order to realize the SR, $i_s$ should go through the MOSFET channel in P Mode stage. $V_{gs,S5}$ and $V_{gs,S8}$ should be at a positive level during the P Mode stage in the positive half cycle, while $V_{gs,S6}$ and $V_{gs,S7}$ should be at a positive level during the P Mode stage in the negative half cycle. As a result, $D_s$ is not a fixed value. $D_s$ can be calculated as

$$D_s = \frac{t_{P\ \mathrm{Mode}}}{2T_s} \tag{1}$$

where $T_s$ is the switching period and $t_{P\ \mathrm{Mode}}$ is the length of the P Mode stage in a switching period.

From the analysis above, it can be known that in the SR of the *CLLC* converter, the controlled variable is the duty cycle of the secondary side drive signal, $D_s$.

### *B. Time-Domain Estimation of $D_s$ and Its Difficulties in Practical Implementation*

The value of $D_s$ varies with the working condition of the *CLLC* converter. The key of performing the SR in the *CLLC* converter is the fast and accurate estimation of $D_s$.

The specific value of $D_s$ under a given working condition can be calculated using the time domain operation method [29]. The base value for the voltage, the current, and the impedance are defined in (2). The transformer turns ratio $n$ is set as 1 for simplicity

$$z_{\mathrm{base}} = \sqrt{\frac{L_{r1}}{C_{r1}}} = \sqrt{\frac{L_{r2}}{C_{r2}}}\ ;\ \ u_{\mathrm{base}} = U_{\mathrm{in}}\ ;\ i_{\mathrm{base}} = \frac{u_{\mathrm{base}}}{z_{\mathrm{base}}}\ . \tag{2}$$

Then, the per-unit form time-domain expressions of $i_p$, $i_s$, $u_{cr1}$, and $u_{cr2}$ in P Mode stage and O Mode stage can be expressed as (3) and (4), respectively

$$\begin{cases} i_p\ (\phi) = P_1\ \cos\phi - P_2 \sin\phi + k_1 P_4 \sin(k_1\phi) + P_3 \cos(k_1\phi) \\ i_s\ (\phi) = P_1\ \cos\phi - P_2 \sin\phi - k_1 P_4 \sin(k_1\phi) - P_3 \cos(k_1\phi) \\ u_{cr1}(\phi) = P_1\ \sin\phi + P_2 \cos\phi - P_4 \cos(k_1\phi) + \frac{P_3}{k_1} \sin(k_1\phi) + 1 \\ u_{cr2}(\phi) = P_1\ \sin\phi + P_2 \cos\phi + P_4 \cos(k_1\phi) - \frac{P_3}{k_1} \sin(k_1\phi) - M \end{cases} \tag{3}$$

$$\begin{cases} i_p\ (\phi) = O_1\ \cos(k_2\phi) - O_2 k_2 \sin(k_2\phi) \\ u_{cr1}\ (\phi) = O_2\ \cos(k_2\phi) + \frac{O_1}{k_2} \sin(k_2\phi) + 1 \end{cases} \tag{4}$$

where $\phi = 2\pi f_r t$, $f_r = 1/(2\pi\sqrt{L_{r1}C_{r1}}) = 1/(2\pi\sqrt{L_{r2}C_{r2}})$, $k = L_m / L_{r1}$, $k_1 = \sqrt{1/(1+2k)}$, $k_2 = \sqrt{1/(1+k)}$, and $M = U_{\mathrm{out}} / U_{in}$. $P_1$, $P_2$, $P_3$, $P_4$, $O_1$, $O_2$, and $M$ are undetermined variables.

As the primary side current $i_p$, the secondary side current $i_s$, the voltage across the primary side resonant capacitor $u_{Cr1}$, and the voltage across the secondary side resonant capacitor $u_{Cr2}$ are all consecutive, the following boundary conditions should be satisfied:

$$\begin{cases} i_{p,P}\ (0) + i_{p,O}\ (\phi_2) = 0 \\ i_{s,P}\ (0) = 0 \\ u_{cr1,P}\ (0) + u_{cr1,O}\ (\phi_2) = 0 \\ u_{cr2,P}\ (0) + u_{cr2,P}\ (\phi_1) = 0 \\ i_{p,P}\ (\phi_1) - i_{p,O}\ (0) = 0 \\ i_{s,P}\ (\phi_1) = 0 \\ u_{cr1,P}\ (\phi_1) - u_{cr1,O}\ (0) = 0 \end{cases} \tag{5}$$

where the subscript *P* means the corresponding variable used the expression in (3), and the subscript *O* means the corresponding

variable used the expression in (4). $\phi_1$ and $\phi_2$ are the lengths of the P Mode stage and the O Mode stage, respectively. $\phi_1$ and $\phi_2$ are also undetermined variables.

Combining (3), (4), and (5), equations as shown in (6) can be derived. There are 7 equations ($F_1$ to $F_7$) and 9 undetermined variables ($P_1$, $P_2$, $P_3$, $P_4$, $O_1$, $O_2$, $M$, $\phi_1$, and $\phi_2$) in (6). There are more undetermined variables than equations, so extra equations are needed. In practice, the switching frequency $f_s$ is a known variable to the controller because $f_s$ is determined by the controller. Moreover, the voltage gain $M$ is also known because the voltage sensor of the converter can get the value of the input voltage $U_{\text{in}}$ and the output voltage $U_{\text{out}}$, and $M$ can be calculated

$$\begin{cases} \boldsymbol{F}_1 = P_1 + P_3 + O_1\cos(k_2\phi_2) - O_2k_2\sin(k_2\phi_2) = 0 \\ \boldsymbol{F}_2 = P_1 - P_3 = 0 \\ \boldsymbol{F}_3 = P_2 - P_4 + 1 + O_2\cos(k_2\phi_2) + \frac{O_1}{k_2}\sin(k_2\phi_2) + 1 = 0 \\ \boldsymbol{F}_4 = P_2 + P_4 - M + P_1\sin\phi_1 + P_2\cos\phi_1 \\ \quad + P_4\cos(k_1\phi_1) - \frac{P_3}{k_1}\sin(k_1\phi_1) - M = 0 \\ \boldsymbol{F}_5 = P_1\cos\phi_1 - P_2\sin\phi_1 + k_1P_4\sin(k_1\phi_1) \\ \quad + P_3\cos(k_1\phi_1) - O_1 = 0 \\ \boldsymbol{F}_6 = P_1\cos\phi_1 - P_2\sin\phi_1 - k_1P_4\sin(k_1\phi_1) \\ \quad - P_3\cos(k_1\phi_1) = 0 \\ \boldsymbol{F}_7 = P_1\sin\phi_1 + P_2\cos\phi_1 - P_4\cos(k_1\phi_1) + \frac{P_3}{k_1}\sin(k_1\phi_1) \\ \quad + 1 - (O_2 + 1) = 0. \end{cases} \tag{6}$$

Assuming the value of $M$ is $M_0$, the following two equations are derived:

$$\begin{cases} F_8 = \phi_1 + \phi_2 - \frac{f_r}{f_s}\pi = 0, \\ F_9 = M - M_0 = 0. \end{cases} \tag{7}$$

Combining (6) and (7), $\phi_1$ can be solved accurately. The mode duration $t_{P\ \text{Mode}}$ can be calculated as

$$t_{P\ \text{mode}} = \frac{\phi_1}{\pi f_r}. \tag{8}$$

Denote $f_n = f_s / f_r$. Combining (1) and (8), the duty cycle of the secondary side PWM $D_s$ can be calculated as

$$D_s = \frac{\phi_1 f_s}{2\pi f_r} = \frac{\phi_1}{2\pi} f_n. \tag{9}$$

However, it is difficult to solve $\phi_1$ from $F_1$ to $F_9$ because items related to $\phi_1$ (i.e., $sin\phi_1$, $cos\phi_1$, $\sin(k_1\phi_1)$, and $\cos(k_1\phi_1)$) are all in the form of trigonometric functions, which are highly nonlinear items. As a result, it is difficult to obtain an analytic expression for $\phi_1$. The specific value of $\phi_1$ can only be obtained from numerical iteration, which is very complex and impractical for real-time calculation in an embedded controller.

In summary, $D_s$ can be estimated accurately using the time domain model $F_1$ to $F_9$, but the time consumption of the calculation is large so that the practical implementation estimation is difficult.

## III. Proposed Battery Charging Method With Natural Synchronous Rectification Features

### A. Core Idea of the Proposed Method

From the analysis above, it has been shown that the real-time estimation of $D_s$ is hard because of the complex numerical calculation required for solving time domain equations. The numerical solving process is not likely to be simplified, which raises the following question: Is it possible to get the value of $D_s$ without doing complex numerical calculations?

The numerical solving process is unavoidable because the working condition is not constrained and is unknown for the controller. For a certain value of the output voltage, the output current may be of any value. As a result, the estimation method for $D_s$ must be a general method that applies for any possible working condition.

However, in battery charging applications, the working condition of the converter is constrained. The typical battery charging curve is illustrated in Fig. 3.

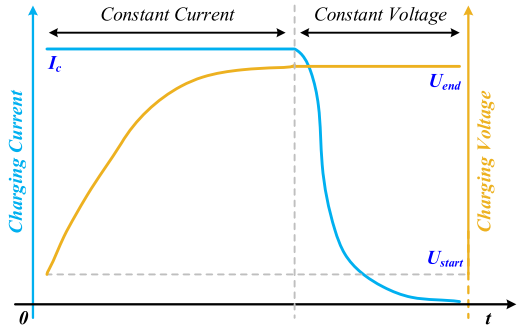


Fig. 3. Typical battery charging curve.

As shown in Fig. 3, the charging process consists of a constant current (CC) charging stage and a constant voltage (CV) charging stage. Usually, the battery is charged from its start charging voltage $U_{\text{start}}$. Before the battery voltage reaches the end charging voltage $U_{\text{end}}$, the charging current is constant at $I_c$, and the converter works under CC mode. After the battery voltage reaches $U_{\text{end}}$, the converter should work under constant voltage mode, maintaining the output voltage at $U_{\text{end}}$. During this stage, the charging current will decrease gradually. When the charging current decreases to zero, the charging process ends.

The working condition during the CC stage is fully constrained. The value of the output current at any value of output voltage is known in advance. The working condition during the CV stage is partly constrained. Although the specific value of output current is unknown, it is less than $I_c$. Because the working condition in the battery charging application is constrained, it is possible to use a simple special-purpose method to realize SR instead of the complex general-purpose method discussed in Section II.

The core idea of the proposed method is as follows: find special working conditions where the length of the P Mode stage is constant. Match those special working conditions with the working condition of battery charging as much as possible by parameter design. Thus, $D_s$ can be obtained directly from (9) without equation-solving or sensor-detection. As a result, natural SR is realized.

### B. Derivation of the Working Conditions Where the Length of the P Mode Stage Is $\pi$

From Section II, it can be known that the difficulty of solving $\phi_1$ comes from trigonometric items related to $\phi_1$. In order to simplify the equations, the value of $\phi_1$ is fixed at $\pi$. Then,

trigonometric items related to $\phi_1$ are as follows:

$$\begin{cases} sin\ \phi_1 = 0\ cos\ \phi_1 = 1, \\ \sin(k_1\phi_1) = \sin(k_1\pi) \quad \cos(k_1\phi_1) = \cos(k_1\pi). \end{cases} \tag{10}$$

With (10), (6) can be simplified as follows:

$$\begin{cases} \boldsymbol{F}_1 = P_1 + P_3 + O_1\cos(k_2\phi_2) - O_2k_2\ \sin(k_2\phi_2) = 0 \\ \boldsymbol{F}_2 = P_1 - P_3 = 0 \\ \boldsymbol{F}_3 = P_2 - P_4 + 1 + O_2\cos(k_2\phi_2) + \frac{O_1}{k_2}\sin(k_2\phi_2) + 1 = 0 \\ \boldsymbol{F}_4 = P_2 + P_4 - M - P_2 + P_4\cos(k_1\phi_1) \\ -\frac{P_3}{k_1}\sin(k_1\phi_1) - M = 0 \\ \boldsymbol{F}_5 = -P_1 + k_1P_4\sin(k_1\pi) + P_3\cos(k_1\pi) - O_1 = 0 \\ \boldsymbol{F}_6 = -P_1 - k_1P_4\sin(k_1\pi) - P_3\cos(k_1\pi) = 0 \\ \boldsymbol{F}_7 = -P_2 - P_4\cos(k_1\pi) + \frac{P_3}{k_1}\sin(k_1\pi) - O_2 = 0. \end{cases} \tag{11}$$

Based on (11), $P_1$, $P_2$, $P_3$, $P_4$, $O_1$, $O_2$, and $M$ can be expressed as trigonometric functions of $\phi_2$

$$\begin{cases} P_1 = -\frac{k_1k_2\sin(k_1\pi)\sin(k_2\phi_2)}{A} \\ P_2 = -1 \\ P_3 = -\frac{k_1k_2\sin(k_1\pi)\sin(k_2\phi_2)}{A} \\ P_4 = \frac{k_2\sin(k_2\phi_2)(\cos(k_1\pi)+1)}{A} \\ O_1 = \frac{2k_1k_2\sin(k_1\pi)\sin(k_2\phi_2)}{A} \\ O_2 = \frac{2k_1\sin(\pi k_1)(\cos(k_2\phi_2)-1)}{A} \\ M = \frac{k_2\sin(k_2\phi_2)(\cos(k_1\pi)+1)}{A} \end{cases} \tag{12}$$

where$A = k_2\sin(k_2\phi_2) - 2k_1\sin(k_1\pi) + 2k_1\sin(k_1\pi)\cos(k_2\phi_2) + k_2\cos(k_1\pi)\sin(k_2\phi_2)$.

Combining (3), (10), and (12), the per-unit value of the output current $I_{o,\mathrm{unit}}$ can be calculated as

$$\begin{aligned} I_{o,\mathrm{unit}} &= \int_0^{\phi_1} i_s\, d\phi \\ &= \frac{-2P_4\sin\left(\frac{k_1\pi}{2}\right)^2 \pm \frac{P_3}{k_1}\sin(k_1\pi)}{\phi_1 += \phi_2} \\ &= \frac{2}{\pi+\phi_2} = \frac{2}{\pi}f_n. \end{aligned} \tag{13}$$

In (12), the expression of $M$ can be rewritten as

$$\frac{\cos(k_2\phi_2)}{\sin(k_2\phi_2)} - \frac{1}{\sin(k_2\phi_2)} = \frac{k_2[\cos(k_1\pi)+1]}{2k_1\sin(k_1\pi)}\left(\frac{1}{M}-1\right). \tag{14}$$

Define

$$B = \frac{k_2[\cos(k_1\pi)+1]}{2k_1\sin(k_1\pi)}\left(\frac{1}{M}-1\right). \tag{15}$$

Then, (14) can be further rewritten as

$$\left(1+B^2\right)\cos^2(k_2\phi_2) - 2\cos(k_2\phi_2) + \left(1-B^2\right) = 0. \tag{16}$$

Equation (16) is a simple quadratic equation so that $\phi_2$ can be solved as

$$\phi_2 = \frac{1}{k_2}\arccos\left(\frac{1-B^2}{1+B^2}\right). \tag{17}$$

Combining $F_8$ with (17), the following can be derived:

$$f_n = \frac{f_s}{f_r} = \frac{k_2\pi}{k_2\pi+\arccos\left(\frac{1-B^2}{1+B^2}\right)}. \tag{18}$$

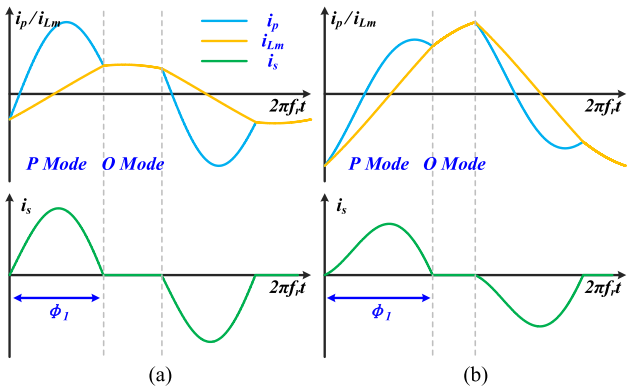


Fig. 4. Steady state waveforms when $I_{o,\mathrm{unit}}$ is (a) 0.3 and (b) 0.1.

Combining (13) with (18), $I_{o,\mathrm{unit}}$ can be further expressed as

$$I_{o,unit} = \frac{2k_2}{k_2\pi+\arccos\left(\frac{1-B^2}{1+B^2}\right)}. \tag{19}$$

Since the input voltage $U_{\mathrm{in}}$ is constant, the voltage gain $M$ is in proportion to the output voltage $U_{\mathrm{out}}$. As a result, (19) shows the relationship between $I_{o,\mathrm{unit}}$ and $U_{\mathrm{out}}$ (the output U-I characteristics) when the length of the P Mode stage is fixed at $\pi$. Conversely, if $I_{o,\mathrm{unit}}$ and $U_{\mathrm{out}}$ are controlled using the relationship shown in (19), the length of the P Mode stage will be fixed $\pi$. These are the special working conditions where the length of the P Mode stage $\phi_1$ is constant. The constant value of $\phi_1$ is $\pi$.

### *C. Relationship Between the Length of the P Mode Stage and the Output Current*

Using the method proposed in Section II, the other undetermined variables ($P_1$, $P_2$, $P_3$, $P_4$, $O_1$, $O_2$, $M$, and $\phi_1$) in $F_1$ to $F_9$ can also be solved. As a result, the steady state waveforms of the *CLLC* converter under a given working condition can be obtained. Fig. 4 shows the steady-state waveforms of two different working conditions. In Fig. 4, the values of $k$ and $M$ are 5 and 1.45, respectively. In Fig. 4(a), the value of $I_{o,\mathrm{unit}}$ is 0.3. In Fig. 4(b), $I_{o,\mathrm{unit}}$ is 0.1. The voltage gain of the two working conditions is the same.

In Fig. 4, the length of the P Mode stage when $I_{o,\mathrm{unit}}$ is 0.1 is longer than that of the working condition when $I_{o,\mathrm{unit}}$ is 0.3. The curve of the relationship between $I_{o,\mathrm{unit}}$ and $\phi_1$ is plotted, as shown in Fig. 5.

From Figs. 4 and 5, it can be known that if the voltage gain $M$ (i.e., the output voltage $U_{\mathrm{out}}$) is fixed, the smaller $I_{o,\mathrm{unit}}$ is, the larger $\phi_1$ will be. In Fig. 5, the slope of the curve is small around the region where $\phi_1$ is about $\pi$. That means in working conditions that satisfy (19), the increment of $\phi_1$ is relatively small if $I_{o,\mathrm{unit}}$ decreases.

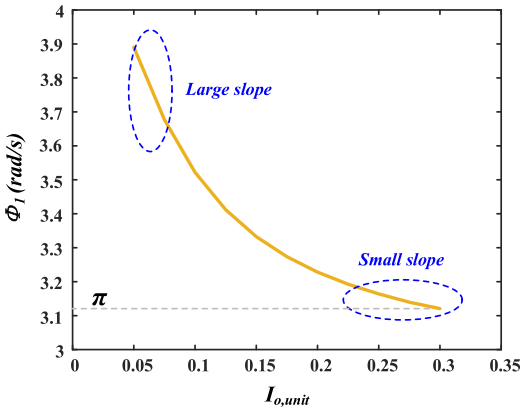


Fig. 5. Curve of the relationship between $I_{o,\mathrm{unit}}$ and $\phi_1$.

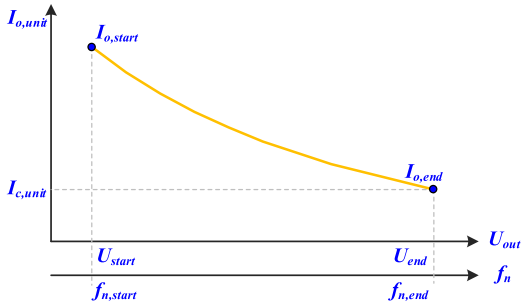


Fig. 6. Output *U–I* curve when $\phi_1$ is fixed at $\pi$.

### *D. Parameter Matching Design Procedure of the Proposed Battery Charging Method*

In (19), if $U_{\mathrm{out}}$ increases, $M$ will increase, so $B$ will decrease. Finally, $I_{o,\mathrm{unit}}$ will decrease. As a result, the output U-I characteristics expressed by (19) is a drop curve as shown in Fig. 6.

In Fig. 6, $f_{n,\mathrm{start}}$ and $f_{n,\mathrm{end}}$ are the values of $f_n$ when $U_{\mathrm{out}}$ is $U_{\mathrm{start}}$ and $U_{\mathrm{end}}$, respectively. $I_{o,\mathrm{start}}$ and $I_{o,\mathrm{end}}$ are the values of $I_{o,\mathrm{unit}}$ when $U_{\mathrm{out}}$ is $U_{\mathrm{start}}$ and $U_{\mathrm{end}}$, respectively. According to Fig. 3, the charging current between $U_{\mathrm{start}}$ and $U_{\mathrm{end}}$ is a constant value. In order to match the output *U–I* characteristics with the working conditions of the battery charging process, the following condition should be satisfied:

$$I_{o,\mathrm{end}} \geq I_{c,\mathrm{unit}}\ I_{c,\mathrm{unit}} = \frac{I_c}{i_{\mathrm{base}}} \tag{20}$$

$I_{c,\mathrm{unit}}$ is the per-unit value of $I_c$. In order to realize the abovementioned matching of the working condition, a parameter matching design procedure for the resonant tank is proposed.

The flowchart of the proposed parameter matching design procedure is illustrated in Fig. 7.

The proposed parameter matching design procedure needs the following design indices in advance: $U_{\mathrm{start}}$, $U_{\mathrm{end}}$, $I_c$, $U_{\mathrm{in}}$, $f_{n,\mathrm{start}}$, $f_{n,\mathrm{end}}$, and $f_r$.

$U_{\mathrm{start}}$, $U_{\mathrm{end}}$, and $I_c$ are related to the characteristics of the battery, which can be obtained from the datasheet. $U_{\mathrm{in}}$ is related to the specific application, while $f_{n,\mathrm{start}}$, $f_{n,\mathrm{end}}$, and $f_r$ are tradeoff parameters. Large $f_r$ can help increase the power density, but

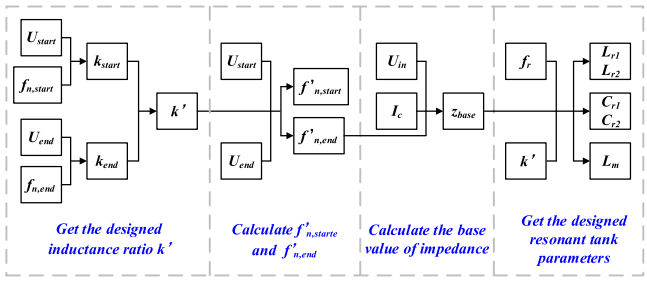


Fig. 7. Flowchart of the proposed parameter matching design procedure.

the switching loss may increase. Choosing smaller $f_{n,\mathrm{start}}$ and $f_{n,\mathrm{end}}$ will result in a narrower range of the switching frequency, but inductance ratio $k$ will be smaller. As a result, the conduction loss may increase.

The proposed parameter matching design procedure is as follows.

1) Get the designed inductance ratio $k'$. Inductance ratio $k$ influences the slope of the voltage gain curve ($M\ v.s.\ f_n$). The larger $k$ is, the larger the slope of the voltage gain curve will be [2]. Under the condition that constraints of $f_{n,\mathrm{start}}$ and $f_{n,\mathrm{end}}$ are satisfied, $k$ should be as big as possible to decrease the conduction loss.
   a) Calculate $k_{\mathrm{start}}$, which is the maximum value of $k$ that makes $U_{\mathrm{out}}$ equal to $U_{\mathrm{start}}$ when $f_n$ is no less than $f_{n,\mathrm{start}}$. The value of $k_{\mathrm{start}}$ can be calculated by solving the following problem:

$$\max\ k$$
$$s.t.\ f_{n,\mathrm{start}} \geq \frac{k_2\pi}{k_2\pi + \arccos\left(\frac{1-B(U_{\mathrm{start}})^2}{1+B(U_{\mathrm{start}})^2}\right)} \tag{21}$$

   where $B(U_{\mathrm{start}})$ is the value of $B$ when $U_{\mathrm{out}}$ equals $U_{\mathrm{start}}$.
   b) Calculate $k_{\mathrm{end}}$, which is the maximum value of $k$ that makes $U_{\mathrm{out}}$ equal to $U_{\mathrm{end}}$ when $f_n$ is no less than $f_{n,\mathrm{end}}$. The value of $k_{\mathrm{end}}$ can be calculated by solving the following problem:

$$\max\ k$$
$$s.t.\ f_{n,\mathrm{end}} \geq \frac{k_2\pi}{k_2\pi + \arccos\left(\frac{1-B(U_{\mathrm{end}})^2}{1+B(U_{\mathrm{end}})^2}\right)} \tag{22}$$

   where $B(U_{\mathrm{end}})$ is the value of $B$ when $U_{\mathrm{out}}$ equals to $U_{\mathrm{start}}$.
   c) Calculate $k'$, where

$$k' = \min\left(k_{\mathrm{start}},\ k_{\mathrm{end}}\right). \tag{23}$$

2) Calculate $f'_{n,\mathrm{start}}$ and $f'_{n,\mathrm{end}}$, which are the actual values of $f_n$ under inductance ratio $k'$ when $U_{\mathrm{out}}$ is $U_{\mathrm{start}}$ and $U_{\mathrm{end}}$, respectively. Values of $f'_{n,\mathrm{start}}$ and $f'_{n,\mathrm{end}}$ are as

follows:

$$\begin{cases} f'_{n,\text{start}} = \dfrac{k'_2\pi}{k'_2\pi+\arccos\left(\frac{1-B(U_{\text{start}})^2}{1+B(U_{\text{start}})^2}\right)} \\ f'_{n,\text{end}} = \dfrac{k'_2\pi}{k'_2\pi+\arccos\left(\frac{1-B(U_{\text{end}})^2}{1+B(U_{\text{end}})^2}\right)} \\ k'_2 = \sqrt{1/1+k'}\ . \end{cases} \tag{24}$$

Since $k'$ is the smaller of $k_{\text{start}}$ and $k_{\text{end}}$, $f'_{n,\text{start}}$ and $f'_{n,\text{end}}$ satisfy the following conditions:

$$f'_{n,\text{start}} \geq f_{n,\text{start}},\ f'_{n,\text{end}} \geq f_{n,\text{end}}. \tag{25}$$

3) Calculate the base value of the impedance, $z_{\text{base}}$.

Combining (18) with (19), the relationship of $I_{o,\text{unit}}$ and $f_n$ is obtained as

$$I_{o,\text{unit}} = \frac{2}{\pi}\ f_n. \tag{26}$$

The value of $I_{o,\text{end}}$ is set at $I_{c,\text{unit}}$ for the best matching, so that $I_{c,\text{unit}}$ can be expressed as

$$I_{c,\text{unit}} = I_{o,\text{end}}\ = \frac{2}{\pi}\ f'_{n,\text{end}}. \tag{27}$$

Then, the base value of current $i_{base}$ can be calculated as

$$i_{\text{base}} = \frac{I_c}{I_{c,\text{unit}}}\ = \frac{\pi}{2f'_{n,\text{end}}}\ I_c. \tag{28}$$

Finally, $z_{\text{base}}$ can be calculated as

$$z_{\text{base}} = \frac{U_{\text{in}}}{i_{\text{base}}}\ = \frac{2f'_{n,\text{end}}U_{\text{in}}}{\pi I_c}\ . \tag{29}$$

4) Calculate the designed resonant tank parameters. Based on (2) and (4), the following equation group is derived:

$$\left\{ z_{\text{base}} = \sqrt{\frac{L_{r1}}{C_{r1}}},\ f_r = \frac{1}{\left(2\pi\sqrt{L_{r1}C_{r1}}\right)},\ k' = \frac{L_m}{L_{r1}}. \right. \tag{30}$$

Primary side resonant tank parameters can be calculated by solving (30)

$$\begin{cases} C_{r1} = \dfrac{I_c}{4f'_{n,\text{end}}f_rU_{\text{in}}} \\ L_{r1} = \dfrac{f'_{n,\text{end}}U_{\text{in}}}{\pi^2 f_r I_c} \\ L_m = \dfrac{k'f'_{n,\text{end}}U_{\text{in}}}{\pi^2 f_r I_c}\ . \end{cases} \tag{31}$$

Secondary side resonant tank parameters can be calculated as

$$C_{r2} = n^2\ C_{r1} \text{ and } L_{r2} = \frac{L_{r1}}{n^2} \tag{32}$$

where $n$ is the transformer turns ratio.

A design case is also provided to demonstrate the proposed parameter matching design method. In the design case, a battery pack containing 30 LiPo cells connected in series is considered. The capacity of the battery pack is 3 Ah. Then, the start charging voltage $U_{\text{start}}$ is 210 V, the end charging voltage $U_{\text{end}}$ is 294 V, and the constant charging current $I_c$ is 3 A. The input voltage $U_{\text{in}}$ is set at 200 V. The transformer turns ratio is set at 1. Details of the design indices and the designed resonant tank parameters are listed in Table I.

TABLE I
DESIGN CASE OF THE PROPOSED PARAMETER MATCHING DESIGN METHOD

| The design indices | | | |
|---|---|---|---|
| $U_{start}$ | 210V | $U_{end}$ | 294V |
| $I_c$ | 3A | $f_r$ | 70kHz |
| $f_{n,start}$ | 0.9 | $f_{n,end}$ | 0.7 |
| $U_{in}$ | 200V | | |
| The design results | | | |
| $L_{r1}/L_{r2}$ | 67.82uH | $C_{r1}/C_{r2}$ | 76.22nF |
| $L_m$ | 223.8uH | $k'$ | 3.3 |
| $f'_{n,start}$ | 0.94 | $f'_{n,end}$ | 0.70 |

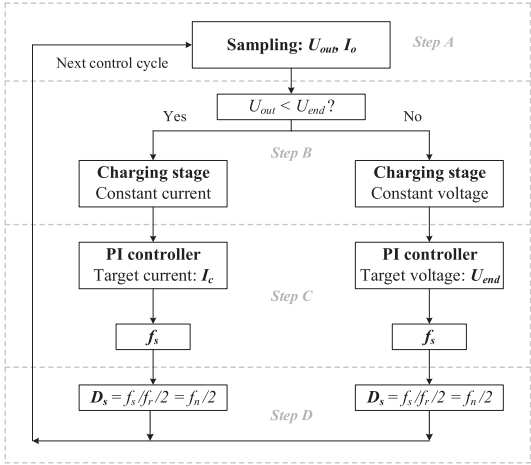


Fig. 8. Step-by-step flowchart of the natural SR control in proposed battery charging method.

### *E. Synchronous Rectification Control of the Proposed Battery Charging Method*

The step-by-step flowchart of the natural SR control in proposed battery charging method is illustrated in Fig. 8. The implementation of the natural SR control consists four steps in a control cycle.

*Step A*: Sampling. The latest values of $U_{\text{out}}$ and $I_o$ are sampled from sampling circuit.

*Step B*: Judging the charging stage. If $U_{\text{out}}$ is less than $U_{\text{end}}$, set the charging stage as CC charging stage. Otherwise, set the charging stage as CV charging stage.

*Step C*: Close loop regulation. If the converter works under CC charging stage, $I_o$ is regulated by a proportional–integral (PI) controller. The target value for $I_o$ is $I_c$. If the converter works under CV charging stage, $U_{\text{out}}$ is regulated by a PI controller. The target value for $U_{\text{out}}$ is $U_{\text{end}}$. Switching frequency, $f_s$, is updated by the PI controller.

*Step C*: Calculating and setting $D_s$. From (9), $D_s$ can be calculated as

$$D_s = \frac{f_s}{2f_r}\ = \frac{f_n}{2}\ . \tag{33}$$

From (33), it can be known that $D_s$ is only related to the per-unit value of the switching frequency. As a result, the calculation of $D_s$ is very easy, and the time consumption of the calculation can be ignored. From the analysis in Section III-D, it can be

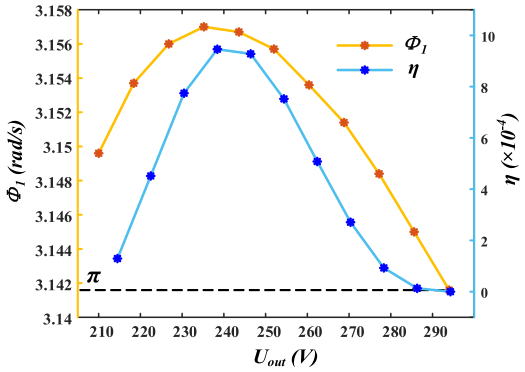


Fig. 9. Curves of $\phi_1$ and $\eta$ during the CC charging stage.

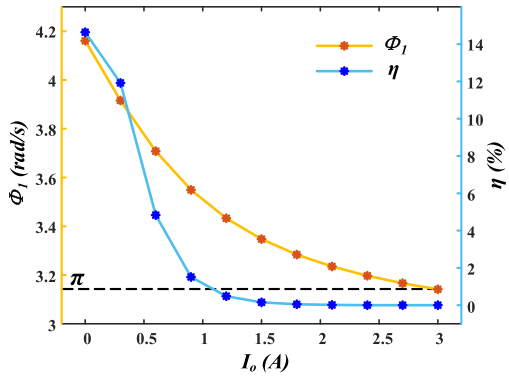


Fig. 10. Curves of $\phi_1$ and $\eta$ during the CV charging stage.

known that for the matching-designed resonant tank, the actual working conditions of the battery charging process are close to but not the same as the special working conditions expressed by (19).

In the CC charging stage, $I_{\rm o}$ is less than the output current calculated by (19) according to Fig. 6. The closer $U_{\rm out}$ is to $U_{\rm end}$, the smaller the difference will be. In the CV stage, $I_{\rm o}$ is less than $I_{o,\rm end} \times i_{\rm base}$, and the difference will become larger as the charging process goes on because $I_{\rm o}$ will finally decrease to zero, according to Fig. 3.

Since $I_{\rm o}$ in the actual charging process is less than the required output current in (19), the actual length of the P Mode stage will be longer than $\pi$, according to Section III-C. As a result, a part of the secondary side current will go through the body diodes. However, the SR errors of the proposed method are very small. The SR effect of the proposed method is almost the same as complete SR. The detailed evaluation of the SR effect of the proposed method is provided as follows.

Taking the design case in Table I as an example, the evaluation can be performed in two aspects. The first is to analyze the difference between the actual value of $\phi_1$ and $\pi$. The other is to calculate the ratio of $i_{s,\rm RMS,diode}$ to $i_{s,\rm RMS}$, where $i_{s,\rm RMS,diode}$ is the rms value of the secondary current that goes through the diodes, and $i_{s,\rm RMS}$ is the rms value of the secondary current. Define this ratio as $\eta$; $\eta$ can show the amount of the current that is not synchronous rectified directly and is calculated as follows:

$$\eta = \frac{i_{s,\rm RMS,diode}}{i_{s,\rm RMS}}. \tag{34}$$

Using the method proposed in Section II, the actual value of $\phi_1$ and the value of $\eta$ during the CC charging stage and the CV charging stage can be calculated. The results are illustrated in Fig. 9 and Fig. 10, respectively.

According to the article presented in [30], usually more than 95% of the charging energy is transmitted in the CC stage. As a result, the effect of SR during the CC stage is of vital importance. In Fig. 9, the maximum value of $\phi_1$ is less than 3.158 (i.e., the maximum error of $D_s$ is less than 0.52%). The estimation error for $D_s$ in the method is very small.

In addition, as shown in Fig. 2, the waveform of $i_s$ during the P Mode stage is like a sine wave. The value of $i_s$ near the end of the P Mode stage is very small (near zero), so the value of $i_{s,\rm RMS,diode}$ and $\eta$ will be even smaller. In Fig. 9, the maximum value of $\eta$ is less than $10 \times 10^{-4}$. Thus, $i_{s,\rm RMS,diode}$ is negligible compared to $i_{s,\rm RMS}$. As a result, in the CC charging stage, the SR effect of the proposed battery charging method is nearly the same as complete SR.

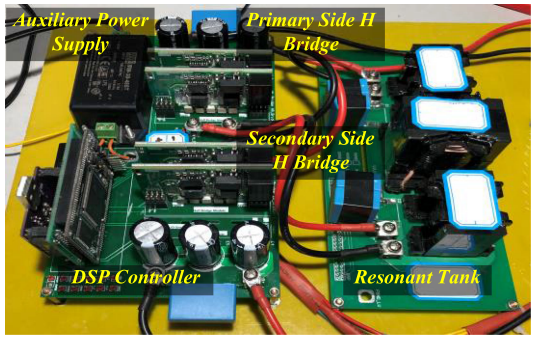


Fig. 11. Figure of the lab-level prototype.

In the CV charging stage, the actual value of $\phi_1$ becomes larger than $\pi$ as $I_o$ decreases, according to Fig. 10. However, the SR effect of the proposed method is not influenced much. Since only about 5% of the charging energy is transmitted in the CV charging stage, the decrease of the SR effect in the CV stage does not have significant influence on the whole charging process.

Furthermore, even in the CV stage, $\eta$ is less than 2% when $I_o$ is between 1 and 3 A, according to Fig. 10. For this range, $i_{s,\rm RMS,diode}$ is also negligible compared to $i_{s,\rm RMS}$. When $I_o$ is less than 1 sA, $\eta$ increases rapidly. But even for the working condition that $I_o$ is about zero, $\eta$ is also less than 15%, which means most of the secondary current (more than 85%) is going through the MOSFET channel instead of the body diode. Besides, when $I_o$ is small, the share of the loss caused by $i_{s,\rm RMS,diode}$ in the total loss will decrease, so the increase of $\eta$ does not have significant influence on efficiency.

### F. Summary and Comparison

The proposed battery charging method with natural SR features consists of a parameter matching design procedure and simple SR control.

TABLE II
SYNCHRONOUS RECTIFICATION PERFORMANCE COMPARISON

| | Voltage-based SR method [20-22] | Current-based SR method [1,23,24] | Estimation method based on FHA model [25, 27] | Estimation method based on EHA and time domain model [26, 28] | The proposed method |
|---|---|---|---|---|---|
| Type | General purpose | General purpose | General purpose | General purpose | Special purpose |
| Cost | High | High | Low | Low | Low |
| Extra sensor | Yes | Yes | No | No | No |
| High-voltage application | No | No | Yes | Yes | Yes |
| High-frequency application | Yes | No | Yes | Yes | Yes |
| Influence by oscillation | Large | Small | Small | Small | Small |
| Calculation complexity | Low | Low | Low | High | Low |
| System complexity | High | High | Low | Low | Low |
| Accuracy | High | High | Low | High | High |
| Implementation | Simple | Simple | Simple | Complex | Simple |

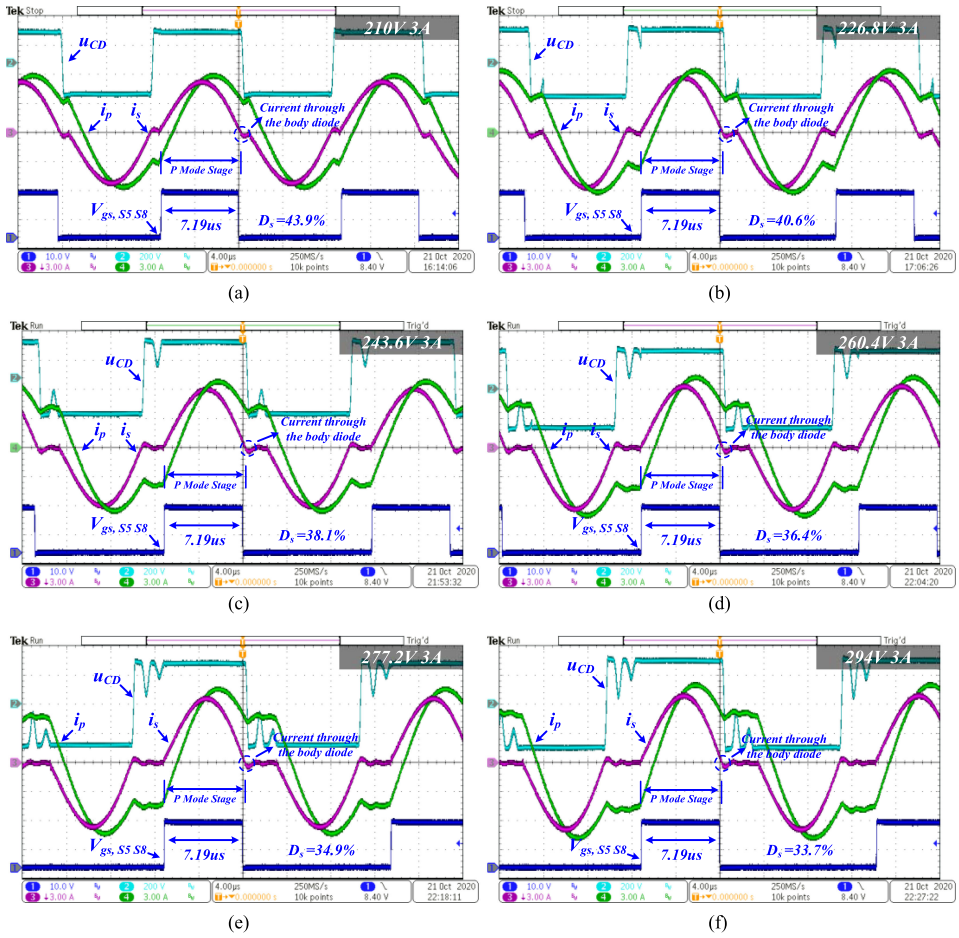


Fig. 12. Waveforms during the CC charging stage. $U_{\rm out}$ is (a) 210, (b) 226.8, (c) 243.6, (d) 260.4, (e) 277.2, and (f) 294 V.

With the proposed parameter matching design procedure, the working condition of the converter during the battery charging process is very similar to the working condition that $\phi_1$ is constant at $\pi$. As a result, SR can be realized by (33) easily without sensor detection or the software estimation. Natural SR is realized.

Performances of SR of the proposed battery charging method and of existing SR methods are compared in Table II.

## IV. EXPERIMENTAL VERIFICATION

A lab-level prototype is built to verify the proposed battery charging method, shown in Fig. 11. The parameters of the prototype are shown in Table III.

The prototype is built according to the design results in Table I. The actual resonant frequency is 69.5 kHz, so the time length of the P Mode stage when $\phi_1$ is $\pi$ is 7.19 $\mu$s. In the experimental verification, the working condition of the charging process is the same as the working condition defined in Table I. Experimental

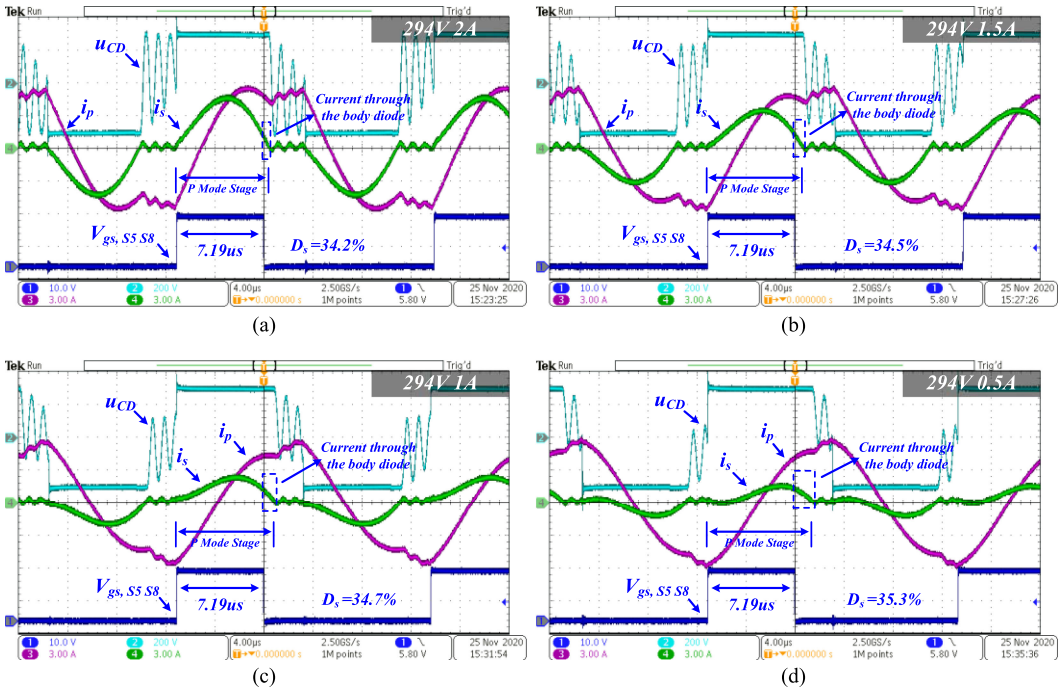


Fig. 13. Waveforms during the CV charging stage. $I_o$ is (a) 2, (b) 1.5, (c) 1, and (d) 0.5 A.

TABLE III
PARAMETERS OF THE LAB-LEVEL PROTOTYPE

| General parameters | | | |
|---|---|---|---|
| DSP controller | TMS320F28335 | MOSFET | C3M0120090J |
| Resonant tank | | | |
| Turns ratio | 1 | $L_m$ | 224uH |
| $L_{r1}/L_{r2}$ | 68uH | $C_{r1}/C_{r2}$ | 77nF |
| Resonant frequency | | 69.5kHz | |
| Time length of the P Mode stage when $\phi_1$ is $\pi$ | | 7.19us | |

waveforms of the converter under different working conditions during the CC and the CV charging stage are illustrated in Figs. 12 and 13.

In Fig. 12(a)–(f), the output current $I_o$ is constant at 3 A and the output voltage $U_{\text{out}}$ is 210, 226.8, 243.6, 260.4, 277.2, and 294 V. In Fig. 13(a)–(d), $U_{\text{out}}$ is constant at 294 V and $I_o$ is 2, 1.5, 1, and 0.5 A. From Fig. 12, it can be known that as $U_{\text{out}}$ increases from 210 to 294 V, the switching frequency $f_s$ decreases (i.e., the period of gate drive signals $V_{gs,\ S5}$ and $V_{gs,\ S8}$ increases), and from Figs. 12(f) and 13, it can be known that as $I_o$ decreases from 3 to 0.5 A, $f$ increases. At the same time, the positive pulse width of $V_{gs,\ S5}$ and $V_{gs,\ S8}$ is fixed at 7.19 $\mu$s, which is the time length of the P Mode stage when $\phi_1$ is $\pi$ in the designed prototype. $D_s$ changes from 43.9% to 33.7% when output voltage increases from 210 to 294 V in CC charging stage, and $D_s$ changes from 35.3% to 33.7% when output current increases from 0.5 to 3 A in CV charging stage. As a result, $D_s$ decreases as $f_s$ decreases and vice versa, which is consistent with (33). From the analysis above, it is confirmed that the proposed SR control was operating correctly during the CC charging stage and the CV charging stage.

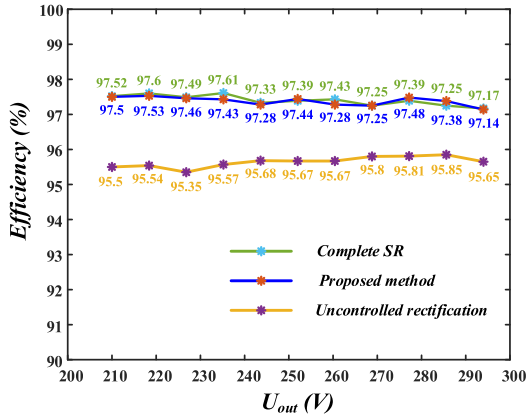


Fig. 14. Comparison of SR effect in the CC charging stage.

In Fig. 12, the actual time length of the P Mode stage was very close to 7.19 $\mu$s, and the current through the body diode (marked by the blue dotted cycle) was very small compared to the synchronous rectified part of $i_s$. The experimental results are consistent with the analysis in Section III-E.

The comparison of SR effect in the CC charging stage is illustrated in Fig. 14. In Fig. 14, the output current $I_o$ was 3 A while the output voltage $U_{\text{out}}$ varied from 210 to 294 V. The complete SR was realized by manually changing $D_s$ to make all of $i_s$ go through the MOSFET channel. Uncontrolled rectification means $D_s$ is zero so that all of $i_s$ goes through the body diode.

In Fig. 14, there is a significant efficiency increase (1.45%–2.11%) between the proposed method and uncontrolled rectification. The efficiencies of the proposed method and of complete SR are nearly the same (maximum efficiency difference is 0.18%)

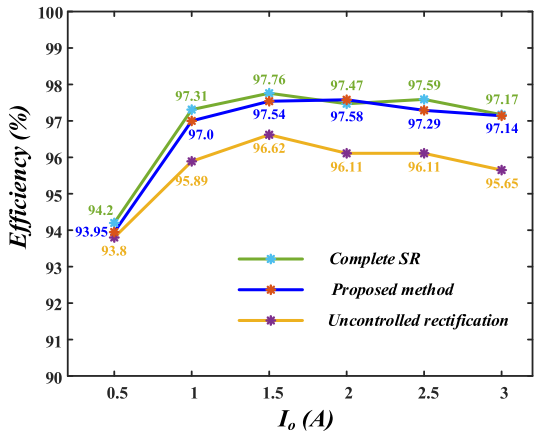


Fig. 15. Comparison of SR effect in the CV charging stage.

during the entire CC charging stage. The experimental results verify that the proposed method can achieve SR as well as complete SR.

In Fig. 13, the actual time length of the P Mode stage increases as $I_o$ decreases. Since the positive pulse width of $V_{gs,\ S5}$ and $V_{gs,\ S8}$ is fixed at 7.19 $\mu$s, the share of the current through the body diode (marked by the blue dotted square) increases gradually. The results are consistent with the analysis proposed in Sections III-C and E.

A comparison of SR effect in the CC charging stage is illustrated in Fig. 15. In Fig. 15, the output voltage $U_{\text{out}}$ is 294 V while the output current $I_o$ varies from 0.5 to 3 A. In Fig. 15, there is also a significant efficiency increase (0.92%–1.49%) between the proposed method and uncontrolled rectification when $I_o \geq 1$ A. The SR effect of the proposed method is also apparent in the CV charging stage.

When $I_o$ is 0.5 A, efficiency of the three methods is similar and decreases significantly compared to efficiency when $I_o \geq 1$ A. This shows that SR is not the major limiting factor of efficiency in light load conditions. As a result, the relatively large $D_s$ estimation error in light load conditions does not have a significant negative influence on efficiency, which is consistent with the analysis in Section III-E.

Furthermore, the efficiency of the proposed method and complete SR is also very close (maximum efficiency difference is 0.31%). The experimental results verify that the proposed method has a SR effect comparable to complete SR during the entire CV charging stage.

## V. Conclusion

In this article, a novel battery charging method with natural SR features is proposed for the full-bridge *CLLC* converter. The proposed method consists of a parameter matching design procedure and SR control. After the parameter matching design procedure, SR can be realized naturally without sensor detection or software estimation. The effectiveness of the proposed method is verified by experimental results. The contribution of this article can be summarized as follows.

1) A novel SR principle is proposed and implemented. The parameter design process is taken into consideration for SR realization.
2) The proposed battery charging method provides a complete and integrated solution for the *CLLC* converter in battery charging-related applications. Traditionally, the parameter design and SR are two independent processes in the *CLLC* converter design. In the proposed method, the two processes are integrated. Once the parameter design is finished using the proposed parameter matching design procedure, the SR is realized naturally. As a result, a considerable amount of time and effort spent on the parameter design and the SR tuning process can be saved.

## Appendix

| Variable | Physical meaning |
|---|---|
| $f_r$ | Resonant frequency. |
| $f_s$ | Switching frequency. |
| $D_p$ | Duty cycle of primary side switches. |
| $D_s$ | Duty cycle of secondary side switches. |
| $k$ | Inductance ratio. |
| $k_1$ | Scale factor of the lower eigen frequency in P mode to $f_r$. |
| $k_2$ | Scale factor of the eigen frequency in O mode to $f_r$. |
| $P_1$ to $P_4$ | Undetermined coefficients of time-domain expressions in P mode. |
| $O_1$ and $O_2$ | Undetermined coefficients of time-domain expressions in O mode. |
| $\phi_1$ | Length of P mode stage. |
| $\phi_2$ | Length of O mode stage. |
| $M$ | Voltage gain. |
| $I_c$ | Constant charging current. |
| $U_{\text{start}}$ | Start charging voltage. |
| $U_{\text{end}}$ | End charging voltage. |

## References

[1] W. Chen, P. Rong, and Z. Lu, "Snubberless bidirectional DC–DC converter with new CLLC resonant tank featuring minimized switching loss," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3075–3086, Sep. 2010.

[2] J. Jung, H. Kim, M. Ryu, and J. Baek, "Design methodology of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1741–1755, Apr. 2013.

[3] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen, and J. Lai, "Design of bidirectional DC–DC resonant converter for vehicle-to-grid (V2G) applications," *IEEE Trans. Transp. Electrific.*, vol. 1, no. 3, pp. 232–244, Oct. 2015.

[4] A. Soni and A. K. Dhakar, "Bi-directional CLLC resonant converter with integrated planar transformer for energy storage systems," in *Proc. IECON 46th Annu. Conf. IEEE Ind. Electron. Soc.*, 2020, pp. 4255–4260.

[5] J. Min and M. Ordonez, "Bidirectional resonant CLLC charger for wide battery voltage range: Asymmetric parameters methodology," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6662–6673, Jun. 2021.

[6] B. Liu, M. Qiu, L. Jing, X. Wang, and M. Chen, "Design of high-performance bidirectional DC/DC converter applied for more electric aircraft," *J. Eng.*, vol. 2018, no. 13, pp. 520–523, 2018.

[7] X. Lin, K. Sun, J. Lin, Z. Zhang, and W. Kong, "A multi-port bidirectional power conversion system for reversible solid oxide fuel cell applications," in *Proc. Int. Power Electron. Conf. (ECCE Asia)*, Niigata, Japan, 2018, pp. 3460–3465.
[8] Y. Xuan, X. Yang, W. Chen, T. Liu, and X. Hao, "A novel three-level CLLC resonant DC–DC converter for bidirectional EV charger in DC microgrids," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2334–2344, Mar. 2021.
[9] B. Li, Q. Li, and F. C. Lee, "A WBG based three phase 12.5 kW 500 kHz CLLC resonant converter with integrated PCB winding transformer," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 469–475.
[10] C. Zhang, P. Li, Z. Kan, X. Chai, and X. Guo, "Integrated half-bridge CLLC bidirectional converter for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3879–3889, May 2018.
[11] H. Wu, Y. Jia, F. Yang, L. Zhu, and Y. Xing, "Two-stage isolated bidirectional DC–AC converters with three-port converters and two DC buses," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4428–4439, Dec. 2020.
[12] Y.-C. Liu, C. Chen, K.-D. Chen, Y.-L. Syu, and N. A. Dung, "High-frequency and high-efficiency isolated two-stage bidirectional DC–DC converter for residential energy storage systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 1994–2006, Sep. 2020.
[13] A. M. Ammar, K. Ali, and D. J. Rogers, "A bidirectional GaN-based CLLC converter for plug-in electric vehicles on-board chargers," in *Proc. IECON 46th Annu. Conf. IEEE Ind. Electron. Soc.*, 2020, pp. 1129–1135.
[14] C. Wei, D. Zhu, H. Xie, Y. Liu, and J. Shao, "A SiC-based 22kW bidirectional CLLC resonant converter with flexible voltage gain control scheme for EV on-board charger," in *Proc. PCIM Eur. Digit. Days; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, 2020, pp. 1–7.
[15] C. Wei, D. Zhu, H. Xie, and J. Shao, "A 6.6kW high power density bidirectional EV on-board charger based on SiC MOSFETs," in *Proc. PCIM Eur.; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, 2019, pp. 246–252.
[16] P. He, A. Mallik, A. Sankar, and A. Khaligh, "Design of a 1-MHz high-efficiency high-power-density bidirectional GaN-based CLLC converter for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 68, no. 1, pp. 213–223, Jan. 2019.
[17] Y. Wang, B. Chen, Y. Hou, Z. Meng, and Y. Yang, "Analysis and design of a 1-MHz bidirectional multi-CLLC resonant DC–DC converter with GaN devices," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1425–1434, Feb. 2020.
[18] Z. Zhang, C. Liu, Y. Si, Y. Liu, Q. Lei, and S. Ai, "Investigation of design methodology of planar transformers for EV on board chargers," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 4139–4145.
[19] Z. Zhang, C. Liu, M. Wang, Y. Si, Y. Liu, and Q. Lei, "High-efficiency high-power-density CLLC resonant converter with low-stray-capacitance and well-heat-dissipated planar transformer for EV on-board charger," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10831–10851, Oct. 2020.
[20] H. Park, M. Kim, H. Choi, J. Jung, S. G. Cheon, and C. U. Lee, "Synchronous rectification method for high frequency CLLC resonant converter," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, 2019, pp. 1–4.
[21] Z. Zhang, C. Liu, Y. Si, Y. Liu, and Q. Lei, "Investigation of adaptive synchronous rectifier (SR) driving scheme for LLC/CLLC resonant converter in EV on-board chargers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 2185–2191.
[22] N. Chen *et al.*, "A synchronous rectification scheme based on inductor voltage sensing for CLLC bidirectional resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 1713–1719.
[23] T. Schobre, K. Siebke, and R. Mallwitz, "Operation analysis and implementation of a GaN based bidirectional CLLC converter with synchronous rectification," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, Genova, Italy, 2019, pp. 1–10.
[24] T. Schobre, K. Siebke, and R. Mallwitz, "Design of a GaN based CLLC converter with synchronous rectification for on-board vehicle charger," in *Proc. PCIM Eur.; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, 2019, pp. 1–5.
[25] S. Zou, J. Lu, A. Mallik, and A. Khaligh, "Bi-directional CLLC converter with synchronous rectification for plug-in electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 998–1005, Mar./Apr. 2018.
[26] A. Sankar, A. Mallik, and A. Khaligh, "Extended harmonics based phase tracking for synchronous rectification in CLLC converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6592–6603, Aug. 2019.
[27] T. Schneider, S. Kratz, R. Wegener, and S. Soter, "Symmetrical bidirectional CLLC-converter with simplified synchronous rectification for EV-charging in isolated DC power grids," in *Proc. IEEE 28th Int. Symp. Ind. Electron.*, 2019, pp. 990–995.
[28] X. Ren, L. Pei, S. Song, J. Zhang, Y. Pei, and L. Wang, "A digital sensor-less synchronous rectification algorithm for symmetrical bidirectional CLLC resonant converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 962–968.
[29] Z. Lv, X. Yan, Y. Fang, and L. Sun, "Mode analysis and optimum design of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 1513–1520.
[30] J. P. Rivera-Barrera, N. Muñoz-Galeano, and H. O. Sarmiento-Maldonado, "SoC estimation for lithium-ion batteries: Review and future challenges," *Electronics*, vol. 6, 2017, Art. no. 102.

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