Unified Control Scheme of Grid-Connected Inverters for Autonomous and Smooth Transfer to Stand-Alone Mode

Minho Kwon, Sungyoul Park, Chang-yeol Oh, Jongpil Lee, *Member, IEEE*, and Sewan Choi, *Fellow, IEEE*

***Abstract*—As one of the approaches for a grid-sustaining inverter, the inverter should cover not only grid-connected (GC) mode but also stand-alone (SA) mode for power supply to local loads; therefore, there are separate control loops for each mode. In order for an uninterruptible power supply to the local load, it should be seamless to change from GC mode to SA mode. This carries two types of issues. One is a transient state caused by switching the control loops. The other is an uncontrolled state during the time interval between a grid failure and its detection, called clearing time. These can lead to unstable voltage for the local load. Hence, a smooth and autonomous mode switching method is required even if the fault detection is late. Existing mode transfer methods considering both the issues have been accompanied by a slow dynamic response, additional sensors, restriction of adopting filter, or controller complexity due to third-order plant. To overcome them, in this article, a control scheme realized by a unified control loop is proposed for smooth and autonomous mode switching with a novel antiderailing control. Furthermore, the proposed control scheme can achieve a high bandwidth for the output power control in GC mode because it is based on controlling the current flowing the inverter-side inductor, and both filter types, *LC* and *LCL*, can be adopted. To validate the proposed concept, simulations and experiments were conducted. The results show that the proposed control scheme can be used to achieve autonomous and smooth mode transition even under reactive power reference and reactive load conditions.**

***Index Terms*—Autonomous, distributed control, grid-forming, grid-sustaining, mode transfer, seamless.**

I. Introduction

RESEARCH on controllers for grid-connected (GC) inverters has previously focused on the fundamental functions of power converters as a grid-feeding system, such as synchronization with the utility grid, harmonic compensation, and maximum power point tracking. As the proportion of renewable energy systems (RESs) in the utility grid gradually increases, the power generated from RESs can no longer be ignored in terms of the management of the utility grid because their stochastic characteristics can lead to grid instability. Hence, additional grid-supporting functions are required, such as reactive power control, low/high voltage/frequency ride through, and grid impedance estimation, along with electric energy storage systems for frequency regulation, peak shifting, etc. Recently, advanced functions for reducing reliance on the utility grid have been studied to realize a grid-sustaining or grid-forming system [1]–[5]. As one of the approaches to create such a system, an inverter should cover not only the GC mode but also the stand-alone (SA) mode for power supply to local loads. The control target of the inverter is different in each mode because regulating the output power of the inverter is required in the GC mode, whereas in the SA mode, the inverter needs to regulate the output voltage for the local load. Accordingly, there are separate control loops for each mode. Switching between the control loops can be realized by forcing careful initial values in compensators (e.g., an integral term in a proportional–integrator (PI) compensator) with accurate timing [6]–[9]. Mismatched initial values or timing leads to an unstable transient response, or worse, over- or undervoltage faults on the inverter. However, it is not easy to calculate precise initial values and detect the timing under varied and unexpected conditions.

To achieve smooth mode transition, combined control schemes presented in [10] and [11] have been implemented by combining control loops between the GC and SA modes and are realized by changing the reference values according to operation mode to avoid the need for the careful setting of the initial values in the compensators. However, these schemes do not consider the transient response during the period between a grid failure and its detection, which is called the clearing time. Another combined scheme proposed in [12] contributes to reducing the transient response in the clearing time by providing an appropriate time for mode transition. However, this method is only effective in the voltage swell condition during the clearing time. It does not consider the voltage sag condition that occurs when energy is imported from the grid.

It is not always easy to determine the accurate timing for changing either the control loop or reference value because some

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time is required to detect a grid failure. Sensitive detection for quick decision making can lead to the incorrect operation caused by noise, disturbance, etc. To overcome this problem, unified control loops have been presented in [13]–[19] that are able to cover both the GC and SA modes without changing the control loop or reference value. Droop control-based schemes in [13]–[15] realize an autonomous mode transition system, but it is difficult to have an enough dynamic bandwidth for achieving smooth mode transition. Control schemes in [16]–[19] require a mathematical model of plants, but it is not usually easy to obtain the accurate model of them.

Indirect current control-based schemes were introduced in [20]–[24]. In this type of scheme, the output current of the inverter is regulated by controlling the voltage and phase across the grid-side inductors. Even though the control loop for the output current does not work properly during a grid outage, the output voltage is regulated within a limited range, which contributes to a stable voltage during the clearing time. However, the output filter for realizing the indirect current control method is restricted to an *LCL* type. Because the *LCL* filter is not always the best in all aspects, the restriction of filter type can be an obstacle. Also, it is desirable to adopt a triple closed loops for the output current control as proposed in [22]–[24] because the transfer function from modulation index to grid-side inductor current is a third-order system. The triple closed loops are implemented by the following: an inner loop for controlling the inverter-side inductor current, a middle loop for controlling the capacitor voltage, and an outer loop for controlling the grid-side inductor current. This cannot outperform a single loop controller in terms of the bandwidth and stability. Moreover, additional current sensors lead to increasing the cost and volume of the inverter.

This article proposes a control scheme realized by a unified control loop to achieve autonomous and smooth mode transition from GC mode to SA mode under both conditions of exporting power to the grid and importing power from the grid. The proposed scheme is oriented to allow no change in the control loop and no forcing of initial values in the compensators when the operating mode is transferred, thereby enabling smooth mode transition. Moreover, the control target of the proposed scheme is autonomously determined by whether the output voltage and frequency are within a predefined range. These characteristics contribute to minimizing the voltage transient and maintaining a stable power supply to the local load even during unexpected grid outages. Additionally, because the proposed control scheme is based on the controlling current flowing the inverter-side inductor, both filter types, *LC* and *LCL*, can be adopted, and a high control bandwidth can be achieved.

II. Traditional Control Scheme

A three-phase half-bridge inverter with an *LC* filter and a local load is shown in Fig. 1. A transfer switch S_i between the local load and the utility grid is controlled by the inverter. This can be utilized to disconnect from the utility grid to the local load when the utility grid failure is detected. While the utility protection switch S_u is governed by the utility [22].

A traditional synchronous reference frame (SRF) based con-

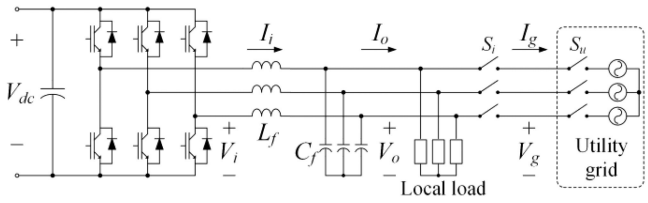

Fig. 1. GC inverter with a local load.

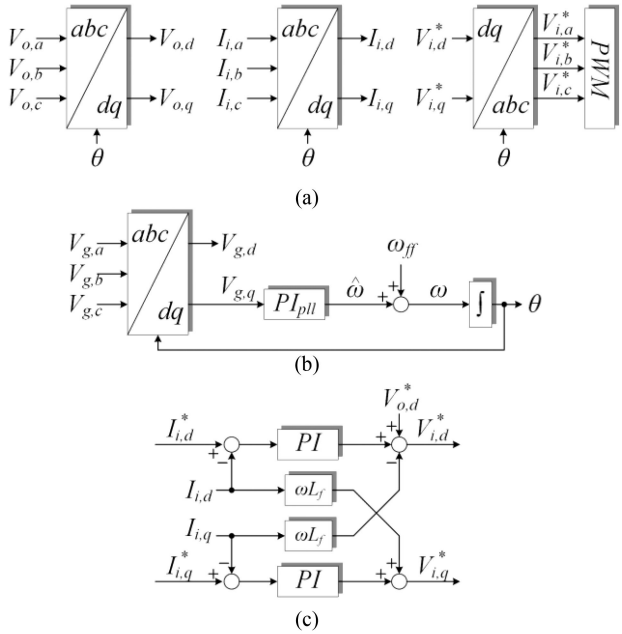

Fig. 2. Traditional SRF-based control block diagram. (a) *dq* coordination. (b) SRF-PLL. (c) Inner current control loop.

shown in Fig. 2(a) and (b), are implemented using the amplitude invariant method, and *d* and *q* axes are defined as the real and imaginary, respectively. Synchronization with the utility grid is implemented using an SRF phase-locked loop (PLL), as shown in Fig. 2(b). The control loop for regulating the current flowing the filter inductor (L_f) is shown in Fig. 2(c). These are widely used as an inner current control scheme for inverters. In GC mode, both switches S_i and S_u have been turned ON, regulating the output power of the inverter can be realized by using the *PQ* open-loop control, as shown in Fig. 3(a). The outputs of the *PQ* open-loop control become the reference of the output current of the inverter as follows:

$$\begin{bmatrix} I_{o,d}^* \\ I_{o,q}^* \end{bmatrix} = \frac{2}{3} \cdot \frac{1}{V_{o,d}^2 + V_{o,q}^2} \cdot \begin{bmatrix} V_{o,d} & -V_{o,q} \\ V_{o,q} & V_{o,d} \end{bmatrix} \cdot \begin{bmatrix} P^* \\ Q^* \end{bmatrix} \quad (1)$$

where P^* and Q^* are the active and reactive power references, respectively. In SA mode, S_i is open to disconnect the inverter and the load from the grid; therefore, the inverter should constantly regulate the output voltage to maintain a stable power supply to the load, which can be implemented by the voltage controller, as shown in Fig. 3(b).

Fig. 4 shows the simplified wiring diagrams among the inverter, the load, and the utility grid according to operating status, where the inverter has been expressed by replacing it

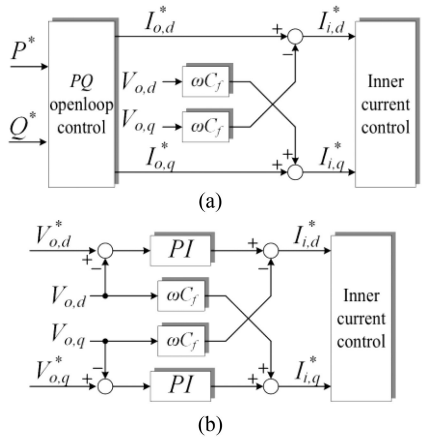

Fig. 3. Outer control loops. (a) *PQ* open-loop control loop for GC mode. (b) Output voltage control loop for SA mode.

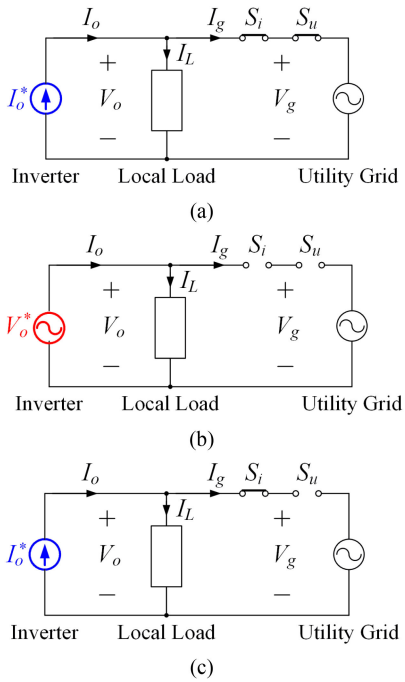

Fig. 4. Simplified wiring diagrams according to operating status. (a) GC mode. (b) SA mode. (c) Clearing time.

the controllers are tracking their reference well. In GC mode, the grid is normal (S_i and S_u are closed) and the inverter controls the output current, as shown in Fig. 4(a). In SA mode, S_i and S_u are open and the inverter controls the output voltage, as shown in Fig. 4(b). Fig. 4(c) shows another situation in which the grid has unexpectedly failed (S_u is open) as S_i is not open yet because the failure has not been detected.

The voltage and current phasors for each status in Fig. 4 are depicted in Fig. 5, when the local load is an *RC* load, P^* is greater than the active power of the load, and Q^* is zero value. In the case of the GC mode, both the output voltage (V_o) and the voltage induced by the load are the same as the grid voltage (V_g), and therefore, the current flowing through the load (I_L) is

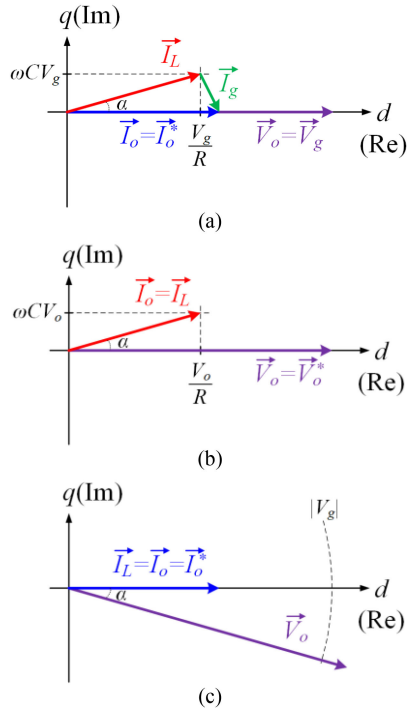

Fig. 5. Phasor diagram depicted in Fig. 4. (a) GC mode. (b) SA mode. (c) Clearing time.

determined by its impedance and voltage, as follows:

$$\begin{bmatrix} I_{L,d} \\ I_{L,q} \end{bmatrix} = \begin{bmatrix} \frac{1}{R} & -\omega C \\ \omega C & \frac{1}{R} \end{bmatrix} \cdot \begin{bmatrix} V_{g,d} \\ V_{g,q} \end{bmatrix} \tag{2}$$

where R and C are the resistance and capacitance of the load, respectively. The phase angle of the I_L vector is determined as follows:

$$\alpha = \tan^{-1}(\omega CR). \tag{3}$$

The output current (I_o) tracking its reference is determined by (1), and the grid current (I_g) is determined as the difference between I_o and I_L, as follows:

$$\begin{bmatrix} I_{g,d} \\ I_{g,q} \end{bmatrix} = \begin{bmatrix} I_{o,d} \\ I_{o,q} \end{bmatrix} - \begin{bmatrix} I_{L,d} \\ I_{L,q} \end{bmatrix}. \tag{4}$$

In SA mode, V_o is regulated by the inverter as its reference. Thus, I_o is determined by the impedance of the load as follows:

$$\begin{bmatrix} I_{o,d} \\ I_{o,q} \end{bmatrix} = \begin{bmatrix} I_{L,d} \\ I_{L,q} \end{bmatrix} = \begin{bmatrix} \frac{1}{R} & -\omega C \\ \omega C & \frac{1}{R} \end{bmatrix} \cdot \begin{bmatrix} V_{o,d} \\ V_{o,q} \end{bmatrix}. \tag{5}$$

During the clearing time, I_L is determined as I_o, which is tracking $I_o{}^*$ as in the GC mode. Thus, V_o is determined by I_o and the load impedance, as follows:

$$\begin{bmatrix} V_{o,d} \\ V_{o,q} \end{bmatrix} = \frac{1}{(\omega CR)^2 + 1} \cdot \begin{bmatrix} R & -\omega CR^2 \\ \omega CR^2 & R \end{bmatrix} \cdot \begin{bmatrix} I_{o,d} \\ I_{o,q} \end{bmatrix} \tag{6}$$

where the phase angle of the V_o vector is the same as in (3). In this case, $V_{o,d}$ is increased, caused by P^* greater than the

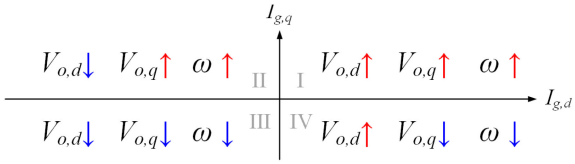

Fig. 6. Trend of the deviations depending on the cutoff grid current.

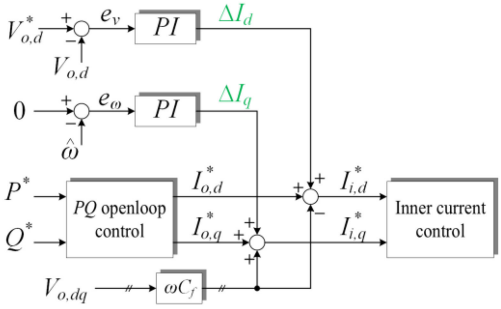

Fig. 7. Ideal concept of the proposed control scheme.

active power of the load, and also, $V_{o,q}$ is decreased, which leads to a decreasing ω caused by the uncontrolled $V_{o,q}$ in the PLL block. On the other hand, in the case of *RL* load, it can be inferred that $V_{o,q}$ and ω are increased. And if P^* is smaller than the active power of the load, decreasing $V_{o,d}$ can be inferred. Concretely, these voltage and frequency variations depend on the grid current at the time of disconnection from the utility grid. The cutoff grid current is determined as the current difference between the output and the local load. Fig. 6 shows the trend of the deviations depending on the cutoff grid current. The case of Fig. 5(c) is an example of the fourth-quadrant cutoff grid current, as shown in Fig. 6. To supply stable power to the local load even under an unexpected failure of the utility grid, the variations in the output voltage and frequency during the clearing time should be minimized. In this article, remote loads, which may be located between S_i and S_u, are omitted in order to simplify the analysis. If there are the remote loads, they can be interpreted by including them in the local load. In that case, the current phasor in Fig. 5(b) will be changed depending on the remote load condition; however, the trend of the deviations is not different.

III. Proposed Control Scheme

A. Ideal Concept

The proposed mode transfer scheme is oriented to avoid a sudden change in control loops by integrating the control loops for the GC and SA modes, thereby achieving autonomous and smooth mode transitions. Fig. 7 shows the ideal concept of the proposed control scheme. Two control loops compensating the output voltage and frequency for the SA mode are integrated with the *PQ* open-loop control for the GC mode, where the reference $V^*_{o,d}$ is set as the nominal magnitude of the grid voltage, and $\hat{\omega}$ is the output of the compensator in the PLL and its reference is

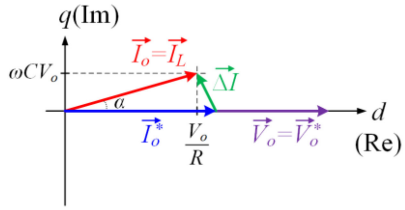

Fig. 8. Phasor diagram of the proposed control scheme for an example of the fourth-quadrant cutoff grid current.

zero. The inner current reference is determined as follows:

$$\begin{bmatrix} I^*_{i,d} \\ I^*_{i,q} \end{bmatrix} = \begin{bmatrix} I^*_{o,d} \\ I^*_{o,q} \end{bmatrix} + \begin{bmatrix} 0 & \omega C_f \\ \omega C_f & 0 \end{bmatrix} \cdot \begin{bmatrix} V_{o,d} \\ V_{o,q} \end{bmatrix} + \begin{bmatrix} \Delta I_d \\ \Delta I_q \end{bmatrix} \quad (7)$$

where ΔI_d is the output of PI block compensating the output voltage and ΔI_q is the output PI block compensating the frequency.

In GC mode, under the magnitude and frequency of the grid voltage that are exactly the same as the expected value ($V^*_{o,d}$ and ω_{ff}), the errors e_v and e_ω are ideally zero. Therefore, both ΔI_d and ΔI_q are zero, which means that the outer loops for the voltage and frequency control do not affect the current references in the control block; therefore, the inverter is operated as a current source by commanded *PQ* reference. On the other hand, after disconnection from the utility grid, the outer loops are autonomously activated because of the voltage and frequency variations, and the inner current reference (I^*_i) is smoothly adjusted to regulate the output voltage and frequency, where a constant *PQ* reference does not affect the dynamic response for regulating them; therefore, the inverter is operated as a voltage source. In other words, it has a decoupling characteristic between the outer loops and *PQ* open loop even though I^*_i is determined by the sum of their outputs.

As a result, the proposed control scheme does not need to change the control loop according to the operating mode and can cover not only in GC and SA modes but also during the clearing time. This contributes to an autonomous and smooth mode transition. Fig. 8 depicts the voltage and current phasors showing the steady state of the proposed control scheme after disconnection from the grid under unchanged *PQ* reference and the load conditions. The steady-state value of ΔI_{dq} is an opposite vector of the cutoff grid current.

B. Practical Concept

Indeed, the ideal concept, as shown in Fig. 7, is impracticable because the expected values of the grid voltage and frequency are not exactly the same as the real values. The expected values are a constant value, but the practical grid voltage and frequency are considered normal within some range; moreover, there are noise, small perturbations, possible tolerance, etc. Even if the difference between the expected and real values is quite small, it leads to saturation of the PI compensators of the outer loops or acts as a disturbance on the current control loop, thereby leading to an unstable control system.

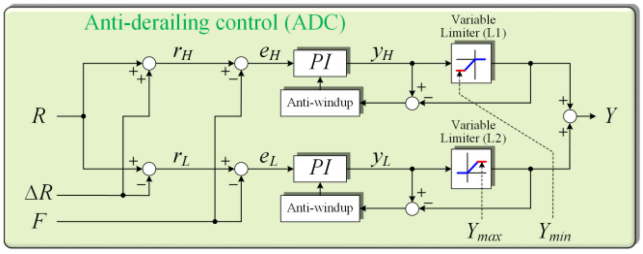

Fig. 9. ADC for replacing the outer voltage and frequency control loops.

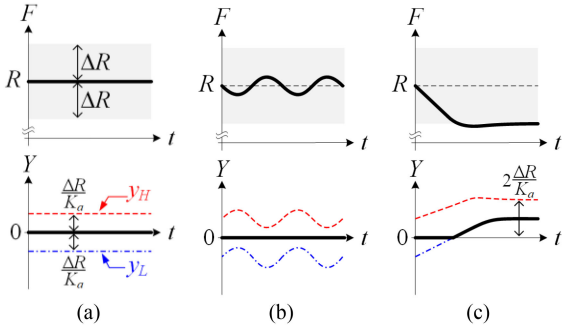

Fig. 10. Key waveforms showing the characteristic of the ADC. (a) Scenario I. (b) Scenario II. (c) Scenario III.

Hence, an antiderailing control (ADC) for regulating voltage and frequency is proposed to implement the proposed scheme as a practical method, as shown in Fig. 9, where R, ΔR, F, and Y are a reference, an allowable range, a feedback signal, and an output signal, respectively. The upper limit value of $L1$ and the lower limit value of $L2$ are fixed at zero, but the upper limit value of $L2$ and the lower limit value of $L1$ are utilized to limiting Y. Fig. 10 shows the key waveforms showing the characteristic of the ADC when Y can compensate for F. There are the following three example scenarios.

1) *Scenario I*: There is no noise or perturbation on F, which is being well regulated by a system other than the ADC, and its reference is equal to R. Because the errors e_H and e_L are the constant positive and negative values, respectively, and y_H and y_L are in saturation with a positive and negative value, respectively, which are as follows:

$$y_H = \frac{\Delta R}{K_a} \tag{8}$$

$$y_L = -\frac{\Delta R}{K_a} \tag{9}$$

where K_a is the antiwindup gain of the PI compensator [25]. The output Y is a zero value owing to the upper and lower limiters.

2) *Scenario II*: There is some fluctuation in the feedback signal, but its magnitude is within the allowable range, and the average of F is still regulated by another system. This fluctuation leads to fluctuations in the output of the PI compensators. The magnitude and phase of fluctuation on y_H and y_L are dominantly determined by PI gains. Within the allowable range of the feedback, y_H is greater than zero, and y_L is smaller than zero; therefore, Y is still zero owing to the limiters.

3) *Scenario III*: Eliminating the regulation for the feedback leads to its divergence to rising or falling. This scenario shows that the feedback diverges to falling caused by the absence of its regulation. The decreasing feedback signal leads to an increase in the outputs of the PI compensators. When the increasing y_L approaches zero, the lower-side PI compensator becomes activated, and Y becomes equal to y_L; therefore, the feedback signal is regulated as r_L by the lower-side PI compensator, where the reference of the lower-side PI compensator is as follows:

$$r_L = R - \Delta R. \tag{10}$$

The upper-side PI compensator is still in saturation, and its output is as follows:

$$y_H = 2\frac{\Delta R}{K_a}. \tag{11}$$

In the same condition, if the feedback signal diverges to rising, the upper-side PI compensator becomes activated; therefore, the feedback signal is regulated as r_H. Its reference is as follows:

$$r_H = R + \Delta R. \tag{12}$$

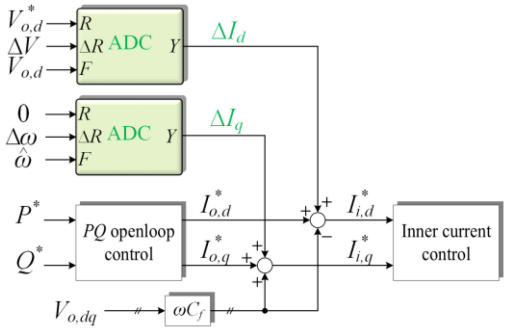

Fig. 11. Final proposed control scheme.

Accordingly, the voltage and frequency control loops of the proposed control scheme in Fig. 7 can be replaced by the ADC, as shown in Fig. 11. This contributes to eliminating the effect of noise, small perturbation, and sensing tolerance within a predefined allowable range in the GC mode. The only output voltage or frequency out of the range, such as in the case of grid failure, activates the ADCs in order to regulate them.

Fig. 12 shows simulation results showing a mode transfer situation from the proposed control scheme under the conditions listed in Tables I and II. The same values of the PI gains have been used for both compensators in the ADC and set by a design procedure for the traditional loop, as shown in Figs. 2 and 3. $V^*_{o,d}$ has been set to the peak value of a phase voltage for a nominal value of the utility grid. The allowable bands for the output voltage and frequency have been set to 1.6% (5 V) and 0.8% (0.5 Hz) for the nominal values, respectively. The

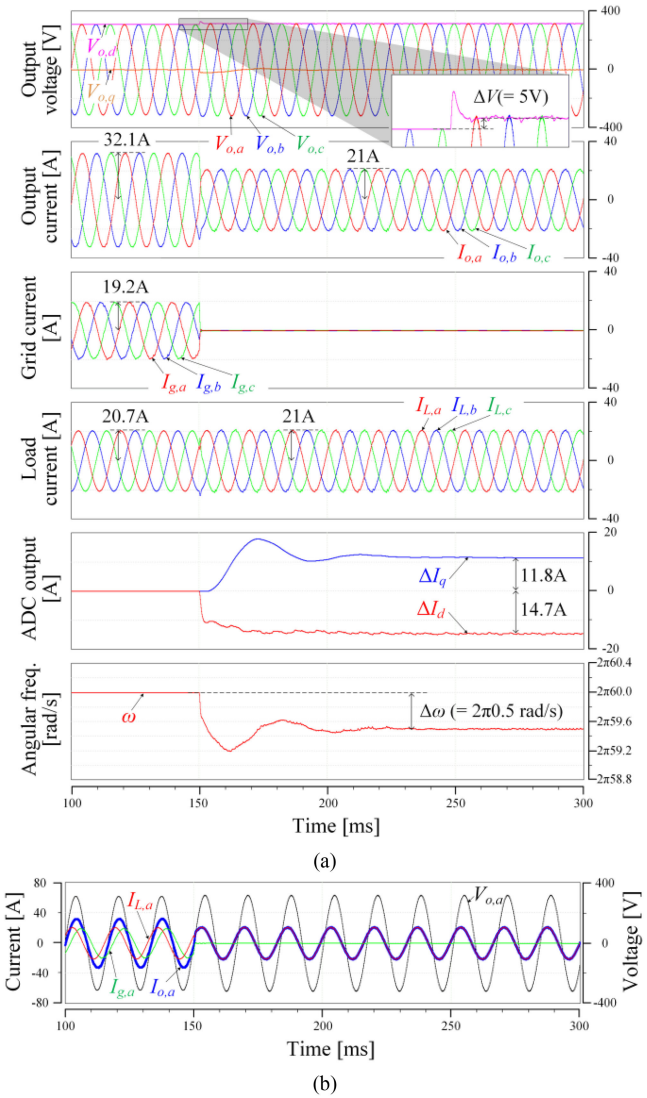

Fig. 12. Simulation result showing mode transition of the proposed control in the time domain. (a) Overall key waveforms. (b) *a*-phase voltage and currents.

TABLE I
PARAMETERS USED IN SIMULATION AND EXPERIMENT

Parameters	Symbols	Values	Unit
Nominal grid voltage	V_g	380	$V_{L\text{-}L}$
Nominal angular frequency	ω_{ff}	$2\pi60$	rad/s
Output voltage reference	$V_{o,d}^*$	$220\sqrt{2}$	V
Filter inductance	L_f	150	μH
Filter capacitanc	C_f	25	μF
Switching frequency	f_s	20	kHz
DC voltage	V_{dc}	750	V
Allowable voltage band	ΔV	5	V
Allowable angular frequency band	$\Delta\omega$	$2\pi0.5$	rad/s

TABLE II
POWER REFERENCES AND LOAD CONDITION FOR SIMULATION

Parameters	Symbols	Values	Unit
Active power refereene	P^*	15	kW
Reactive power reference	Q^*	0	VAR
Local load resistance	R_L	18.15	Ω
Local load capacitance	C_L	100	uF

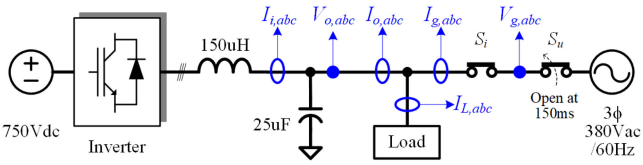

Fig. 13. Simulation schematic and measurement points.

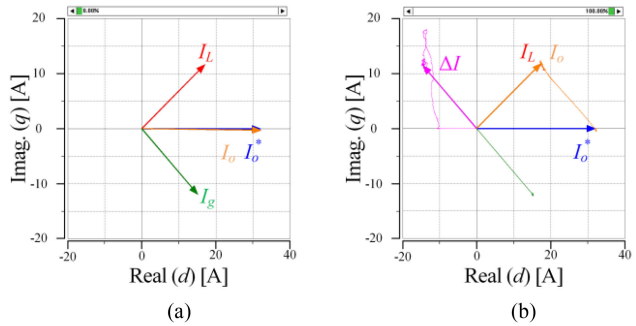

Fig. 14. Simulation result in the complex domain at (a) 100 and (b) 300 ms.

simulation schematic and the measurement points of the voltages and currents are shown in Fig. 13.

Before 150 ms, both S_i and S_u have been closed, which means normal conditions of the utility grid. The output current reference according to *PQ* reference can be calculated by (1), as follows: $I_{o,d}^* = 32.1$ A and $I_{o,q}^* = 0$ A. The load current can be obtained by its impedance and voltage, as follows: $I_{L,d} = 17.1$ A and $I_{L,q} = 11.7$ A. The current difference between I_o and I_L is being injected into the grid. As S_u is turned OFF at 150 ms, I_g becomes zero, which leads to deviations of V_o and ω. However, V_o and ω are regulated within a predetermined range, although it shows a little overshoot. As a result, it can be seen that the voltage and current of the load are scarcely changed even though S_u is unexpectedly turned OFF. Fig. 12(b) shows the *a*-phase voltage and currents overlapped on a grid to show phase difference among them. Before 150 ms, I_o is in phase with the V_o because of zero value of Q^*; meanwhile, the phase of I_L is leading V_o because the load is capacitive. The phase of I_g is lagging V_o caused by the difference between I_o and I_L. After 150 ms, I_o becomes equal to I_L, which is still leading V_o.

For the same simulation data, the vector diagrams, as shown in Fig. 14, to show current phasors before and after S_u is turned OFF have been plotted by the PSIM simulation tool. The phasors, as shown in Fig. 14(a), are the current vectors at 100 ms and correspond with the waveforms in Fig. 12(b) before 150 ms. In this figure, I_o is approximately equal to I_o^*, which means that it is well regulated, and it can be seen that the three vectors of I_o, I_L, and I_g are in equilibrium, and ΔI does not appear because it is a zero value. The phasors of the final state (at 300 ms) and their moving trajectories are shown in Fig. 14(b). It can be seen that I_o is moved from I_o^* to I_L, I_g goes to zero, and ΔI is presented, where ΔI becomes an opposite vector of I_g ideally, but it is not precisely opposite because the load current has a slight variation caused by both V_o and ω deviated as much as

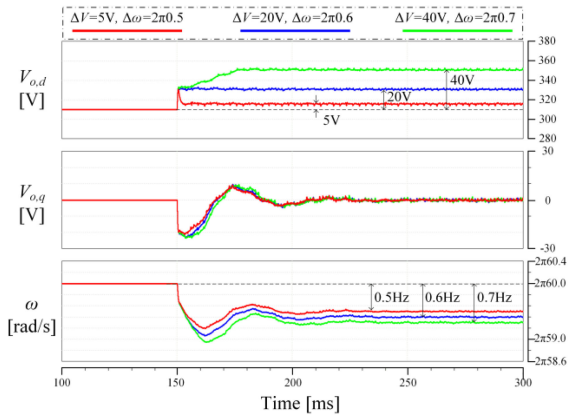

Fig. 15. Simulation result showing the output voltage and frequency deviation according to different allowable bands.

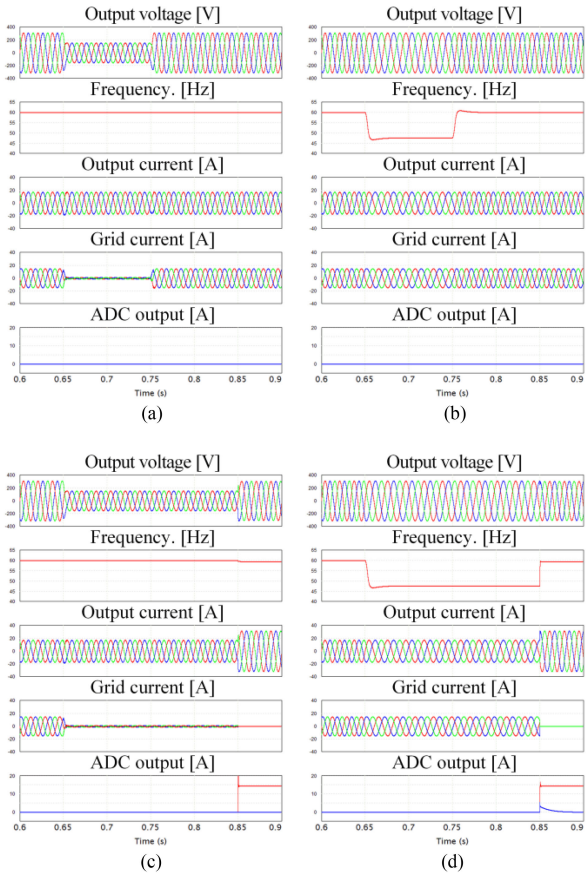

Fig. 16. Simulation results of LVRT and LFRT condition. (a) Voltage sag for 100 ms. (b) Frequency sag for 100 ms. (c) Voltage sag over 200 ms. (d) Frequency sag over 200 ms.

ΔV and $\Delta\omega$, respectively. The real and imaginary values of each phasor from the simulation result are listed in Table III.

C. Wider Normal Range Condition

When a normal operating range of the grid voltage and frequency is wide, ΔR is should be set larger than the range

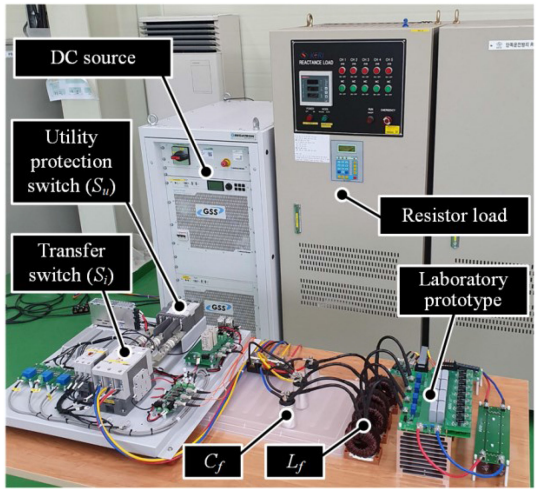

Fig. 17. Experimental setup.

TABLE III
CURRENT VALUE FROM SIMULATION RESULT

Parameters	Symbols [Unit]	@100ms		@300ms	
		d	q	d	q
Output current reference	I_o^* [A]	32.1	0	32.1	0
Output current	I_o [A]	32.1	-0.3	17.4	11.8
Load current	I_L [A]	17.1	11.7	17.4	11.8
Grid current	I_g [A]	15	-12	0	0
ADC output	ΔI [A]	0	0	-14.7	11.8

to prevent activating of ADC within the range. If ΔR is a large value, the time for activation of PI compensator in the ADC may be longer; however, an autonomous and smooth transition is still valid. To shorten this time, K_a should be increased [25].

Fig. 15 shows the output voltage and frequency deviation according to different allowable bands. Under the greatest allowable band conditions ($\Delta V = 40$ V and $\Delta\omega = 2\pi 0.7$), the settling time has been the longest because it took longer for $V_{o,d}$ to go out of the range; however, there is no voltage overshoot, and the percent undershoots on ω have been almost the same under the three conditions.

D. Voltage/Frequency Ride Through

To keep the output current even under voltage/frequency sag/swell condition, ΔI_{dq} should be forced as zero until S_i is opened. The forcing can be implemented by adjusting the limiter values in their ADCs. Fig. 16 shows simulation results of low voltage ride through (LVRT) and low-frequency ride-through (LFRT) operations. The simulation condition is keeping the output current for 200 ms under the output voltage or frequency sag condition. In Fig. 16(a) and (b), the voltage and frequency sags are recovered after 100 ms, respectively; thus, the operation mode stays in GC mode. As shown in Fig. 16(c) and (d), when the sags last for 200 ms, S_i is opened to disconnect from the grid and the output voltage regulation is started by disabling the forcing for the ADCs.

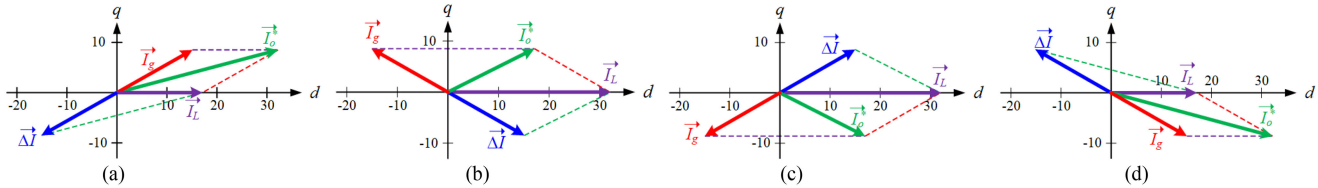

Fig. 18. Current phasor diagram from each experimental condition. (a) First-quadrant grid current. (b) Second-quadrant grid current. (c) Third-quadrant grid current. (d) Fourth-quadrant grid current.

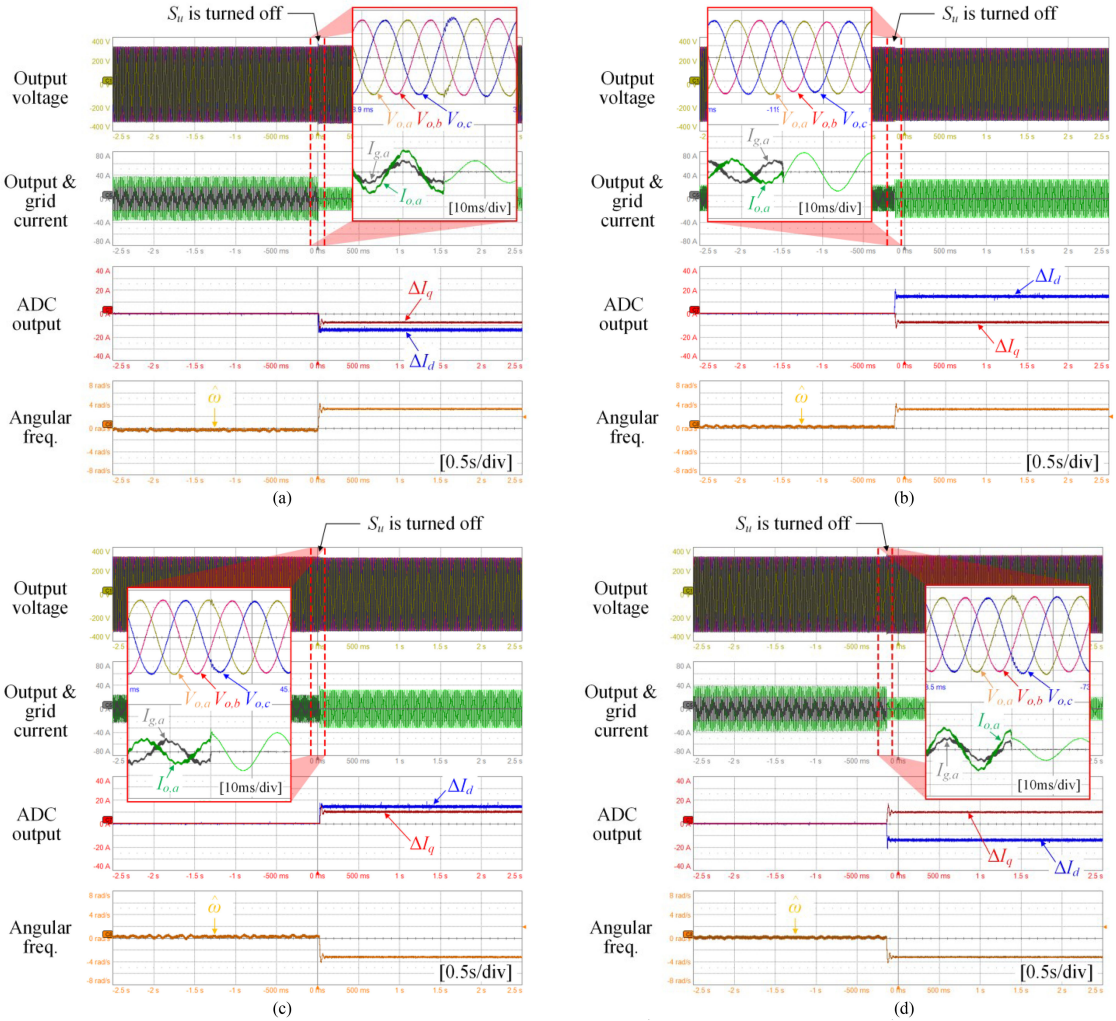

Fig. 19. Experimental result of mode transition. (a) Under first-quadrant grid current. (b) Under second-quadrant grid current. (c) Under third-quadrant grid current. (d) Under fourth-quadrant grid current.

IV. Experimental Results

To demonstrate the feasibility of the proposed control scheme, a laboratory prototype, a 30-kW three-phase half-bridge inverter, was used. The experimental setup is shown in Fig. 17. The proposed control is realized by a 32-b digital signal processor (TMS320F28377D from TI). A programmable dc power supply is utilized for the dc source. The utility grid is directly connected through S_i and S_u. S_i will be open after an islanding is detected. However, the islanding detection is not focused on this article; hence, S_i has always been turned ON in this experiment. The specifications of the prototype and the experimental schematic are the same with simulation, which is given in Table I and Fig. 13, respectively. The local load has been implemented by a resistor load only. Instead, to provide proof of four cases according to the cutoff grid current, the *PQ* reference and the load power have been set differently, as listed in Table IV. These conditions determine the cutoff grid current and are classified

TABLE IV
EXPERIMENTAL CONDITIONS

Parameters	Symbols	Unit	Conditions			
			I	*II*	*III*	*IV*
Active power referece	P^*	kW	15	8	8	15
Reactive power referece	Q^*	kVar	4	4	-4	-4
Resistive load power	P_L	kW	8	15	15	8

TABLE V
CURRENT VALUE ACCORDING TO EXPERIMENTAL CONDITIONS

Parameters	Symbols [Unit]	Conditions			
		I	*II*	*III*	*IV*
Output current referece	$I_{o,d}{}^*$ [A]	32.1	17.1	17.1	32.1
	$I_{o,q}{}^*$ [A]	8.6	8.6	-8.6	-8.6
Load current	$I_{L,d}$ [A]	17.1	32.1	32.1	17.1
	$I_{L,q}$ [A]	0	0	0	0
Grid current	$I_{g,d}$ [A]	15	-15	-15	15
	$I_{g,q}$ [A]	8.6	8.6	-8.6	-8.6
ADC output	ΔI_d [A]	-15	15	15	-15
	ΔI_q [A]	-8.6	-8.6	8.6	8.6

by the position of the quadrant of the cutoff grid current with respect to the *dq* axes, as shown in Fig. 6.

Depending on the conditions, the experimental results can be expected, as shown in Fig. 18. For all conditions, unquestionably, there is no reactive current flowing the load because it is a resistor load. Under the first condition [see Fig. 18(a)], the magnitude of I_o^* is greater than that of I_L because P^* is greater than P_L, and I_o^* is leading I_L owing to a positive value of Q^*; therefore, the phasor of I_g is on the first quadrant. Under the second condition [see Fig. 18(b)], I_o^* is smaller than I_L and leading I_L; therefore, the phasor of I_g is on the second quadrant. Under the third condition [see Fig. 18(c)], I_o^* is smaller than I_L and lagging I_L; therefore, the phasor of I_g is on the third quadrant. Under the fourth condition [see Fig. 18(d)], I_o^* is greater than I_L and lagging I_L; therefore, the phasor of I_g is on the fourth quadrant. When the grid current is zero due to the disconnection, it can be expected that the vector of ΔI becomes an opposite vector of I_g, as shown in Fig. 18. Each current value shown in Fig. 18 is listed in Table V and can be calculated using the experimental conditions listed in Table IV and the nominal grid voltage.

Four experimental waveforms according to the conditions are provided in Fig. 19. In order to show the mode transition performance of the proposed control scheme, S_u has been opened at an arbitrary time during operation in GC mode. The waveforms of ΔI_{dq} and $\hat{\omega}$ have been implemented using a digital-to-analog converter. These have different aspects depending on the experimental conditions. Before S_u is turned OFF, the output voltage is determined by the grid voltage, and the output current is regulated by the inverter according to the *PQ* reference listed in Table IV. Even though I_L is not seen in the figure, it can deemed the difference between I_o and I_g; moreover, I_o after opening S_u is almost the same as I_L. It can be seen that ΔI_{dq} and $\hat{\omega}$ are zero, meaning that the ADCs have not been activated because the output voltage and frequency are within the allowable range. Disconnecting the utility grid by opening S_u gives rise to deviations in the output voltage and frequency. However, it can be seen that the deviations are regulated within predefined values of ΔV and $\Delta\omega$. Note that the transient on the output voltages, at the moment the grid is disconnected, is quite small, as shown in zoomed waveforms in Fig. 18. This shows that the output voltage and frequency are well regulated in spite of an unexpected disconnection from the grid, which means that the control target of the inverter is changed from the output power to the output voltage autonomously and smoothly. Although there are some harmonics on the current waveforms in the experimental result, considering only the fundamental waves, it can be seen that the phasors in Fig. 18 correspond with the experimental waves by looking ΔI_{dq} and the magnitude and phase of $I_{o,a}$ and $I_{g,a}$ in Fig. 19.

V. CONCLUSION

In this article, a control scheme was proposed that achieves autonomous and smooth mode transition from the GC mode to the SA mode by integrating the control loops for both modes. Through an analysis based on an ideal concept, the operating principle and problem in the traditional schemes were derived. A practical method using the ADC was also proposed. Through experimental results using a laboratory prototype, it was confirmed that the output voltage and frequency are regulated autonomously and smoothly within a limited range, even during an unexpected outage of the utility grid.

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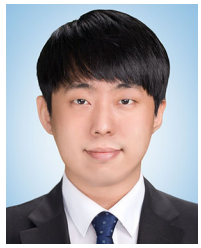

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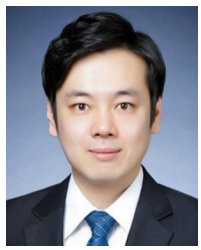

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