The Impact of Inverter Dead-Time in Single-Phase Wireless Power Transfer Systems

Utkarsh D. Kavimandan, *Graduate Student Member, IEEE*, Veda Prakash Galigekere, *Senior Member, IEEE*, Burak Ozpineci, *Fellow, IEEE*, Omer Onar, *Senior Member, IEEE*, and Satish M. Mahajan, *Senior Member, IEEE*

***Abstract*—In this article, the effect of the dead-time on a single-phase wireless power transfer (WPT) system is studied in detail. In practice, the dead-time is always placed between the complementary switching pulses of the inverter phase-leg. At higher operating frequencies, the dead-time issues in the resonant inverter become critical, especially as the power level increases. The detailed analysis of the dead-time on a WPT system is discussed for different operating conditions of the inverter duty-cycle and power factor. The switching characteristics of the WPT system inverter are analyzed, and the notch phenomenon that appears at the output of the inverter is also discussed. A notch equation based on the observations is derived to predict the notch occurrence during the system operation. Furthermore, the mathematical expressions are presented for different notch conditions. Subsequently, the effect of the notches on the sensitivity and the power transfer of the series–series compensated WPT system is analyzed. Finally, the approach is verified experimentally on an 8-kW WPT system prototype, and the results are compared with the theoretical analysis.**

***Index Terms*—Dead-time, notch, sensitivity analysis, voltage polarity reversal (VPR), wireless power transfer (WPT).**

I. Introduction

THE introduction of wireless charging systems for electric vehicles (EVs) can alleviate the range anxiety among EV consumers and assist in the adoption of EVs. Wireless power transfer (WPT) systems comprise of coupled inductor coil pairs, which resonate at a high-frequency (HF). The magnetic field stored between the air-gap is utilized to transfer power from the source to the load. WPT systems have distinct benefits such as noncontact power transfer, convenient, and safe operations in inclement weather conditions, and improved aesthetics as compared to the plug-in charging systems. Consequently, the WPT systems have been promoted in applications such as EV charging, consumer electronics, biomedical applications, and autonomous underwater vehicles (AUVs) [1]–[7]. The implementation of dynamic WPT systems to accomplish the in-motion charging of EVs may help in reducing the battery size, thereby reducing the overall weight and cost of the EVs.

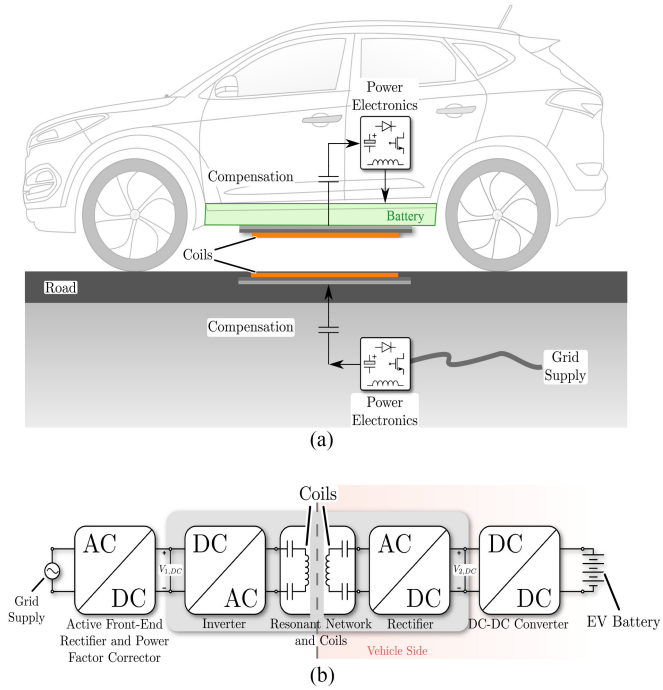

Fig. 1. (a) Typical WPT system for EV charging (b) block schematic of WPT system for EV charging.

Fig. 1(a) depicts a typical configuration of a WPT system for an EV battery charging application and Fig. 1(b) shows the typical block schematic of the WPT system. The transmitter-coil is embedded in the road while the associated power electronics are placed roadside. The EV is equipped with the receiver-coil installed underneath the chassis and the on-board power electronics to regulate the battery charging process. At first, the ac supply from the grid is rectified to a dc voltage by adopting an intermediate active rectifier with power-factor-correction stage. The rectified dc voltage is converted to an HF ac voltage and is applied to the compensation network and the transmitter-coil.

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Utkarsh D. Kavimandan and Satish M. Mahajan are with the Electrical and Computer Engineering Department, Tennessee Technological University, Cookeville, TN 38505 USA (e-mail: udkavimand42@tntech.edu; smahajan@tntech.edu).

Veda Prakash Galigekere, Burak Ozpineci, and Omer Onar are with the Oak Ridge National Laboratory, National Transportation and Research Center, Knoxville, TN 37932 USA (e-mail: galigekerevn@ornl.gov; burak@ornl.gov; onaroc@ornl.gov).

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The primary compensation network is used to reduce the reactive power requirement from the primary power source [7]. Due to the time-varying magnetic field, an emf is induced in the receiver coil, which is further rectified and applied to the battery.

The secondary-side compensation network is implemented to improve the power transferred to the load. An intermediate dc–dc regulation is sometimes adopted to control the battery charging process, as shown in Fig. 1(b). The inverter at the primary-side typically comprises of an H-bridge (full-bridge) configuration and constitutes of two phase-legs. The main design challenges in the WPT system is to sustain the rated power transfer and maintain the efficiency despite variations in the critical performance parameters such as operating frequency, misalignment between the coils, and the variations in the load conditions. Consequently, the present research in the WPT systems is associated with the new HF inverter architectures [8]–[10], different compensation schemes [11]–[14], different coil designs [15]–[18], different control algorithms to improve the system performance [19]–[23], and different shielding techniques to mitigate the electromagnetic emissions [24]–[26]. However, the system and device-level implementation issues such as dead-time have not been studied in detail.

A dead-time is defined as the time interval during which both the switches in the inverter phase-leg are OFF. A dead-time is always introduced between the complementary switching instances of the inverter phase-leg to avoid the shoot-through of the input dc source. If the issues associated with dead-time are not addressed appropriately, it may result in waveform distortions. With the introduction of the high-power and HF WPT systems, the issues of dead-time have become more prominent. Multiple papers have investigated this phenomenon in applications such as dual active bridge (DAB) converters and resonant dc–dc converters [27]–[32]. Detailed theoretical analysis on the isolated bidirectional converters due to the dead-time and the phenomenon of voltage-polarity reversal (VPR) is reported in [27]. In [29], the effect on the switch commutations in the series resonant converter is reported, and a method to eliminate the VPR is discussed. The dead-time effect on the WPT inverter has been reported in [33] and [34]. Reference [33] examines the dead-time impact on the DAB configuration of the WPT system and discusses a control strategy to eliminate the dead-time effect. In [34], the dead-time effect on the WPT inverter is reported, and the inverter switching losses are evaluated. The dead-time effect creates excess switching transitions at the inverter output, which results in the excess switching losses [34]–[36] In [37], the dead-time effect on the charging profile of the BMW i3 is evaluated without any experimental validation.

Considering the situation above, this article presents a detailed theoretical analysis and experimental verification of the dead-time effect on the WPT system inverter. This article is organized as follows: Section II illustrates the detailed operational waveforms for different operating conditions of the WPT full-bridge inverter. The conditions for the occurrence of VPR or notches are presented, and the notch equation is derived. Section III presents the Fourier series representation of the notch for the different operating conditions. Subsequently, the impact of notches on the fundamental component of the voltage and its harmonics are also presented. The sensitivity analysis and the impact on the power transfer due to the dead-time effect are discussed in Section IV. Section V presents the experimental validation results for the theoretical analysis, and Section VI concludes this article.

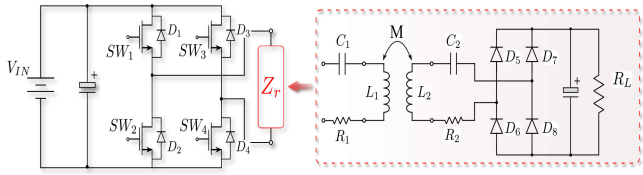

Fig. 2. Simplified circuit of WPT system with primary and secondary side equivalent to the resonant impedance, Z_r.

II. Switching Characteristics of a WPT HF Inverter

Due to its simplicity, a series–series compensated WPT system is used for the dead-time analysis in this article. A typical WPT system can be simplified to an equivalent circuit with a resonant load, Z_r as shown in Fig. 2, where V_{IN} is the dc input source and the resonant load is connected across the phase-legs of the full-bridge inverter comprising of the MOSFET switches, SW_1 to SW_4. A typical control objective in a WPT system is to control the power transferred to the load. The easiest method to control the flow of power is by implementing a modulation scheme for the inverter. Several fixed-frequency modulation techniques can be applied to the full-bridge inverter to control the fundamental voltage component [38]. However, a traditional-phase shift control to modulate the inverter output is considered in this article. The phase-shift angle, α is defined such that: 0° phase-shift between the inverter phase-legs (gate signals of the diagonal MOSFETs) results in the full duty-cycle and 180° phase-shift achieves zero duty-cycle at the inverter output.

Following assumptions are made to study the switching characteristics of the inverter in the WPT system:

1) MOSFETs are ideal, and they turn ON and OFF instantly.
2) MOSFET output capacitance is zero in the analysis, since it does not have any impact on the system operation as also validated by the experimental results.
3) The series equivalent load is resonant during the entire operation;

A. Switching Characteristics Without Dead-Time

Fig. 3 depicts the ideal switching characteristics and the equivalent circuit operation of an inverter without dead-time, which is not feasible in practical applications but addressed here for baseline discussions. The waveform v_{GS_i} denotes the gate pulses of the corresponding MOSFET switches, v_{ao} and v_{bo} indicate the pole voltages (or phase voltages) of the inverter phase-legs, v_{ab} is the square-wave voltage across the inverter phase-legs, $v_{ab_{01}}$ (dashed sine wave) is the fundamental component of the inverter output voltage, and i_{ab} (sine wave in red) is the sinusoidal current flowing through the load impedance, and ϕ is the phase angle between the fundamental component of the voltage and the sinusoidal current. The modes of operation without any dead-time are listed as follows:

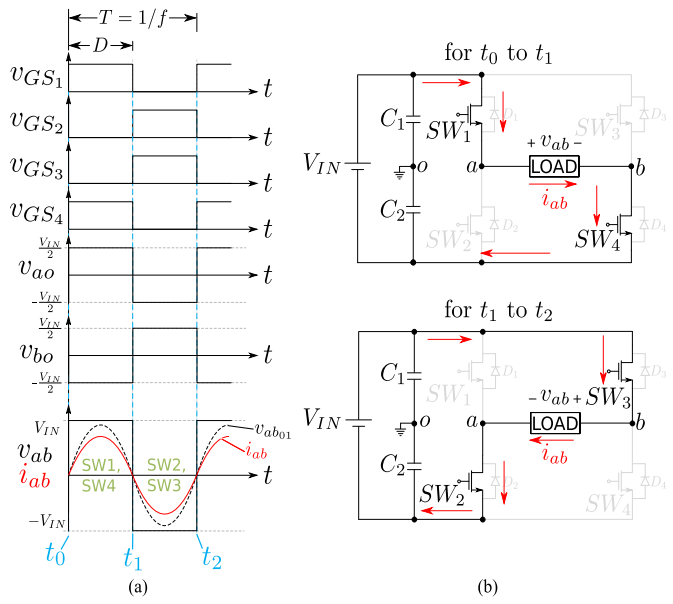

Fig. 3. (a) Operational waveforms of WPT system without the dead-time, and (b) operational modes of WPT system without the dead-time.

Mode 1: From t_0 to t_1- Switch SW_1 and SW_4 are ON and SW_2 and SW_3 are OFF. The current is positive and flows through SW_1 and SW_4. The pole voltage v_{ao} is positive and v_{bo} is negative. Consequently, the output voltage across the load is $+V_{IN}$.

Mode 2: From t_1 to t_2- Switch SW_2 and SW_3 are ON and SW_1 and SW_4 are OFF. The current is negative and flows through SW_2 and SW_3. The pole voltage v_{ao} is negative and v_{bo} is positive, which results in the output voltage across the load to be $-V_{IN}$.

B. Switching Characteristics With Dead-Time

1) Case 1: When the phase-angle, $\phi = 0$ and phase-shift, $\alpha = 0$, the corresponding switching characteristics and modes of operation are depicted in Fig. 4, where t_d is the dead-time interval between the complementary switching instances of the inverter. During the dead-time, both the switches in the inverter phase-leg are OFF, and the current flows through the MOSFET body-diodes. If the current changes polarity during the dead-time, the pole voltages change polarities. Consequently, the polarity of the inverter output voltage changes and the VPR occurs. The term "notch," which is depicted in Fig. 4(a), will be used to refer the VPR in this article according to the author's judgment. *Mode 1:* From t_0 to t_1- No switch is ON. The current (marked in red) is positive and flows through the antiparallel diodes D_2 and D_3. The pole voltage, v_{ao} is negative and v_{bo} is positive. Therefore, the output voltage across the load is $-V_{IN}$.

Mode 2: From t_1 to t_2- Switch SW_1 and SW_4 are ON and SW_2 and SW_3 are OFF. The current is positive and flows through SW_1 and SW_4. The pole voltage v_{ao} is positive and v_{bo} is negative. Therefore, the output voltage across the load is $+V_{IN}$.

Mode 3: From t_2 to t_3- No switch is ON. The current is positive and flows through antiparallel diodes D_2 and D_3. The pole voltage v_{ao} is negative and v_{bo} is positive. Hence, the output voltage across the load is $-V_{IN}$.

Mode 4: From t_3 to t_4 - No switch is ON, and the current changes polarity from positive to negative at t_3; therefore, the current flows through the antiparallel diodes D_1 and D_4. The pole voltage v_{ao} is positive and v_{bo} is negative, which results in the output voltage across the load to be $+V_{IN}$ during this time interval.

Mode 5: From t_4 to t_5 - Switch SW_2 and SW_3 are ON and SW_1 and SW_4 are OFF. The current is negative and flows through SW_2 and SW_3. The pole voltage v_{ao} is negative and v_{bo} is positive, which results in the output voltage across the load to be $-V_{IN}$.

Mode 6: From t_5 to t_6 - No switch is ON, and the current is negative and goes through the antiparallel diodes D_1 and D_4. The pole voltage v_{ao} becomes positive while v_{bo} turns negative. Subsequently, the output voltage across the load becomes $+V_{IN}$.

2) Case 2: When $0 < \phi < \frac{\psi_{t_d}}{2}$ and $\alpha = 0$, the corresponding switching characteristics and operational modes are illustrated in Fig. 5, and ψ_{t_d} is the dead-time angle defined in (2).

Mode 1: From t_0 to t_1 – No switch is ON, and the current is negative. Therefore, it flows through the antiparallel diodes D_1 and D_4. The pole voltage v_{ao} becomes positive while v_{bo} turns negative. Subsequently, the output voltage across the load is $+V_{IN}$.

Mode 2: From t_1 to t_2- All the switches are OFF. The mode of operation is the same as *Mode 1* in *Case 1*. The current is positive and forces the conduction of body-diodes D_2 and D_3. Consequently, the output voltage across the load is $-V_{IN}$. *Mode 3* (from t_2 to t_3), *Mode 4* (from t_3 to t_4), *Mode 5* (from t_4 to t_5), and *Mode 6* (from t_5 to t_6) are similar to the *Mode 2, Mode 3, Mode 4,* and *Mode 5* in *Case 1*, respectively. It must be noted that for the specified condition of ϕ, and α, the notch occurs at the inverter output during the dead-time interval.

3) Case 3: When $\phi = \frac{\psi_{t_d}}{2}$ and $\alpha = 0$, the corresponding switching characteristics and operational modes are depicted in Fig. 6.

Mode 1 (from t_0 to t_1) is similar to that in *Case 2*. At time instance t_1, the current changes its polarity and SW_1 and SW_4 turns ON. The change in the current direction occurs at the end of the dead-time; therefore, it does not affect the polarity of the inverter output voltage. *Mode 2* (from t_1 to t_2) and *Mode 3* (from t_2 to t_3) are the same as *Mode 2* and *Mode 3* in *Case 1*, respectively. At instance t_3, the current changes direction from positive to negative and the SW_2 and SW_3 turn ON.

Mode 4 (from t_3 to t_4) and *Mode 5* (from t_4 to t_5) are similar to *Mode 5* and *Mode 6* of *Case 1*, respectively. As seen in Fig. 6(a), no notch appears at the inverter output during the dead-time interval.

4) Case 4: When $\phi = 0$, and $\alpha = \frac{\psi_{t_d}}{2}$, the relevant operational waveforms and modes are illustrated in Fig. 7.

Mode 1 (from t_0 to t_1)/ *Mode 7* (from t_6 to t_7), *Mode 2* (from t_1 to t_2)/*Mode 6* (from t_5 to t_6), *Mode 4* (from t_3 to t_4), and *Mode 9* (from t_8 to t_9) are similar to *Mode 1, Mode 2, Mode 3,* and *Mode 6* of *Case 2*, respectively. *Mode 3:* From t_2 to t_3- Switch SW_1 is ON, and the current is positive. Consequently, the body-diode, D_3 conducts. Both the pole voltages (v_{ao} and v_{bo}) are positive, resulting in the zero-voltage level at the inverter output.

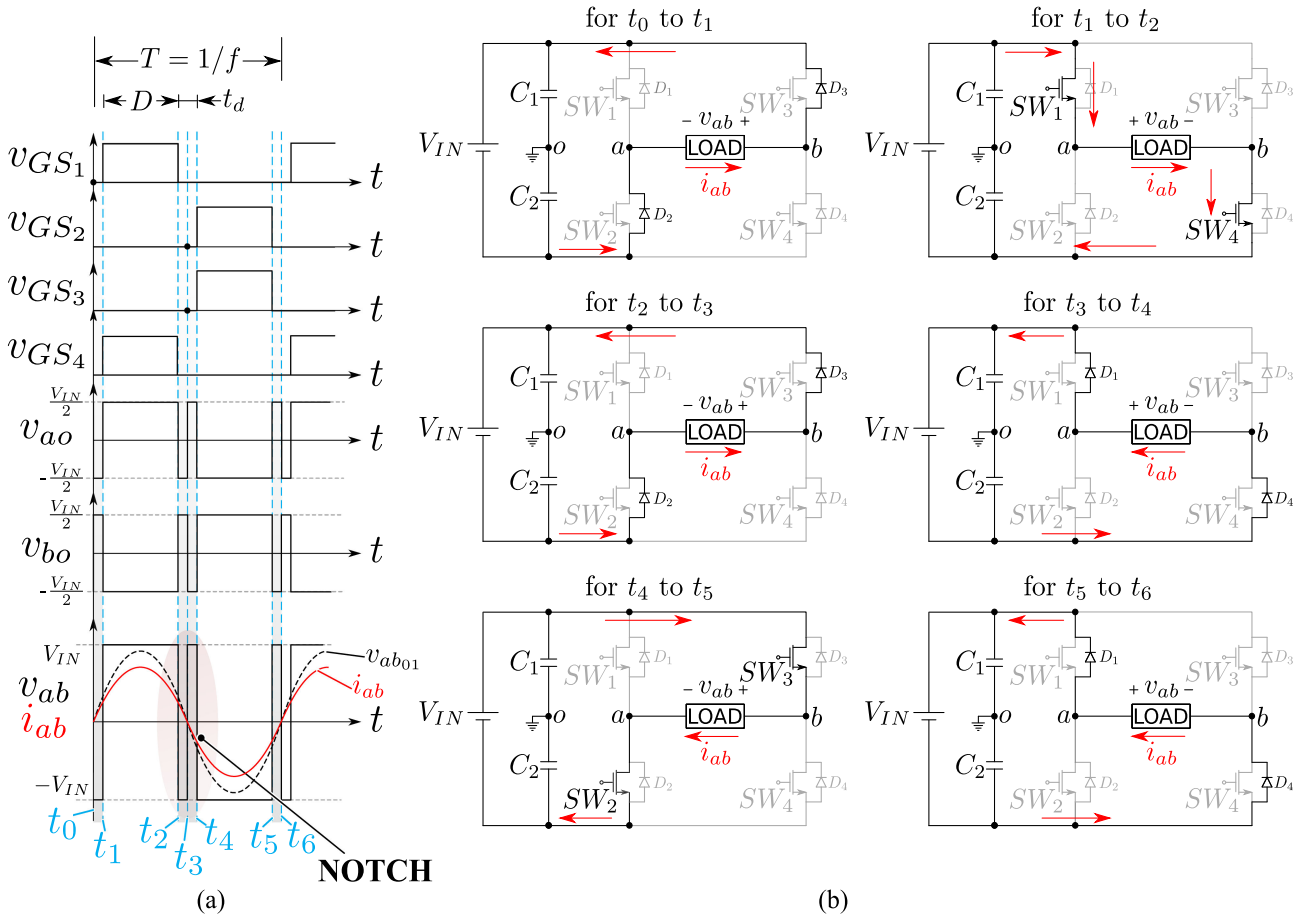

Fig. 4. *Case 1*, $\phi = 0$, $\alpha = 0$: (a) Operational waveforms of WPT system considering the dead-time, and (b) operational modes of WPT system with dead-time.

Mode 5: From t_4 to t_5- Switch SW_4 is ON, and the flow of current through the load is positive. The body-diode, D_2 turns ON, and both the pole voltages are negative, resulting in zero level at the inverter output.

Mode 8: From t_7 to t_8- Switch SW_2 is ON, and the flow of the current is negative. Therefore, the difference between the pole voltages is zero, resulting in the zero-level at the inverter output.

Mode 10: From t_9 to t_{10}- Switch SW_3 is ON, and the current flow is in a negative direction which conducts body-diode D_1 of switch SW_1. Consequently, both the pole voltages are positive and the output of the inverter is clamped to zero. It must be noted that the notch appears for the defined conditions of phase angle and phase-shift angle as shown in Fig. 7(a).

5) Case 5: When $\phi = 0$, and $\alpha = \psi_{t_d}$ the switching characteristics and the operational modes are illustrated in Fig. 8.

Mode 1 (from t_0 to t_1) and *Mode 7* (from t_6 to t_7): Switch SW_3 is ON, and the flow of current is in a negative direction, which forces the body-diode, D_1 of switch SW_1 to turn-ON. Since both the pole voltages are positive, the resultant voltage across the load is zero.

Mode 2: From t_1 to t_2- Switch SW_1 is ON, and the flow of current is in a positive direction. The body-diode, D_3 of switch SW_3 turns-ON and allows the flow of current in a positive direction. Both the pole voltages are positive similar to that of *Mode 1* and result in the zero voltage across the inverter output.

Mode 3, Mode 4, Mode 5, and *Mode 6* are similar to that of *Mode 4, Mode 5, Mode 8,* and *Mode 9* of *Case 4* and are intuitive from Fig. 8, where the notch does not appear in the inverter voltage during this operating mode.

6) Case 6: The switching characteristics and operational modes when $\phi > 0$, and $\alpha > 0$ such that $\theta_v - \phi < \frac{\psi_{t_d}}{2}$ are depicted in Fig. 9, where the notch appears at the inverter output for the given operating conditions. Following are the modes of operation:

Mode 1 (from t_0 to t_1), *Mode 4* (from t_3 to t_4), *Mode 5* (from t_4 to t_5), and *Mode 9* (from t_8 to t_9) are similar to *Mode 1, Mode 2, Mode 3,* and *Mode 5* of *Case 5*, respectively. Moreover, *Mode 10* (from t_9 to t_{10}) is similar to *Mode 6* of *Case 5* and has been excluded from Fig. 9(b) for brevity.

Mode 2: From t_1 to t_2 - Switch SW_1 and Switch SW_3 are ON, and the flow of current is in the negative direction. Since two of the switches are ON, the current can maintain its direction without forcing the conduction of body-diodes. Since both the pole voltages are positive, the voltage at the inverter output is zero.

Mode 3: From t_2 to t_3 - Switch SW_1 is ON, and the direction of the current is negative. Due to the negative direction of the

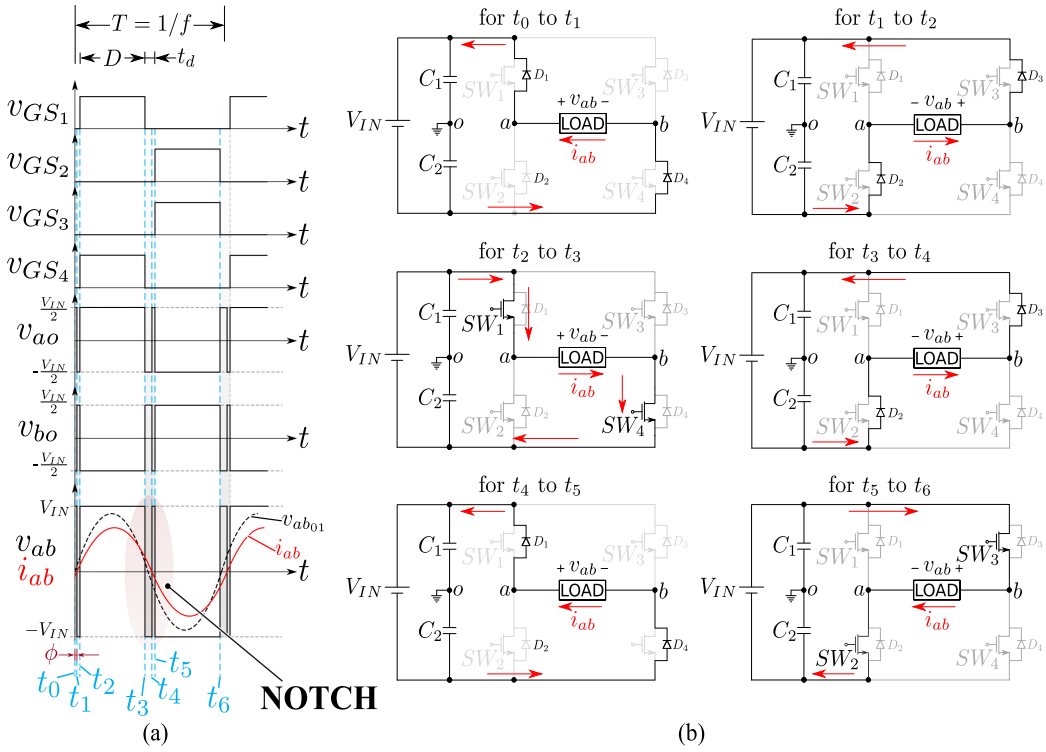

Fig. 5. *Case 2*, $\phi = \frac{\psi t_d}{4}$, $\alpha = 0$: (a) Operational waveforms of WPT system considering the dead-time, and (b) operational modes of WPT system with dead-time.

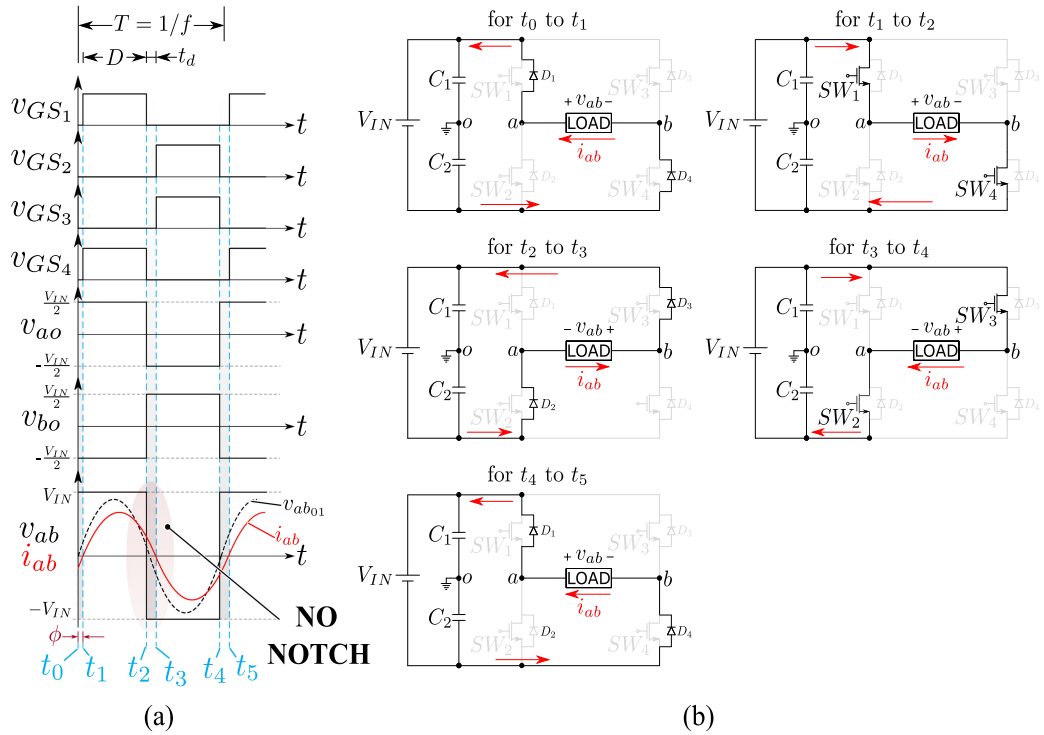

Fig. 6. *Case 3*, $\phi = \frac{\psi t_d}{2}$, $\alpha = 0$: (a) Operational waveforms of WPT system considering the dead-time, and (b) operational modes of WPT system with dead-time.

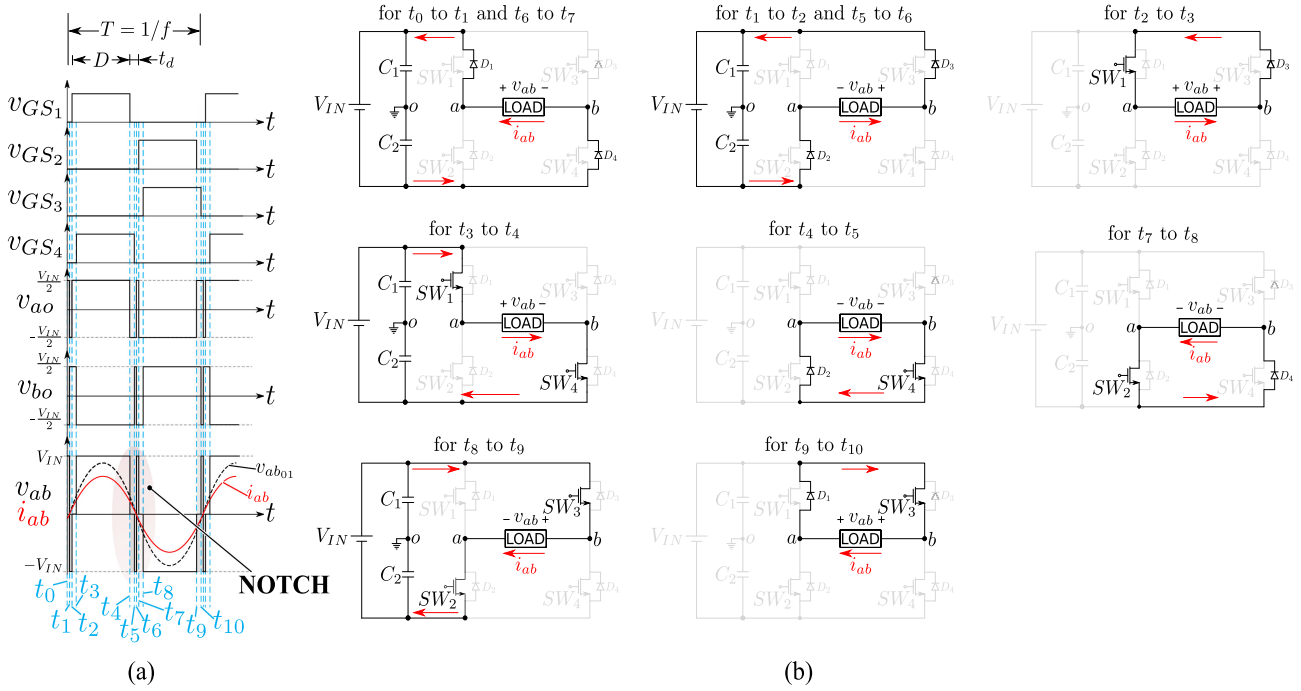

Fig. 7. *Case 4*, $\phi = 0, \alpha = \frac{\psi_{t_d}}{2}$: (a) Operational waveforms of WPT system considering the dead-time, and (b) operational modes of WPT system with dead-time.

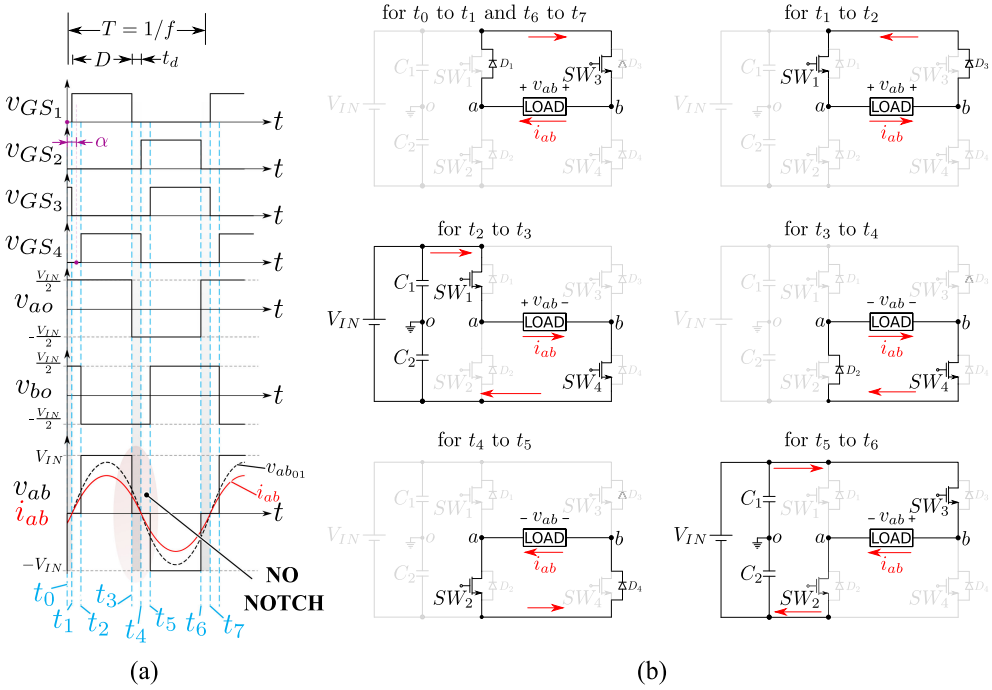

Fig. 8. *Case 5*, $\phi = 0, \alpha = \psi_{t_d}$: (a) Operational waveforms of WPT system considering the dead-time, and (b) operational modes of WPT system with dead-time.

current, the body-diode, D_4 of switch SW_4 conducts. The pole voltages, v_{ao} is positive and v_{bo} is negative. Subsequently, the output voltage across the inverter is $+V_{IN}$.

Mode 6: From t_5 to t_6 - Switch SW_4 is ON, and the direction of the current is positive, which forces the conduction of body-diode, D_2. The pole voltages, v_{ao} and v_{bo} are negative. Therefore, the output voltage across the inverter is clamped to zero.

Mode 7: From t_6 to t_7 - Switches SW_2 and SW_4 is ON, and the direction of the current is positive, which results in zero voltage level at the inverter output. *Mode 8:* From t_7 to t_8 - Switch SW_2 is ON, and the direction of the current is positive. Due to the positive direction of the current, the body-diode, D_3 conducts. The pole voltages, v_{ao} is negative and v_{bo} is positive. Subsequently, the output voltage across the inverter is $-V_{IN}$.

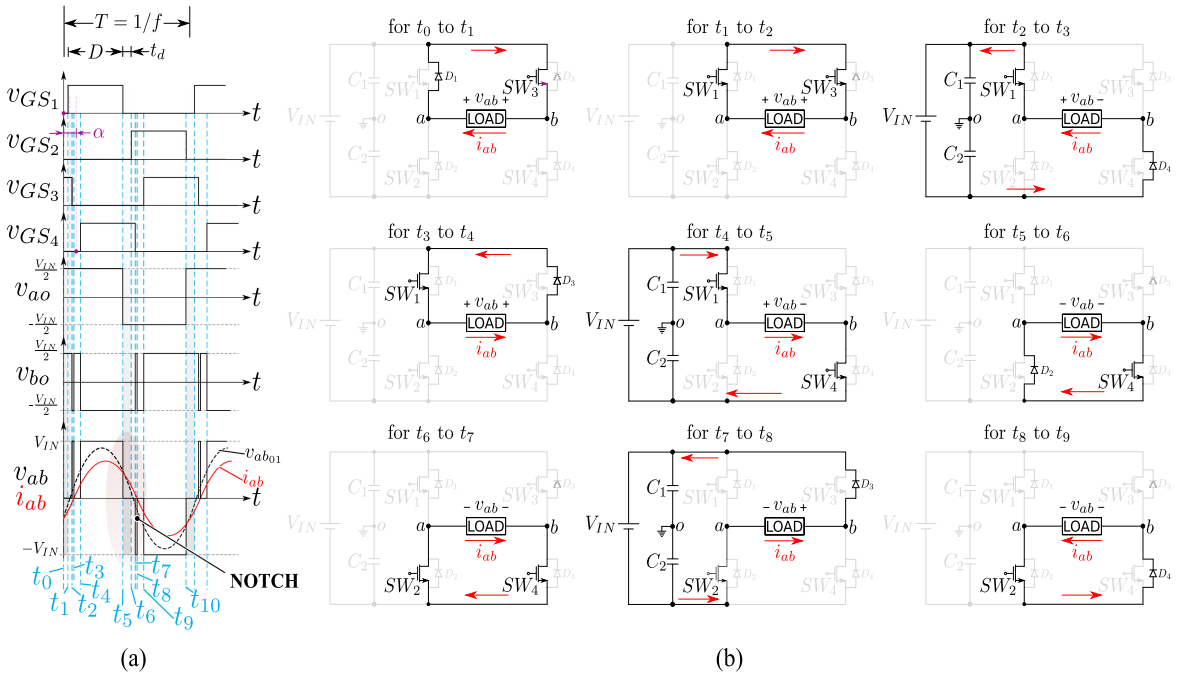

Fig. 9. *Case 6*, $\theta_v - \phi < \frac{\psi_{t_d}}{2}$: (a) Operational waveforms of WPT system considering the dead-time, and (b) operational modes of WPT system with dead-time.

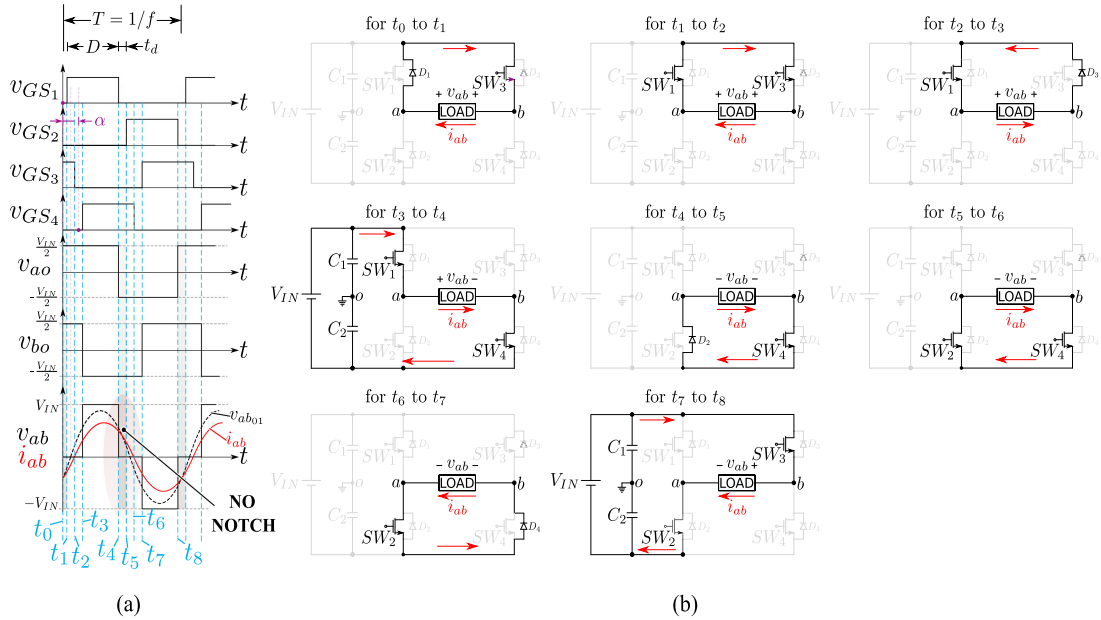

Fig. 10. *Case 7*, $\theta_v - \phi > \frac{\psi_{t_d}}{2}$: (a) Operational waveforms of WPT system considering the dead-time, and (b) operational modes of WPT system with dead-time.

7) Case 7: Fig. 10 shows the switching characteristics when $\phi > 0$, and $\alpha > 0$ such that $\theta_v - \phi > \frac{\psi_{t_d}}{2}$. As can be seen from Fig. 10(a), the notch does not appear at the inverter output because the current direction does not change during the dead-time interval. *Mode 1* (from t_0 to t_1), *Mode 2* (from t_1 to t_2), *Mode 3* (from t_2 to t_3), *Mode 4* (from t_3 to t_4), *Mode 5* (from t_4 to t_5), *Mode 6* (from t_5 to t_6), and *Mode 7* (from t_6 to t_7), are similar to *Mode 1, Mode 2, Mode 3, Mode 5, Mode 6, Mode 7,* and *Mode 9* of *Case 6*, respectively.

Mode 8: From t_7 to t_8- Switches SW_2, and SW_3 are ON, and the direction of the current is negative. Consequently, the pole voltages v_{ao} is negative and v_{bo} is positive and results in $-V_{IN}$ at the inverter output.

Table I summarizes the appearance of the notches at the inverter output for the various operating conditions mentioned above. The dead-time analysis in this article is conducted for an inductive load (or lagging power factor). However, due to the half-wave symmetry of the traditional phase-shift control, the

TABLE I
SUMMARY OF NOTCH OCCURRENCE FOR DIFFERENT CONDITIONS OF PHASE-SHIFT ANGLE AND PHASE ANGLE

Phase Angle, ϕ=? Phase-Shift, α=?	Is NOTCH Present?	Case No.	Figure No.
ϕ=0, α=0	YES	*Case 1*	Fig. 4
$\phi=\frac{\psi_{t_d}}{4}$ (inductive), α=0	YES	*Case 2*	Fig. 5
$\phi=\frac{\psi_{t_d}}{2}$ (inductive), α=0	NO	*Case 3*	Fig. 6
$\phi>\frac{\psi_{t_d}}{2}$ (inductive), α=0	NO	-	-
ϕ=0, $\alpha=\frac{\psi_{t_d}}{2}$	YES	*Case 4*	Fig. 7
ϕ=0, $\alpha=\psi_{t_d}$	NO	*Case 5*	Fig. 8
ϕ=0, $\alpha>\psi_{t_d}$	NO	-	-
$\phi>0$, $\alpha>\psi_{t_d}$: $\theta_v-\phi<\frac{\psi_{t_d}}{2}$	YES	*Case 6*	Fig. 9
$\phi>0$, $\alpha>\psi_{t_d}$: $\theta_v-\phi>\frac{\psi_{t_d}}{2}$	NO	*Case 7*	Fig. 10

conditions for the occurrence of notches with a capacitive load (or leading power-factor) will be similar to that of an inductive load. It can be implied from Table I that the notches in the inverter can be avoided if the following notch equation defined in (1) is satisfied during the operation of the WPT system:

$$|\theta_v - \phi| \geq \frac{\psi_{t_d}}{2} \tag{1}$$

where θ_v is the angle between the square wave voltage and its fundamental component such that $\theta_v = \frac{\alpha}{2}$ for the traditional phase-shift control [38], and $\theta_v \in \mathbb{R}^+$, $\phi \in \mathbb{R}^+$. ψ_{t_d} is the dead-time angle given by

$$\psi_{t_d} = 2\pi \times f \times t_d \tag{2}$$

where t_d is the dead-time in seconds and f is the switching frequency in Hz.

From the analysis mentioned above, it is evident that the notches in the WPT system results due to the changes in the flow of the current direction during the dead-time interval. The changes in the current direction force the conduction of the MOSFET body-diodes and consequently results in the undesired switching instances in the inverter output. These unwanted switching instances affect the volt–seconds integral of the inverter output, which in turn affects the fundamental component and the harmonic spectrum of the square-wave voltage.

III. EFFECT OF DEAD-TIME ON THE FUNDAMENTAL COMPONENT AND HARMONICS OF THE INVERTER VOLTAGE

The theoretical analysis of the dead-time in a WPT system was discussed in Section II. In this section, the mathematical expressions for the inverter waveform with the notch are described and the effects of the notch on the fundamental component and harmonics are evaluated. A typical inverter output voltage with a notch is shown in Fig. 11 and its Fourier series representation is expressed as

$$v_{ab} = a_o + \sum_{n=1}^{\infty}[a_n \cos(n\omega t) + b_n \sin(n\omega t)]. \tag{3}$$

Due to the half-wave symmetry and odd symmetry of the waveform, the Fourier coefficients, $a_0 = 0$, $a_n = 0$ (for all

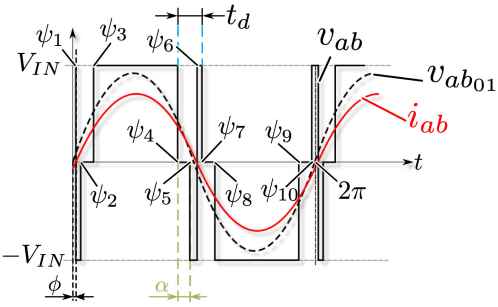

Fig. 11. Typical output of the full-bridge inverter with notch.

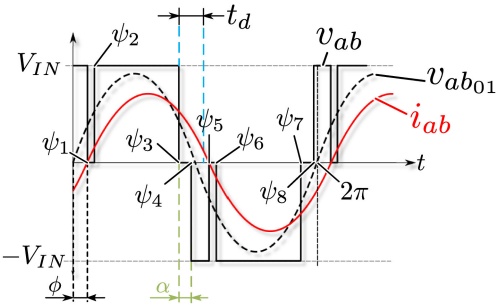

Fig. 12. Typical output of the full-bridge inverter with notch, $\alpha < \phi$.

values of n, where $n \in \mathbb{N}^+$), and b_n is evaluated as follows

$$b_n = \frac{1}{\pi}\int_0^{2\pi} f(x)\ \sin(n\omega t)\ d\omega t \tag{4}$$

where *f(x)* is the periodic function (waveform v_{ab}) represented in Fig. 11. Solving (4) yields

$$\begin{aligned} b_n = \frac{V_{in}}{n\pi}[&-2\cos(n\psi_1) + \cos(n\psi_2) + \cos(n\psi_3) \\ &- \cos(n\psi_4) - \cos(n\psi_5) + 2\cos(n\psi_6) \\ &- \cos(n\psi_7) - \cos(n\psi_8) + \cos(n\psi_9) + \cos(n\psi_{10})]. \end{aligned} \tag{5}$$

The angle $\psi_{i's}$ are defined according to the operating conditions of phase-angle, ϕ, phase-shift, α, and the dead-time angle, ψ_{t_d}. Consequently, the rms value of the nth harmonic of the waveform depicted in Fig. 11 is given as

$$\begin{aligned} v_{ab_n} = \frac{b_n}{\sqrt{2}} = \frac{V_{in}}{\sqrt{2}n\pi}[&-2\cos(n\psi_1) + \cos(n\psi_2) + \cos(n\psi_3) \\ &- \cos(n\psi_4) - \cos(n\psi_5) + 2\cos(n\psi_6) \\ &- \cos(n\psi_7) - \cos(n\psi_8) + \cos(n\psi_9) + \cos(n\psi_{10})] \end{aligned} \tag{6}$$

$$v_{ab_n} = \frac{V_{in}}{\sqrt{2}n\pi}\ C_{\psi_i}. \tag{7}$$

It can be seen in Fig. 11 that the notch appears twice in the given half-cycle of the square-waveform. If the angle ψ_1 is greater than ψ_2 such that, $\psi_1 - \psi_2 > 0$, the multiple notches in Fig. 11 are replaced by a single notch as depicted in Figs. 12 and 13. After comparing the waveforms in Figs. 12 and 13, it is intuitive that the width of the notch varies according to the operating conditions of ϕ and α. If α is less than ϕ the notch

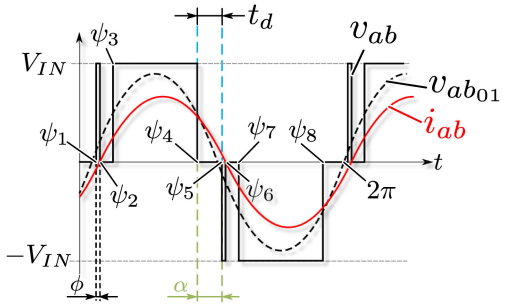

Fig. 13. Typical output of the full-bridge inverter with notch, $\alpha > \phi$.

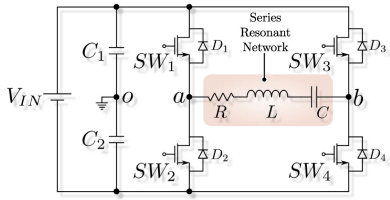

Fig. 14. Equivalent circuit with a series resonant load.

TABLE II
PARAMETERS OF THE SERIES RESONANT CIRCUIT

Parameters	Value
Inductor, L	100 µH
Capacitor, C	25.33 nF
Resistance, R	1 Ω
Resonant frequency, f	100 kHz
Dead-time, t_d	1 µs
DC input voltage, V_{IN}	450 V

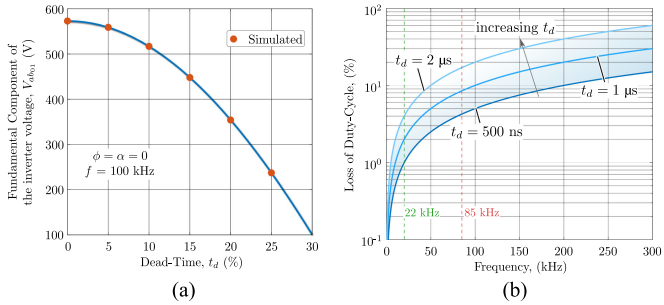

Fig. 15. (a) Inverter fundamental component as a function of dead-time, and (b) Loss of inverter duty-cycle as a function of frequency.

is wide as shown in Fig. 12, and if α is greater than ϕ, the notch is narrow as depicted in Fig. 13. However, the Fourier series representations of both the waveforms are similar and only the value of the angle $\psi_{i's}$ are different. Both the waveforms in Figs. 12 and 13 follow the half-wave symmetry and odd symmetry, consequently the Fourier coefficients, $a_0 = a_n = 0$ (for all n). The Fourier coefficients b_n are given as

$$b_n = \frac{V_{in}}{n\pi}[-\cos(n\psi_1) + \cos(n\psi_2) - \cos(n\psi_3) - \cos(n\psi_4) + \cos(n\psi_5) - \cos(n\psi_6) + \cos(n\psi_7) + \cos(n\psi_8))] \quad (8)$$

Similar to the previous case (with two notches), the angles $\psi_{i's}$ depend on the operating conditions, and the rms value of the nth harmonic of the waveforms depicted in Figs. 12 and 13 is expressed as

$$v_{ab_n} = \frac{b_n}{\sqrt{2}} = \frac{V_{in}}{\sqrt{2}n\pi}[-\cos(n\psi_1) + \cos(n\psi_2) - \cos(n\psi_3) - \cos(n\psi_4) + \cos(n\psi_5) - \cos(n\psi_6) + \cos(n\psi_7) + \cos(n\psi_8))] \quad (9)$$

$$v_{ab_n} = \frac{V_{in}}{\sqrt{2}n\pi}\, C_{\psi_i}. \quad (10)$$

To verify the mathematical expressions mentioned above, a series resonant load connected across a full-bridge inverter is considered as shown in Fig. 14, and the parameters for the analysis are listed in Table II. Using (6)–(10), and the parameters of the series resonant circuit, the effect of dead-time on the fundamental component of the inverter voltage is depicted in Fig. 15(a), where the increase in the dead-time reduces the fundamental component of the inverter voltage. Furthermore, the effect of dead-time on the fundamental component increases with the increase in the operating frequency. Fig. 15(b) depicts the loss of inverter duty-cycle as a function of frequency for different dead-times, where the dead-time of 1 μs results in the loss of $\sim 2.3\%$ of inverter duty-cycle at 22 kHz. However, with the same value of the dead-time, 85 kHz operating frequency results in $\sim 8\%$ loss of the inverter duty-cycle. The increase in the operating frequency further reduces the fundamental component of the inverter and therefore, the dead-time effect at the higher operating frequencies becomes prominent. Notably, the 1 μs dead-time selection is based on the manufacturer's suggestion of having at least 600 ns dead-time with a safety margin addition.

Fig. 16 shows theoretical and simulated results for the effect of dead-time on the fundamental component and its harmonics for variations in the phase-shift angle. Fig. 16(a) and (c) shows that the theoretical predictions are in good agreement with the simulated results. The comparison of the harmonics in the inverter output voltage with and without notches at full inverter duty-cycle and unity power factor are shown in Fig. 16(b). The harmonic spectrum shows that the notch in the inverter output reduces the lower-order harmonics and increases the higher-order harmonics for the specified operating condition. Furthermore, comparing Fig. 16(b) and (d), it can be seen that the harmonic content in the inverter can be controlled by varying the phase-angle and duty-cycle of the inverter. Ideally, the resonant network allows only the fundamental component of the inverter voltage to couple with the secondary [39], and consequently, the higher order harmonics are suppressed by the resonant network. However, the increase in the harmonic content of the inverter square-wave may increase the switching losses and thermal stresses across the MOSFET switches. If the voltage/current stresses due to the notch exceeds the maximum tolerable limits, the MOSFET switch may get damaged permanently. In addition, the increase in the switching losses will also affect the efficiency of the overall system. The loss of fundamental

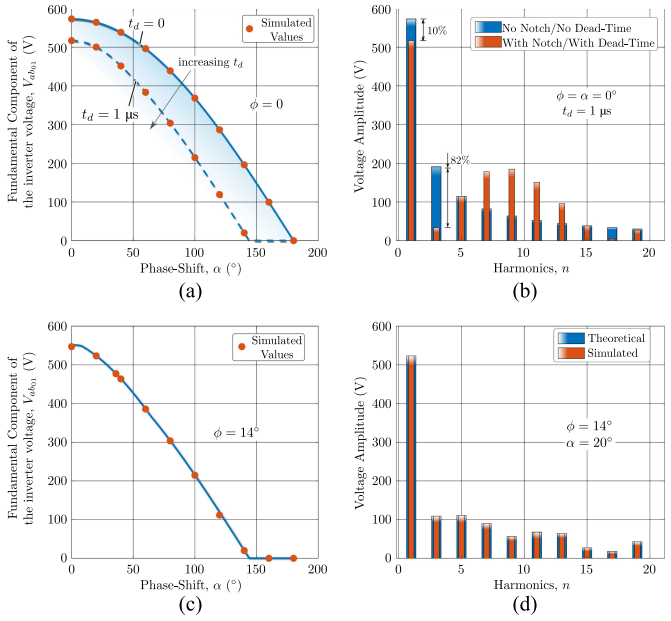

Fig. 16. (a) Inverter fundamental component as a function of phase-shift angle $\phi = 0°$, (b) comparison of harmonic spectrum with and without the notch, (c) inverter fundamental component as a function of phase-shift angle $\phi = 14°$, and (d) comparison of the harmonic spectrum between theoretical values and simulated results.

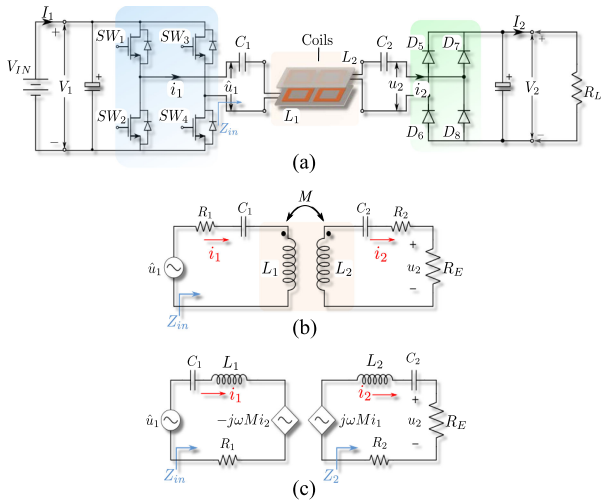

Fig. 17. (a) Circuit schematic of the WPT system, (b) FHA of WPT system, and (c) mutually coupled circuit model of WPT system.

component impacts the WPT system characteristics, too, and will be studied in Section IV.

IV. Sensitivity Analysis Due to the Dead-Time Effect

Fig. 17(a) shows the circuit schematic of a WPT system, where V_1, I_1 are the dc input voltage and current at the primary-side, V_2, I_2 are the dc output voltage and current at the secondary-side across the load, L_1 and L_2 are the primary and secondary-side self-inductances of the transmitter and receiver coils, respectively, C_1 and C_2 are the primary and secondary-side series compensation capacitors, and R_L is the dc load assumed to be purely resistive. M is the mutual inductance between the transmitter and receiver coil and is expressed as $M = k\sqrt{L_1 L_2}$, where k is the coupling-coefficient between the coils.

The resonant frequency of the WPT system is considered to be identical on both primary and secondary-sides and is given by

$$\omega = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}. \tag{11}$$

The mutually coupled model with the first harmonic approximation (FHA) is considered for the dead-time analysis, as shown in Fig. 17(b) and (c). The rms value of the primary-side ac voltage, $\hat{u}_1$ can be calculated as

$$\hat{u}_1 = \frac{V_1}{\sqrt{2}n\pi} C_{\psi_i} \tag{12}$$

where C_{ψ_i} is defined in Section III and depends on the operating condition of α, and ϕ. The ac voltage and current at the input of the secondary rectifier is given as follows:

$$u_2 = \frac{2\sqrt{2}}{\pi} V_2 \tag{13}$$

$$i_2 = \frac{\pi}{2\sqrt{2}} I_2. \tag{14}$$

The equivalent load resistance at the input of the diode rectifier is written as[40]

$$R_E = \frac{8}{\pi^2} R_L. \tag{15}$$

The primary-side impedance of the WPT is given as

$$Z_1 = R_1 + j\omega L_1 + \frac{1}{j\omega C_1}. \tag{16}$$

The secondary-side impedance of the WPT is expressed as

$$Z_2 = R_2 + j\omega L_2 + \frac{1}{j\omega C_2}. \tag{17}$$

The reflected impedance at the input is given as [41]

$$Z_{in} = Z_1 + \frac{\omega^2 M^2}{Z_2 + R_E}. \tag{18}$$

Equation (18) can be further simplified into real and imaginary components as

$$Z_{in} = R_1 + \frac{\omega^2 M^2 (R_2 + R_E)}{(R_2 + R_E)^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)} + j\left[\frac{\left(\omega L_1 - \frac{1}{\omega C_1}\right) - \omega^2 M^2 \left(\omega L_2 - \frac{1}{\omega C_2}\right)}{(R_2 + R_E)^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)}\right]. \tag{19}$$

The primary track current can be calculated using (12) and (18) as

$$i_1 = \frac{\hat{u}_1}{Z_{in}} = \frac{\hat{u}_1 (Z_2 + R_E)}{[Z_1 (Z_2 + R_E) + (\omega M)^2]}. \tag{20}$$

The ac transconductance gain of the system is defined as the ratio of the secondary current to the primary inverter voltage

TABLE III
WPT SYSTEM PARAMETERS

Parameters	Value
Primary-side self-inductance, L_1	74.56 μH
Secondary-side self-inductance, L_2	85.52 μH
Primary-side compensation capacitor, C_1	47.76 nF
Secondary-side compensation capacitor, C_2	40.8 nF
Resonant frequency, f	85 kHz
Coupling coefficient, k	0.15
DC load resistance, R_L	13 Ω
DC input voltage, V_1	210 V
Dead-time, t_d	1 μs
Primary-coil dimension	711×711×20 (mm)
Secondary-coil dimension	381×482×25.4 (mm)
Air-gap, d	150 mm

and can be calculated from (12)–(19) as

$$G_{iv_{AC}} = \frac{i_2}{\hat{u}_1} = \frac{\omega M}{[Z_1(Z_2 + R_E) + (\omega M)^2]}. \quad (21)$$

By substituting (12), and (14) in (21), the dc transconductance gain of the system is obtained as

$$G_{iv_{\text{DC}}} = \frac{I_2}{V_1} = \frac{2C_{\psi_i}\omega M}{\pi^2[Z_1(Z_2 + R_E) + (\omega M)^2]}. \quad (22)$$

The ac voltage gain of the system is defined as the ratio of the voltage across the equivalent load to the inverter voltage and is given as

$$G_{v_{\text{AC}}} = \frac{u_2}{\hat{u}_1} = \frac{\omega M R_E}{[Z_1(Z_2 + R_E) + (\omega M)^2]} \quad (23)$$

Similarly, the dc voltage gain is calculated from (12), (13), and (23) as

$$G_{v_{\text{DC}}} = \frac{V_2}{V_1} = \frac{C_{\psi_i}\omega M R_E}{4[Z_1(Z_2 + R_E) + (\omega M)^2]} \quad (24)$$

The dc output power across the load is obtained as

$$P_{\text{OUT}_{\text{DC}}} = I_2^2 R_L = \frac{(2C_{\psi_i}V_1\omega M)^2 R_L}{\{\pi^2[Z_1(Z_2 + R_E) + (\omega M)^2]\}^2}. \quad (25)$$

From (21)–(25), it is apparent that the transconductance gain, voltage gain, and the output power are functions of operating frequency, load resistance, mutual inductance, and the inverter voltage. Assuming that the operating frequency, load resistance, and the mutual inductance are constant, the effect of the dead-time on the WPT system can be easily analyzed. Using the parameters in Table III and (21)–(25), the effect of the dead-time on the sensitivity of the system is analyzed by considering the full duty-cycle (zero phase-shift) of the inverter at unity power factor and is depicted in Fig. 18. It is important to mention that, for a 22 kHz system, the load impedance is adjusted such that the output power at $t_d = 0$ is same as that of a 85 kHz WPT system. Comparison of Fig. 18(a) with (b), and (c) with (d) shows that the loss of the inverter duty-cycle due to the dead-time affects the dc voltage gain and the dc transconductance gain of the system. However, the ac voltage gain and transconductance gains are not affected due to the dead-time effect. The secondary current and voltage of the SS-WPT system depend on the primary inverter voltage. Consequently, the variations in the inverter voltage directly affect the secondary current and secondary voltage. Subsequently, the output power delivered to the load is also affected if the notches persistently occur in the inverter waveform, and are depicted in Fig. 18(e) and (f).

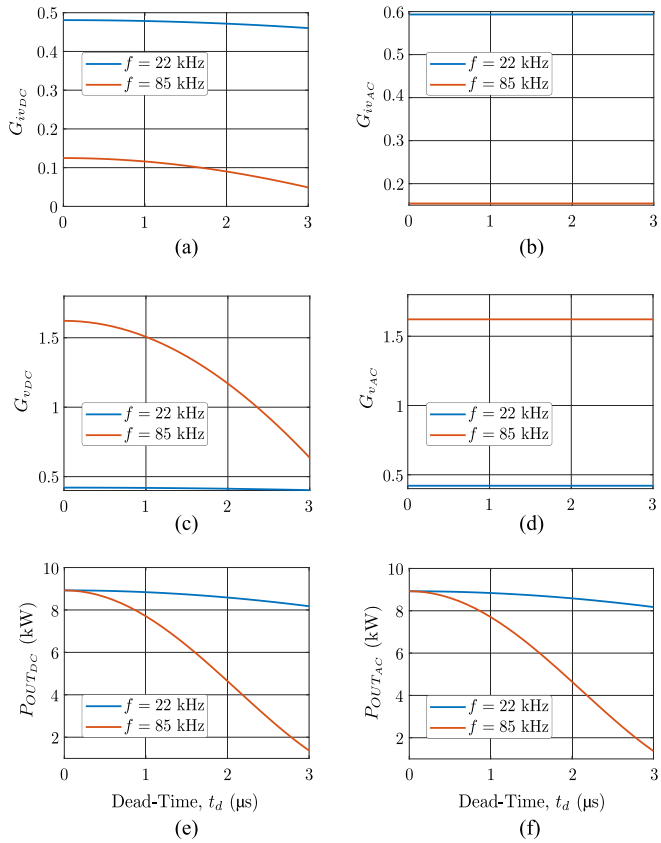

Fig. 18. Sensitivity analysis of WPT system: (a) dc transconductance gain, (b) ac transconductance gain, (c) dc voltage gain, (d) ac voltage gain, (e) dc output power, and (f) ac output power.

V. EXPERIMENTAL RESULTS

In this section, the notch equation from Section II, the analytical expressions from Section III, and the sensitivity analysis presented in Section IV are verified on a WPT system. Moreover, it is ensured that the analytical curves from the previous sections are reiterated by considering the experimental parameters (listed in Table III) to provide a fair comparison between the theoretical and experimental results.

Fig. 19(a) shows the experimental setup of the series–series compensated WPT system prototype which is similar to the one in reference [42]. The inverter configuration of the WPT system is shown in Fig. 19(b) and consists of CAS325M12HM2 SiC 1200V/325A half-bridge MOSFET modules from CREE/Wolfspeed. The MOSFET modules are arranged in full-bridge configuration with CGD15HB62LP gate-drivers from CREE. The minimum dead-time of 1μs is selected for the safe operation of the MOSFET inverter. A TMS320F28335 DSP control card from Texas Instruments is used to provide gate-pulses to the full-bridge inverter. The transmitter and receiver coils are fabricated and comprise of 6 AWG bifilar Litz

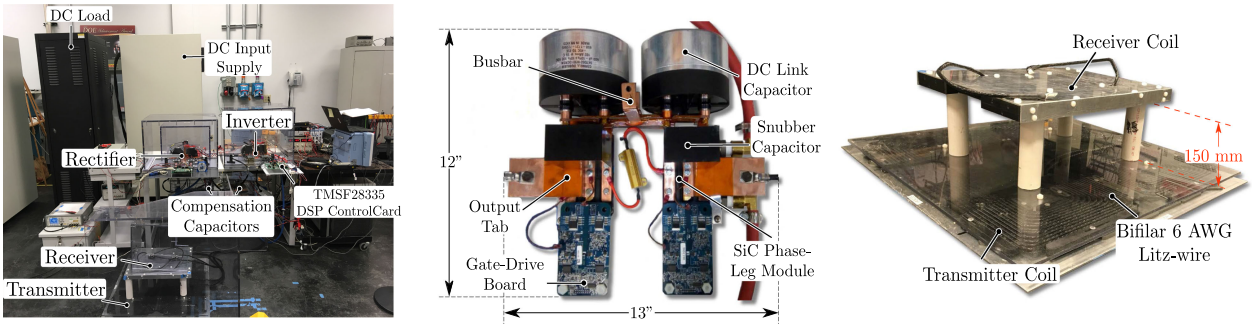

Fig. 19. (a) Experimental setup, (b) inverter configuration, and (c) transmitter and receiver coil pair.

wire, as shown in Fig. 19(c). The air-gap between the coil pairs is maintained constant at 150 mm, and the dimensions of the coils are listed in Table III. The primary-side and secondary-side compensation capacitors were assembled with a series–parallel combination of CSP 120/200 conduction cooled capacitors from *Celem Power Capacitors*. The secondary rectifier utilizes 600V/100A APT2X101DQ60 J ultrafast phase-leg rectifier modules. Fig. 20 shows the experimental waveform of the WPT system prototype with two different values of the dead time between the complementary switching instances of the inverter phase-leg. $\hat{u}_1$ and i_1 are the voltage and current of the primary inverter, respectively, u_2 and i_2 are the voltage and current at the input of the diode rectifier, respectively, v_{C_1} and v_{C_2} are the voltages across the primary and secondary compensation capacitors, respectively, and V_1, V_2 are the dc input and output voltages of the WPT system, respectively. Due to the parasitic components of the system, the resonant frequency of the experimental prototype is found to be 81.6 kHz with the parameters listed in Table III. The input phase-angle, ϕ is maintained at $\sim 0^\circ$ and the inverter is operated at full duty-cycle ($\alpha = 0$) for the experimental waveforms in Fig. 20. Consequently, (1) is not satisfied and the notch occurs in the inverter voltage. Furthermore, the current at the rectifier input decreases from ~ 26 to ~ 19 A due to the increase in the value of dead-time and can also be noticed from the experimental waveforms. This change in the current value attributes the dead-time effect in the WPT system.

Fig. 21 shows the waveforms of the inverter voltage and current at different operating conditions of the phase angle and inverter duty-cycle. The dead-time is maintained constant at $1; \mu s$, and the input phase angle at the inverter is varied by tuning the switching frequency in the open-loop configuration. As shown in Fig. 21, the notches occur at the inverter output if the notch equation is not satisfied.

Fig. 21(a) shows the waveforms for full inverter duty-cycle and a phase-angle, ϕ of approximately $\sim 6.6^\circ$. The dead-time angle for 1 μs dead-time is calculated to be $\sim 15^\circ$. Therefore, according to (1), the difference between the phase angle, ϕ and phase-shift, θ_v is less than $0.5\psi_{t_d}$, and the notches occur in the inverter voltage. Fig. 21(i) shows the waveforms for full inverter duty-cycle with $\phi \sim 26^\circ$.

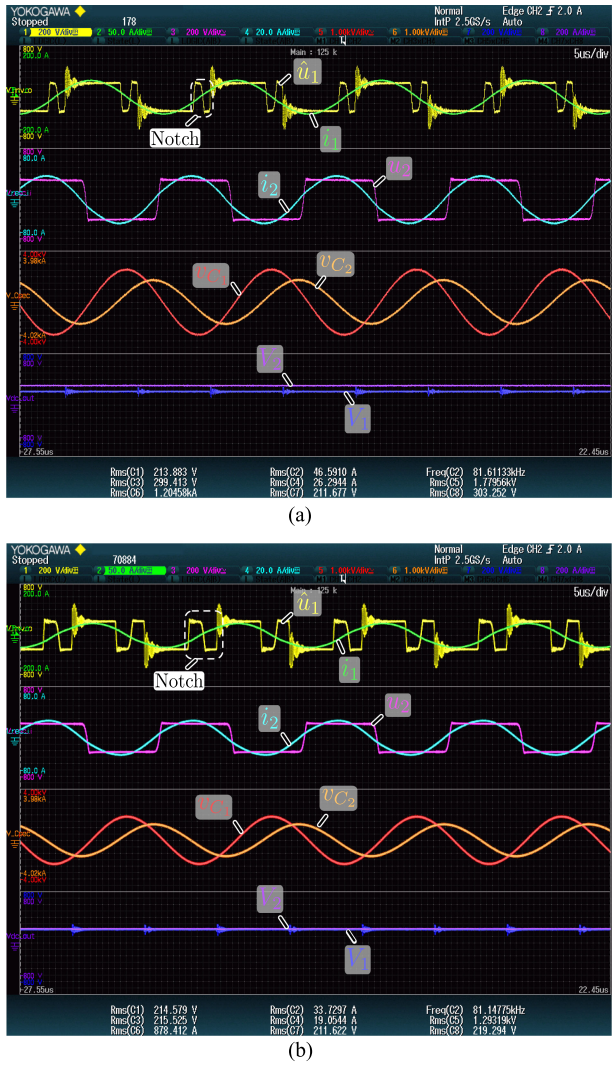

Fig. 20. Experimental result: (a) with $t_d = 1.5\mu$s, and (b) with $t_d = 2.5\mu$s.

The operating condition in Fig. 21(i) satisfies (1) and the notches do not occur in the inverter voltage. As discussed in Section III, the width of the notch and the number of instances for the occurrence depend on the operating conditions of ϕ and α.

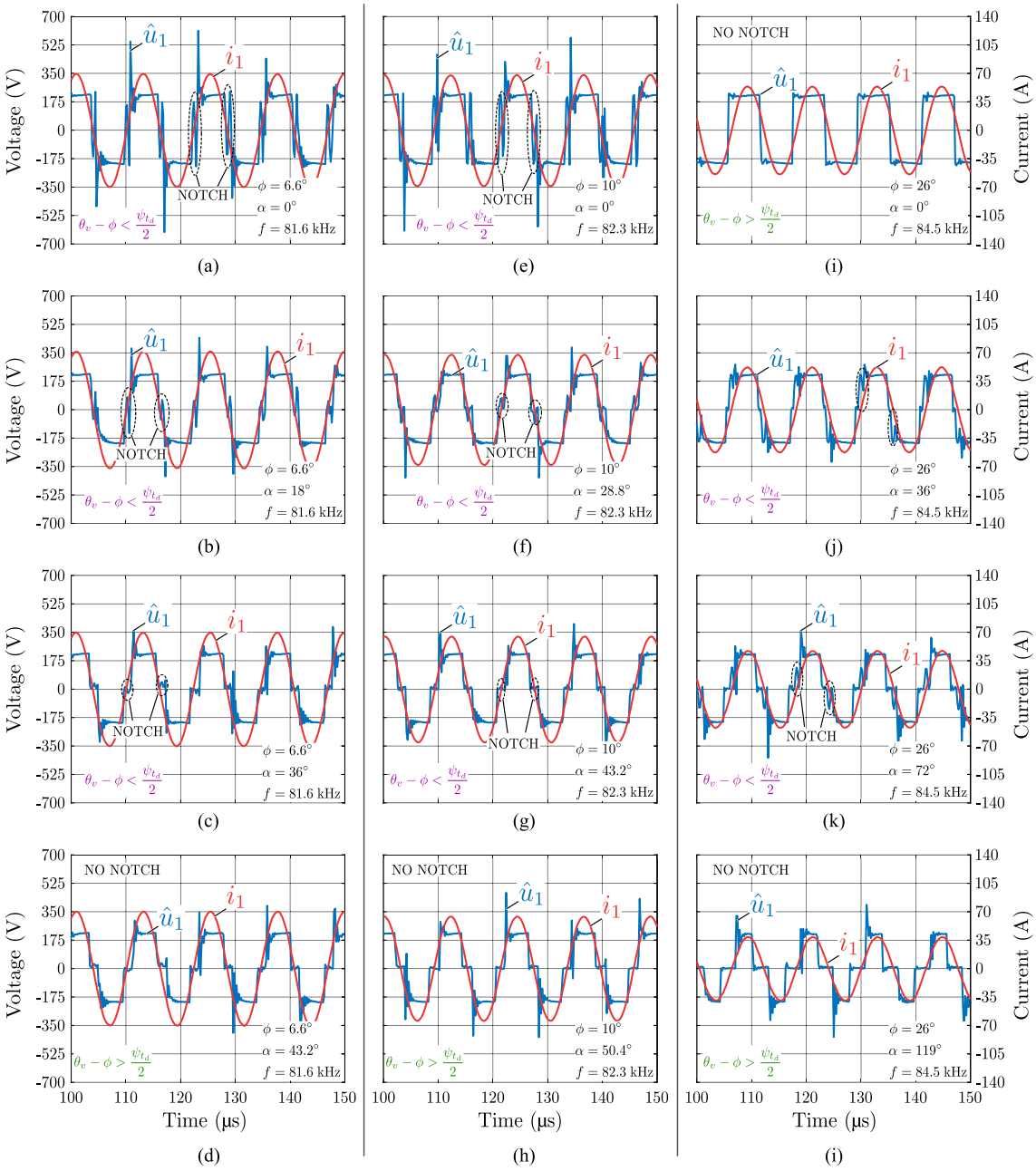

Fig. 21. Experimental result of inverter voltage and current at different conditions.

Furthermore, comparison of the inverter output waveforms in Fig. 21(a) and (e) shows that, the width of the notch varies with the conditions of ϕ and α. Besides, comparing Fig. 21(a), (f), and (k), it can be noticed that, the number of instances for the occurrence of the notch also varies with the conditions of the phase-angle and the inverter duty-cycle. The operating condition in Fig. 21(a) results in two notches in the inverter half-cycle and the operating condition in Fig. 21(f) and (k) results in only one notch in the inverter output half-cycle. The dead-time angle is the function of the operating frequency and therefore increases with the increase in operating frequency. Consequently, the value of phase-angle or phase-shift angle required to overcome the notch also increases.

Fig. 22 shows the comparison of the harmonics between the theoretical and experimental rms values for two different cases. The experimental waveforms of the inverter contain a lot of ringing and were not considered during the mathematical analysis performed in Section III. Therefore, the experimental voltage waveform of the inverter is recorded and filtered using a simple low-pass filter with the stop band frequency of 800 kHz using MATLAB software. Fig. 22(a) shows the comparison of harmonics with the full inverter duty-cycle, and the dead-time of 1 μs with no notch at the inverter output. The experimental values of the harmonic content in the inverter are in close agreement with the theoretical predictions for both the cases depicted in Fig. 22. Due to the distortions (notches) in the inverter voltage,

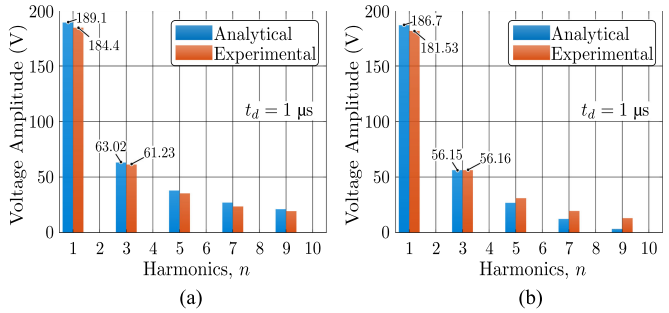

Fig. 22. Comparison of harmonics: (a) $f = 84.5$ kHz, $\phi \sim 26°$, $\alpha = 0°$, and (b) $f = 84.5$ kHz, $\phi \sim 26°$, $\alpha = 18°$.

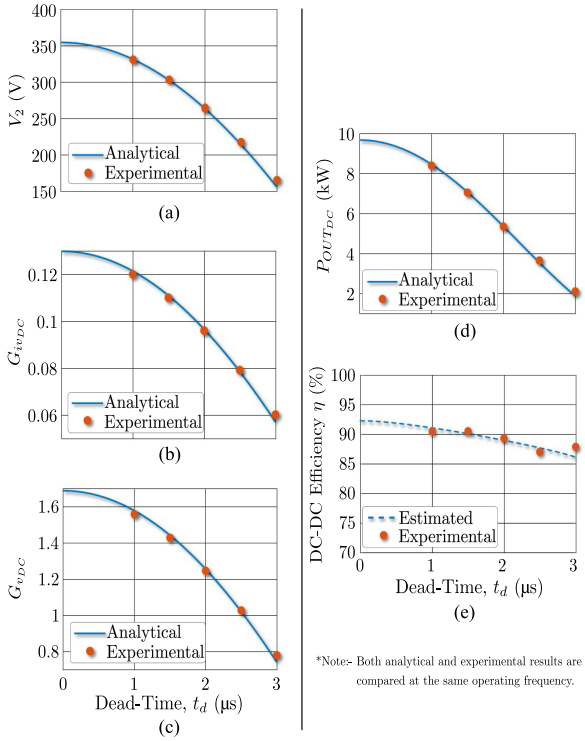

Fig. 23. Experimental result: (a) DC output voltage, (b) DC transconductance gain, (c) DC voltage gain, (d) DC output power, and (e) efficiency.

it is difficult to accurately measure the input phase-angle, ϕ between the inverter voltage and current. Therefore, a small error persists between the theoretical and experimental values of the harmonics. Moreover, the error between the theoretical and experimental values of the fundamental component and the third harmonic of the inverter voltage is within 3%.

Fig. 23 shows the comparison of theoretical and experimental results for different WPT parameters with the full inverter duty-cycle and unity PF ($\alpha = \phi = 0$).

Equation (24) and the parameters in Table III were used to calculate the output dc voltage shown in Fig. 23(a). The dc output voltage without any dead-time effect is predicted to be 360 V. However, with a 1 μs dead-time, the dc output voltage is found to be 327 V resulting in a reduction of approximately $\sim 10\%$ of the output voltage. Furthermore, as the dead-time between the complementary switching pulses increases, the dc output voltage of the system decreases, and the theoretical predictions match the experimental validations. The dc transconductance gain and dc voltage gain of the system decreases with the increase in the dead-time, and the theoretical predictions closely match the experimental results, as shown in Fig. 23(b), and (c).

The comparison of the theoretical and experimental results on the output power due to the dead-time is depicted in Fig. 23(d), and the output power of the system decreases from 8.4 kW with 1 μs dead-time to 2.1 kW with 3 μs dead-time with the same dc input voltage of 210 V. The dead-time effect increases the requirement of the input voltage to sustain the rated power delivery to the load. Therefore, to ensure the nominal output power, the dead-time effect must be considered while designing the WPT system. Furthermore, the increase in the input voltage will result in the increased voltage stresses on the MOSFET switches. Fig. 23(e) shows the experimental values of the dc–dc efficiency of the WPT system during the dead-time analysis. The maximum efficiency of 90.5 % is achieved during the dead-time study.

VI. Conclusion

In this article, the effect of the dead-time between the complementary switching pulses of the resonant inverter was studied in detail. It was found that the change in the current direction during the dead-time results in the VPR/notch in the inverter output voltage. The inverter circuit operations were studied for the different operating conditions of the input phase-angle and inverter duty-cycle. The observations in the circuit operations were used to derive the notch equation, which was used to predict the occurrence of the notches in the inverter voltage. The notch results in the loss of the volt–seconds integral, and consequently, reduces the fundamental component of the voltage. The notches in the inverter voltage also affect the harmonic spectrum due to the multiple switching instances in the fundamental switching cycle. Furthermore, different combinations of input phase angle and inverter duty-cycle could be used to control the harmonic contents in the inverter voltage.

The reduction in the fundamental component due to the notch affects the dc transconductance gain and dc voltage gain of the system. Subsequently, it was also found that the power transferred to the load reduces due to the occurrence of the notch. The experimental validation results were compared with the theoretical predictions on an 8 kW WPT system prototype. The theoretical predictions conducted for the different values of the dead-time were in good agreement with the experimental results. The output power of 8.4 kW was recorded with the dead-time of 1 μs, and maximum dc–dc efficiency of 90.5% was achieved during the dead-time analysis. Furthermore, the output power delivered to the load decreased due to the increase in the dead-time. Therefore, the dead-time effect increases the input voltage requirement at the primary-side to sustain the rated power transfer to the load.

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Utkarsh D. Kavimandan (Graduate Student Member, IEEE) received the B.E. degree in instrumentation and control engineering from the University of Pune-Affiliated Institution in Nashik, Maharashtra, India, in 2012, and the M.S. degree in electrical engineering from Wright State University, Dayton, OH, USA, in 2016. He is currently working toward the Ph.D. degree in electrical engineering with the Tennessee Technological University, Cookeville, TN, USA

He is a Graduate Research Assistant with the Center for Energy Systems Research (CESR), Tennessee Technological University. From August 2015 to December 2015, he interned with Ametek/Prestolite Power in Troy, OH, USA. In 2018 and 2019 he worked as an ASTRO Intern with Power Electronics and Electric Machinery (PEEM) Group, Oak Ridge National Laboratory, Knoxville, TN, USA. His current research interests include wireless charging for electric vehicles and resonant converters.

Veda Prakash Galigekere (Senior Member, IEEE) was born in Bengaluru, India, in 1982. He received the B.E. degree in electrical engineering from Visvesvaraya Technological University, Bengaluru, India, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from Wright State University, Dayton, OH, USA, in 2007 and 2012, respectively.

In 2008 and 2012, he was an Intern with the General Electric Global Research Center, Bengaluru, India. From 2012 to 2016, he was with Lear Corporation, Southfield, MI, USA. He is currently a Research and Development Staff Member and Acting Group Leader of Electric Drives Research Group with Oak Ridge National Laboratory, Oak Ridge, TN, USA. His research interests include high-power wireless power transfer, high-frequency resonant converters, impedance source converters, and small-signal modeling and control of pulsewidth modulation dc–dc converters.

Dr. Galigekere was a Guest Associate Editor of the *IEEE Transactions on Power Electronics*. He is currently an Associate Editor of the *IEEE Transactions on Industry Applications*.

Burak Ozpineci (Fellow, IEEE) received the B.S. degree in electrical engineering from Orta Dogu Technical University, Ankara, Turkey, in 1994, and the M.S. and Ph.D. degrees in electrical engineering from the University of Tennessee, Knoxville, TN, USA, in 1998 and 2002, respectively.

He joined the Post-Master's Program with the Power Electronics and Electric Machinery Group, Oak Ridge National Laboratory (ORNL), Knoxville, TN, USA, in 2001, where he was a Full Time Research and Development Staff Member, in 2002, the Group Leader of the Power and Energy Systems Group, in 2008, and the Power Electronics and Electric Machinery Group, in 2011. He is currently working as the Section Head for the Vehicle and Mobility System Research Section and managing the Electric Drive Technologies Program with ORNL. He also works as a Joint Faculty with the Bredesen Center, University of Tennessee.

Omer Onar (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the Illinois Institute of Technology, Chicago, IL, USA, in 2010.

He received the Alvin M. Weinberg Fellowship at the U.S. Department of Energy's Oak Ridge National Laboratory, Oak Ridge, TN, USA, in July 2010, and joined the Power Electronics and Electric Machinery Group. At Oak Ridge National Laboratory, he worked on advanced power electronics and electric drives, renewable energy, energy storage systems, and wireless power transfer systems. He is currently a Research and Development Staff Member and Group Leader of Vehicle Power Electronics Research Group with Oak Ridge National Laboratory, Oak Ridge, TN, USA.

Dr. Onar was a recipient of the U.S. Department of Energy Vehicle Technologies Office Distinguished Achievement Team Award, the UT-Battelle Research Accomplishment Team Award for his work on wireless power transfer systems, in 2016, and the Research and Development 100 Award jointly with Toyota TEMA for Wireless Charging of Electric Vehicles. He is an Associate Editor of the *IEEE Transactions on Transportation Electrification* and the *IEEE Transactions on Power Electronics*.

Satish M. Mahajan (Senior Member, IEEE) received the B.E. degree in electrical engineering from the University of Poona, Pune, India, in 1978, the M.S. degree in electrical engineering from the State University of New York at Buffalo, Buffalo, NY, USA, in 1983, and the Ph.D. degree in electrical engineering from the University of South Carolina, Columbia, SC, USA, in 1987.

Since 1987, he has been the Faculty of the Electrical and Computer Engineering Department, Tennessee Technological University (TTU), Cookeville, TN, USA. He is currently the Director of the Center for Energy Systems Research (CESR) at the TTU. His research interests include the physical phenomena of optoelectronic and HV devices, and modeling of conventional and renewable power systems.