Stochastic Power Loss Analysis of Differential Power Processing

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***Abstract*—This article presents stochastic power loss analysis for differential power processing (DPP). A stochastic model is developed to analyze power loss scaling in a DPP system based on probability distributions of loads or sources. Scaling factors are introduced to describe how losses change with DPP system size and load or source power variance. Expected power losses of representative DPP topologies are analyzed and compared to losses of a conventional dc–dc converter with the same total switch die area and magnetic volume. The results quantify performance trends of DPP architectures. Models and scaling factors are verified with SPICE simulations and experimental results. The analytical framework, scaling factors, and quantitative models provide useful guidelines for designing large-scale DPP systems. This article is accompanied by a video file demonstrating the modeling procedures and the experimental setup.**

***Index Terms*—Battery management systems, data center power management, dc–dc converters, differential power processing (DPP), photovoltaic systems, series modules, stochastic models.**

I. Introduction

The emerging differential power processing (DPP) concept offers important advantages in systems with load or source modules connected in series. DPP converters process a small fraction of total power to reduce overall conversion stress and enhance system efficiency and functionality. This article, extended from [1], presents a systematic way to analyze power flows and losses in general DPP architectures. For the first time, a stochastic model is developed for quantitative evaluation based on the statistics of load or source power. The analysis models power loss scaling and loss distribution within a DPP system. It reveals how DPP benefits scale with system size and the degree of module power mismatch, offering design insights.

DPP architectures follow from battery active equalization circuits, including switched-inductor (buck–boost) types [2], [3], switched-capacitor types [4], [5], and ac-link or dc-link fully coupled types based on flyback [6]–[8], forward [9], half-bridge [10], and dual-active-bridge (DAB) converters [11], [12]. Similar topologies were later applied to photovoltaic (PV) systems to manage mismatch among series PV cells [13], [14]. Control strategies and architectures have been proposed to achieve PV maximum power point tracking (MPPT) [15]–[20]. DPP architectures have also been implemented in emerging dc systems such as data center servers [21], [22] and multiprocessor systems [23]–[25].

Power flows in DPP systems are usually dynamic and unpredictable [26]. Power distribution and mismatch among series voltage domains are influenced by factors that include aging, manufacturing variation, temperature differences [4], illuminance variation [27], [28], and random task requests for data center servers [21]. Potentially, each module power is a random process. Previous work to analyze how power loss and power ratings of DPP converters change with statistical variance has been based on numerical simulations or data-driven methods [29]–[31]. An analytical method to evaluate performance with large-scale stochastic loads or sources is needed and is the main focus here.

In this article, DPP topologies are grouped into two primary categories: fully coupled DPP and ladder DPP. We perform a systematic analysis of power flow for each, and develop a stochastic model to predict conduction loss and its distribution. The purpose of the stochastic model is not to predict all losses in DPP systems, but rather to understand how performance scales with system dimension and load or source power variance. The model provides guidance on topology selection and design optimization. Instead of estimating loss for a specific case, the model is an ensemble evaluation for stochastic power distributions (e.g., Gaussian, Poisson, Bernoulli, etc.). A scaling factor, $\mathcal{S}(\bullet)$, is introduced to describe how loss changes with system size or module power variance. Representative DPP topologies are analyzed and compared to a reference N:1 DAB converter [32], [33], given the same total switch die area and magnetic core

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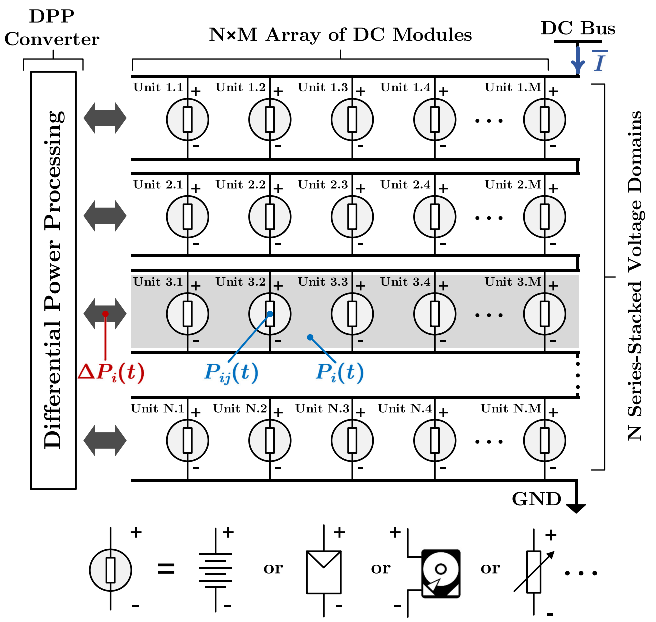


Fig. 1. An $N \times M$ DPP system with N series-stacked voltage domains, each comprising M load or source modules. $P_{ij}(t)$ and $P_i(t)$ are the power of one dc module and of one voltage domain, respectively; $\Delta P_i(t)$ is the power mismatch for one voltage domain.

size. The models are validated with SPICE simulations and with experiments designed to test loss scaling.

In the remainder of this article, Section II introduces stochastic modeling for the primary DPP categories and develops loss scaling factors. Section III demonstrates typical circuit implementations and derives output resistance for loss analysis. Section IV compares various DPP topologies against the reference N:1 DAB converter, derives performance trends, and verifies these with SPICE simulations. Section V generalizes the model to include module power correlation. Section VI validates the model with experimental results. Section VII concludes this article. Extended derivations for the models, and an application case study on a DPP-powered data storage server, are provided in the Appendix.

II. Stochastic Model for DPP Loss

Fig. 1 shows a general DPP system. An $N \times M$ array of load or source modules is configured in N series-stacked voltage domains. Each domain comprises M modules connected in parallel. Analysis in this article is based on modular loads, and analysis for modular sources follows the same procedure. Denote the power consumption of the jth load in the ith voltage domain as $P_{ij}(t)$. The total *domain power* consumed within the ith voltage domain is

$$P_i(t) = P_{i1}(t) + P_{i2}(t) + \cdots + P_{iM}(t). \tag{1}$$

DPP converters deliver power mismatch $\Delta P_i(t)$ among series voltage domains. In practical applications, the power distribution can be complicated, with unpredictable patterns or correlations. In this article, each individual load power $P_{ij}(t)$, domain power $P_i(t)$, and mismatched power $\Delta P_i(t)$ is modeled as a random

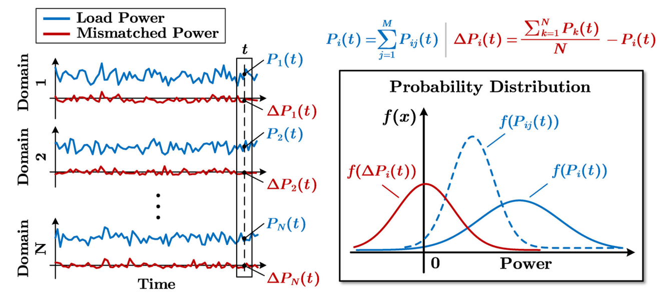


Fig. 2. Load power and mismatched power of each voltage domain is a random process with a probability distribution (Gaussian distributions are shown here as an example).

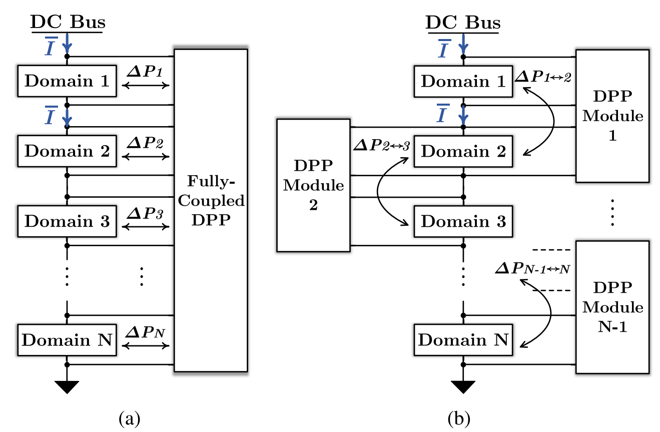


Fig. 3. Typical DPP architectures. (a) Fully coupled DPP. (b) Ladder DPP.

process as indicated in Fig. 2. Their values at any time instant t are random variables with certain probability distributions. We first analyze the case when all module powers are statistically independent with identical distributions (i.i.d.), and later extend the analysis to cases with correlation. In the case with i.i.d. loads, individual load power mean values $\mathbb{E}[P_{ij}(t)]$ and variances $\mathrm{Var}[P_{ij}(t)]$ are identical and are denoted as μ_0 and σ_0^2. Each domain has the same voltage, denoted as V_0. A more general case allows unbalanced voltages (as when each domain has its own power droop characteristic), but matched domain voltages are explored here for clarity. The analytical framework in this article can be applied to DPP systems with more complicated patterns such as unmatched load power expectations across voltage domains.

A. Fully Coupled DPP and Ladder DPP

The two primary DPP categories are shown in Fig. 3. Fig. 3(a) depicts the architecture of a fully coupled DPP converter, in which all voltage domains are coupled by the DPP circuitry. A typical fully coupled DPP circuit functions as a multiport dc–dc converter [13], with a direct power flow path between any two domains. Due to the series architecture, the same bus current $\overline{I}(t) = \frac{\sum_{k=1}^{N} P_k(t)}{N V_0}$ flows through each voltage domain plus its corresponding DPP port. The instantaneous differential power processed for the ith voltage domain is

$$\Delta P_i(t) = \overline{I}(t)V_0 - P_i(t) = \overline{P}(t) - P_i(t). \tag{2}$$

Here, $\overline{P}(t) = \sum_{k=1}^{N} P_k(t)/N$ is the arithmetic average of the N domain powers. Equation (2) indicates that in a fully coupled DPP converter, the differential power processed at the ith port is the power mismatch between the average domain power $\overline{P}(t)$ and the ith domain power $P_i(t)$. With i.i.d. loads, the power rating of each port in a fully coupled DPP is the same.

Fig. 3(b) shows the architecture of a domain-to-domain or ladder DPP system, in which multiple standalone dc–dc converters (termed *DPP submodules*) link neighboring voltage domains. The differential power processed for one voltage domain is related to multiple DPP submodules

$$P_i(t) + \Delta P_{i\leftrightarrow i+1}(t) - \Delta P_{i-1\leftrightarrow i}(t) = \overline{I}(t)V_0 = \overline{P}(t) \quad (3)$$

where $\Delta P_{i\leftrightarrow i+1}(t)$ is the differential power that the ith submodule delivers from the ith domain to the $(i+1)$th domain ($\Delta P_{i\leftrightarrow i+1}(t) = 0$, if $i = 0$ or N). Reorganizing (3), we get

$$\Delta P_{i\leftrightarrow i+1}(t) = \sum_{k=1}^{i}(\overline{P}(t) - P_k(t)) = \sum_{k=1}^{i} \Delta P_k(t)$$

$$= i \times \overline{P}(t) - \sum_{k=1}^{i} P_k(t). \quad (4)$$

In a ladder DPP converter, there is no direct power path between nonneighboring voltage domains. Differential power must go through multiple submodules to manage nonneighboring domains, potentially resulting in differential power accumulation. As indicated in (4), the ith submodule needs to process the accumulated mismatched power of the first i voltage domains, i.e., $\sum_{k=1}^{i} \Delta P_k(t)$. This will cause additional power to be processed in a ladder DPP system compared to a fully coupled DPP system. It also leads to varied power ratings among submodules in a ladder DPP converter.

In some DPP architectures, the power flow may be impacted by the control methods [34], [35]. Modeling the power loss of these architectures is beyond the scope of this article, but the stochastic analytical framework developed here can be extended to cover these cases.

B. Stochastic Loss Model and Scaling Factor

In Fig. 1, parameters N, M, and σ_0^2 impact the differential power processed by DPP converters. Here, we develop a stochastic model with i.i.d. loads to quantify the impact. Scale-dependent loss (i.e., loss that scales with system size or load power variance) is derived based on processed differential power. Losses that are expected to be approximately scale independent, such as control power and losses linked to switching frequency, are not included in the model but are explored during experiments to test scaling validity. The expected value of scale-dependent power loss is used to describe the average loss of a DPP system. For comparison, a stochastic loss model is derived for a conventional N:1 DAB converter delivering the same total load power $\sum_{i=1}^{N} P_i(t)$, and this is used as a reference case. Detailed derivations of the expected scale-dependent power loss are provided in Appendix I.

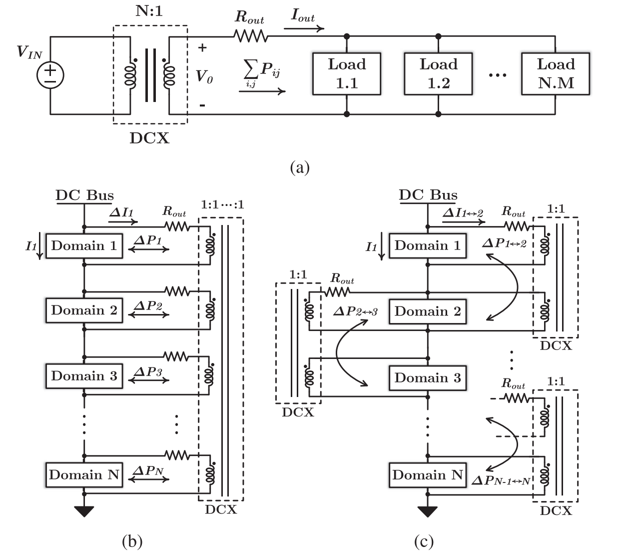


Fig. 4. Equivalent circuit model for loss analysis of (a) conventional N:1 dc–dc converter based on a DAB, (b) fully coupled DPP, and (c) ladder DPP.

Fig. 4 shows equivalent circuit models of the reference converter and of the two typical DPP architectures. Conduction loss dominates scale-dependent losses, and is captured by aggregating internal losses into an effective output resistance, R_{out}, for each module or circuit. Switching loss, core loss, control power, and other nonideal effects can be added, typically as polynominal functions of the processed power, to enhance accuracy, but the modeling procedure for any of these follows from that presented below.

1) Conventional Reference N:1 DAB: A stochastic loss model for a conventional N: 1 DAB converter supplying V_0 is derived here as a comparative reference or baseline. This converter can be modeled as an N:1 transformer with an output resistance R_{out} [36], as shown in Fig. 4(a). All loads are connected in parallel at the output. The expected loss in this converter when processing full power is

$$\mathbb{E}[P_{loss}(t)] = \mathbb{E}[R_{out} I_{out}^2(t)] = \frac{R_{out}}{V_0^2}\mathbb{E}\left[\left(\sum_{i=1}^{N} P_i(t)\right)^2\right]$$

$$= \left(MN\sigma_0^2 + M^2N^2\mu_0^2\right) \times \frac{R_{out}}{V_0^2} \Rightarrow \underbrace{\mathcal{S}(M^2\, N^2\mu_0^2)}_{scaling\ factor}. \quad (5)$$

Detailed derivations are provided in Appendix I. We use symbol $\mathcal{S}(\bullet)$ to represent a performance scaling factor that describes how power loss changes with system size or load power variance. As indicated by (5), loss in the reference converter depends on average load power as well as on load variance, and scales quadratically with the total average load power $MN\mu_0$ unless the variance σ_0^2 is extremely high.

2) Fully Coupled DPP Converter: As illustrated in Fig. 4(b), a fully coupled DPP topology can be modeled as an N-port network coupled with an N-winding transformer with uniform turns ratios. Each port has an effective output resistance R_{out}, matched for this analysis. The ith port processes $\Delta P_i(t)$, so the

TABLE I
STOCHASTIC POWER LOSS MODELS OF N:1 DAB CONVERTER AND TWO GENERAL DPP ARCHITECTURES ($M \geq 1$, $N \geq 2$)

	Expected Power Loss of the i^{th} DPP Port/Submodule	Expected Total Power Loss	Scaling Factor
N:1 DAB Converter	N/A	$(MN\sigma_0^2 + M^2N^2\mu_0^2) \times \frac{R_{out}}{V_0^2}$	$\mathcal{S}(M^2N^2\mu_0^2)$
Fully-Coupled DPP	$\frac{M(N-1)}{N}\sigma_0^2 \times \frac{R_{out}}{V_0^2}$	$M(N-1)\sigma_0^2 \times \frac{R_{out}}{V_0^2}$	$\mathcal{S}(MN\sigma_0^2)$
Ladder DPP	$\frac{M(N-i)i}{N}\sigma_0^2 \times \frac{R_{out}}{V_0^2}$	$\frac{M(N-1)(N+1)}{6}\sigma_0^2 \times \frac{R_{out}}{V_0^2}$	$\mathcal{S}(MN^2\sigma_0^2)$

instantaneous loss and expected loss at the ith port are

$$P_{loss.i}(t) = \Delta I_i(t)^2 R_{out} = \left(\frac{\Delta P_i(t)}{V_0}\right)^2 R_{out}$$
$$= R_{out}\left(\frac{\overline{P}(t) - P_i(t)}{V_0}\right)^2 \quad (6)$$
$$\mathbb{E}[P_{loss.i}(t)] = \frac{R_{out}}{V_0^2} \times \frac{M(N-1)}{N}\sigma_0^2. \quad (7)$$

Here, $\Delta I_i(t)$ is the current flowing through R_{out} at each port and is also the mismatch between the average current and domain load current: $\Delta I_i(t) = \overline{I}(t) - I_i(t)$. Notice that $\mathbb{E}[P_{loss.i}(t)]$ is proportional to σ_0^2 because $P_{loss.i}(t)$ depends on $\Delta I_i^2(t)$. Each port has the same expected loss, and the total is

$$\mathbb{E}[P_{loss}(t)] = \sum_{i=1}^{N} \mathbb{E}[P_{loss.i}(t)]$$
$$= M(N-1)\sigma_0^2 \times \frac{R_{out}}{V_0^2} \Rightarrow \underbrace{\mathcal{S}(MN\sigma_0^2)}_{scaling\ factor}. \quad (8)$$

The loss scaling in (8) is linear in N, M, and σ_0^2 but independent of the average load power μ_0.

3) Ladder DPP Converter: In a ladder DPP topology, each submodule can be modeled as a 1:1 transformer with output resistance R_{out}, as illustrated in Fig. 4(c). The ith submodule is processing $\Delta P_{i \leftrightarrow i+1}(t)$, so the instantaneous and expected loss of the ith submodule are

$$P_{loss.i}(t) = \Delta I_{i \leftrightarrow i+1}(t)^2 R_{out} = \left(\frac{\Delta P_{i \leftrightarrow i+1}(t)}{V_0}\right)^2 R_{out}$$
$$= R_{out}\left(\frac{i \times \overline{P}(t) - \sum_{k=1}^{i} P_k(t)}{V_0}\right)^2 \quad (9)$$
$$\mathbb{E}[P_{loss.i}(t)] = \frac{R_{out}}{V_0^2} \times \frac{M(N-i)i}{N}\sigma_0^2. \quad (10)$$

Here, $\Delta I_{i \leftrightarrow i+1}(t)$ is the effective current that flows through R_{out} at each submodule and is equal to the accumulated mismatched current of the top i voltage domains: $\Delta I_{i \leftrightarrow i+1}(t) = \sum_{k=1}^{i} \Delta P_k(t)/V_0 = \sum_{k=1}^{i} \Delta I_k(t)$. Expected loss varies among submodules, and the total expected loss is

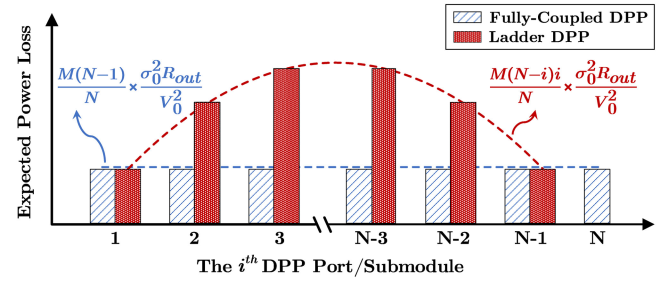


Fig. 5. Expected power loss of the ith port or submodule in a fully coupled DPP converter and a ladder DPP converter with N series voltage domains.

$$\mathbb{E}[P_{loss}(t)] = \sum_{i=1}^{N-1} \mathbb{E}[P_{loss.i}(t)]$$
$$= \frac{M(N-1)(N+1)}{6}\sigma_0^2 \times \frac{R_{out}}{V_0^2} \Rightarrow \underbrace{\mathcal{S}(MN^2\sigma_0^2)}_{scaling\ factor}. \quad (11)$$

The loss scales linearly with M and σ_0^2, and quadratically with N. Compared to a fully coupled DPP converter, a ladder DPP converter has a higher scaling factor with N since differential power accumulates along the series stack. Notice that the total loss is still independent of the average load power μ_0.

Table I summarizes the expected power loss and scaling factors of the three architectures. For DPP solutions, the expected loss scales linearly with variance σ_0^2 but is independent of average load power μ_0. This is consistent with the fundamental benefit: loss in a DPP system is determined by power differences, expected to be only a fraction of total load power. If the individual load powers match, a DPP system has no conduction loss.

Fig. 5 plots the expected loss distribution in a fully coupled DPP converter and a ladder DPP converter. In a fully coupled DPP, the expected loss is uniformly distributed among different ports, whereas in a ladder DPP, submodules closer to center of the series stack tend to process more power and generate more power loss.

III. OUTPUT RESISTANCE ANALYSIS FOR VARIOUS DPP TOPOLOGIES

In a DPP architecture, the switch count and magnetic component count track the number of voltage domains N. A reasonable approach is to compare alternatives given the same total semiconductor switch size and magnetic component volume.

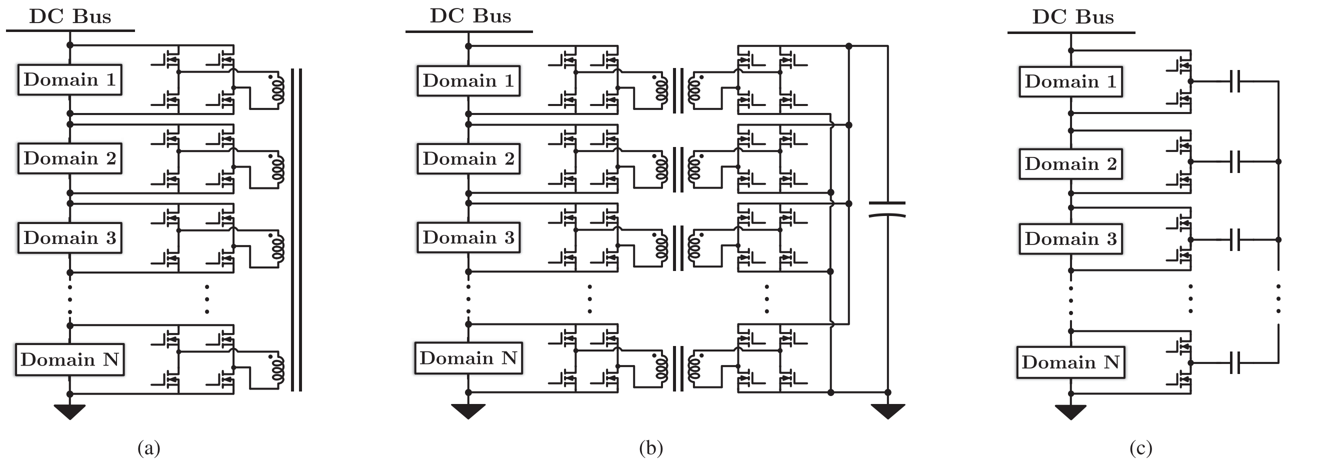


Fig. 6. Fully coupled DPP topologies. (a) Ac fully coupled DPP [12], [21]. (b) Dc fully coupled DPP [11], [22]. (c) Dickson-SC DPP [5].

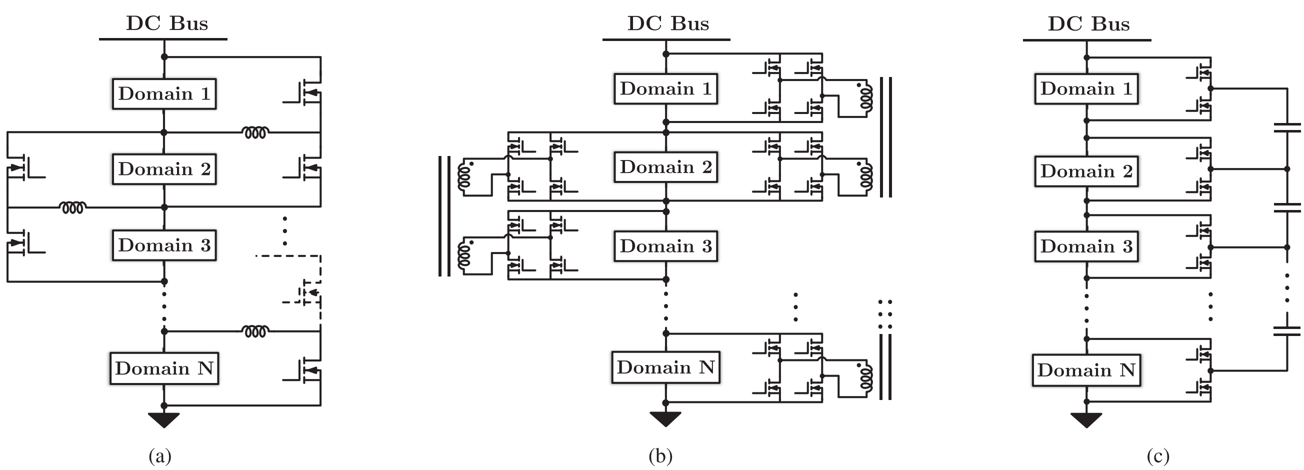


Fig. 7. Ladder DPP topologies. (a) Ladder DPP with buck–boost cells [2], [17], [19], [24], [26], [29]–[31]. (b) Ladder DPP with DAB cells. (c) Ladder-SC DPP [4]–[6], [16], [23].

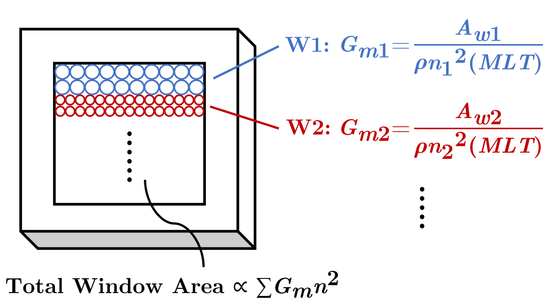


Fig. 8. Magnetic core window area distribution and winding conductance. Total core window area is proportional to $\sum G_m n^2$. A_w represents the distributed window area for each winding, n is the effective number of turns in each winding, ρ is the winding resistivity, and MLT is the mean length per turn, set to be identical for all windings.

In this section, DPP topologies are explored this way. Their output resistance R_{out} is analyzed and compared with that of the reference converter under the following constraints.

1) *Identical total semiconductor die area:* For switches, semiconductor die area scales linearly with the $G_{sw} V_{sw}^k$ product [37], [38]. G_{sw} is switch conductance; V_{sw} is switch blocking voltage; and coefficient k, typically 2, depends on material and process. The total semiconductor die area is represented as the sum $\sum G_{sw} V_{sw}^2$ for all switches, constrained to be identical for topologies compared here and normalized to $G_{SW} V_0^2$.
2) *Identical total volume of magnetic components:* In this article, total volume of magnetic components is evaluated using core window area, which in turn tracks core cross sectional area. As illustrated in Fig. 8, the window area of each winding is proportional to $G_m n^2$ (assume each winding is assigned the same fill factor). G_m is the winding conductance and n is the number of series turns. Here, n is determined by flux limits on volts per turn, and volts-per-turn values of all related topologies are scaled to V_0. The total window area is represented as the sum $\sum G_m n^2$ over all windings, constrained to be identical for topologies compared here and normalized to G_M. Switched-capacitor topologies do not require magnetics.

To model the output resistance R_{out} in Fig. 4, $R_{ds(on)}$ of each switch and winding dc resistance are lumped together and constrained as above.

Figs. 6 and 7 exhibit several typical circuit implementations of fully coupled DPP architectures and ladder DPP architectures,

TABLE II
COMPARISON BETWEEN THE REFERENCE CONVERTER AND DIFFERENT DPP TOPOLOGIES ($N \geq 2$)

Topologies			Semiconductor Switches				Transformer/Inductor Windings				Output Resistance R_{out}
			Switch Count	Voltage Rating	$R_{ds(on)}$	RMS[a] Current	Winding Count	Turns[b]	Winding Resistance	RMS[c] Current	
N:1 Converter (Conventional Reference)	DAB	Primary[d]	4	NV_0	$\frac{8N^2}{G_{SW}}$	$\frac{\sqrt{2}}{2N} I_{out}$	1	N	$\frac{2N^2}{G_M}$	$\frac{I_{out}}{N}$	$\frac{32}{G_{SW}} + \frac{4}{G_M}$
		Secondary[e]	4	V_0	$\frac{8}{G_{SW}}$	$\frac{\sqrt{2}}{2} I_{out}$	1	1	$\frac{2}{G_M}$	I_{out}	
Fully-Coupled DPP	Ac-Coupled		$4N$	V_0	$\frac{4N}{G_{SW}}$	$\frac{\sqrt{2}}{2}\Delta I_i$	N	1	$\frac{N}{G_M}$	ΔI_i	$\frac{8N}{G_{SW}} + \frac{N}{G_M}$
	Dc-Coupled		$8N$	V_0	$\frac{8N}{G_{SW}}$	$\frac{\sqrt{2}}{2}\Delta I_i$	$2N$	1	$\frac{2N}{G_M}$	ΔI_i	$\frac{32N}{G_{SW}} + \frac{4N}{G_M}$
	SC-based (FSL)		$2N$	V_0	$\frac{2N}{G_{SW}}$	$\sqrt{2}\Delta I_i$	N/A	N/A	N/A	N/A	$\frac{8N}{G_{SW}}$
Ladder DPP	Buck-Boost-cell		$2N-2$	$2V_0$	$\frac{8N-8}{G_{SW}}$	$\sqrt{2}\Delta I_{i\leftrightarrow i+1}$	$N-1$	2	$\frac{4N-4}{G_M}$	$2\Delta I_{i\leftrightarrow i+1}$	$\frac{32N-32}{G_{SW}} + \frac{4N-4}{G_M}$
	DAB-cell		$8N-8$	V_0	$\frac{8N-8}{G_{SW}}$	$\frac{\sqrt{2}}{2}\Delta I_{i\leftrightarrow i+1}$	$2N-2$	1	$\frac{2N-2}{G_M}$	$\Delta I_{i\leftrightarrow i+1}$	$\frac{32N-32}{G_{SW}} + \frac{4N-4}{G_M}$

[a,c] These two columns list rms current in each component. For the reference converter, they list the rms current in each component on the primary side or the secondary side; for DPP topologies, they list the rms current of each component in the ith port or submodule.
[b] This column lists the number of turns per winding, normalized to a volts-per-turn value of V_0.
[d,e] These two rows show primary side and secondary side information of the reference converter. Semiconductor die area $G_{SW}V_0^2$ and winding window area G_M are allocated equally across the primary and secondary sides.

respectively. An energy buffering capacitor can be added in parallel to each voltage domain for stable voltage. Table II compares these topologies to the reference converter, in terms of normalized quantities. In Table II, the root-mean-square (rms) current in each component is calculated based on the output current (I_{out}) or the effective differential current (ΔI_i or $\Delta I_{i\leftrightarrow i+1}$) as defined in Fig. 4. For the reference DAB converter, the semiconductor die area $G_{SW}V_0^2$ and winding window area G_M are equally distributed between the primary and secondary sides; for DPP converters, they are equally distributed among DPP ports or submodules.

To model R_{out} of magnetic-based topologies [reference converter, Figs. 6(a) and (b), and 7(a) and (b)], the component rms current is calculated with the following approximations. First, trapezoidal current waveforms in topologies with active bridges [reference converter, Figs. 6(a) and (b), and 7(b)] are treated as square waves. Second, the inductor current in the DPP topology with buck–boost cells [see Fig. 7(a)] has low ripple. Based on switch $R_{ds(on)}$, winding dc resistance, and rms current, effective output resistance R_{out} of the magnetic-based topologies can be obtained.

Fig. 6(a) shows an ac fully coupled DPP converter with full bridge coupling to a multiwinding transformer. This converter comprises $4N$ switches, each blocking V_0, and N windings. Volts-per-turn values are scaled to V_0, so each winding contains one turn per unit. The resistances of each switch and each winding are $\frac{4N}{G_{SW}}$ and $\frac{N}{G_M}$. The rms currents in each switch and transformer winding at the ith port are $\frac{\sqrt{2}}{2}\Delta I_i$ and ΔI_i, respectively, so the conduction loss at the ith port is

$$\begin{aligned} P_{loss.i} &= \left(\frac{\sqrt{2}}{2}\Delta I_i\right)^2 \frac{4N}{G_{SW}} \times 4 + \Delta I_i^2 \frac{N}{G_M} \\ &= \Delta I_i^2 R_{out}. \end{aligned} \tag{12}$$

TABLE III
R_{out} MODELING OF SC DPP TOPOLOGIES AT SSL ($N \geq 2$)

Topologies	Capacitor Count	Charge[a] Transfer	Output Resistance R_{out} (@ SSL)
Dickson-SC DPP	N	$\frac{\Delta I_i}{f_{sw}}$	$\frac{1}{Cf_{sw}}$ (Fig. 4a)
Ladder-SC DPP	$N-1$	$\frac{\Delta I_{i\leftrightarrow i+1}}{f_{sw}}$	$\frac{1}{Cf_{sw}}$ (Fig. 4b)

[a] This column lists the charge transfer per half switching cycle of the ith capacitor (from top to bottom) in a SC DPP.

This indicates that the output resistance of each port is $\frac{8N}{G_{SW}} + \frac{N}{G_M}$. Results for R_{out} of other magnetic-based DPP topologies and the reference converter can be modeled similarly and are summarized in Table II.

To model R_{out} of switched-capacitor (SC) DPP topologies [Figs. 6(c) and 7(c)], power loss should be analyzed at both the slow switching limit (SSL) and fast switching limit (FSL) [37]. Fig. 6(c) shows a Dickson-SC DPP converter in which all voltage domains are coupled through capacitors. Since charge can be transferred through the capacitors between any two voltage domains within one switching cycle, there is a direct power flow path between arbitrary voltage domains, and the circuit functions like a fully coupled DPP topology. Fig. 7(c) shows a ladder-SC DPP in which neighboring voltage domains are linked by one capacitor. Charge can transfer only between two neighboring voltage domains in each switching cycle, so this functions like a ladder-DPP topology.

At the SSL, power loss of a SC converter is dominated by capacitor charge sharing loss. Table III summarizes charge transfer of each capacitor and R_{out} at the SSL for a Dickson-SC DPP and ladder-SC DPP. Denote the capacitance as C and the switching frequency as f_{sw}. The energy buffering capacitor at each voltage domain should be large, with a stable voltage, so its charge sharing loss is neglected. In the Dickson-SC DPP, charge transfer of the ith capacitor is $\Delta I_i/f_{sw}$ per half switching cycle, so the charge sharing loss at the ith port is

$$P_{loss.i} = \frac{\Delta Q_i^2}{C} f_{sw} = \frac{(\Delta I_i/f_{sw})^2}{C} f_{sw} = \Delta I_i^2 R_{out}. \quad (13)$$

Accordingly, R_{out} of the Dickson-SC DPP as defined in Fig. 4(b) is $\frac{1}{Cf_{sw}}$. In the ladder-SC DPP, charge transfer of the ith capacitor that links the ith and $(i+1)$th voltage domains is $\sum_{k=1}^{i} \Delta I_k/f_{sw} = \Delta I_{i\leftrightarrow i+1}/f_{sw}$ per half switching cycle. Similarly, R_{out} of the ladder-SC DPP as defined in Fig. 4(c) is also $\frac{1}{Cf_{sw}}$. Although ladder-SC topologies have the same R_{out}, they generate higher power loss due to differential power accumulation, especially if the voltage domain is close to the stack center or if N is large. Note that SC capacitor sizing also relates to capacitor utilization and voltage ratings, which is outside the scope of this work. Detailed comparison of various SC topologies and their passive component utilization and sizing can be found in [39].

At the FSL, capacitor charge sharing loss of a SC DPP is negligible. Conduction loss dominates. All capacitors act as fixed voltage sources. In this case, both the Dickson-SC DPP and the ladder-SC DPP function like fully coupled DPP circuits and are equivalent. Each switch at the ith domain conducts $2\Delta I_i$ for half a switching cycle, and corresponded R_{out} value of the SC-based DPP at FSL is listed in Table II. For a unified comparison, internal capacitor power loss is not included here, and SC DPP topologies are compared with the reference converter as fully coupled circuits based on conduction loss at the FSL.

As listed in Table II, R_{out} of a dc fully coupled DPP is four times of that in an ac fully coupled DPP due to doubling of switch and winding counts and doubling of "dc–ac–dc" differential power conversion stages [21]. At the FSL, the two SC DPP topologies have the same conduction loss as that of an ac fully coupled DPP without considering winding loss. Although an SC topology has no winding loss, the capacitor charge sharing loss is nonnegligible if the capacitors are not large enough or if the switching frequency is not high enough.

Table II also indicates that with a fixed total switch die area and a fixed total magnetic volume, output resistance of DPP topologies increases linearly with the number of voltage domains due to the linear growth of component count, whereas R_{out} of the reference converter is fixed.

IV. DPP Scaling and Performance Trends

This section explores DPP performance trends as the system size or power variance scales up. In DPP systems, the processed differential power increases as load power variance increases, and advantages in terms of output resistance diminish when N scales up, as shown in Table II. To evaluate trends, a comparative expected loss ratio $\beta = \frac{\mathbb{E}[P_{loss,DPP}]}{\mathbb{E}[P_{loss,ref}]}$ can be used as a performance metric. The coefficient of variance $C_V = \frac{\sigma_0}{\mu_0}$ is used to represent the normalized variance of $P_{ij}(t)$. Values of β for a variety of topologies have been calculated based on the analysis. Lower values are better, and DPP advantages disappear if $\beta > 1$.

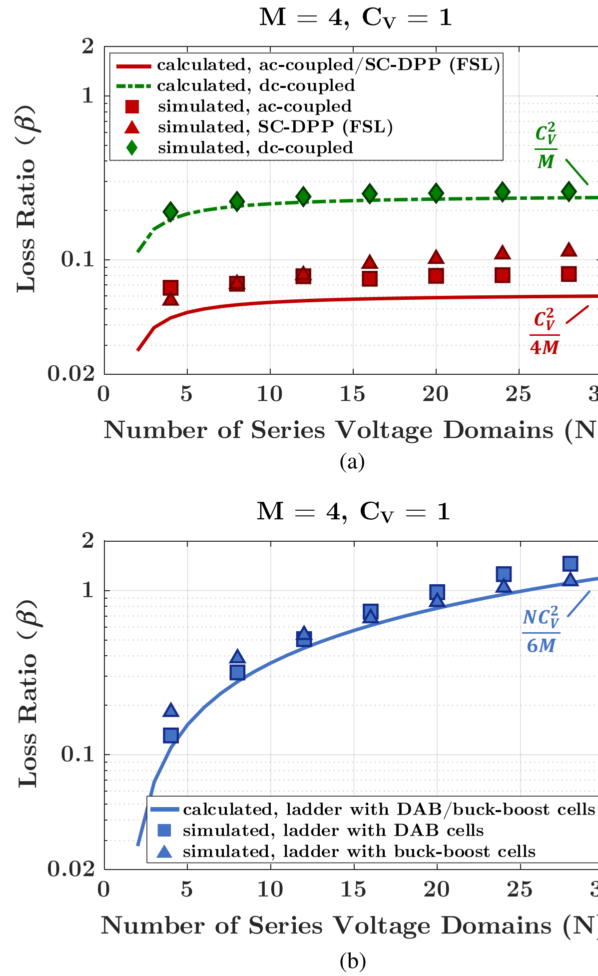


Fig. 9. Calculated and simulated loss ratio β as a function of N in (a) fully coupled DPP converters and (b) ladder DPP converters.

The calculated β values and their asymptotic limits as M, N, and C_V scale up are plotted in Figs. 9–11.

Calculated results have been compared to Monte Carlo simulations in SPICE, in which a random sequence is generated for each load power. In simulations, the domain voltage V_0 is 5 V, and the domain power is mostly below 10 W. For a given M, N, and C_V, each simulation was run 10 000 times to obtain an average power loss. For each case, simulated β was obtained as the ratio of the simulated average DPP loss to the calculated loss of the reference converter delivering the same total power. Switch $R_{ds(on)}$ and winding resistance in each topology are set based on Table II. Since the Dickson-SC DPP and the ladder-SC DPP are equivalent with fast switching, the simulation uses a ladder-SC DPP at the FSL. When comparing SC DPP circuits to the reference converter, winding conduction loss has been excluded.

Figs. 9–11 compare calculated and simulated β values for various DPP topologies as functions of load array dimensions N and M, and coefficient of variance C_V. Considering the scaling of R_{out}, when N increases, the expected loss of fully coupled DPP topologies increases as N^2, the same growth rate as for the reference converter. The expected power loss of ladder DPP

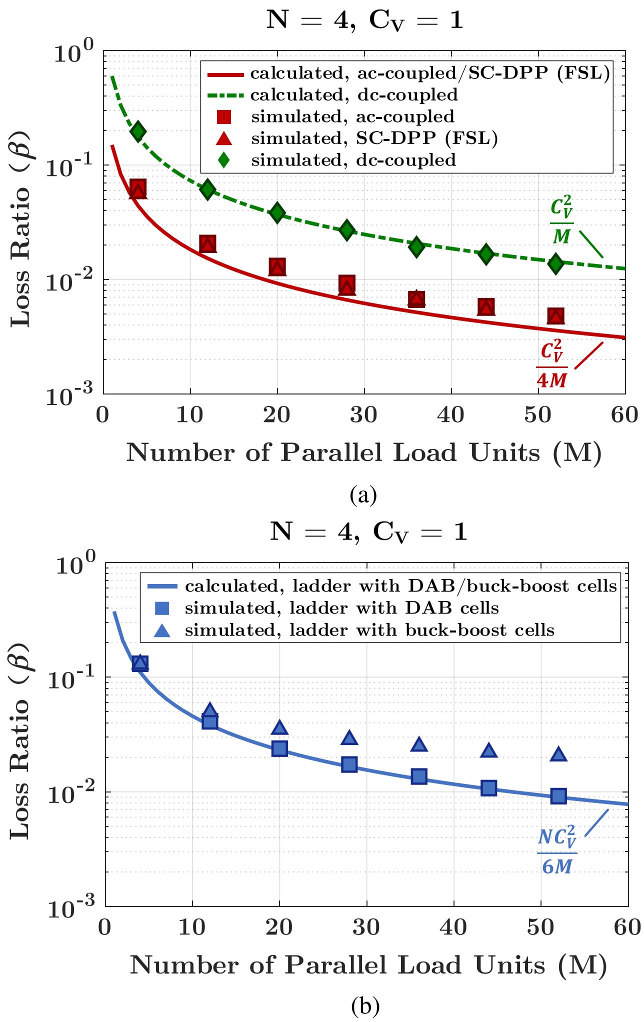


Fig. 10. Calculated and simulated loss ratio β as a function of the number of the parallel loads M in (a) fully coupled and (b) ladder DPP converters.

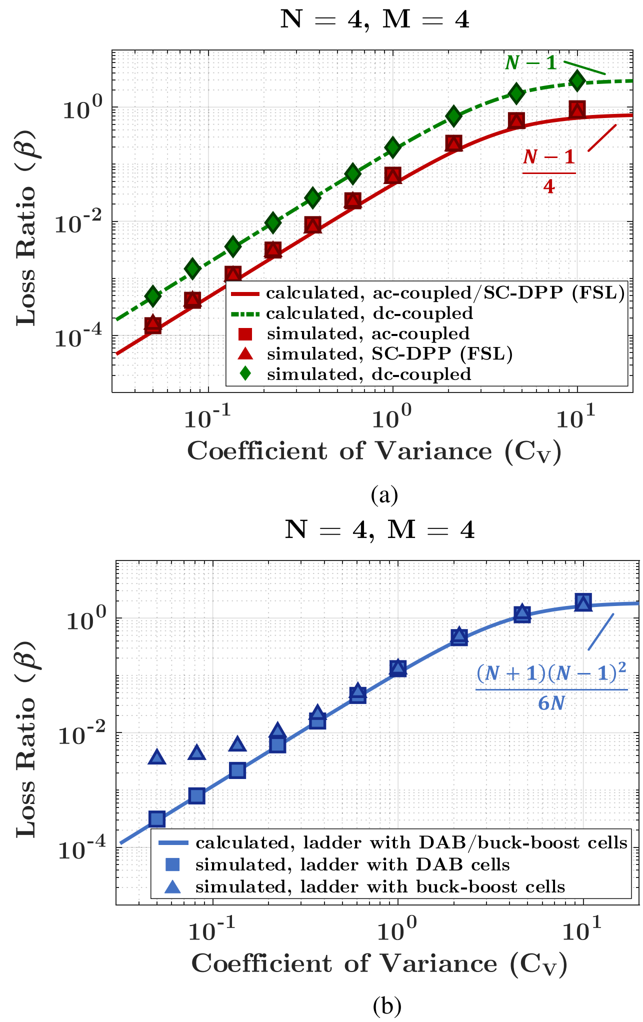


Fig. 11. Calculated and simulated loss ratio β as a function of coefficient of variance C_V in (a) fully coupled and (b) ladder DPP converters.

topologies grows as N^3. Therefore, as N scales up, β of fully coupled DPP topologies converges to an upper limit, but β of ladder DPP topologies keeps increasing, as shown in Fig. 9. The figure suggests that ladder DPP circuits lose their advantages for $N \geq 25$, given $M = 4$ and $C_V = 1$.

When the number of parallel load units M increases, the expected loss in both fully coupled DPP and ladder DPP circuits increases as M, while the expected loss in the reference converter tracks M^2. Thus, the loss ratio β decreases for both fully coupled DPP and ladder DPP circuits with increasing M, as shown in Fig. 10. As M increases, power consumption of each voltage domain becomes relatively more balanced since multiple random loads with the same probability distribution in parallel will narrow the domain population variance. The asymptotic limits are $\beta \to \frac{C_V^2}{4M}$ for an ac-coupled or a SC DPP (FSL), $\beta \to \frac{C_V^2}{M}$ for a dc-coupled DPP, and $\beta \to \frac{NC_V^2}{6M}$ for a ladder DPP with DAB or buck-boost cells.

Fig. 11 shows log-log plots of β for various DPP topologies as a function of C_V. As C_V increases, power variation among voltage domains increases, so the DPP converters need to process more power. Thus, β increases with C_V for all DPP topologies, but it converges to an upper limit. This is because the power loss of the reference converter, as in (5), is ultimately dominated by $MN\sigma_0^2$ when C_V (i.e., $\frac{\sigma_0}{\mu_0}$) increases, the same rate of increase with C_V as for DPP topologies. Asymptotic upper limits of β for ac-coupled or SC DPP (FSL), dc-coupled DPP, and ladder DPP with DAB or buck–boost cells are $\frac{N-1}{4}$, $N-1$, and $\frac{(N+1)(N-1)^2}{6N}$, respectively.

In Figs. 9–11, calculated ratios match simulated ones well, validating the stochastic model. Mismatches are caused by active bridge trapezoidal current waveforms [see Figs. 6(a) and (b), and 7(b)], inductor current ripple in buck–boost cells [see Fig. 7(a)], and capacitor charge sharing loss in SC converters [see Figs. 6(c) and 7(c)]. For larger M or smaller C_V, the average differential power processed by each buck–boost cell is reduced. In this case, inductor ripple current becomes comparable to average current, yielding increased mismatch between calculated and simulated results for ladder DPP with buck-boost cells, as shown in Figs. 10(b) and 11(b).

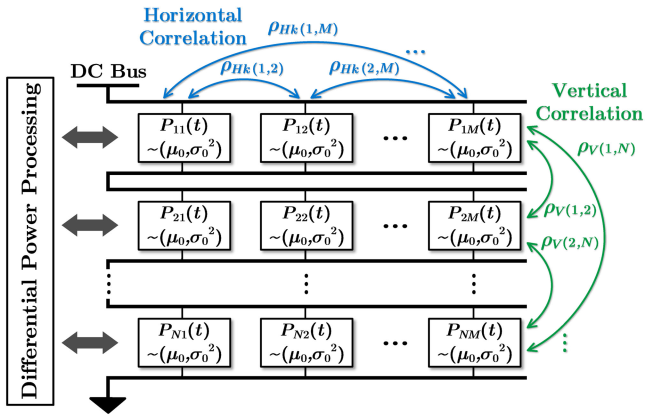


Fig. 12. Two types of load correlation in an $N \times M$ DPP system. (1) Vertical correlation across different voltage domains is denoted in green. (2) Horizontal correlation between loads within one voltage domain is denoted in blue.

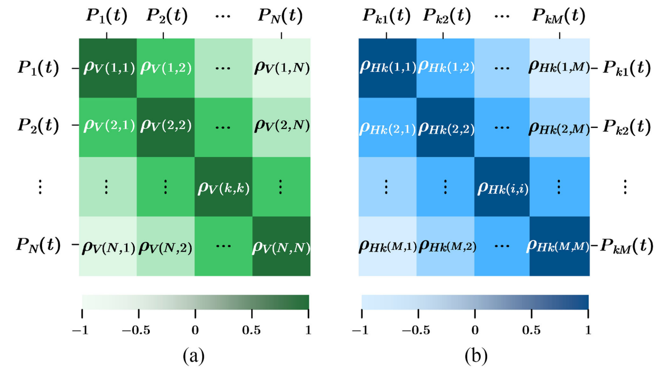


Fig. 13. (a) Vertical correlation matrix $\boldsymbol{\rho_V}$: $\rho_V(i,j)$ is the correlation coefficient between the ith and jth domain power, $P_i(t)$ and $P_j(t)$. (b) Horizontal correlation matrix $\boldsymbol{\rho}_{Hk}$: $\rho_{Hk}(i,j)$ is the correlation coefficient between the ith and jth load power in the kth domain, $P_{ki}(t)$ and $P_{kj}(t)$.

Figs. 9–11, together with Tables I–III, provide useful design insights for DPP architectures. For example, the asymptotic upper limit of β in an ac-coupled DPP topology is $\frac{C_V^2}{4M}$ as N increases. When $M = 4$, $N \geq 2$, and $C_V = 1$, the loss ratio of an ac-coupled DPP converter is below 0.0625, indicating at least 16x loss reduction compared to the reference converter. A dc-coupled DPP converter can offer at least 4x reduction under the same conditions. If $M > C_V^2$, then β of fully coupled DPP converters will be always less than 1, indicating that under this condition a fully coupled DPP solution will be more efficient than the reference converter for arbitrary N. For a ladder DPP converter, β will be larger than 1 if N exceeds $\frac{6M}{C_V^2}$, indicating that a ladder DPP converter will lose advantages if N is large. It should be pointed out, however, that ladder DPP circuits are attractive if load variance is limited. A C_V value of 0.1, for instance, supports a large value of N before β exceeds unity. Figs. 9–11 and Tables I and II reveal that ac-coupled DPP solutions stand out from others explored here, although SC solutions are equally good if the FSL applies.

V. DPP Performance With Load Correlation

Load (or source) power correlation is common in DPP applications, such as when managing partial shading in a solar panel array, thermal hot spots in a series battery pack, or task distribution algorithms for a hard-disk storage cluster. In this section, the i.i.d. condition is relaxed to generalize the stochastic loss analysis. Each load power $P_{ij}(t)$ is given the same distribution but the values are not independent. Detailed derivations are provided in Appendix I.

As shown in Fig. 12, load correlation can happen between loads across different voltage domains (*vertical correlation*) or between loads within one voltage domain (*horizontal correlation*). These can be described using correlation matrices as in Fig. 13. Fig. 13(a) is the vertical correlation matrix $\boldsymbol{\rho}_V$, in which each entry $\rho_V(i,j)$ represents the correlation coefficient between the ith domain power $P_i(t)$ and jth domain power $P_j(t)$. Fig. 13(b) shows the horizontal correlation matrix $\boldsymbol{\rho}_{Hk}$ of the kth voltage domain, in which $\boldsymbol{\rho}_{Hk}(i,j)$ is the correlation coefficient of the ith load power $P_{ki}(t)$ and jth load power $P_{kj}(t)$ within the kth domain. These are Pearson's correlation coefficients [40]: $\rho = \mathrm{Cov}[X,Y]/\sqrt{\mathrm{Var}[X]\mathrm{Var}[Y]} \in [-1,1]$, where X and Y are two random variables. The expected power loss of a fully coupled DPP converter when considering load correlation is

$$\mathbb{E}[P_{loss}(t)] = \frac{R_{out}}{NV_0^2}\Bigg(\underbrace{(N-1)\sum_{k=1}^{N}\mathrm{Var}[P_k(t)]}_{①} \\ \underbrace{-\,2\sum_{1\leq i<j\leq N}\mathrm{Cov}[P_i(t),P_j(t)]}_{②}\Bigg). \quad (14)$$

In part ① of (14), the variance of each domain power, $\mathrm{Var}[P_k(t)]$, can be expanded as

$$\mathrm{Var}[P_k(t)] = \sum_{i=1}^{M}\mathrm{Var}[P_{ki}(t)] + 2\sum_{1\leq i<j\leq M}\mathrm{Cov}[P_{ki}(t),P_{kj}(t)] \\ = \Bigg(M + 2\sum_{1\leq i<j\leq M}\rho_{Hk}(i,j)\Bigg)\underbrace{\mathrm{Var}[P_{ij}(t)]}_{=\sigma_0^2}. \quad (15)$$

In part ②, the covariance between arbitrary two domain powers, $\mathrm{Cov}[P_i(t),P_j(t)]$, can be expressed as

$$\mathrm{Cov}[P_i(t),P_j(t)] = \rho_V(i,j)\sqrt{\mathrm{Var}[P_i(t)]\mathrm{Var}[P_j(t)]}. \quad (16)$$

Equations (14)–(16) indicate that positive vertical correlation $\rho_V(i,j) > 0$ reduces the total expected power loss, whereas positive horizontal correlation $\rho_{Hk}(i,j) > 0$ increases the total expected power loss.

The worst-case horizontal load correlation is to have $\rho_{Hk}(i,j) = 1$ for two arbitrary loads within the k^{th} voltage domain, i.e., two arbitrary loads are linearly related and change exactly in the same direction. In this case, the kth domain power variance reaches a maximum of $\mathrm{Var}[P_k(t)] = M^2\sigma_0^2$, and that domain can be treated as a single load.

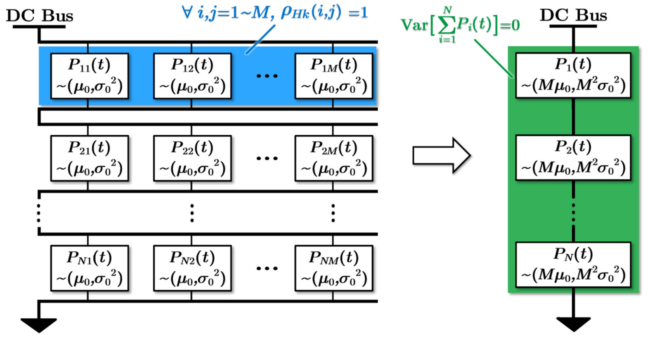


Fig. 14. Power loss of a fully coupled DPP converter reaches its maximum with worst case load correlation, where $\rho_{Hk}(i,j) = 1$ for all loads within a voltage domain, and $\mathrm{Var}[\sum_{k=1}^{N} P_k(t)] = 0$.

The worst-case vertical correlation can be analyzed by reorganizing (14) as

$$\mathbb{E}[P_{loss}(t)] = \frac{R_{out}}{V_0^2}\left(\sum_{k=1}^{N}\mathrm{Var}[P_k(t)] - \frac{\mathrm{Var}\left[\sum_{k=1}^{N} P_k(t)\right]}{N}\right). \quad (17)$$

The worst-case vertical correlation is when $\mathrm{Var}[\sum_{k=1}^{N} P_k(t)] = 0$, i.e., the total power across all voltage domains is constant.

With both worst-case horizontal and vertical correlation, an $N \times M$ DPP system becomes equivalent to a system in which each voltage domain contains a single load with mean power $M\mu_0$ and power variance $M^2\sigma_0^2$, and the system load power $\sum_{k=1}^{N} P_k(t)$ is constant, as depicted in Fig. 14. In this case, the expected loss of a fully coupled DPP converter is

$$\mathbb{E}[P_{loss}(t)] = M^2 N\sigma_0^2 \times \frac{R_{out}}{V_0^2} \Rightarrow \underbrace{\mathcal{S}(M^2 N\sigma_0^2)}_{scaling\,factor}. \quad (18)$$

Worst-case horizontal correlation results in the expected loss scaling quadratically with M. Worst-case vertical correlation increases the domain scaling rate from $N-1$ to N. Based on (18), comparing an ac-coupled DPP to the reference converter under worst-case load correlation, the upper limit of β is $\frac{C_V^2}{4}$. In practice, C_V is usually less than one, and an ac-coupled DPP converter can reduce the expected loss by at least a factor of four even with arbitrary load correlation. When C_V is lower, the benefits are substantial.

VI. Experimental Verification

To validate the stochastic model, a 30×20 LED array was built and tested as a large-scale DPP system with probabilistic load distribution. Random load tasks (independent or correlated) were set up and assigned to the LED array, which is supported by an ac fully coupled DPP converter. Measured average DPP power loss was compared to the expected conduction power loss predicted by the model to validate scaling factors. The analytical framework developed in this article is applicable to a range of DPP applications. An extended application study and model verification on a data storage server powered by DPP are provided in Appendix II.

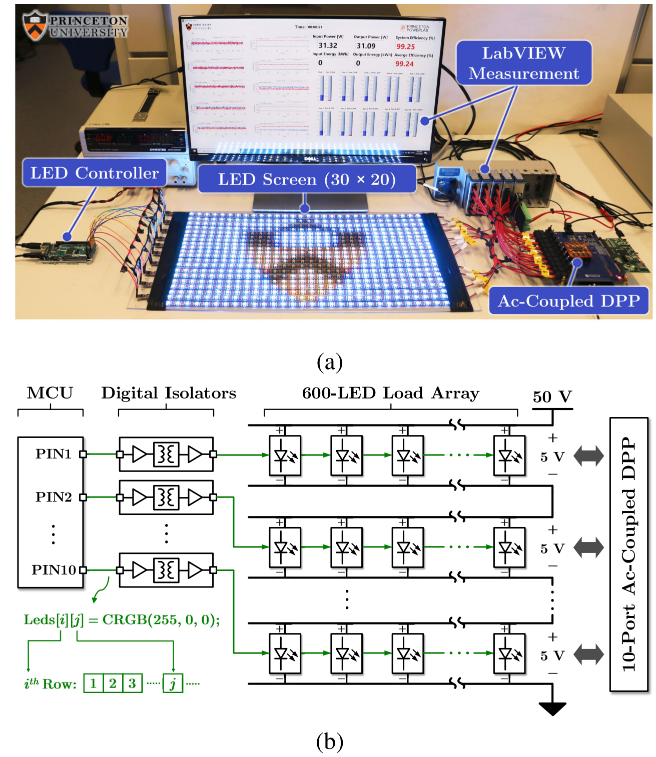


Fig. 15. (a) Experimental test bench with a 30×20 LED array. (b) Power and signal configuration. 600 LEDs are divided into 10 series-stacked voltage domains and supported by a 10-port ac-coupled DPP converter. Each LED is individually addressable from the MCU controller.

Recall that the stochastic model captures conduction losses, expected to dominate scale-dependent DPP system losses. Switching loss, core loss, and control and auxiliary losses could be weakly load dependent, so the key validation challenge is to determine whether total losses measured in experiments show the same scaling effects as conduction losses in the model.

A. Experimental Setup

Fig. 15 shows an overview of the test bench. The 30×20 LEDs were divided into ten voltage domains, connected in series to a 50 V dc bus. Each voltage domain supplied 5 V to 60 LEDs, and the full load power of the 600-LED screen is 108 W. Differential power of the ten domains was processed by a ten-port ac-coupled DPP circuit [21]. All 60 LEDs in each voltage domain were controlled by a serial signal path connected to a digital pin on the microcontroller (Arduino Mega) through a digital isolator (ADuM1200). Each LED was controlled individually by the microcontroller. A LabVIEW measurement system (cDAQ-9178 & NI9221 & NI9227) monitored and recorded total input power, load power of each voltage domain, and average power loss of the DPP system, in real time.

Fig. 16(a) shows the DPP prototype. A ten-winding printed-circuit-board (PCB) transformer in the center is surrounded by ten half-bridge ports. Each port couples one voltage domain to the transformer, and has the same R_{out} as that of a full-bridge

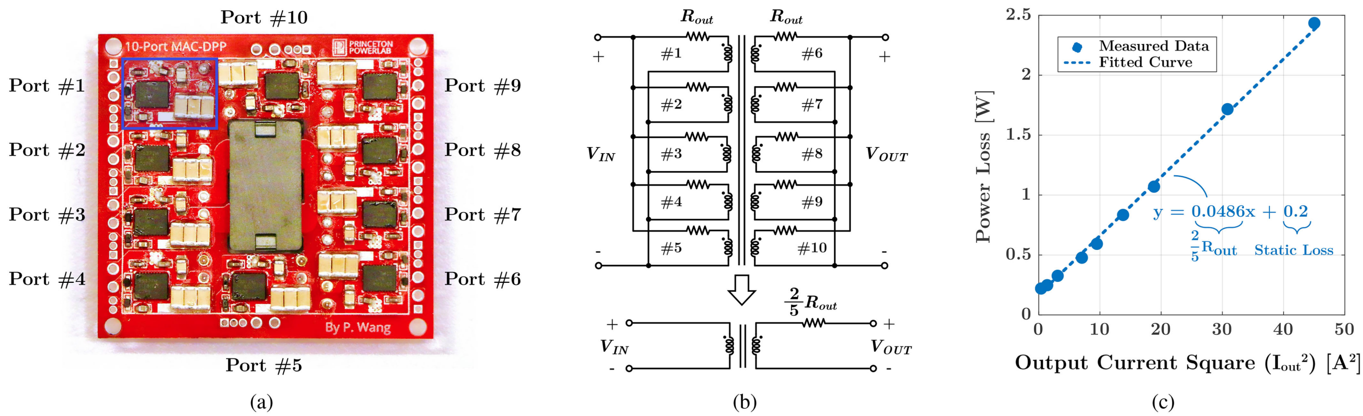


Fig. 16. (a) Prototype of a 10-port ac-coupled DPP. (b) Equivalent circuits of the ac-coupled DPP prototype when delivering power from 5 ports to 5 ports ($V_{IN} = V_{OUT} = 5\,\mathrm{V}$). (c) Measured power loss versus the square of output current for 5-port-to-5-port power delivery. This measurement is performed on common ground without sampling resistors, etc., so the 485 mW control and auxiliary losses are not captured in static loss here.

TABLE IV
KEY COMPONENT VALUES OF THE AC-COUPLED DPP PROTOTYPE

Half-Bridge Switch	Transformer Core	External Series Inductor	Blocking Capacitor
TI - DrMOS CSD95377Q4M	Ferroxcube ELP18-3C95	Coilcraft SLC7649S, 100 nH	Murata X5R 100 μF $\times$ 3

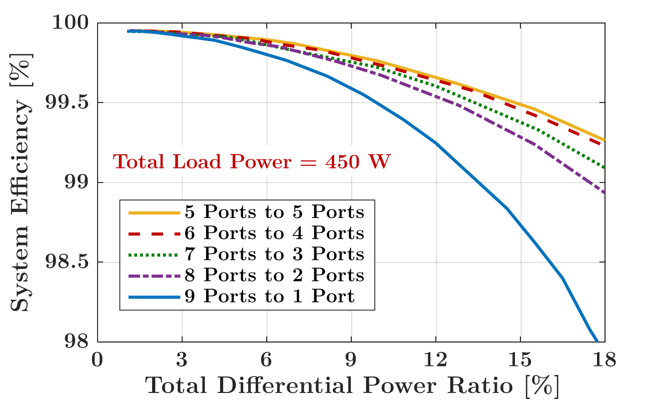


Fig. 17. System efficiency versus total processed differential power ratio (i.e., $\frac{\Sigma|\Delta P_i|}{\text{Total System Power}}$) when supporting 450 W load (i.e., rated system power of the DPP prototype) in various differential power delivery scenarios (e.g., *9 Ports to 1 Port* indicates the differential power is delivered from 9 voltage domains to 1 domain). The 485 mW control and auxiliary losses are not included in the system losses here.

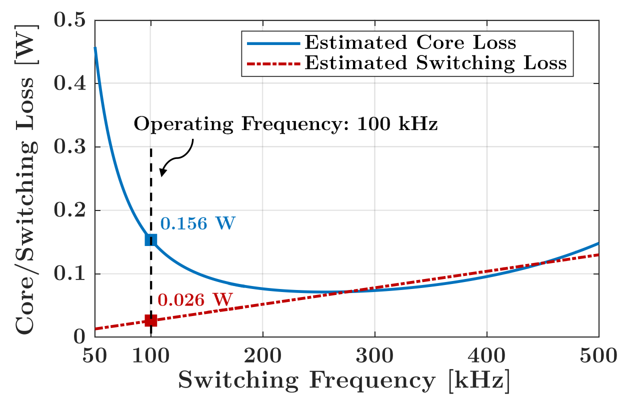


Fig. 18. Estimated magnetic core loss and switching loss as a function of the switching frequency.

implementation given the same switch die area and magnetic size. The prototype measures 4 cm $\times$ 3.5 cm $\times$ 0.76 cm, switches at 100 kHz, and supports up to 450 W system power with a power density of 700 W/in^3. Key component values are listed in Table IV. System efficiency when supporting 450 W load for various operating conditions is plotted in Fig. 17. More details about the prototype can be found in [21].

R_{out} of each port was measured with a five-port-to-five-port power delivery test in which five ports are connected in parallel as the input and five other ports are in parallel as the output. Fig. 16(b) depicts the equivalent circuit of this test. In this case, the DPP prototype is equivalent to a dc–dc converter with an output resistance of $\frac{2}{5}R_{out}$. The measured power loss versus I_{out}^2 is plotted in Fig. 16(c). Measured data are fitted with a line. The slope is the output resistance $\frac{2}{5}R_{out}$ and the intercept comprises switching loss and magnetic core loss. The R_{out} value is estimated as $0.12\,\Omega$.

Fig. 18 shows estimated core loss and switching loss as a function of switching frequency. When switching at 100 kHz, the estimated core loss is 156 mW, the switching loss is 26 mW and the sum is 182 mW. The current meter (NI-9227) was calibrated with an Agilent 34401A digital multimeter. Its tolerance is ± 1 mA on a 5 A scale, translating into 50 mW of power measurement tolerance on the full 50 V stack, or 5 mW for each 5 V port. Control and auxiliary losses (including level shifters, resistive dividers, etc.) were measured with inactive switches, and totalled 485 ± 50 mW. Gate drives were powered from a separate source (which also powers the microcontroller and other auxiliary circuits). Thus, estimated loss above and beyond conduction loss totals 667 ± 50 mW.

This difference is observed in all measurements. As will be noted below, it is load independent and has minimal impact on scaling. Since the article is not seeking to design an extreme-performance DPP implementation and it is vital to have

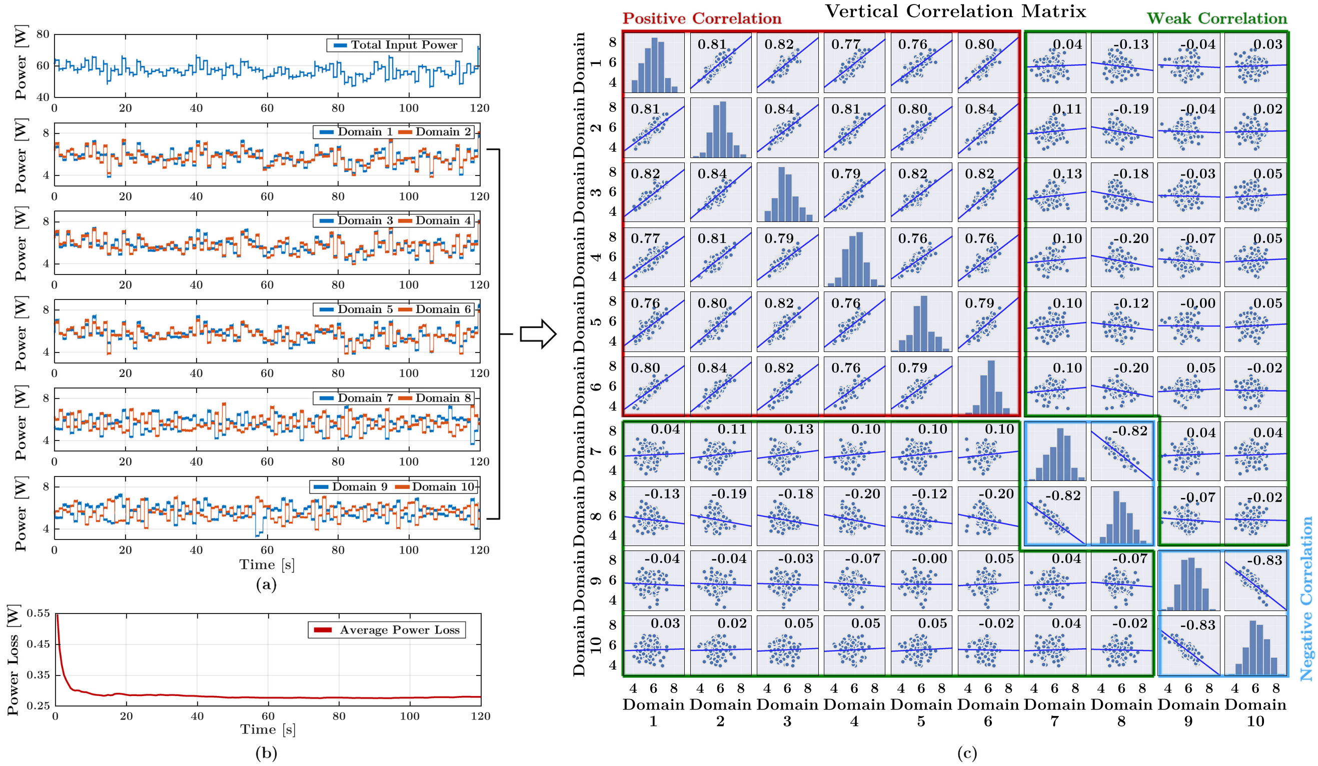


Fig. 19. (a) Measured total system input power and each domain load power in LabVIEW. (b) Measured average power loss of the DPP system in LabVIEW. (c) Vertical correlation matrix based on sampled data (2 min) of each domain power. Diagonal histograms plot the distribution of each domain power. Nondiagonal scatter plots depict power correlation between each pair of domains and the correlation coefficients.

extensive real-time measurements, control overhead power is not optimized in the design and might be higher than in a commercial implementation. An alternative way to verify the loss analysis is to develop a thermal model for the system and use thermal images and calorimetric methods to differentiate the static loss and loss scaling.

In the random load experiment, power to each LED is controlled by a random variable ξ that follows a Bernoulli distribution, $\mathrm{Bernoulli}(p)$. Here, p is the probability of turning on the LED. The load power of each LED therefore follows $P_{ij} = \xi P_{on}$, where $P_{on} = 0.18\,\mathrm{W}$ is the power consumption of one LED at full brightness, and the value of $\xi \in \{0, 1\}$ is updated once per second. By changing the turn-ON probability p, the number of active loads per voltage domain M, and the vertical and horizontal load correlations, various random load tasks can be set up on the LED screen.

Fig. 19 illustrates the method for comparing measured average power loss to expected power loss from the stochastic model. Fig. 19(a) shows the instantaneous input system power and domain power measured by LabVIEW when performing a particular random load task. Measured average power loss over time is displayed in Fig. 19(b). For each random load task in the experiments, the full system is operated long enough for measured average power loss to converge (typically 10 min).

The expected power loss is obtained from statistics of the sampled domain power waveforms. As shown in Fig. 19(c),

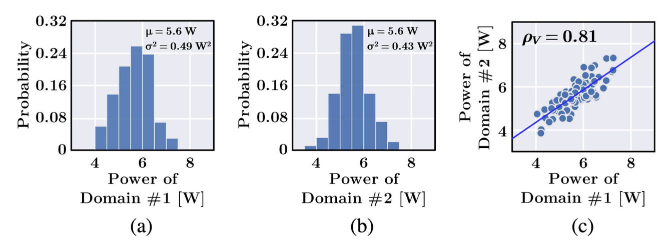
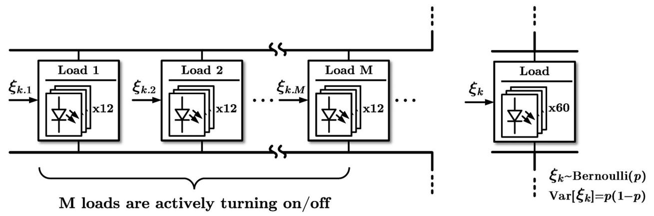


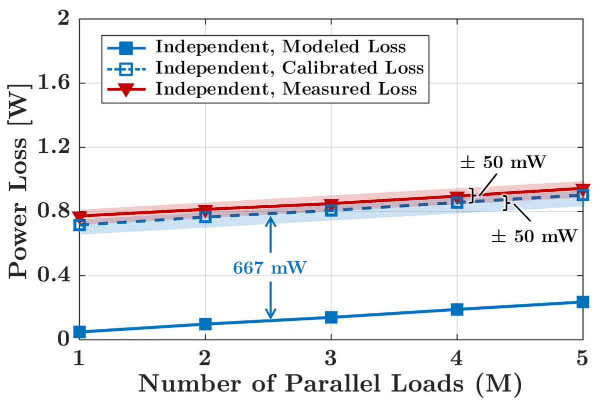
Fig. 20. Example zooms from Fig. 19(c). (a) Diagonal histogram of domain #1. (b) Diagonal histogram of domain #2. (c) Nondiagonal scatter plot of domain #1 power and domain #2 power.

measured power waveforms of all voltage domains are sampled every second and plotted in the vertical correlation matrix. Fig. 20 zooms in on three example diagonal and nondiagonal entries in Fig. 19(c). The diagonal entries [such as Figs. 20(a) and (b)] are histograms of domain powers $P_1(t)$ through $P_{10}(t)$. The variance of each domain power, $\mathrm{Var}[P_k(t)]$ in part 1 of (14), can be obtained from the histograms. Horizontal correlation within a voltage domain is also reflected in the probability distribution of each diagonal histogram. The nondiagonal scatter plots [such as Fig. 20(c)] describe vertical correlation coefficients between any two domain powers. For scatter plots in Fig. 19(c), red boxes show positive correlation, blue boxes show negative correlation, and green boxes show weak correlation. $\mathrm{Cov}[P_i(t), P_j(t)]$ in part 2 can be obtained from correlation coefficients of nondiagonal scatter plots. The statistical information provided in Fig. 19(c) can be

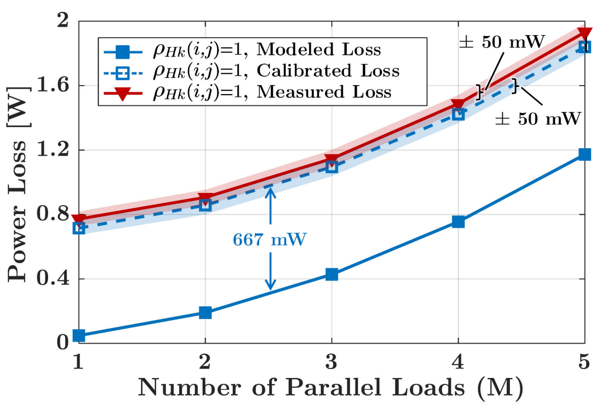


(a) (b)

Fig. 21. Experimental setup to validate the model as (a) M increases and (b) σ_0^2 increases.



(a)



(b)

Fig. 22. Comparison between expected power loss and measured average loss as M increases in the case of (a) independent load. (b) Worst-case horizontal load correlation. The calibrated loss is the sum of modeled loss and estimated 667 mW overhead.

used in the model to predict the expected power loss of a DPP system based on (14).

B. Power Loss Scaling With M and σ_0^2

To validate stochastic model scaling with M and σ_0^2, we perform two experiments as shown in Fig. 21. Vertical correlation is not considered in this subsection.

In the M scaling experiment [see Fig. 21(a)], sets of 12 LEDs in each voltage domain are bundled as one load and controlled by one random variable. The turn-ON probability of each load is fixed at 0.5. By controlling the number of active loads (nonactive loads are kept OFF), M can be adjusted from 1 to 5. Fig. 22

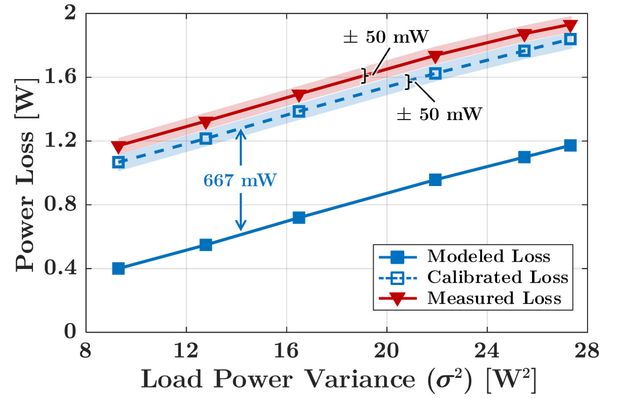


Fig. 23. Comparison between expected power loss and measured average loss when σ_0^2 increases. The calibrated loss is the sum of modeled loss and the estimated 667 mW overhead.

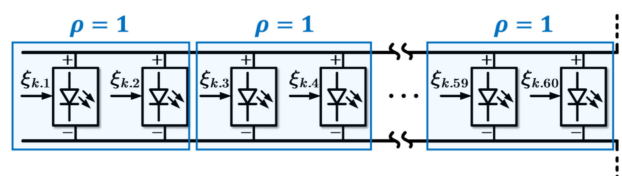


Fig. 24. Experimental setup for horizontal correlation. Here each horizontally correlated group contains two correlated LEDs with $\rho = 1$.

compares measured average loss and expected loss with and without horizontal correlation as M increases. The figure shows the conduction loss from the model, the modeled loss plus the estimated 667 mW overhead (shown as *calibrated loss*), and the total measured loss. The results confirm that average power loss of this ac-coupled DPP circuit scales linearly with M when loads are independent, but scales quadratically with M with worst-case horizontal correlation, as predicted by (8) and (18). The tracking match is as tight as the power measurement tolerance supports, with error bounds ($\pm$50 mW) highlighted.

To test σ_0^2 scaling, all 60 LEDs in each voltage domain are bundled as one load as shown in Fig. 21(b), and the load power variance is adjusted by changing the turn-ON probability p. Fig. 23 compares the measured average loss and expected loss as a function of σ_0^2. The figure shows the conduction loss from the model, the calibrated loss with added 667 mW overhead, and the measured total loss. The average loss of this ac-coupled DPP circuit increases linearly with load variance σ_0^2, consistent with the scaling factor in (8). The tracking match is as tight as power measurement tolerance supports.

C. Impact of Load Correlation

Fig. 24 shows the setup to test horizontal correlation. In the experiment, each LED is controlled individually with $p = 0.5$. Positive horizontal correlation is created by dividing 60 LEDs in a voltage domain equally into horizontally correlated groups in which $\rho = 1$ for LEDs within a group. Fig. 24 shows an example in which each horizontal group contains two LEDs. By increasing the number of LEDs in a horizontal group, a stronger positive horizontal correlation is created.

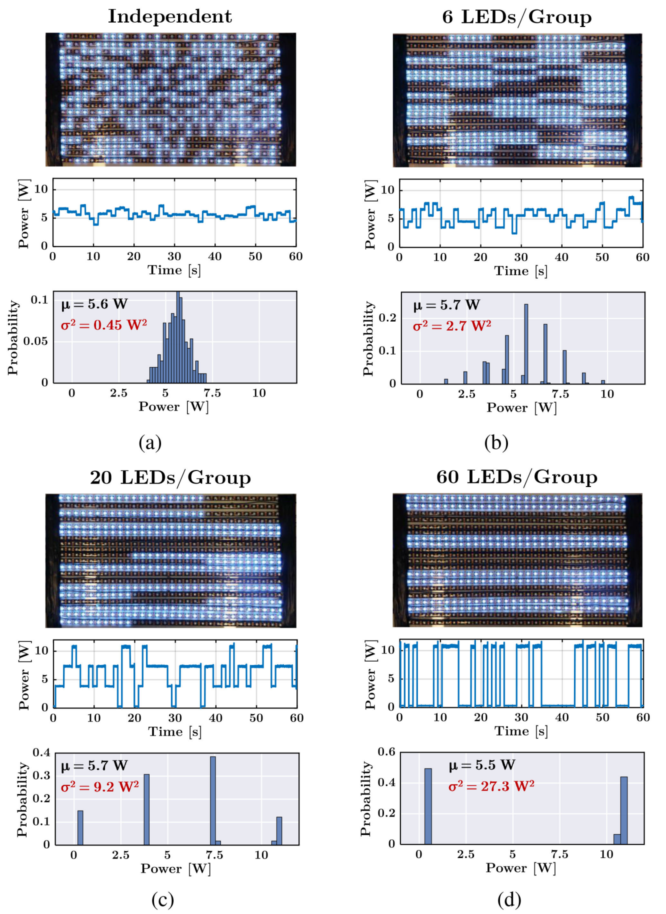


Fig. 25. LED screen pattern, power waveform and the probability histogram of domain #1 when 60 LEDs of each voltage domain are (a) independent, (b) horizontally grouped with 6 LEDs/group, (c) horizontally grouped with 20 LEDs/group, and (d) horizontally grouped with 60 LEDs/group.

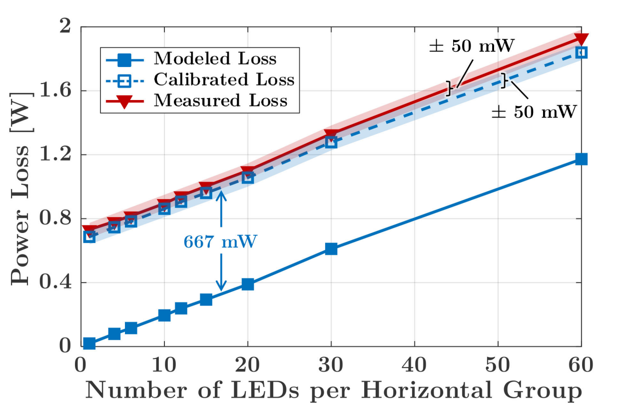


Fig. 26. Comparison between expected power loss and measured average loss as the number of LEDs per horizontal group increases. A larger number of LEDs per group represents a stronger positive horizontal correlation. The calibrated loss is the sum of modeled loss and estimated 667 mW overhead.

Figs. 25 and 26 show experimental results for horizontal correlation. Fig. 25 shows four cases of horizontal correlation as LEDs of each voltage domain shift from independent to fully correlated. The number of correlated LEDs per group increases from zero (i.e., independent), to six LEDs, 20 LEDs, and then 60

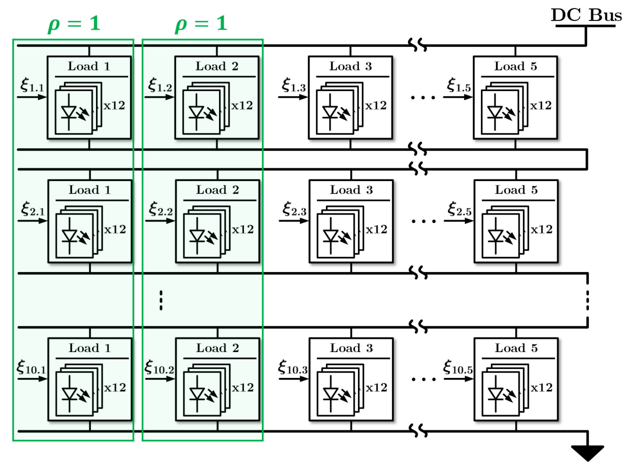


Fig. 27. Experimental setup for vertical load correlation. Here is an example in which two vertically correlated groups are set up. In each vertical correlated group, $\rho = 1$ for any two loads within the group.

LEDs per group. When all LEDs are independent, the domain power consumption has a single smooth peak in its histogram that follows a binomial distribution, and variance is small. When LEDs are horizontally correlated and the number of LEDs per correlated group increases, multiple split peaks appear in the histogram, with a higher power variance, as indicated by the power waveforms and probability histograms of domain #1. Fig. 26 compares the measured average loss to the expected loss and the calibrated loss with 667 mW overhead as the number of LEDs per horizontal group increases. The tracking match to the model is as tight as the power measurement tolerance supports. Figs. 25 and 26 confirm that positive horizontal correlation increases power variance, and thus the system needs to process more power and generates more loss. More positive horizontal correlation leads to higher DPP system loss, consistent with conclusions in Section V.

To test vertical load correlation, sets of 12 LEDs in a voltage domain are bundled as one load and controlled with $p = 0.5$. Each domain contains five loads in total. As shown in Fig. 27, vertical correlation is created by grouping one load from each voltage domain, with $\rho = 1$ for loads within a vertical group. Fig. 27 demonstrates an example with two vertically correlated groups. By increasing the number of correlated groups, stronger positive vertical correlation can be generated. In this case, loads in each domain are controlled by five independent random variables, i.e., loads are vertically correlated but horizontally independent. Therefore, the distribution and variance of each domain power (part 1 of (14)) remain unchanged. DPP power loss variation in this experiment is only related to vertical load correlation (part 2 of (14)).

Figs. 28 and 29 show experimental results for vertical correlation. Fig. 28 plots the power distribution histogram of domain #1 and power correlation between domains #1 and #2 (domain #1 and #2 are shown as an example here). As the number of vertically correlated groups increases, positive load correlation across voltage domains becomes stronger and ρ_V increases from 0 to 1. During this process, the power distribution histogram of

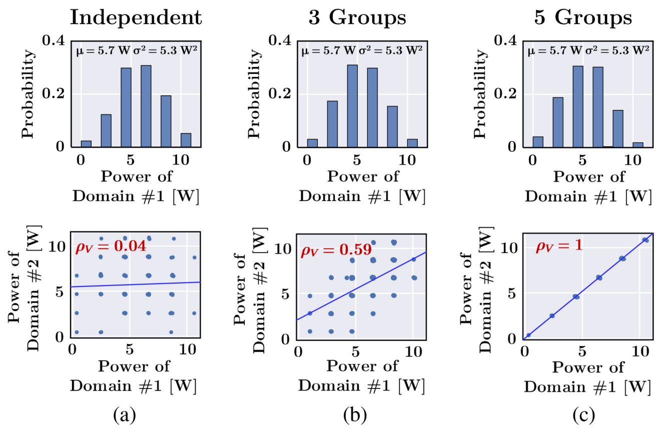


Fig. 28. Power distribution histogram of domain #1 and power correlation graph between domains #1 and #2 when the number of vertically correlated groups is (a) zero (independent), (b) three, (c) five (fully correlated).

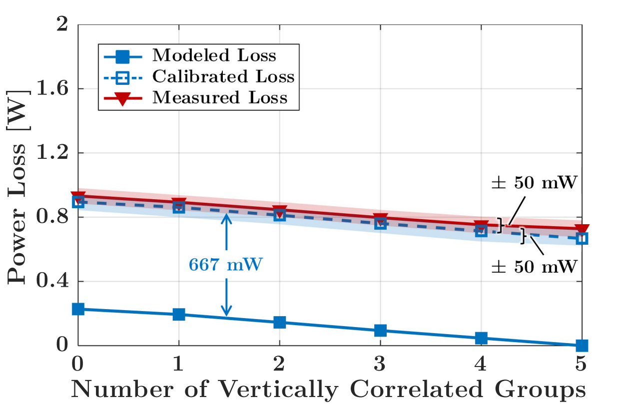


Fig. 29. Comparison between expected power loss and measured average loss as the number of vertically correlated groups increases. A larger number of correlated groups represents a stronger positive vertical correlation. The calibrated loss is the sum of modeled loss and estimated 667 mW overhead.

each voltage domain changes little, as expected. The measured average loss, calibrated loss with 667 mW overhead, and expected loss are compared in Fig. 29. The average loss of a fully coupled DPP system decreases when ρ_V increases, validating the conclusions in Section V. Again, the tracking match is as tight as the power measurement tolerance supports, and error bounds are highlighted.

VII. Conclusion

This article explores scaling of DPP systems by means of stochastic models. An analytical framework is developed to estimate average power loss of a DPP topology under probabilistic load distributions. Scaling factors are introduced to describe how power loss scales as the dimension (N, M), average load power (μ_0), and load power variance (σ_0^2) of a modular load array change. The scaling characteristics of general DPP topologies were analyzed and compared, providing useful design guidelines for selecting DPP topologies. The analytical framework was verified by SPICE simulations and experimental results. The results show that many DPP topologies reduce power loss substantially even with power coefficients of variance as high as 1, with greater benefits as variance decreases. The results also indicate that in a DPP system with relatively balanced load, power loss caused by differential power processing will be low. Switching loss, core loss, and other static losses may be significant. The analytical framework, scaling factors, and stochastic models provide useful guidelines for designing large-scale DPP systems.

Appendix I
Derivations of the Expected Power Loss

This appendix derives expected power loss for the stochastic model under conditions of independent loads and of correlated loads. Definitions and constraints are the same as those introduced in Sections II and V.

A. Expected Power Loss With Independent Load

In Section II, the stochastic model is developed based on *independent and identically distributed* (i.i.d.) individual load powers $P_{ij}(t)$. With this condition, the domain powers $P_i(t)$ are also i.i.d..

For the conventional reference converter, loss is related to total load power, and the expected value in (5) can be derived as

$$\begin{aligned}\mathbb{E}[P_{loss}(t)] &= \frac{R_{out}}{V_0^2}\mathbb{E}\left[\left(\sum_{i=1}^{N} P_i(t)\right)^2\right]\\ &= \frac{R_{out}}{V_0^2}\left\{\sum_{i=1}^{N}\mathbb{E}[P_i^2(t)] + 2\sum_{1\le i<j\le N}\mathbb{E}[P_i(t)P_j(t)]\right\}\\ &\overset{\text{(i)}}{=} \frac{R_{out}}{V_0^2}\left(N\mathbb{E}[P_i^2(t)] + N(N-1)\mathbb{E}^2[P_i(t)]\right).\end{aligned} \tag{19}$$

Here, line (i) follows because P_i values are i.i.d.. Therefore, $\mathbb{E}[P_i(t)]$ and $\mathbb{E}[P_i^2(t)]$ are identical for $i = 1, \ldots, N$, and $\mathbb{E}[P_i(t)P_j(t)] = \mathbb{E}^2[P_i(t)]$ for any $i \neq j$. Considering $P_i(t) = P_{i1}(t) + \cdots + P_{iM}(t)$, where $P_{i1}(t), \ldots, P_{iM}(t)$ are also i.i.d., $\mathbb{E}[P_i^2(t)]$ and $\mathbb{E}^2[P_i(t)]$ in (19) can be expanded to

$$\begin{aligned}\mathbb{E}[P_i^2(t)] &= M\mathbb{E}[P_{ij}^2(t)] + M(M-1)\mathbb{E}^2[P_{ij}(t)]\\ \mathbb{E}^2[P_i(t)] &= (M\mathbb{E}[P_{ij}(t)])^2 = M^2\mathbb{E}^2[P_{ij}(t)].\end{aligned} \tag{20}$$

Substituting (20) into (19), the expected power loss is

$$\begin{aligned}\mathbb{E}[P_{loss}(t)] &= \frac{R_{out}}{V_0^2}\Big\{MN\left(\mathbb{E}[P_{ij}^2(t)] - \mathbb{E}^2[P_{ij}(t)]\right)\\ &\qquad + M^2N^2\mathbb{E}^2[P_{ij}(t)]\Big\}\\ &\overset{\text{(i)}}{=} \frac{R_{out}}{V_0^2}\Big(MN\underbrace{\mathrm{Var}[P_{ij}(t)]}_{=\sigma_0^2} + M^2N^2\underbrace{\mathbb{E}^2[P_{ij}(t)]}_{\mu_0^2}\Big).\end{aligned} \tag{21}$$

Line (i) is based on $\mathrm{Var}[X] = \mathbb{E}[X^2] - \mathbb{E}^2[X]$.

To calculate expected loss of DPP converters, $P_i'(t) = P_i(t) - \mathbb{E}[P_i(t)]$ is defined to subtract out the mean value $M\mu_0$ of $P_i(t)$, so that $\mathbb{E}[P_i'(t)] = 0$. The i.i.d. property still holds for $P'_i(t)$. For a fully-coupled DPP with this loading condition, instantaneous power loss at each port has the same probability distribution. The expected power loss at the ith port can be derived from (6) as

$$\begin{aligned}
\mathbb{E}[P_{loss.i}(t)] &\overset{\text{(i)}}{=} \frac{R_{out}}{V_0^2}\mathbb{E}\left[\left(\frac{\sum_{k=1}^{N} P'_k(t)}{N} - P'_i(t)\right)^2\right] \\
&= \frac{R_{out}}{V_0^2}\mathbb{E}\left[\left(\sum_{k\neq i}\frac{1}{N}P'_k(t) + \frac{1-N}{N}P'_i(t)\right)^2\right] \\
&\overset{\text{(ii)}}{=} \frac{R_{out}}{V_0^2}\left\{\sum_{k\neq i}\frac{1}{N^2}\mathbb{E}[P_k'^2(t)] + \frac{(1-N)^2}{N^2}\mathbb{E}[P_i'^2(t)]\right\} \\
&\overset{\text{(iii)}}{=} \frac{R_{out}}{V_0^2}\frac{N-1}{N}\mathbb{E}[P_i'^2(t)] \\
&\overset{\text{(iv)}}{=} \frac{R_{out}}{V_0^2}\frac{N-1}{N}\left(\mathbb{E}[P_i^2(t)] - \mathbb{E}^2[P_i(t)]\right) \\
&= \frac{R_{out}}{V_0^2}\frac{N-1}{N}\mathrm{Var}[P_i(t)] \\
&\overset{\text{(v)}}{=} \frac{R_{out}}{V_0^2}\frac{M(N-1)}{N}\underbrace{\mathrm{Var}[P_{ij}(t)]}_{=\sigma_0^2}.
\end{aligned} \tag{22}$$

Here, lines (i) and (iv) change the variables between $P_i(t)$ and $P'_i(t)$; (ii) follows because $P'_1(t),\ldots,P'_N(t)$ are independent with zero mean, and hence $\mathbb{E}[P'_i(t)P'_j(t)] = 0$ for any $i \neq j$; (iii) follows because $P'_i(t)$ values are identically distributed, and hence $\mathbb{E}[P_i'^2(t)]$ is the same for all i; (v) follows because all $P_{ij}(t)$ values are i.i.d., and hence $\mathrm{Var}[P_i(t)] = \mathrm{Var}[P_{i1}(t) + \cdots + P_{iM}(t)] = M\mathrm{Var}[P_{ij}(t)]$.

In a ladder DPP, power loss varies among submodules. Similar to (22), the expected power loss at the ith submodule can be calculated from (9) as

$$\begin{aligned}
\mathbb{E}[P_{loss.i}(t)] &= \frac{R_{out}}{V_0^2}\mathbb{E}\left[\left(i\overline{P}'(t) - \sum_{k=1}^{i}P'_k(t)\right)^2\right] \\
&= \frac{R_{out}}{V_0^2}\mathbb{E}\left[\left(\sum_{k=1}^{i}\left(\frac{i}{N}-1\right)P'_k(t) + \sum_{k=i+1}^{N}\frac{i}{N}P'_k(t)\right)^2\right] \\
&= \frac{R_{out}}{V_0^2}\left\{\sum_{k=1}^{i}\left(\frac{i}{N}-1\right)^2\mathbb{E}[P_k'^2(t)] + \sum_{k=i+1}^{N}\frac{i^2}{N^2}\mathbb{E}[P_k'^2(t)]\right\} \\
&= \frac{R_{out}}{V_0^2}\frac{(N-i)i}{N}\mathbb{E}[P_k'^2(t)] \\
&= \frac{R_{out}}{V_0^2}\frac{M(N-i)i}{N}\underbrace{\mathrm{Var}[P_{ij}(t)]}_{=\sigma_0^2}.
\end{aligned} \tag{23}$$

B. Expected Power Loss With Correlated Load

In Section V, load correlation is considered to generalize the stochastic loss model. The i.i.d. condition is relaxed so that each load power has identical probability distribution but is not necessarily independent. In this case, $\mathbb{E}[P_{ij}(t)]$ and $\mathrm{Var}[P_{ij}(t)]$ are still identical for each load; $\mathbb{E}[P_i(t)] = M\mu_0$ is identical for each domain, but $\mathrm{Var}[P_i(t)] = M\sigma_0^2 + 2\sum_{k\neq l}\mathrm{Cov}[P_{ik}(t), P_{il}(t)]$ might vary among domains due to load correlation. In this case, expected total power loss of a fully coupled DPP in (14) can be derived as

$$\begin{aligned}
\mathbb{E}[P_{loss}(t)] &= \frac{R_{out}}{V_0^2}\mathbb{E}\left[\sum_{k=1}^{N}\left(\overline{P}(t) - P_k(t)\right)^2\right] \\
&= \frac{R_{out}}{V_0^2}\mathbb{E}\left[\frac{1}{N}\left((N-1)\sum_{k=1}^{N}P_k^2(t) - 2\sum_{1\le i<j\le N}P_i(t)P_j(t)\right)\right] \\
&= \frac{R_{out}}{NV_0^2}\left\{(N-1)\sum_{k=1}^{N}\mathbb{E}[P_k^2(t)] - 2\sum_{1\le i<j\le N}\mathbb{E}[P_i(t)P_j(t)]\right\} \\
&\overset{\text{(i)}}{=} \frac{R_{out}}{NV_0^2}\left\{(N-1)\sum_{k=1}^{N}\left(\mathbb{E}[P_k^2(t)] - \mathbb{E}^2[P_k(t)]\right)\right. \\
&\qquad\left. - 2\sum_{1\le i<j\le N}\mathrm{Cov}[P_i(t), P_j(t)]\right\} \\
&= \frac{R_{out}}{NV_0^2}\left\{(N-1)\sum_{k=1}^{N}\mathrm{Var}[P_k(t)]\right. \\
&\qquad\left. - 2\sum_{1\le i<j\le N}\mathrm{Cov}[P_i(t), P_j(t)]\right\}.
\end{aligned} \tag{24}$$

Line (i) follows because $\mathbb{E}[P_i(t)P_j(t)] = \mathbb{E}[P_i(t)] \times \mathbb{E}[P_j(t)] + \mathrm{Cov}[P_i(t), P_j(t)]$, and $\mathbb{E}[P_i(t)]$ are identical for $i = 1,\ldots,N$. Equation (17) can be obtained by rearranging (24) as

$$\begin{aligned}
\mathbb{E}[P_{loss}(t)] &= \frac{R_{out}}{NV_0^2}\left\{N\sum_{k=1}^{N}\mathrm{Var}[P_k(t)]\right. \\
&\qquad\left. - \left(\sum_{k=1}^{N}\mathrm{Var}[P_k(t)] + 2\sum_{1\le i<j\le N}\mathrm{Cov}[P_i(t), P_j(t)]\right)\right\} \\
&\overset{\text{(i)}}{=} \frac{R_{out}}{V_0^2}\left\{\sum_{k=1}^{N}\mathrm{Var}[P_k(t)] - \frac{\mathrm{Var}\left[\sum_{k=1}^{N}P_k(t)\right]}{N}\right\}.
\end{aligned} \tag{25}$$

Here, (i) holds because $\mathrm{Var}[X_1 + X_2 \ldots + X_N] = \sum_{k=1}^{N}\mathrm{Var}[X_k] + 2\sum_{k\neq l}\mathrm{Cov}[X_k, X_l]$.

Appendix II Application Study and Model Verification on a Data Storage Server

To further verify the model in a practical application, we recorded the power profiles of a data storage server (in [21]) and applied them to a SPICE simulation (PLECS v4.5). The data storage server contains ten series voltage domains. Each domain supplies 5 V to multiple parallel hard disk drives (HDDs). A random read/write program was running on the server. Fig. 30 shows

TABLE V
AVERAGE POWER CONSUMPTION AND DPP POWER LOSS OF EACH VOLTAGE DOMAIN AND OF THE TOTAL SYSTEM

Domain	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	Simulated Domain Average	Simulated Total System	Modeled Total System
Average Power [W]	9.10	9.17	9.13	9.21	9.19	9.12	9.10	9.17	9.19	9.19	9.16	91.6	91.6
DPP Power Loss [mW]	2.73	2.62	2.51	2.52	2.67	2.66	2.68	2.53	2.46	2.70	2.61	26.1	24.5

* The system operated for 60 seconds. Conduction losses are considered. Switching loss, core loss, control, and other auxiliary losses are not included.

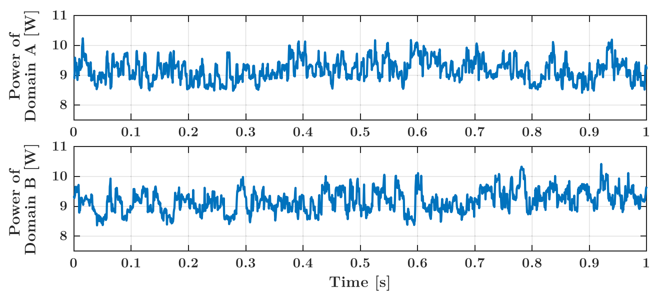


Fig. 30. Power consumption waveforms of two example voltage domains when the data storage server is running a random read/write program.

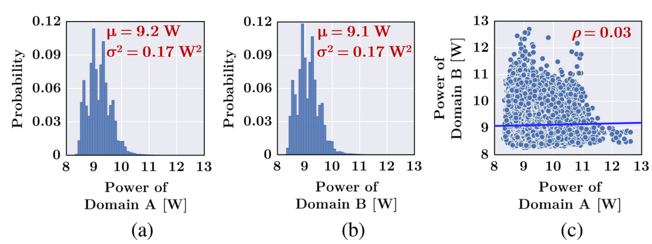


Fig. 31. Probability distribution and correlation of the two example domain powers. (a) Power distribution histogram of domain A. (b) Power distribution of domain B. (c) Correlation plot of domain A power and domain B power.

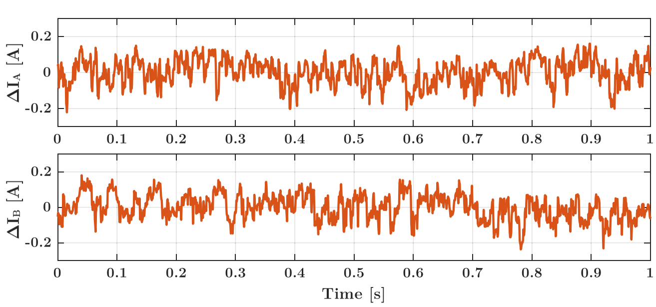


Fig. 32. Differential current (ΔI_i) of the two example voltage domains.

power waveforms of two example voltage domains. Probability distributions of the two domain powers and their correlation are plotted in Fig. 31. Fig. 31 indicates that the measured ten domain powers are i.i.d. Differential current waveforms of the two example voltage domains are plotted in Fig. 32.

In the SPICE simulation, a DPP system with ten series domains was built and supported by an ac fully coupled DPP converter [see Fig. 6(a)]. Here, each domain contains one random load with the recorded domain power profile, so in this system $N = 10, M = 1, V_0 = 5\,\mathrm{V}, \mu_0 = 9.2\,\mathrm{W}$, and $\sigma_0^2 = 0.17\,\mathrm{W}^2$. For the DPP converter, each switch $R_{ds(on)}$ is set as $0.1\,\Omega$ and each winding resistance is set as $0.2\,\Omega$, yielding $R_{out} = 0.4\,\Omega$. Table V lists the average power consumption and DPP power loss of each voltage domain and of the total system. It also compares the modeled system power loss [based on (8)] to the simulated system power loss. As shown in the table, the modeled system loss (24.5 mW) is within 6% of the simulated system loss (26.1 mW), validating the stochastic loss model.

REFERENCES

[1] P. Wang, R. C. N. Pilawa-Podgurski, P. T. Krein, and M. Chen, "Performance limits of differential power processing," in *Proc. IEEE Workshop Control Model. Power Electron.*, Aalborg, Denmark, 2020, pp. 1–8.
[2] G. L. Brainard, "Non-dissipative battery charger equalizer," U.S. Patent 5479083, Dec. 26, 1995.
[3] Y. S. Lee and M. W. Cheng, "Intelligent control battery equalization for series connected lithium-ion battery strings," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1297–1307, Oct. 2005.
[4] C. Pascual and P. T. Krein, "Switched capacitor system for automatic series battery equalization," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1997, pp. 848–854.
[5] Y. Ye, K. W. E. Cheng, Y. C. Fong, X. Xue, and J. Lin, "Topology, modeling, and design of switched-capacitor-based cell balancing systems and their balancing exploration," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4444–4454, Jun. 2017.
[6] H. Schmidt and C. Siedle, "The charge equalizer—a new system to extend battery lifetime in photovoltaic systems, UPS and electric vehicles," in *Proc. IEEE Int. Telecom. Energy Conf.*, 1993, pp. 146–151.
[7] S. T. Hung, D. C. Hopkins, and C. R. Mosling, "Extension of battery life via charge equalization control," *IEEE Trans. Ind. Electron.*, vol. 40, no. 1, pp. 96–104, Feb. 1993.
[8] A. M. Imtiaz and F. H. Khan, "'Time shared flyback converter' based regenerative cell balancing technique for series connected Li-ion battery strings," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5960–5975, Dec. 2013.
[9] N. H. Kutkut, D. M. Divan, and D. W. Novotny, "Charge equalization for series connected battery strings," *IEEE Trans. Ind. Appl.*, vol. 31, no. 3, pp. 562–568, May/Jun. 1995.
[10] S. K. Dam and V. John, "A modular fast cell-to-cell battery voltage equalizer," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9443–9461, Sep. 2020.
[11] M. Evzelman, M. M. Ur Rehman, K. Hathaway, R. Zane, D. Costinett, and D. Maksimovic, "Active balancing system for electric vehicles with incorporated low-voltage bus," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7887–7895, Nov. 2016.
[12] M. Liu, Y. Chen, Y. Elasser, and M. Chen, "Dual frequency hierarchical modular multilayer battery balancer architecture," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3099–3110, Mar. 2021.
[13] T. Shimizu, M. Hirakata, T. Kamezawa, and H. Watanabe, "Generation control circuit for photovoltaic modules," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 293–300, May 2001.
[14] G. R. Walker and J. C. Pierce, "Photovoltaic DC-DC module integrated converter for novel cascaded and bypass grid connection topologies–Design and optimization," in *Proc. IEEE Power Electron. Specialists Conf.*, 2006, pp. 1–7.
[15] C. Olalla, D. Clement, M. Rodriguez, and D. Maksimovic, "Architectures and control of submodule integrated DC-DC converters for photovoltaic applications," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2980–2997, Jun. 2013.

[16] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "Resonant switched-capacitor converters for sub-module distributed photovoltaic power management," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1189–1198, Mar. 2013.
[17] S. Qin, S. T. Cady, A. D. Domínguez-García, and R. C. N. Pilawa-Podgurski, "A distributed approach to maximum power point tracking for photovoltaic submodule differential power processing," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2024–2040, Apr. 2015.
[18] A. H. Chang, A. Avestruz, and S. B. Leeb, "Capacitor-less photovoltaic cell-level power balancing using diffusion charge redistribution," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 537–546, Feb. 2015.
[19] C. Liu, D. Li, Y. Zheng, and B. Lehman, "Modular differential power processing (mDPP)," in *Proc. IEEE Workshop Control Model. Power Electron*., 2017, pp. 1–7.
[20] H. Jeong, S. Park, J. Jung, T. Kim, A. -R. Kim, and K. A. Kim, "Segmented differential power processing converter unit and control algorithm for photovoltaic systems," *IEEE Trans. Power Electron*., vol. 36, no. 7, pp. 7797–7809, Jul. 2021.
[21] P. Wang, Y. Chen, J. Yuan, R. C. N. Pilawa-Podgurski, and M. Chen, "Differential power processing for ultra-efficient data storage," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4269–4286, Apr. 2021.
[22] E. Candan, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "A series-stacked power delivery architecture with isolated differential power conversion for data centers," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3690–3703, May 2016.
[23] A. Stillwell and R. C. N. Pilawa-Podgurski, "A resonant switched-capacitor converter with GaN transistors for series-stacked processors with 99.8% power delivery efficiency," in *Proc. IEEE Energy Convers. Cong. Expo.*, 2015, pp. 563–570.
[24] P. S. Shenoy and P. T. Krein, "Differential power processing for DC systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1795–1806, Apr. 2013.
[25] P. T. Krein, R. H. Campbell, and N. R. Shanbhag, "System and method for improving power conversion for advanced electronic circuits," U.S. Patent 9116692, Aug. 25, 2015.
[26] M. Kasper, D. Bortis, and J. W. Kolar, "Unified power flow analysis of string current diverters," *Electr. Eng.*, vol. 100, no. 3, pp. 2085–2094, Sep. 2018.
[27] Y. Cao, J. A. Magerko, T. Navidi, and P. T. Krein, "Power electronics implementation of dynamic thermal inertia to offset stochastic solar resources in low-energy buildings," *IEEE Trans. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 4, pp. 1430–1441, Dec. 2016.
[28] P. T. Krein and J. A. Galtieri, "Active management of photovoltaic system variability with power electronics," *IEEE Trans. Emerg. Sel. Topics Power Electron*., to be published, 2021, doi: 10.1109/JESTPE.2020.3006448.
[29] K. A. Kim, P. S. Shenoy, and P. T. Krein, "Converter rating analysis for photovoltaic differential power processing systems," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1987–1997, Apr. 2015.
[30] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein, "Differential power processing for increased energy production and reliability of photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2968–2979, Jun. 2013.
[31] C. Olalla, C. Deline, D. Clement, Y. Levron, M. Rodriguez, and D. Maksimovic, "Performance of power-limited differential power processing architectures in mismatched PV systems," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 618–631, Feb. 2015.
[32] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.
[33] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.
[34] Y. Jeon, H. Lee, K. A. Kim, and J. Park, "Least power point tracking method for photovoltaic differential power processing systems," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1941–1951, Mar. 2017.
[35] Y. Jeon and J. Park, "Unit-minimum least power point tracking for the optimization of photovoltaic differential power processing systems," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 311–324, Jan. 2019.
[36] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," in *Proc. IEEE Power Electron. Specialists Conf.*, 1995, pp. 1215–1221.
[37] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.
[38] B. J. Baliga, "Section 1.6: Ideal drift region for unipolar power devices," in *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2008, pp. 1–22.
[39] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and comparison of passive component volume of hybrid resonant switched-capacitor converters," in *Proc. IEEE Workshop Control Model. Power Electron.*, Toronto, ON, Canada, 2019, pp. 1–8.
[40] D. P. Bertsekas and J. N. Tsitsiklis, "Section 4.2: Covariance and correlation," in *Introduction to Probability*. Nashua, NH, USA: Athena Scientific, 2008, pp. 85–126.

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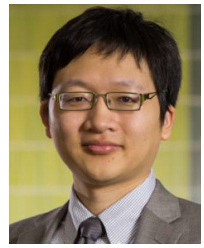

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