Letters

Replacing All ECs With NECs in Step-Up Converters—A Systematic Approach

Guidong Zhang, Weichen Chen, Samson S. Yu, Abdelali El Aroudi, and Yun Zhang

***Abstract*—Proposed in this letter is a novel generalized method to replace all short-life and large-size electrolytic capacitors (ECs) with non-ECs (NECs) in step-up converters. NEC has a longer lifespan and smaller size, leading to extended converter life and reduced converter size. The proposed approach can systematically replace ECs with NECs without affecting the desired converters' output features. After theory elaboration, five representative converters in two schemes are built with ten 150 W/100 V high power density prototypes for experimental verification. Experiments show that these prototypes can reach maximum power density of 2.91 $\mathrm{W/cm^3}$, significantly higher than converters with ECs, and maximum efficiency of 95.64%.**

***Index Terms*—Electrolytic capacitor (EC) replacement, high power density converters, non-EC (NEC), step-up converters.**

I. Introduction

DISTRIBUTED low-voltage renewable energy sources, such as photovoltaic and fuel cells, have led to significant developments in step-up converters [1]. To meet the grid code and reduce voltage ripples, electrolytic capacitors (ECs) with large capacitance are usually employed in these converters [2]. However, ECs usually have short lifetimes and are prone to malfunctions due to electrolyte evaporation caused by repetitive charging and discharging [3], [4]. An EC normally can achieve large capacitance but with a large volume, which results in low electric charge density in terms of "$Q(\mathrm{electriccharge})/V(\mathrm{volume})$," which hinders its applications for portable electronics devices. Furthermore, the single polarity characteristic of ECs can produce only positive or only negative voltage, but not both, which limits many output voltage ranges of advanced step-up converters [5]. For instance, the duty cycle of the converter in [6] with EC can only vary within $[0, 0.5)$, due to the EC's single polarity. It could otherwise have a much wider output voltage range, if a bipolar capacitor [such as a non-EC (NEC)] was employed.

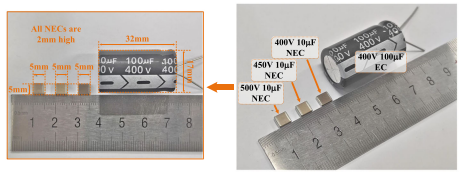

Fig. 1. Volume comparison between an EC and NECs.

NECs include ceramic capacitors and thin-film capacitors. NEC-based converters are preferable in today's electronics market due to their smaller sizes, dual polarity, longer lifetimes, wider frequency ranges, and higher operating temperature [7]. Thus, NEC-based converters can be used in tough environment, such as spacecraft and unmanned aerial vehicle, with little or no maintenance. According to the parameters shown in Fig. 1, the electric charge density of ceramic NECs is much higher than a regular EC, i.e., the size of the NEC is smaller than the EC with same quantity of electric charge. Additionally, NECs with high withstanding voltages, as shown in Fig. 1, are commercially available and inexpensive to purchase, which poses great potential of replacing ECs with NECs in practice. However, one obvious shortcoming of using NECs is that the output voltage ripples of the NEC-based high step-up converters are large due to NECs' low capacitance. Therefore, new designs are required for replacing ECs by NECs.

Most existing NEC-based converters are employed for the driving circuits of LEDs. The key point of replacing ECs with NECs in LED driving circuits is balancing its instantaneous input power and output power, which is the main function of ECs in a traditional LED driving circuit. To replace ECs with NECs in LED driving circuits, many control strategies based on the load characteristics of LED have been proposed, whereby the fundamental idea is to control the compensation network so that the instantaneous input power and output power of the driving circuit are balanced [8], [9]. However, these methods are not useful in step-up converters due to high-frequency ripples, which cannot be alleviated by any control strategies. Moreover, various types of loads can be connected to step-up converters, but LED driving circuits' load is only the LED. Therefore, the existing NEC-based converter design methods for LED driving

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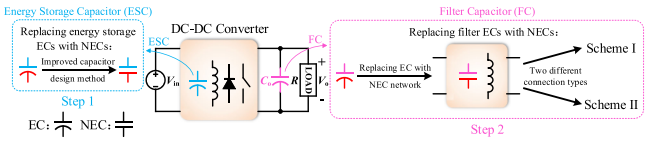

Fig. 2. Two steps of the proposed EC replacement approach.

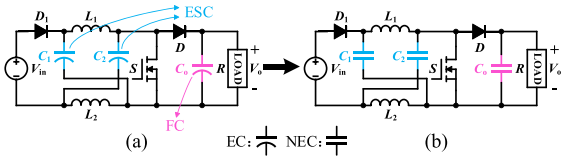

Fig. 3. ESC and FC in (a) ZSC with ECs and (b) ZSC with NECs.

circuits cannot be transferred or applied to NEC-based step-up converters for general uses.

In this study, we propose a generalized EC replacement method to systematically replace ECs with NECs in power converter circuits while maintaining high output voltage quality. The fundamental design ideology of the proposed method is to replace ECs with NECs by modifying and improving the topologies of step-up converters. Although the proposed EC replacement method is designed based on step-up converters in this study, it is also readily applicable to step-down or step-up/down converters. In the following, the proposed EC replacement approach with detailed procedures is elaborated in Section II; prototype experiments are conducted in Section III, which verifies the proposed design method; and finally, a conclusion is drawn in Section IV.

II. Generalized EC Replacement Approach

To systematically replace ECs with NECs in converters, the capacitors are divided in two categories by their functions. One category is the filter capacitor (FC), which is connected in parallel with the output port, and its main function is to reduce output voltage ripples. The other category is the energy storage capacitor (ESC), which acts as an energy transfer medium to maintain the function of the converter. As shown in Fig. 2, there are two steps to replace all ECs with NECs in the converter, whereby Step 1 is to replace the energy-storage ECs with NECs, and Step 2 is to replace the filter ECs with NECs.

A. Step 1: Replacing Energy Storage ECs With NECs

As shown in Fig. 3, a Z-source converter (ZSC) is an example to illustrate the ESC and FC in a converter, which is also an example to illustrate the EC replacement approach.

By analyzing the operation principle of the ZSC in Fig. 3, the average capacitor voltages and their voltage ripple amplitude of C_1 and C_2 can be derived as

$$V_{C_1} = V_{C_2} = \frac{1-d}{1-2d} V_{\text{in}} \tag{1}$$

$$\Delta v_{C_1} = \Delta v_{C_2} = \frac{d}{RC_1 f_{\text{s}}(1-2d)^2} V_{\text{in}} \tag{2}$$

where d is the duty cycle of switch S, R is the resistance load, and f_{s} is the switching frequency.

According to the traditional capacitor design method, capacitors C_1 and C_2 can be derived by

$$\Delta v_{C_1} = \Delta v_{C_2} \le x\% V_{C_1} \tag{3}$$

where $x \in [1, 2]$.

Thus, C_1 and C_2 can be derived as

$$C_1 = C_2 \ge \frac{d}{x\% R f_{\text{s}}(1-d)(1-2d)} = \alpha. \tag{4}$$

The principle of the traditional capacitor selection method is based on reducing capacitor voltage ripples, and this method is the most efficient technique to select or limit ripple of FC. However, capacitors used for energy conversion do not require such large capacitance to reduce ripple since they only require enough capacitance for energy conversion, and voltage ripples will eventually be suppressed by the FC. Moreover, this method with an approximate is used for selecting the capacitance, and then we normally choose a capacitor with larger capacitance in a converter to ensure its correct operation.

Capacitors C_1 and C_2 are ESCs, whereby their function is to transfer energy, i.e., the converter is functional as long as C_1 and C_2 are large enough to transfer energy. The energy charged and discharged by capacitor C_1 in a switching period is calculated as

$$W_{C_1} = \frac{1}{2} C_1 V_{C_{1\_\max}}^2 - \frac{1}{2} C_1 V_{C_{1\_\min}}^2 = C_1 V_{C_1} \Delta v_{C_1}. \tag{5}$$

Thus, the range of C_1 can be determined as

$$\frac{1}{2} C_1 V_{C_1}^2 \ge W_{C_1} \Rightarrow C_1 \ge \frac{2d}{R f_{\text{s}}(1-d)(1-2d)} = \beta. \tag{6}$$

Comparing (4) and (6), β is $1/50$–$1/25$ of α. Therefore, the function of the converter can be maintained even with much low capacitance. Considering a reasonable margin, the capacitance of capacitors can be reduced by 90% to 95% for the ESCs in this case. After replacing the ECs with NECs, the NEC-based ZSC is shown in Fig. 3(b). This analysis can be applied to wide-ranging converters, whereby the ECs can be replaced by NECs.

In this study, five typical step-up converters are employed as examples, with their ECs replaced by NECs, to verify the feasibility of the proposed method. As shown in Fig. 4, ZSC [6], quasi-ZSC (QZSC) [10], switched-boost converter (SBC) [11], quasi-SBC (QSBC) [12], and quadratic boost converter (QBC) [13] are used for demonstration in this letter. All ECs in the five typical step-up converters can be replaced with NECs.

In this step, we only consider replacing energy-storage ECs with NECs, whereas voltage ripples are not taken into account. Therefore, the output voltage ripples of the five NEC-based converters in Fig. 4 are mostly unacceptable in practice. Replacing filter ECs needs more sophisticated calculations and design, which is shown in the following section.

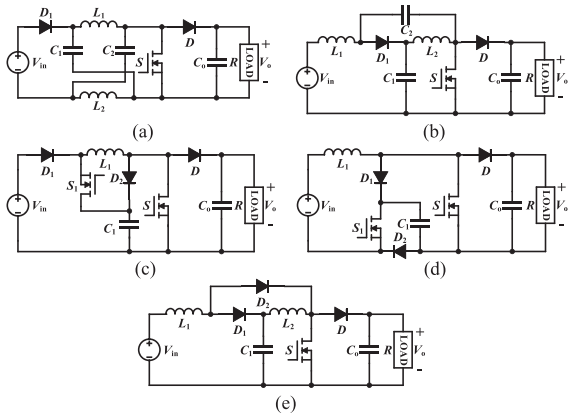

Fig. 4. Five representative converters after EC replacement. (a) NEC-ZSC. (b) NEC-QZSC. (c) NEC-SBC. (d) NEC-QSBC. (e) NEC-QBC.

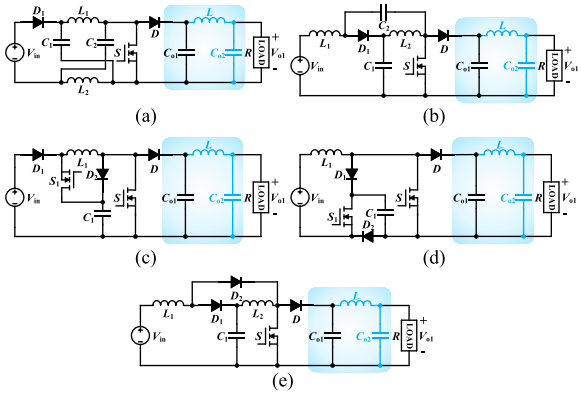

Fig. 5. Five NEC-based converters in *Scheme I*. (a) NEC-I-ZSC. (b) NEC-I-QZSC. (c) NEC-I-SBC. (d) NEC-I-QSBC. (e) NEC-I-QBC.

B. Step 2: Replacing Filter ECs With NECs

Both current and voltage ripples are the reflection of energy fluctuation. To buffer the energy fluctuation, converters need to have collectively a big number of energy storage elements, which include both capacitors and inductors. Therefore, additional inductors can make up the low capacity energy storage of NECs. In this section, two schemes are proposed to realize the replacement of filter ECs.

1) Scheme I: As shown in Fig. 5, an LC pair is cascaded at the output port of the converter, along with $C_{\mathrm{o}1}$ as an energy buffer network to mitigate energy fluctuation. The energy buffer network and its key waveforms are shown in Fig. 6(a) and (b), respectively. The inductor current and capacitor voltage can be derived as

$$L\frac{\mathrm{d}i_L}{\mathrm{d}t}=\begin{cases}-\dfrac{\Delta v_{C_{\mathrm{o}1}}}{d_1T_1}t+\dfrac{1}{2}\Delta v_{C_{\mathrm{o}1}} & ,0\le t<d_1T_1\\ \dfrac{\Delta v_{C_{\mathrm{o}1}}}{(1-d_1)T_1}(t-d_1T_1)-\dfrac{1}{2}\Delta v_{C_{\mathrm{o}1}} & ,d_1T_1\le t\le T_1\end{cases} \tag{7}$$

$$C_{\mathrm{o}2}\frac{dv_{\mathrm{o}1}}{dt}=i_L-I_{\mathrm{o}1} \tag{8}$$

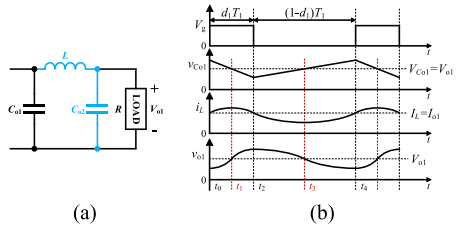

Fig. 6. (a) Energy buffer network. (b) Key waveforms of the energy buffer network.

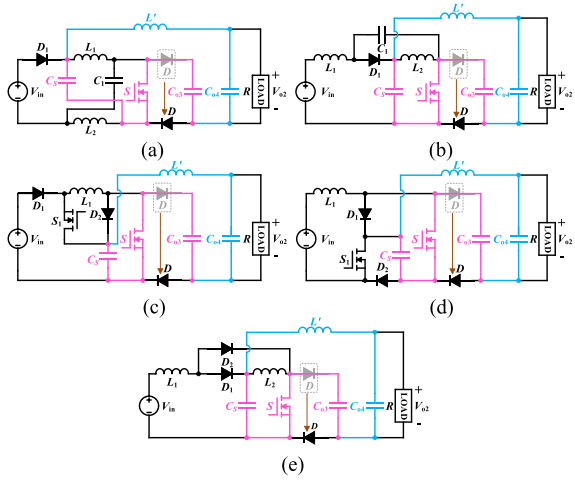

Fig. 7. Five NEC-based converters in Scheme II. (a) NEC-II-ZSC. (b) NEC-II-QZSC. (c) NEC-II-SBC. (d) NEC-II-QSBC. (e) NEC-II-QBC.

where d_1 is the duty cycle, T_1 is the switching period, and $v_{\mathrm{o}1}$ is the output voltage of *Scheme I* converters; $\Delta v_{C_{\mathrm{o}1}}$ is the ripple of $v_{C_{\mathrm{o}1}}$; i_L is the instantaneous current flowing through L; and $I_{\mathrm{o}1}$ is the average current.

According to (7) and (8), the amplitude of the output voltage ripples of *Scheme I* converters can be derived as

$$\Delta v_{\mathrm{o}1}=\frac{\Delta v_{C_{\mathrm{o}1}}d_1^2}{12LC_{\mathrm{o}2}f_1^2} \tag{9}$$

where f_1 is the switching frequency of *Scheme I* converters. Similar to (3), L and $C_{\mathrm{o}2}$ can be calculated by (9).

2) Scheme II: As shown in Fig. 7, diode D is moved to the bottom to bridge C_S in series with $C_{\mathrm{o}3}$ when S is ON (the pink circuit in Fig. 7), and the additional LC pair is cascaded with the pink circuit. For SBC and QSBC, the additional LC pair along with the pink circuit is an additional step-up network, i.e., the voltage gains of NEC-II-SBC and NEC-II-QSBC are higher.

According to Fig. 8, the operation principle of the additional step-up network can be analyzed, and the average output voltage can be derived as

$$V_{\mathrm{o}2}=V_{C_S}+d_2V_{C_{\mathrm{o}3}} \tag{10}$$

where d_2 is the duty cycle of *Scheme II* converters, and V_{C_S} and $V_{C_{\mathrm{o}3}}$ are the average voltage of C_S and $V_{C_{\mathrm{o}3}}$, respectively. Moreover, from Fig. 8(c), capacitor voltage and inductor current

TABLE I
COMPARISONS OF KEY FEATURES OF TRADITIONAL, *SCHEME I*, AND *SCHEME II* CONVERTERS

	Output Voltage Ripple Amplitude				Voltage Gain					Cost (unit: $) & Volume (unit: cm^3) & Weight (unit: g)								
	Traditional	*Scheme I*		*Scheme II*	Traditional		*Scheme I*		*Scheme II*	Traditional			*Scheme I*			*Scheme II*		
ZSC	$\frac{dV_o}{RC_o f}$	$\frac{d^3M}{3RCf}$	$<$	$\frac{d(1-d)M}{2}$	$\frac{1}{1-2d}$	$=$	$\frac{1}{1-2d}$	$=$	$\frac{1}{1-2d}$	21.25	99.0	111.6	20.73	70.8	103.2	20.79	70.8	103.7
QZSC					$\frac{1}{1-2d}$	$=$	$\frac{1}{1-2d}$	$=$	$\frac{1}{1-2d}$	21.25	99.0	111.7	20.73	70.8	103.2	20.79	70.8	103.6
SBC					$\frac{1-d}{1-2d}$	$=$	$\frac{1-d}{1-2d}$	$<$	$\frac{1-d^2}{1-2d}$	29.27	70.2	65.7	28.99	51.5	61.5	29.05	51.5	62.0
QSBC					$\frac{1}{1-2d}$	$=$	$\frac{1}{1-2d}$	$<$	$\frac{1+d}{1-2d}$	29.27	70.2	65.7	28.99	51.5	61.5	29.05	51.5	62.0
QBC					$\frac{1}{(1-d)^2}$	$=$	$\frac{1}{(1-d)^2}$	$=$	$\frac{1}{(1-d)^2}$	22.58	94.5	109.1	22.30	70.2	104.5	22.36	70.2	105.0

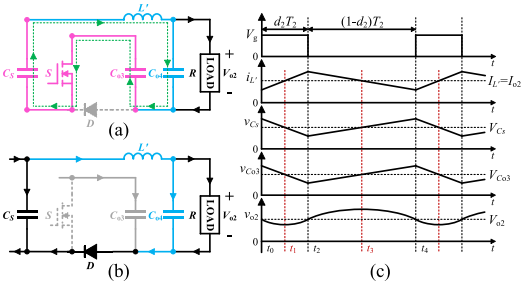

Fig. 8. Additional step-up network of NEC-II converters in different modes. (a) Mode 1. (b) Mode 2. (c) Key waveforms of the additional step-up network.

can be derived as

$$C_{o4}\frac{dv_{o2}}{dt} = i_{L'} - i_{o2} \tag{11}$$

$$\Delta i_{L'} = \frac{d_2(1-d_2)}{L'f_2}V_{Co3} \tag{12}$$

$$I_{L'} = I_{o2} \tag{13}$$

where v_{o2} and i_{o2} are the output voltage and current, respectively; f_2 is the switching frequency; I_{o2} is the average output current of *Scheme II* converters; $i_{L'}$ is the current flowing L'; and $\Delta i_{L'}$ is ripple amplitude of $i_{L'}$. Combining (10)–(13), we can deduce the output voltage ripple as

$$\Delta v_{o2} = \frac{d_2(1-d_2)}{8L'C_{o4}f_2^2}V_{Co3}. \tag{14}$$

Similar to (3), L' and C_{o4} can be calculated by (14).

3) Comparison of Scheme I and Scheme II Converters: The two schemes are different in terms of the connection type of topologies, and the new topologies have different electrical features. Their key electrical characteristic equations are shown in Table I. For simplicity, we assume that all capacitors are equal and denoted as C and $f_1 = f_2 = f, d_1 = d_2 = d, L = L'$, $M = V_o/4LCf^2$, and capacitor C_o is the output capacitor of the traditional converters. It is easy to see that the converters in *Scheme I* have lower output voltage ripples. However, the voltage gains of NEC-SBC and NEC-QSBC are higher in *Scheme II*. Thus, converters with topologies similar to SBC and QSBC are suitable to apply the method developed for *Scheme II*, whereas other converters are suitable for *Scheme I*.

III. EXPERIMENTAL VALIDATION

In this work, ten NEC-based prototypes are built, as shown in Fig. 9. We set $V_o = 100\,\mathrm{V}$, $V_{in} = 30\,\mathrm{V}$, and $f = 100\,\mathrm{kHz}$, and we choose all capacitors to be 10 μF/250 V, L to be 470 μH/3 A, L' to be 33 μH/3 A, and other inductors to be 330 μH/10 A. Moreover, five EC-based prototypes are built, as shown in Fig. 10, and all of their capacitors are 100 μF/160 V. Additionally, 110N20NA and MBR20200 are used as switches and diodes, respectively. The input voltage source is KIKUKUI PWR 800 L. The oscilloscopes used for recording the experimental waveforms and measuring efficiencies are KEYSIGUT DSO9104 A and KEYSIGHT DSOX3104 T, respectively. The voltage differential probes and current probes are KEYSIGHT N2790 A and KEYSIGHT N2782B, respectively. With the proposed approach, ten NEC-based prototypes have very small sizes and high power density, and their power and size are shown in Fig. 9. It is obvious that they have high power density compared to the traditional low-power products. Each converter prototype has a similar size of 10-W Apple USB power adapter.

Experimental waveforms are shown in Figs. 9 and 10. We can see that all the output voltages of these NEC-based converters have very low ripples similar to the EC-based converters. All of their output voltage ripples are less than or equal to 1 V, which is 1% of the output voltage. Moreover, the output voltage spikes of the NEC-based converters are lower than the EC-based converters. The key waveforms of NEC-based converters are consistent with the waveforms shown in Figs. 6(b) and 8(c). Three prototypes of three kinds of ZSC converters are compared in Fig. 10, and the sizes of the NEC-based converters are smaller.

The cost, volume, and weight of 15 converter prototypes are shown in Table I. It can be seen that the NEC-based converters are better in these performance metrics.

The efficiency curves are shown in Fig. 11, and the efficiencies of the NEC-based converters are mostly higher than EC-based converters. The components in the NEC-based and EC-based converters are identical except capacitors. Thus, the higher power loss of EC-based converters is mainly caused by the higher parasitic resistance of EC. Furthermore, all of NEC-based converters have high efficiency with maximum efficiency of 95.64%, which is very high for a low-power converter (150 W).

As examples, four proposed NEC-based converters with a load subject to step changes and with PI closed-loop control are implemented. The system diagram is shown in Fig. 12. The PI parameters are: NEC-I-QZSC: $K_p = 0.001$,

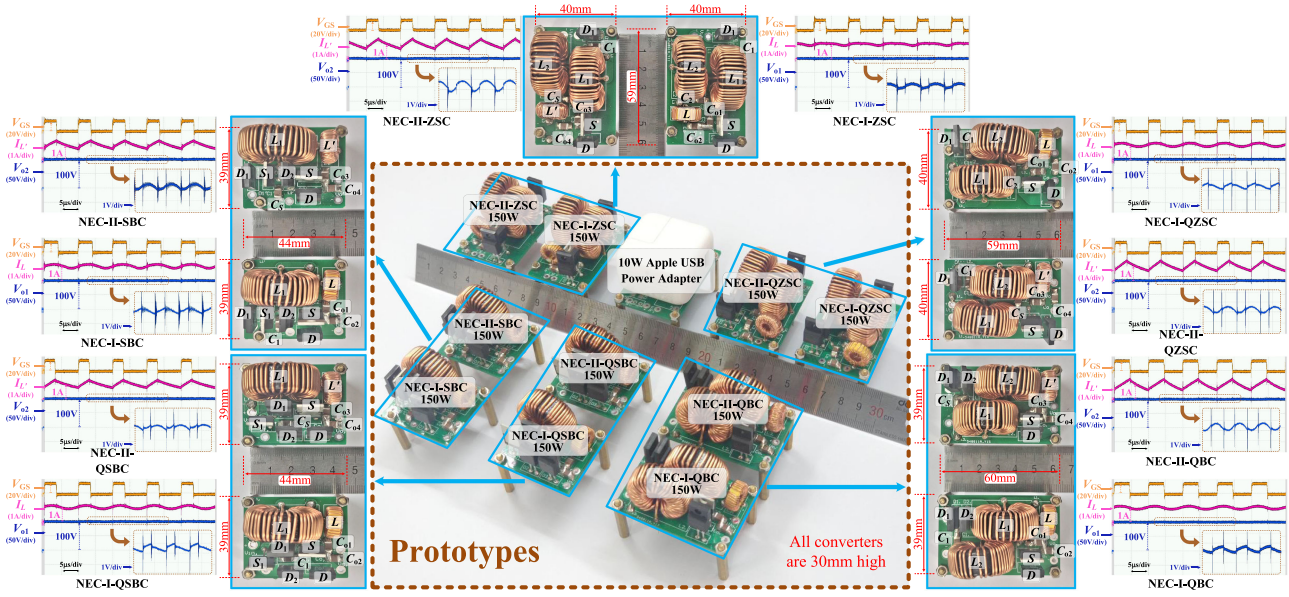

Fig. 9. Proposed NEC-based *Scheme I* and *Scheme II* converters and their corresponding converters prototypes with key waveforms.

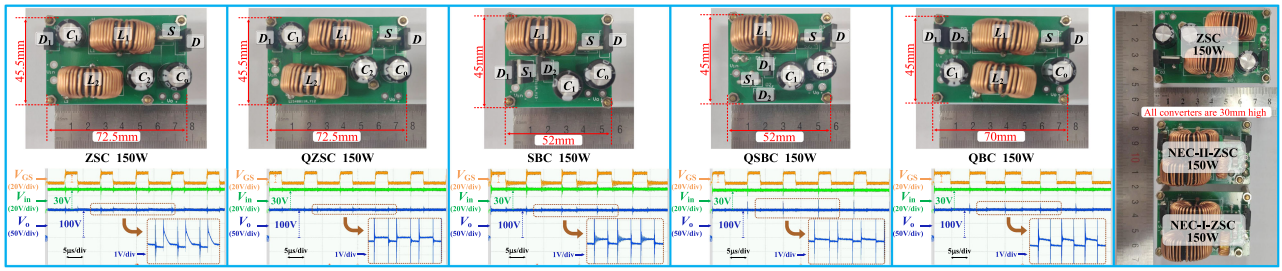

Fig. 10. Traditional EC-based converter prototypes with key waveforms and the prototype comparison of three kinds of ZSC converters.

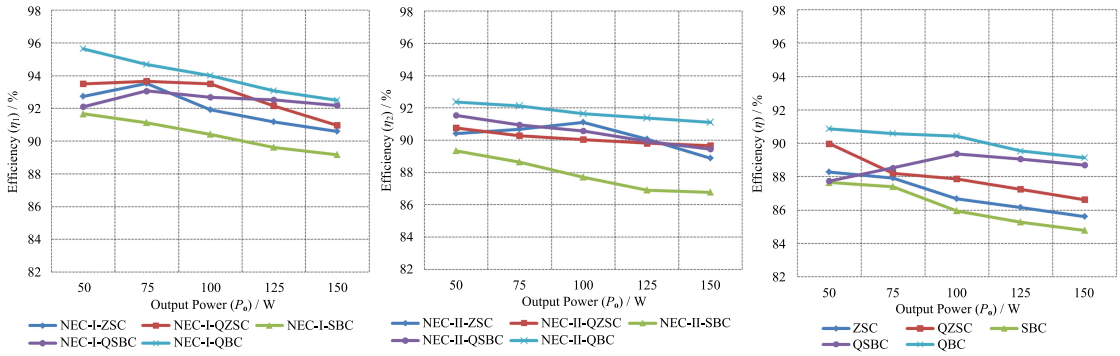

Fig. 11. Efficiency curves of EC-based converters and proposed NEC-based converters with various power.

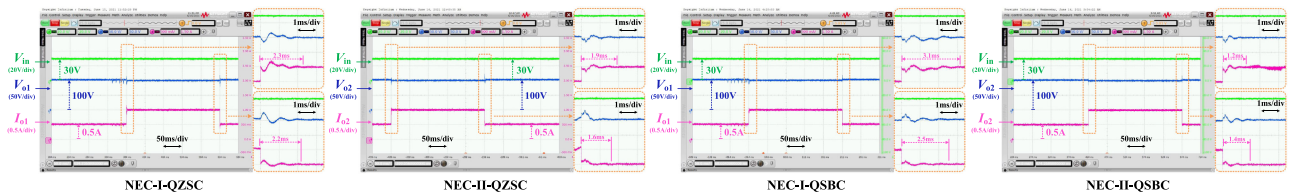

Fig. 12. Closed-loop system diagram of the four NEC-based converters.

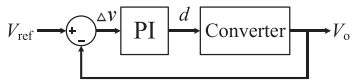

Fig. 13. Experimental results of four proposed NEC-based converters with load step changes: 200Ω → 100Ω → 200Ω.

$K_i = 0.005$; NEC-II-QZSC: $K_p = 0.001$, $K_i = 0.005$; NEC-I-QSBC: $K_p = 0.0009$, $K_i = 0.0045$; and NEC-II-QSBC: $K_p = 0.0005$, $K_i = 0.01$. The experimental results are shown in Fig. 13, the output voltage and current settle in 1–3 ms after the load changes from $200\,\Omega$ to $100\,\Omega$, then back to $200\,\Omega$.

The aforementioned experiments and analysis have thus well verified the proposed EC replacement method.

IV. Conclusion

In this letter, a generalized approach for replacing all ECs with NECs in step-up dc–dc converters has been proposed, whereby detailed analyses and mathematical derivations are presented. With the proposed approach, five typical step-up converters have been changed to NEC-based converters with the proposed two schemes, all of which have smaller sizes, higher power density, longer lifetime, and high efficiency. Two of them (NEC-II-SBC and NEC-II-QSBC) even have higher voltage gains than their EC-based counterparts. To well validate the feasibility of the proposed approach, 15 converter prototypes have been built, and all experimental results agree well with the theoretical analysis.

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