Optimal Integrated Design of a Magnetically Coupled Interleaved H-Bridge

Andrea Stratta, Davide Gottardo, Mauro Di Nardo, Jordi Espina, Liliana de Lillo, *Member, IEEE*, Lee Empringham, *Member, IEEE*, and Mark C. Johnson, *Member, IEEE*

***Abstract*—The application of wide-band gap semiconductors and their integration with other power electronics components (e.g., passives, gate drivers, sensing, thermal management) can meet the growing demand for volume reduction in power electronics systems. The design of such an integrated system is a complex multiphysics problem given the high number of variables to identify, objectives to optimize, and constraints to satisfy. Traditionally, this complex problem is approached subdividing the design in different steps, where in each step, the single components are designed and optimized independently from the others. This might clearly overlook the effect that the design choices of a single subsystem has on other subsystems, leading to suboptimal solutions. In this article, an automated design approach is proposed with the aim of maximizing power density whilst minimizing total losses. As a vessel to investigate the presented optimization workflow, the magnetically coupled interleaved H-bridge topology is chosen as an emblematic example of multivariable design problem. The first step of this approach consists of developing a loss model of the converter, which takes into account components physical dimensions, the temperature dependence, and the circuit parasitics. In the second step, these models are used within a nested optimization procedure in order to estimate the losses for multiple points of load. With the aim of validating both design approach and optimization results, three different optimal solutions have been deeply analyzed with commercial suit, prototyped, and tested. The showed experimental results endorse the adopted design approach confirming the optimality/validity of the manufactured solutions.**

***Index Terms*—Analytical models, dc-dc power converters, design automation, electromagnetic modeling, integrated design, semiconductor device modeling.**

I. Introduction

POWER density and efficiency, together with reliability and reduced costs, are the main drivers for future developments in power electronics. In this context, the introduction of wide band gap (WBG) semiconductor, such as silicone carbide (SiC) and gallium nitride (GaN), resulted in a disruptive technology change with unprecedented improvements in reducing losses and volume. In addition, new packaging and integration technologies (e.g., novel interconnection and bonding techniques, etc.) under development allow unlocking the full WBG transistors potential whilst maintaining low cost and high reliability [1]–[4]. However, the practical application and integration of these new technologies poses a complex design problem, where a large number of design variables belonging to different physics needs to be selected to meet the application requirements. Automated design workflows, including a comprehensive set of models and simulations, are becoming more and more commonly used to solve this complex design problem [5]–[7]. Additionally, if the models are not too expensive in terms of computational time, this automated workflow can be used with optimization algorithm to find the best set of design variables to target different possible objectives (e.g., costs, efficiency, reliability, sustainability). Multidomain and multiobjective (MO) optimization have been largely investigated in the past years and they proved to be of great importance for power electronics design in many fields of applications, from telecommunications power supplies, [8]–[10], to smart transformer application [11] and inductive power transfer converter [12]. Recently published works have also faced the problem of quantifying the model parametric uncertainty and modeling errors and how these might affect the optimization results [13], [14]. When the problem is correctly stated, in addition to efficiency and power density, also reliability and cost can be taken into account as objectives. In [15], an artificial intelligence-aided methodology for optimization of power electronic systems has been proposed, taking into account reliability as a performance metric at design stage. In [16], a comparative study of Si and SiC semiconductors for three-phase photovoltaic inverter application is carried out by means of three objectives optimization targeting efficiency, power density, and costs.

The first step to perform a complex system optimization is to develop comprehensive mathematical models of the constituent system components in order to be able to fully describe the behavior of each subsystem and their interactions. The modeling of each component can clearly involve different domains, e.g., electromagnetic, thermal, etc. and therefore be computationally expensive. The level of details of each submodel is dependant on the final aim of the study, and it is often a compromise

Manuscript received February 2, 2021; revised April 1, 2021 and May 24, 2021; accepted June 23, 2021. Date of publication July 1, 2021; date of current version September 16, 2021. This work was supported by Engineering and Physical Sciences Research Council (EPSRC) Heterogeneous Integration Project under Grant EP/R004501/1. Recommended for publication by Associate Editor D.-C. Lee. *(Corresponding author: Andrea Stratta.)*

Andrea Stratta, Mauro Di Nardo, Liliana de Lillo, Lee Empringham, and Mark C. Johnson are with Power Electronics, Machines and Control Group, The University of Nottingham, NG7 2RD Nottingham, U.K. (e-mail: Andrea.stratta1@nottingham.ac.uk; mauro.dinardo4@nottingham.ac.uk; liliana.delillo@nottingham.ac.uk; Lee.Empringham@nottingham.ac.uk; Mark.Johnson@nottingham.ac.uk).

Davide Gottardo is with the The Thinking Pod Innovations Ltd. (TTPi), NG7 2TU Nottingham, U.K. (e-mail: davide.gottardo@ttpi.tech).

Jordi Espina is with Circontrol, 08232 Barcelona, Spain (e-mail: jordiespina@gmail.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3094025.

Digital Object Identifier 10.1109/TPEL.2021.3094025

between accuracy and computational effort needed to estimate the targeted performance metrics.

Given the complexity of developing fast but accurate models to be included within system optimization procedure, the latter can be faced carrying out separate optimizations on the single subsystems. This approach might clearly lead to suboptimal solutions being neglected or simplified the interaction between subsystems. It is a common procedure, for example, to optimize the cooling system independently. In [17], a dedicated MO optimization is presented to minimize weight and meet the thermal resistance requirements of a cooling system, while [18] minimizes the device junction temperature in a power module. Magnetic components are also often optimized independently from the whole converter, when their geometry and winding arrangement are described by a large number of parameters. In [19], [20], an optimization strategy for high-frequency and high current matrix transformer for resonant converter is presented. Similarly, in [21], the benefits of performing spatial permeability and multilayer coil optimization on toroidal inductors are presented. A dedicated multidomain approach is reported in [22], for the design of a printed circuit board (PCB)-integrated flyback transformer; a procedure considering electrical, magnetic, and geometrical parameters is presented with the aim of minimizing losses and/or footprint area. In [23] and [24], the converter design and the independent inductor optimization are, respectively, described for an interleaved dc–dc converter with coupled output inductor. This circuit topology constitutes the perfect vessel to investigate the advantages of adopting a multiobjectives multidomains approach to the design of the whole power electronics system. In fact, it has been already proved that for this topology, the coupled inductor has a great impact on the behavior of the whole converter; however, the inductor is usually optimized after the modulation has been defined.

In this article, the design of an H-bridge with interleaved outputs through a magnetically coupled inductor is faced with a more holistic approach implementing an automatic design optimization procedure with the aim of reducing the inductive parts volume whilst minimizing the converter total losses. Different operating point of loads (POLs) are considered within the design workflow in order to be able to optimize the system for a wide range of working points.

A comprehensive loss model of the converter is first presented, which takes into account components physical dimensions, the temperature dependence, and the circuit parasitics of both semiconductor devices and inductor. This is a collection of submodels, some of which are well established in the literature, while others have been developed in this article. The first criterion, which these models need to meet, is to be computationally efficient, so that they can be repeatedly launched within an automatized optimization routine. Second, to maintain a general approach, the models employed are based on information that are ready available (e.g., from manufacture datasheet), without the need of any device or magnetic material precharacterization. The proposed model also includes the possibility of achieving zero voltage switching (ZVS) through triangular current mode (TCM) modulation and the effects of pseudotriangular current

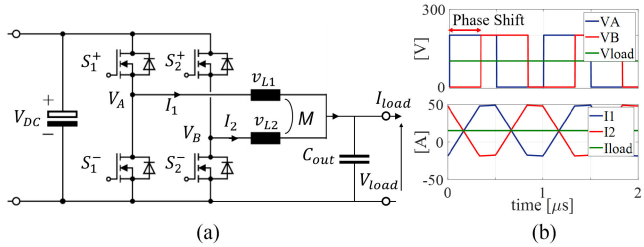

Fig. 1. Magnetically coupled interleaved H-bridge. (a) Topology. (b) Typical output waveforms.

waveforms on the magnetic components performance, thus ensuring that the optimization results are globally valid. An MO stochastic optimization algorithm is then used to identify the optimal design variables describing the inductor geometrical parameters and the modulation parameters of a 200–48-V dc–dc converter using GaN devices. To further increase the power density, a custom inductor manufacturing technique has been used, which widens the core geometry variety that can be explored during the design optimization. Alternatively to the usual commercial solutions, the adopted one also offers significant thermal advantages by using a U-shape winding structure, as shown in [25].

With the aim of validating the proposed approach and verifying the optimality of the solutions, a prototype of the H-bridge has been built with three different inductors, each one of them corresponding to different solutions along the Pareto-front.

To experimentally identify each loss component, the converter has been prototyped with two independent cooling systems. By doing so, the losses of active devices and inductor can be estimated using a colorimetric method.

II. Mutually Coupled Interleaved H-Bridge (MCI-HB)

The selected converter topology consists of a single-phase two-level H-bridge (Fig. 1). The middle points of each leg are interleaved through an output coupled inductor. Similarly to TCM for half-bridges [26], extended TCM (eTCM) [27] is the modulation strategy that allows obtaining zero voltage turn-ON (ZVS) with the proposed topology, by ensuring that the instantaneous current flowing in the output inductor is such that the stray capacitor of the switches is completely discharged prior to their turn-ON. In eTCM, unlike TCM, the positive and negative peak values of the ripple current can be different in magnitude, depending on the phase shift, the values of self and mutual inductance, and the switching frequency. It is worth noticing that, while eTCM operation reduces the switching losses, the associated ripple current increases the device conduction losses and both core and copper losses in the inductor. The modulation strategy (whether to achieve ZVS or maintain hard switching) leading to the highest efficiency depends on the output current value since the relative distribution of the losses changes with the load. It is therefore of paramount importance to consider more operating points at design stage, as will be shown in Section V, in order to avoid obtaining an optimal solution with outstanding

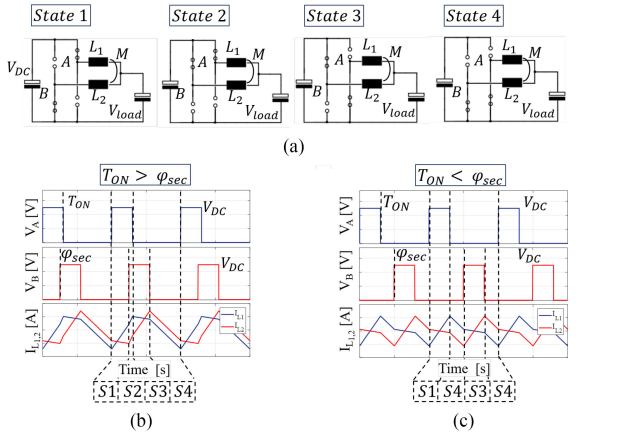

Fig. 2. (a) Four states of the MCI-H bridge; states sequence in case of (b) duty greater than phase shift and (c) duty smaller than phase shift.

performance in the targeted operating point and really poor ones at different loads.

In order to develop an exhaustive loss model which takes into account different modulation strategies to find the optimal balance between device losses and inductor losses, the current waveform needs to be calculated for each operating point. In this section, the output currents of each leg, i_1 and i_2, are described as functions of the inductance values, L and M, switching frequency, f_{sw}, duty cycle, $D = T_{on}/T_{sw}$, and phase shift, φ_{sec}. The low frequency component, i_{load}, is separated from the high-frequency components of the current,i_{L1} and i_{L2}, as follows:

$$i_1 = \frac{i_{\text{load}}}{2} + i_{L1} \quad \text{and} \quad i_2 = \frac{i_{\text{load}}}{2} + i_{L2}. \tag{1}$$

Considering the output capacitor to be an ideal voltage source, i_{L1} and i_{L2} can be calculated writing the coupled inductor equations

$$\begin{bmatrix} v_{L1} \\ v_{L2} \end{bmatrix} = \begin{bmatrix} L & M \\ M & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L1} \\ i_{L2} \end{bmatrix} \tag{2}$$

$$\frac{d}{dt} \begin{bmatrix} i_{L1} \\ i_{L2} \end{bmatrix} = \frac{1}{L^2 - M^2} \begin{bmatrix} L & -M \\ -M & L \end{bmatrix} \begin{bmatrix} v_{L1} \\ v_{L2} \end{bmatrix}. \tag{3}$$

The voltages across the two inductors, v_{L1} and v_{L2}, are defined by the switching pattern, resulting in four possible states [Fig. 2(a)]. In each state, the derivative of the inductor currents can be calculated substituting the actual value of v_{L1} and v_{L2} in (3). In this way, (4) can be derived.

$$\frac{d}{dt} \begin{bmatrix} i_{L1} \\ i_{L2} \end{bmatrix} = \frac{1}{L^2 - M^2} \begin{bmatrix} a_{L1}L - b_{L1}M & L - M \\ a_{L2}L - b_{L2}M & L - M \end{bmatrix} \begin{bmatrix} V_{DC} \\ -V_{\text{load}} \end{bmatrix}$$

where the coefficients $a_{L1}, b_{L1}, a_{L2}, b_{L2}$ are defined for each state as follows:

$$\begin{aligned} &\text{S1}: \quad a_{L1} = 1, \quad b_{L1} = 0, \quad a_{L2} = 0, \quad b_{L2} = 1 \\ &\text{S2}: \quad a_{L1} = 1, \quad b_{L1} = 1, \quad a_{L2} = 1, \quad b_{L2} = 1 \\ &\text{S3}: \quad a_{L1} = 0, \quad b_{L1} = 1, \quad a_{L2} = 1, \quad b_{L2} = 0 \\ &\text{S4}: \quad a_{L1} = 0, \quad b_{L1} = 0, \quad a_{L2} = 0, \quad b_{L2} = 0. \end{aligned} \tag{4}$$

The described current ripple calculation method is general. Indeed, the sequence of states can be varied according to the modulation scheme. In particular, as shown in Fig. 2(b) and (c), depending on whether the ON time is longer or shorter than the phase shift, the sequence can be $S1 \mapsto S2 \mapsto S3 \mapsto S4$ or $S1 \mapsto S4 \mapsto S3 \mapsto S4$.

The results of the presented equations, $i_1(t)$ and $i_2(t)$, are used as input for the device loss model (Section III) and inductor loss model (Section IV) to calculate the converter losses.

III. Device Model

In [28], a model based on the charge equivalent representation of the parasitic MOSFET capacitances was presented. Following this approach, it is possible to estimate the voltage fall and rise times, thanks to the fact that in a half-bridge topology, the charge is directly linked to the energy stored in these capacitances, and the precise calculation of the device internal loss energies can be carried out. This model has been selected among others because it includes the parasitic inductances. The parasitic loop inductances are modeled as lumped parameters. L_d is half of the power loop inductance (from decoupling capacitors to devices). L_{cs} is effectively the mutual coupling between the gate loop inductance and the power loop inductance represented as T equivalent of a coupled inductor. In this section, this approach is extended from Si and SiC MOSFET to GAN-HEMT devices and applied to the considered topology, the MCI-H bridge.

A. MOSFET Model vs. GaN-HEMT Model

From a power electronics application point of view, the main difference between a MOSFET and GaN-HEMT is their behavior during the freewheeling period. When the drain–source voltage is reversed and no positive bias is applied between gate and source, the MOSFET presents an intrinsic n–p junction that allows the current to flow. On the other hand, in a GaN-HEMT, the negative bias on the drain terminal creates a voltage gradient beneath the gate channel, which causes the depletion region to have a negative electrical potential relative to the gate metallization. Once the voltage gradient exceeds the threshold voltage, the device can conduct negative current through the channel. Finally, GaN-HEMT devices do not present associated losses to reverse recovery charge, Q_{rr}, while MOSFETs do, but they have the disadvantage of higher reverse voltage drop, v_{rev}, which is equal to the sum of the channel resistance, $R_{ds}(ON)$, and the threshold voltage, v_{th}. In the case of bipolar gate drivers, a negative bias applied between gate and source, $-v_{gs}$, needs to be added to the threshold voltage to calculate the total reverse voltage drop. These considerations are summed up in Fig. 3.

B. Switching Losses

The model used in this section is presented in Fig. 4(b) for the top device. If the commutation time is sufficiently short, the output inductor currents, I_1 and I_2, can be considered constant during the turn-ON or turn-OFF period. In saturation, the device channel is modeled as a controlled current source. The nonlinear

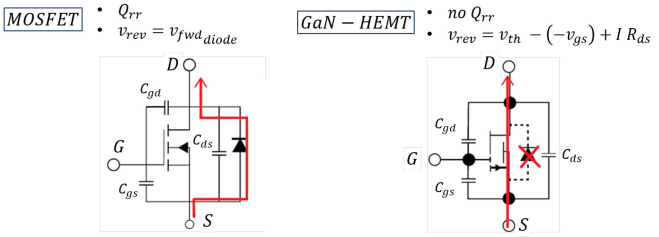

Fig. 3. Device model based on the charge equivalent representation of the parasitic capacitances: differences in reverse conduction between Si or SiC MOSFETs and GaN-HEMT.

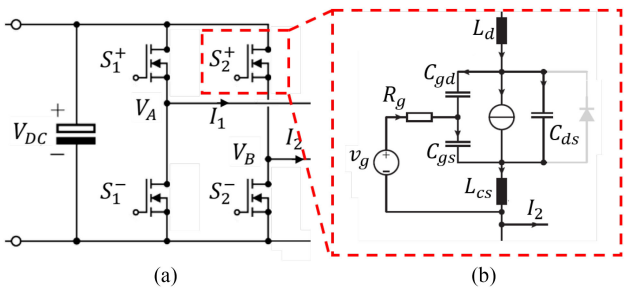

Fig. 4. (a) MCI-H bridge. (b) Device equivalent circuit for switching losses calculation.

transconductance function, g_m, relates the current in the channel, i_{ch}, and the gate voltage, v_{gs}. The voltage-dependent input, output, and reverse transfer capacitances [$C_{oss}(v_{ds})$, $C_{iss}(v_{ds})$, and $C_{rss}(v_{ds})$] are available from the manufacture datasheet and stray capacitances are calculated as the charge equivalent as follows:

$$C_{gs} = \frac{1}{V_{DC}} \int_0^{V_{DC}} [C_{iss}(v_{ds}) - C_{rss}(v_{ds})] dv_{ds} \tag{5}$$

$$C_{ds} = \frac{1}{V_{DC}} \int_0^{V_{DC}} [C_{oss}(v_{ds}) - C_{rss}(v_{ds})] dv_{ds} \tag{6}$$

$$C_{gd} = \frac{1}{V_{DC}} \int_0^{V_{DC}} C_{rss}(v_{ds}) dv_{ds}. \tag{7}$$

To summarize, the parameters used for the MOSFET model and the GaN-HEMT model are parasitic capacitances (C_{gd}, C_{gs}, C_{gds}) and transconductance function ($g_m(i_{ch})$) and they can be extracted from datasheet as discussed in [28].

With the adopted assumptions, the predicted current waveforms are linearized and independent from the temperature. Alternative and more complex methods [29] can be adopted, leading to a more accurate waveform prediction but these are definitely computationally more expensive. Regarding the temperature dependency, more faithful models [30], [31] can be employed; however, they are heavily based on device parameters not available within the manufacturer datasheet. Indeed, these demanding methods require a precharacterization to extract the temperature-dependent properties of the devices.

Adopting a topology with two interleaved half-bridges, Fig. 4(a), the switching losses depend on the applied modulation scheme. As summarized in Fig. 5, by varying the modulation parameters (phase shift, switching frequency, and dead time),

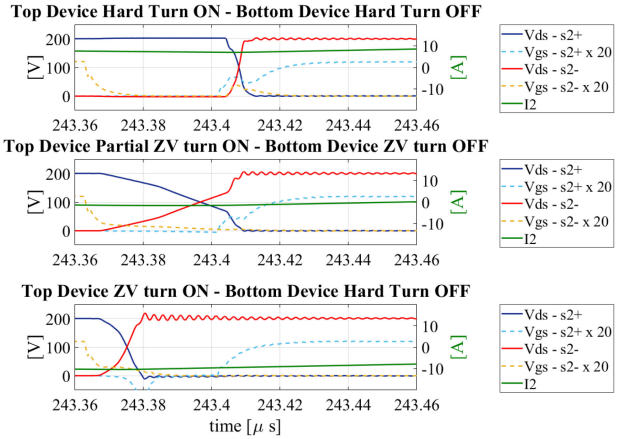

Fig. 5. Five possible switching transitions described for top or bottom device: hard turn-OFF, ZVS turn-OFF, hard turn-ON, ZVS turn-ON, and quasi ZVS turn-ON.

each individual device can experience five different switching transitions: hard turn-OFF, ZVS turn-OFF, hard turn-ON, ZVS turn-ON, and partial ZVS turn-ON. Following an automated design approach, without any *a priori* assumption on the modulation, all these switching events need to be described. The currents $i_1(t)$ and $i_2(t)$ are used as input of the device loss model calculation. Based on their instantaneous values at the switching instant, I_1 and I_2, and their direction, the transitions can be classified as follows.

1) Soft Switching Transitions: I_{oss} is defined as the portion of the drain current that flows in the output capacitance. Referring to one of the bottom devices, S_2^-, ZVS at turn-OFF can be achieved when $|I_2| < 2I_{oss}$, because the current in the channel becomes zero [Fig. 5(b)]. In that case, the current to charge of the parasitic capacitances becomes $I_{oss} = 1/2I_2$, resulting in a slower but quasi loss-less transition.

To have ZVS at turn-ON, the direction of the output current has to be correct to discharge the output capacitance of the devices. Referring to Fig. 4(a), precondition to observe soft commutation is that the output current is positive when bottom device turns ON and negative when the top device turns ON. If this condition is verified, the absolute value of the current can be compared to the minimum current needed to complete the charge and discharge process of the output capacitances during the dead time, I_{ZVS}

$$I_{\text{ZVS}} = \frac{2Q_{oss}}{DT} \tag{8}$$

where Q_{oss} is the output charge of each device, which is a nonlinear function of the drain-to-source voltage, and DT is the period of time that elapses between turn-OFF and turn-ON of devices of the same leg.

If the direction of the current is correct and the absolute value of the output current is greater than I_{ZVS}, ZVS at turn-ON occurs. This condition is shown for the top device in Fig. 5(c). However, once the output capacitance is completely discharged, reverse conduction losses occur through the body diode, in Si or SiC MOSFET, or in the channel in a GaN-HEMT.

TABLE I
COUPLED INDUCTOR GEOMETRIC PARAMETERS

Number of turns	N	Lateral Bar Cross-section	A_{eff}
U-shape width	$wire_w$	Central Bar Cross-section	A_C
U-shape height	$wire_h$	Central Bar gap	l_gC
Insulation distance	d_{iso}	Lateral gap	l_gL

2) Partial Soft Switching Transitions: As described in [32], when the direction of the current is correct to have ZVS but the condition on the absolute value is not respected, partial ZVS occurs. As shown for the top device in Fig. 5(b), once the dead time is finished, the voltage across the output capacitance is $V_{fin} = V_{DC} - (I_2 DT)/(2C_{oss})$, thus resulting in an energy dissipation equal to

$$E_{oss} = \frac{C_{oss} V_{fin}^2}{2}. \tag{9}$$

3) Hard Switching Transitions: If the conditions for ZVS or partial ZVS at turn-ON or turn-OFF are not satisfied, hard switching occurs, as shown in Fig. 5(a). In case of hard turn-ON and hard turn-OFF, transition times and associated energy losses are calculated using the equations presented in [28].

C. Conduction Losses

Instantaneous conduction power loss are calculated as follows:

$$p_{cond}(t) = R_{ds_{ON}}(T_j) i_{ds}(t)^2 \tag{10}$$

where $R_{ds_{ON}}(T_j)$ is the device ON-resistance. In both MOSFETs and GaN-HEMT devices, $R_{ds_{ON}}(T_j)$ depends on V_{gs} and the junction temperature, T_j. In particular, by implementing the curve $R_{ds}(T_j)$, it is possible to have a thermal-dependent device loss model. Alternatively, when the manufacturer datasheet provides the $I_{DS} - V_{DS}$ curves at different temperatures (e.g., at 25°C, 125°C, and 150°C), the conduction losses can be calculated directly from the product of I_{DS} and V_{DS}, and then performing a linear interpolation between the closest available temperature points. In GaN-HEMT devices, current collapse can occur as a result of electron trap formation in AlGaN/GaN HEMTs, which increases ON resistance under dynamic conditions. These effects are not modeled because they became more relevant for small conduction periods.

IV. INDUCTOR MODEL

The coupled inductor is a critical component of the switching cell; its physical implementation can be carried out using different configurations, from the classical transformer structure with concentric windings on the same core column (resulting in high magnetic coupling) to independent solenoid wound on different magnetic cores. The geometry considered in this work is presented in Fig. 6(a), while the parameters used to vary this geometry are listed in Table I. Ferrite bars guiding the magnetic flux can be either cut from bulk or manufactured with near net shape techniques (e.g., gelcasting). The winding arrangement is instead chosen to be compatible with U-shape bonding technique. This configuration has been selected because

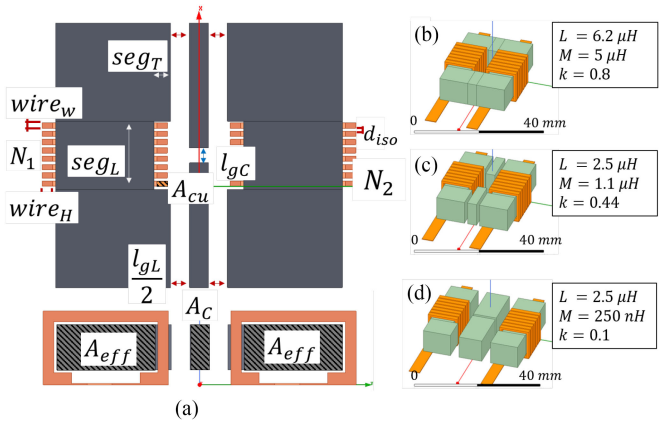

Fig. 6. Proposed coupled inductor. (a) Geometric parametrization. (b)–(d) Range of magnetic coupling that can be achieved varying the geometrical parameters.

it allows to achieve a broad range of possible magnetic couplings. Fig. 6(b)–(d) shows that with the proposed parametrization, by varying the length of gaps, l_{gL} and l_{gC}, together with the ratio between the cross sections of the lateral bars, A_{eff}, and the central bar, A_C, a broad variety of geometries can be investigated featuring a really wide range of magnetic couplings (e.g., from 0.1 to 0.8).

A. Inductance Calculation

The values of self- and mutual inductance are used in the converter model to calculate the current waveforms, which are then used in the various loss models. Consequentially, even a small error in the inductance calculation can cause a cascade of errors that would heavily impact the accuracy of the predicted performance. Additionally, due to the presence of large air-gaps and the adoption of magnetic materials with low permeability, significant fringing and leakage fluxes can be present in this inductor. For this reasons, it is essential to develop an inductance calculation method that is accurate, general, and computationally efficient. Although it is not the most computational efficient approach to estimate the inductances, performing a static finite element analysis (FEA) is the only viable option to accurately take into account the relevant 3-D effects of the magnetic field distribution (e.g., fringing and leakage fluxes). In addition, assuming that the inductor works in linear region, it is possible to perform a single magneto-static finite element (FE) simulation to extract the inductance values. This process has been automatized in Matlab environment using the Ansys-Maxwell FE suit. Under the hypothesis that the inductor is operating in the linear region, it is also possible to extract matrix A relating the average magnetic flux density in each ferrite block to the excitation currents

$$\begin{bmatrix} B_{Lat1} \\ B_{Hor1} \\ B_{cen} \\ B_{Lat2} \\ B_{Hor2} \end{bmatrix} = [A]_{(5\times 2)} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \tag{11}$$

B. Inductor Core Loss Calculation

The instantaneous average flux density, $B(t)$, in each bar is estimated by applying matrix A, estimated with the 3D-FE static simulation, to the instantaneous currents calculated using the converter current model. To evaluate the core losses, the improved generalized Steinmetz equation (iGSE) is used as presented in [33]. Compared to other models, the iGSE takes into account the losses depending on whole cycle. For this reason, when it is needed, the flux density waveform is divided into major loop and minor loop and the total losses are then calculated as follows:

$$P_{b_i} = k_i \sum_{n=1}^{m} \frac{1}{T_n} \Delta B_n^{(\alpha-\beta)} \int_0^{T_n} \left(\frac{dB_n}{dt}\right)^{\alpha} dt \qquad (12)$$

where P_{b_i} is the loss density in the ith bar, m is the number of bars, T_n, ΔB_n, and $\frac{dB_n}{dt}$ are, respectively, the period, the peak-to-peak flux density, and the derivative of the flux density of the nth minor loop. The material loss behavior is modeled through the Steinmetz coefficients, α, β and the improved coefficient k_i for nonsinusoidal excitation

$$k_i = \frac{k}{2\pi^{(\alpha-1)} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{(\beta-\alpha)} d\theta}. \qquad (13)$$

The thermal dependence of core losses from temperature is taken into account using a quadratic expression modifier for the coefficient k

$$k(T_{\text{core}}) = k(T_{\text{ref}})(C_{T2} T_{\text{core}}^2 - C_{T1} T_{\text{core}} + C_T). \qquad (14)$$

Although the iGSE approach does not take into account the dc bias, the relaxation effects, and the variation of SE coefficients with frequency, it is computationally efficient and makes use of coefficients directly available from magnetic materials manufacturer datasheet. More comprehensive alternatives such the ones reported in [34], [35] take into account more phenomena but rely on parameters generally not available on manufacturer datasheet.

C. Winding Loss Calculation

In this section, the loss phenomena in the inductor winding are modeled by taking into account the interactions between the nonuniform current distribution and the magnetic field. In order to estimate the ac losses in the winding, the current distribution has to be calculated using the diffusion equation inside the conductor. As shown in Fig. 7, 1-D field simplifying assumption is made, i.e., it is assumed there is no magnetic field variation along the x-axis, which results in straight magnetic field lines that are parallel to the core bar, $H_x(y)$. As a result, the vector potential, $A_z(y)$, is parallel to the z-axis and varies along the y-axis. Using phasors notation and under 1-D condition, diffusion and magnetic vector potential equations can be written, respectively, as follows:

$$\frac{1}{\mu\sigma} \frac{\partial^2 H_x(y)}{\partial^2 y} = j\omega H_x(y) \qquad (15)$$

$$H_x(y) = \frac{1}{\mu} \frac{\partial A_z(y)}{\partial y} \qquad (16)$$

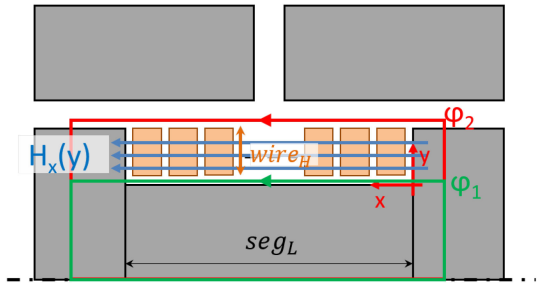

Fig. 7. Winding loss model: considered 1-D field distribution.

where μ is the magnetic permeability, σ is the electric conductivity (as a function of temperature), and ω is the electrical pulsation. General solution of (15) and (16) for the z-component of the magnetic vector potential $A_z(y)$ is

$$A_z(y) = Me^{-\gamma y} + Ne^{\gamma y} \quad \text{and} \quad \gamma = \sqrt{j\omega\mu\sigma} \qquad (17)$$

where M and N are the coefficients of the differential equation solution.

Inside the conductor, it is possible to derive the expression of the magnetic field, and by using Ampere-law, it is possible to calculate the current density $J_z(y)$

$$A_z(y) = M_c e^{-\gamma(y-wire_H)} + N_c e^{\gamma(y-wire_H)} \qquad (18)$$

$$H_x(y) = -\frac{\gamma}{\mu}\left(-M_c e^{-\gamma(y-wire_H)} + N_c e^{\gamma(y-wire_H)}\right) \qquad (19)$$

$$J_z(y) = -\frac{\partial H_x(y)}{\partial y} = d\frac{\gamma^2}{\mu}\left(M_c e^{-\gamma(y-wire_H)} - N_c e^{\gamma(y-wire_H)}\right). \qquad (20)$$

In order to calculate the values of the constants M_c and N_c inside the conductors, boundary condition in $y = 0$ ($H_x(0) = 0$) and Ampere-law applied at loops γ_1 and γ_2 ($\oint H_x(y)d\gamma_1 - \oint H_x(y)d\gamma_2 = NIe^{j\omega\theta}$) are used. Once the spatial distribution is calculated for each harmonics of the exciting current, ${}^k J_z(y)$, total losses in the inductor windings can be calculated as follows:

$$P_{\text{winding}} = Vol_{cu} \sum_{k=1} \int_{d_{iso}}^{wire_h} \frac{{}^k J_z(y) {}^k J_z^*(y)}{\sigma} dy. \qquad (21)$$

V. Optimization Strategy

Being inductor volume and total losses the objectives of the optimization, the PCB layout has been not been considered variable during the design. In particular, the physical position of the devices, gate drivers, and decoupling capacitance and their conductive path are considered to be fixed and not subject to optimization, thus resulting in constant values of parasitic inductance and capacitances. Since these parasitic elements play a key role in the performance of the converter, they are preliminary calculated using ANSYS Q3D extractor tool. The frequency range considered for this calculation is related to the devices turn-ON and turn-OFF time.

The analytical and numerical models presented in the previous sections are implemented in Matlab environment. Since the

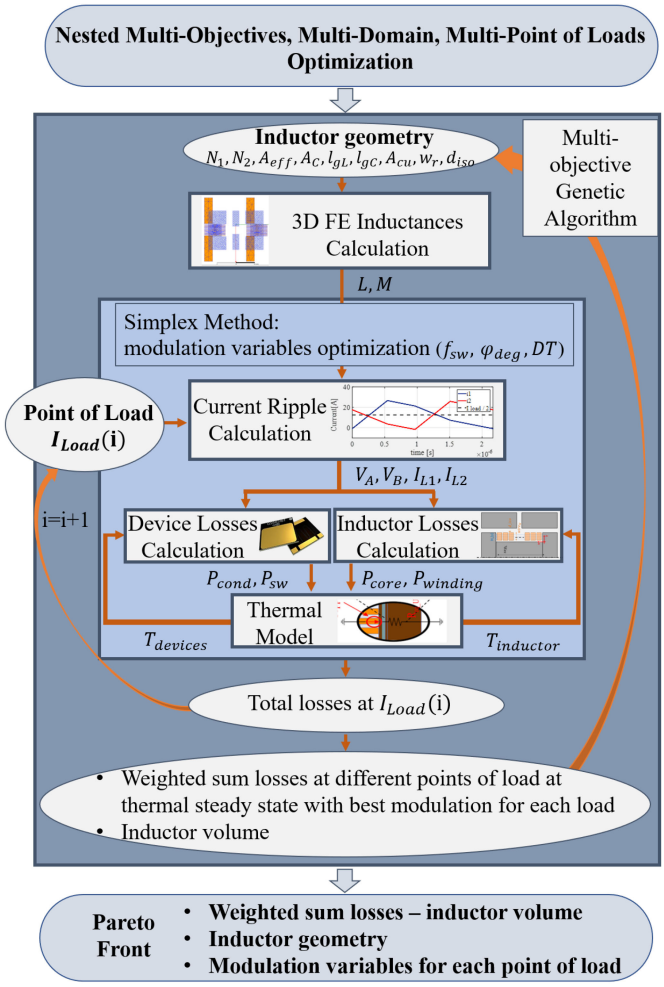

Fig. 8. Proposed optimization strategy.

implemented hybrid analytical-numerical model can take into account the effect of temperature on both the inductor and device losses, a converter thermal model is also developed. The latter allows to estimate the temperature of each component and iteratively updates the loss calculation.

One of the main advantages of the developed loss model is that it can be rapidly executed for different operating loads. As presented in previous sections, converter total losses are the sum of several loss components. By increasing load current (e.g. different point of load), the switching losses become dominant, and the modulation strategy need to be adapted to maintain acceptable total losses. With the aim of optimizing the converter operation for different load scenario, it is necessary to divide the research space into two subsets. The first one includes the physical geometrical parameters of the inductor (called hardware design variables). The second subset consists of the software parameters, which define the modulation technique and the control strategy, namely, switching frequency, phase shift, and dead time. The importance of clearly dividing first and second class stems from the fact that, whereas software parameters can be adjusted during converter operation, once the inductor geometry is defined it cannot be varied in different points of load. Fig. 8 shows the logic block scheme of the proposed optimization strategy. It consists of two nested optimizations: the outer one targets the hardware design variables while the inner one works on the software design variables for each considered operating point. The outer optimization is carried out using an MO stochastic population-based optimization algorithm (NSGA-II embedded in Matlab environment) in order to identify the optimal inductor geometry. The inner optimization makes use of the Nelder–Mead simplex algorithm in order to find the combination of phase shift, switching frequency, and dead time minimizing the total losses for the considered operating POL.

Adopting this optimization workflow, the inductor structure is defined by each GA individual, and the finite element model (FEM) inductance calculation block, the most expensive in terms of computational time, is executed once per functional evaluation. Once self- and mutual inductances of the coupled inductor are evaluated, the current and voltage waveforms can be analytically calculated, and consequentially the losses in the device and inductor at the thermal steady state can be estimated. The inner optimization loop performs these analytical performance evaluation in order to identify the optimal modulation strategy for each POL. Once for each operating points the optimal software design variables are found, the weighed sum of the total losses can be calculated

$$P_{ws} = \sum_{i=1}^{n} w_i \cdot P_i \tag{22}$$

where n is the number of considered operating points, w_i is the relative weight, and P_i is the total losses for the ith operating load. Finally, the performance indexes targeted by the outer optimization loop are calculated and the latter solves the following constrained MO minimization problem:

$$\begin{aligned} &\min\ (P_{ws}, V_{\text{inductor}}) \\ &\text{s.t. } T_{\text{device}} \leq T_{\text{device,max}} \\ &\quad T_{\text{inductor}} \leq T_{\text{inductor,max}} \end{aligned} \tag{23}$$

where V_{inductor} is clearly inductor volume while T_{inductor} and T_{device} are the steady-state temperatures of the inductor and device. The latter have been constrained to be within the maximum allowed values suggested by the respective manufacturers.

The clear advantage of following this design workflow is that the inductor geometry is not optimized to be the most compact and efficient for just one operative point, but to maintain minimum losses over a range of operative points. It is worth to underline that if a single operating point is considered, then only the outer optimization loop is needed, which can target both hardware and software variables at the same time. By adopting this workflow and these optimization algorithms, the outer loop allows estimating the trade-off between total loss and inductor volume while the inner loop quickly identifies the software design variables minimizing the losses for a given POL.

VI. Case Study and Validation

Although the proposed optimization strategy along with the developed loss estimation models is general and can be used

TABLE II
CASE STUDY H-BRIDGE: APPLICATION REQUIREMENTS AND CIRCUIT PARAMETERS

V_{DC}	200 V	$R_{g_{ON}}$	10 Ω
V_{load}	48 V	$R_{g_{OFF}}$	5 Ω
POLs	0 - 15 A	V_g	0 - 6 V
Device	GS66508	L_d	5 nH
Core Mat.	4F1	L_{cs}	0.25nH

TABLE III
CASE STUDY INDUCTORS PARAMETERS

Parameter	Ind. A	Ind.B	Ind.C
L	9.16 μH	8.45 μH	5.30 μH
M	-2.21 μH	-3.65 μH	-2.32 μH
k	0.24	0.43	0.43
N	15	14	13
A_{cu}	0.5 mm^2	0.4 mm^2	0.25 mm^2
A_{eff}	60 mm^2	48 mm^2	26 mm^2
A_C	23 mm^2	8 mm^2	7 mm^2
l_{gL}	6.8 mm	2.1 mm	1.4 mm
l_{gC}	4.2 mm	2.4 mm	2.3 mm

in many different ways (e.g., compare semiconductor device technologies, gate driver circuits, magnetic materials, etc.), in the following, it is applied to optimize multiple dc–dc operating scenarios and preliminary selecting the device technology and core magnetic material. In particular, the dc–dc application features a dc bus voltage of 200 V and four operative points: all of them with an output voltage of 48 V and different currents 0–5–10–15 A. The magnetic material chosen for this application is 4F1 a NiZn ferrite from Ferroxcube, while as semiconductor devices, 650V-30 A GaN Systems GaN HEMT are considered.

From GaN systems datasheet [36], the device ON-resistance as function of temperature, $R_{ds_{ON}}(T_j)$, can be imported. As no data are available for the capacitances thermal dependence, the device switching losses have been considered independent from the junction temperature during this design exercise. Although this is clearly an approximation, the only possible alternative to include this phenomena within the prediction is to precharacterize the device.

Gate driver circuit parameters are selected as indicated in Table II. A specific PCB layout has been designed and analyzed using ANSYS Q3D extractor to calculate the values of power loop parasitic inductance ($L_d = 5$ nH) and parasitic coupling between power and gate loop ($L_{cs} = 0.25$ nH). In this case, the frequency sweep set for the simulation covers up to 100 MHz. The package stray inductances are significantly lower because the selected components are surface-mounted devices, packaged to avoid internal wire bonds and and external leads, thus minimizing the internal current loops.

A. Optimization Results

Fig. 9(a) shows all the the solutions evaluated during the optimization in the volume-weighted losses plane (blue dots) while the Pareto-front is highlighted in black. Here, no weights are applied in the total losses objective function. As expected,

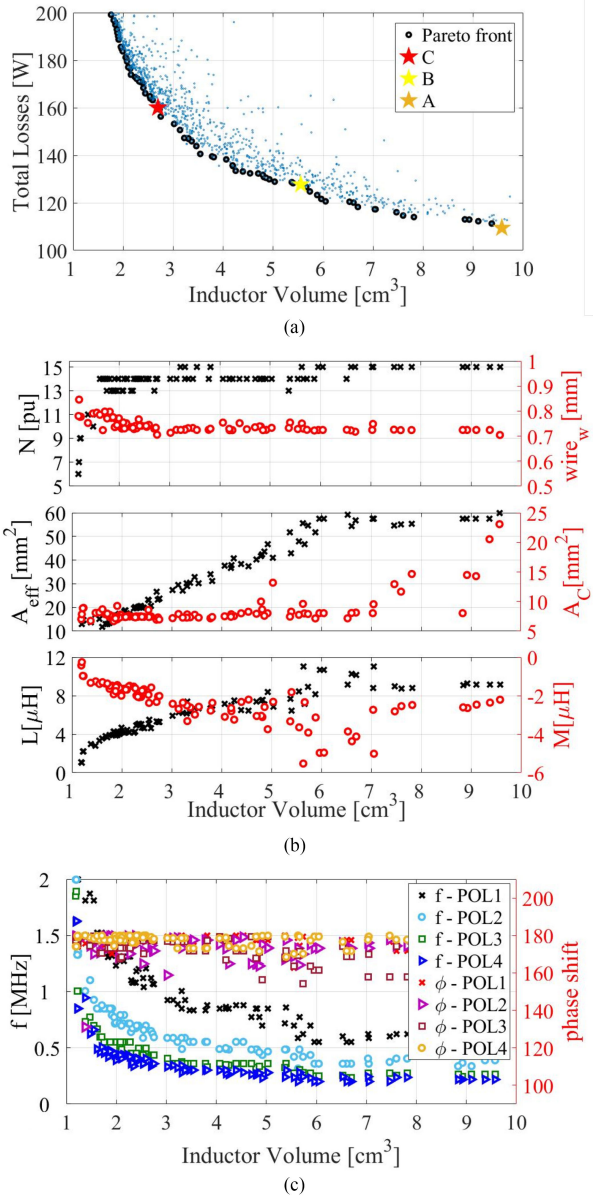

Fig. 9. MPL optimization results. (a) All individuals and Pareto-front. (b) Hardware geometric parameters, inductances, and modulation software parameters variations.

smaller inductors result in higher losses, i.e., the selected performance metrics show a clear competitive behavior (justifying the MO approach).

To have a better understanding of how the optimization algorithm achieved these results, it is worth to analyze the variation of the geometrical parameters of the inductor and the modulation parameters along the Pareto-front [Fig. 9(b)]. Some parameters, like core height and U-shaped width, exhibit a significant variation (i.e., they are reduced to minimize the volume), whereas the number of turns and the U-shaped thickness and the magnetic coupling (ratio between mutual and self inductances) are stable along the Pareto-front. The number of turns trend can be justified via thermal considerations. As it will be thoroughly explained in experimental section, the inductor is integrated on a IMS

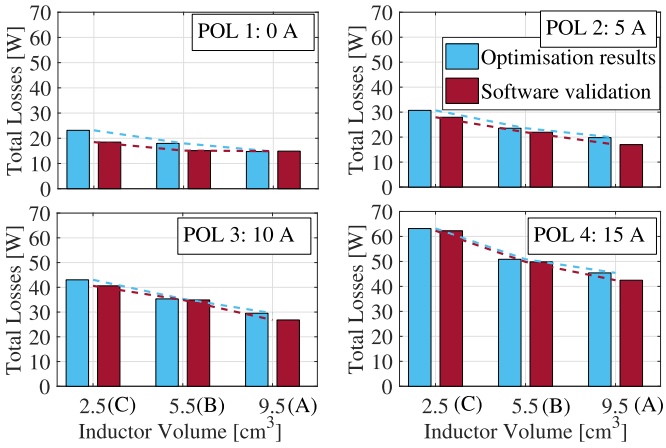

Fig. 10. Total losses: comparison between optimization analytical results and results obtained with commercial software (LT-spice for device losses and Ansys Maxwell for inductor losses).

substrate using the U-shaped winding technique, thus resulting in an excellent thermal path from the copper winding to the heat sink. The optimization algorithm tends to keep a high number of turns (close to its boundary) in order to increase the area for heat dissipation and achieve the best thermal exchange scenario. Fig. 9(b) describes the trends of switching frequency and inverter legs phase shift for all considered points of load. Among the software parameters, the switching frequency is the one that more widely varies along the Pareto-front and also passing from one POL to the other. On the contrary, the phase shift remains almost unchanged along the Pareto-front and it is unaffected by the variation of the output current.

B. *Analysis of the Optimal Solutions*

In this section, a subset of optimal solution is selected from the Pareto-front and further analyzed with commercial softwares. To perform this validation in a broader range of input parameters, three different results have been selected from the Pareto-front. As shown in Fig. 9, they correspond to three different inductors (A with 9.5 cm^3, B with 5.5 cm^3, and C with 2.5 cm^3), each one with a different set of modulation parameters for each POL. The dimensions and parameters of each one of the three inductors are summarized in Table III. For the losses in the devices, the software LTspice is used to estimate its behavior employing models given by the manufacturer. For the coupled output inductor, a transient magnetic simulation in ANSYS Maxwell is performed to calculate the core and winding losses.

Fig. 10 shows in a bar plot the total losses for each of the three inductors in the four POLs. The comparison between optimization results, obtained with the analytical loss model discussed in previous sections, and the commercial software indicates a good agreement with an average error of 7.7%. From an optimization point of view, it is also worth to underline that the trend is always respected, i.e., there are no discrepancies in the derivative of the total losses for each load, thus confirming that the algorithm actions toward losses minimization are valid even when analyzed with commercial software.

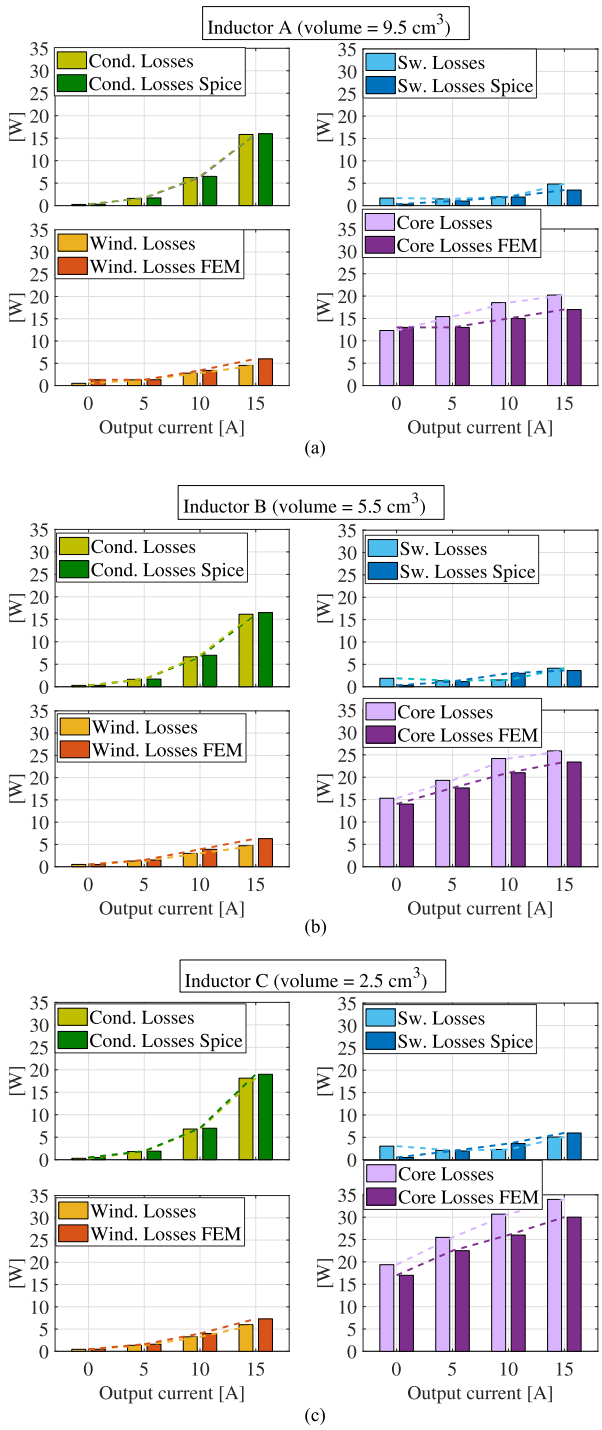

Fig. 11. Comparison between optimization analytical results and results obtained with commercial software (LT-spice for device losses and Ansys Maxwell for inductor losses) for the three selected solutions on the Pareto-front.

In Fig. 11, converter losses are divided into conduction and switching losses, inductor winding, and core losses. Also, in this case, the deviation between analytical and commercial software predictions is below 15%. It is possible to confirm that the trends are respected for each considered load level, proving the accuracy of the implemented loss models. It is worth noting that, while conduction losses and winding losses are fairly constant

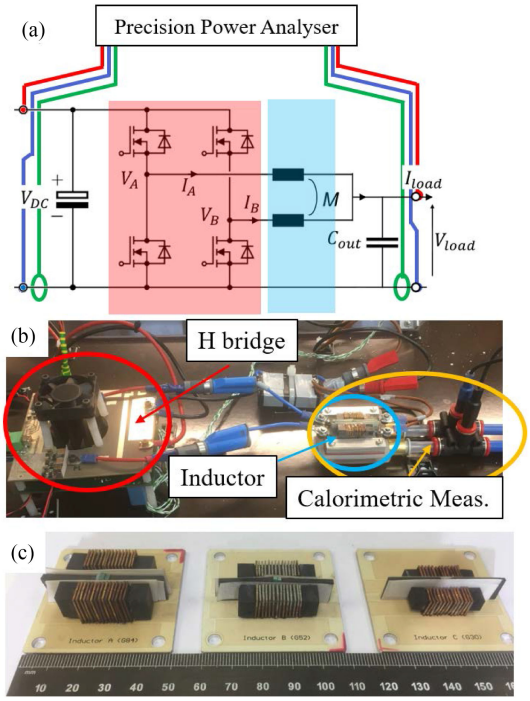

Fig. 12. Experimental test setup. (a) Converter and precision power analyzer schematics. (b) Test setup with inductor cooling system. (c) Three inductors under test.

along the Pareto-front, there is a significant increase of switching losses and core losses as the inductor volume reduces.

From this analysis, it can be concluded that the loss models considered in this study provide estimations that are as reliable as the one obtained with commercial software simulations. But compared to FE software or circuit simulations software, they have the practical advantage of drastically reducing computational time making them suitable to be embedded within an automated optimization routine.

VII. Experimental Results

In order to perform an experimental validation of both optimization strategy and loss models, a H-bridge using 650V-30 A GaN Systems GaN HEMT (GS66508 T) has been designed and prototyped [Fig. 12(b)]. Three different results have been selected from the Pareto-front [Fig. 9(a)], corresponding to three inductors (A with 2.5 cm^3, B with 5.5 cm^3, C with 2.5 cm^3), and have been manufactured [Fig. 12(c)].

The integration of the inductors on insulated metal substrates (IMS) is detailed in Section VII-A. While in simulations it is straightforward to divide the total losses in each component, the experimental identification of the different loss components poses a serious challenge. In this article, as shown in Fig. 12(a), the total losses are measured using a precision power analyzer (KinetiQ PPA5530) while the losses in the inductor are measured using the calorimetric setup described in Section VII-B. Neglecting the losses in the capacitors, it is finally possible to calculate the losses in the device as difference between the total losses and the inductor one.

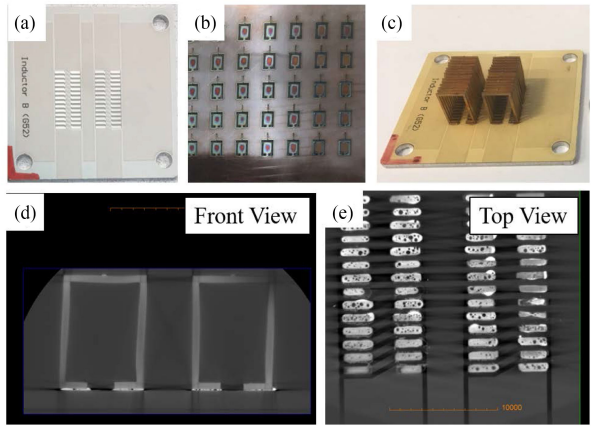

Fig. 13. Inductor manufacturing steps. (a) IMS with patterned copper. (b) Laser-cut copper U-shapes. (c) Windings after U-shape placement. (d) and (e) x-Ray CT scan front and top view of the wingdings.

A. Inductors Manufacturing

The inductor prototypes have been built using a manufacturing technology proposed in [25].

It consists of using a thermally conductive substrate, in this case an IMS, with an appropriate copper pattern, Fig. 13(a), on top of which individual copper parts are soldered to close the current path and create single turns, Fig. 13(c). The copper U-shapes are laser-cut from copper sheets, Fig. 13(b), enabling the possibility to create a large variety of winding geometries. With this approach, each turn is electrically and thermally connected to the IMS substrates, thus improving the thermal performance of the winding. The mechanical quality of the bond-line plays the main role in this aspect. X-ray computed tomography (CT) is performed using Versa XRM-500 (XRADIA Inc., California, USA) to assess the bonding areas in a nondestructive way. Fig. 13(d) and (e) has been extracted from a 3D CT scan and shows front and top views focused on the bond line. Once the winding has been bonded, NiCuZn ferrite (4F1 from Ferroxcube) bars, previously cut in the correct shape using a diamond blade, have been placed to form the optimal magnetic geometry. Finally, the inductor is potted in thermal conductive silicone to establish a good heat transfer from the core to the substrate.

B. Calorimetric Method

The inductor manufacturing technique used in this work allows to cool the inductor using a direct liquid cooling placed in contact with the bottom of the IMS. To do that, a 3D-printed cooler has been designed and prototyped using high-temperature resin in a stereolithography based printer, as shown in Fig. 14(b). By doing so, once the top of the inductor is properly thermally isolated, Fig. 14(c), it is reasonable to suppose that most of the heat dissipated by the inductor goes through the IMS to the coolant. The inductor losses are equal to the total heat dissipated by the inductor, and with the previous assumption, it is possible to write

$$P_{\text{inductor}} = m_v \rho c_p (T_{\text{out}} - T_{\text{in}}) \tag{24}$$

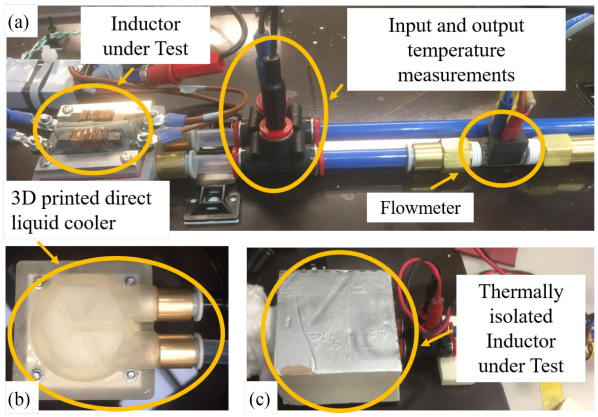

Fig. 14. a) Calorimetric test setup, b) 3D printed liquid cooler, c) inductor after being thermally isolated.

where ρ and c_p are, respectively, the density and the specific heat of the coolant liquid. While m_v is the coolant flow, T_{out} and T_{in} are the temperatures, respectively, at the output and at the input of the cooler. In this test-setup, the temperatures were measured using 4 wires PT100 directly immersed in the liquid just before/after the cooler [Fig. 14(a)]. Being the expected loss values relatively low, in order to have a significant coolant temperature variation, the cooler was operated with a reduced flow rate, thus requiring a high-precision flowmeter (FT-210, 0.1–2.5 L/min).

C. Experimental Measurements

Experimentally measured converter voltages and inductor currents are shown in Fig. 15 for the same POLs considered during the optimization. Orange and purple waveforms are, respectively, the drain-to-source voltages of the bottom devices of the first and second H-bridge legs, V_A and V_B. They are measured using 50 MHz isolated differential voltage probes (CT3685, Cal Test Electronics). The current on the first branch of the inductor i_1 (green waveform) is measured using a Hall effect probe (TCP312 A, Tektronix). While the current flowing on the other branch of the inductor is measured by means of a Rogowsky coil (CWTUM/06/R, PEM), thus giving just the AC ripple,i_{L2} (blue waveform), without the dc component which is visible using the hall effect sensor. Different performances in terms of common mode noise rejection, between the two current probes, result in a different high frequency noise content. In particular, at the switching transitions, the dv/dt is responsible for increased oscillations in the Rogowsky coil measurement.

As expected, for a given POL with smaller inductor, the switching frequency increases. At no load, inductor C is operated at 1.2 MHz while inductor A is operated at 600 kHz; in general, a frequency span from 250 kHz to 1.2 MHz is observed in these examples. On the other hand, with this input–output voltage ratio, a phase shift around 180 is observed as a nearly constant parameter. In order to maintain soft-switching, as the load current increases, the ripple current is increased by reducing the switching frequency. However, in most cases (e.g., all the POLs with load current), a full ZVS would require an excessive

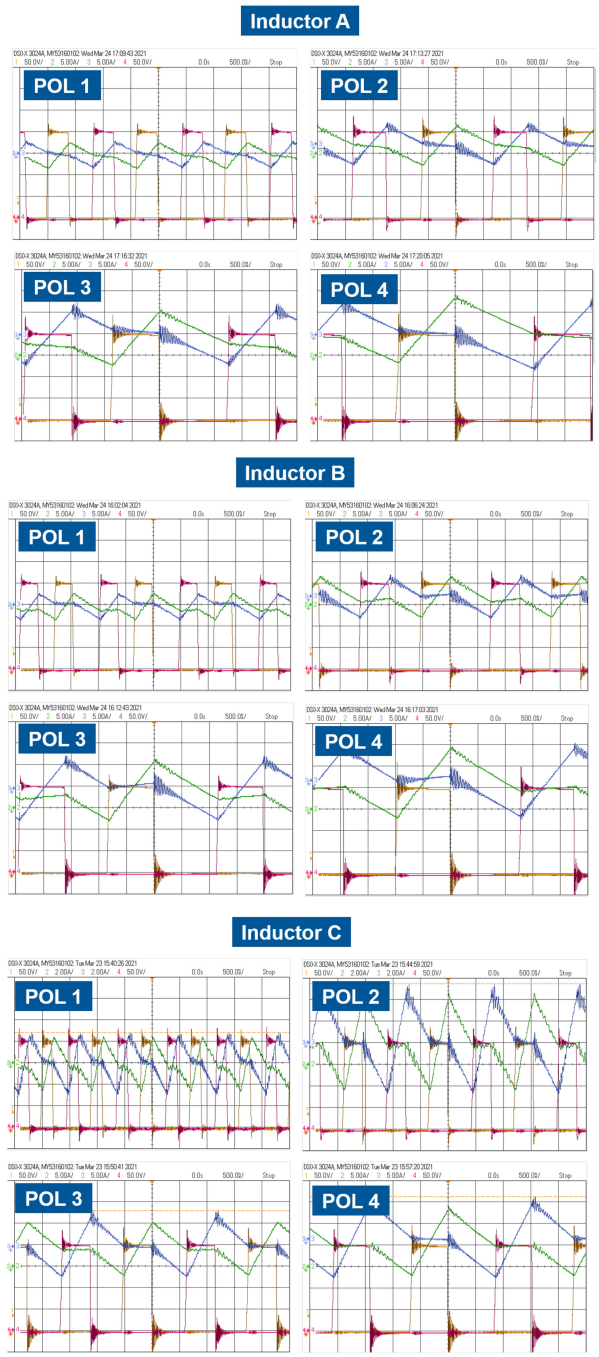

Fig. 15. Experimental voltage and current waveforms for the three different case study inductors. Referring to Fig. 1: V_A (orange), V_B (purple), i_1 (green), i_{L2} AC component of i_2 (blue). YScale: 50 V/ for channel 1 (yellow) and channel 4 (purple); 5 A/ for channel 2 (green) and channel 3 (blue). Time scale: 500 ns.

ripple current, which would negatively affect the other losses components, and for this reason the converter is operated at partial soft switching. In this condition, when the top device turns ON, a slightly negative current is needed to initiate the resonant transition, but since the current level is not sufficient to charge and discharge the output capacitances during the dead time, a portion of the energy stored in the output capacitances is dissipated. This behavior can be clearly identified in the

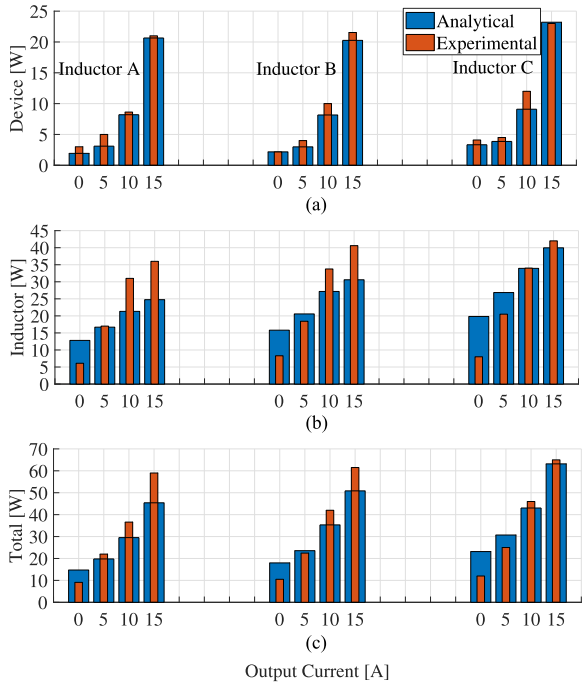

Fig. 16. Comparison between optimization analytical results and experimental results obtained using combined electrical and thermal measurements.

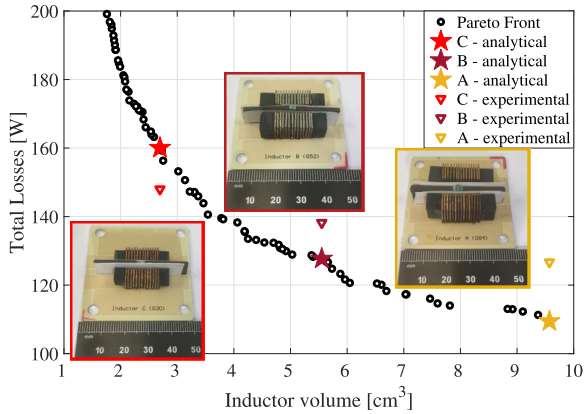

Fig. 17. MPL optimization results: all individuals and Pareto-front and experimentally validated solutions.

POLs with 15 A of load current by observing the change of slope in the voltage waveforms (Fig. 15). Both partial and full ZVS result in decreasing the di/dt, which, as a consequence, reduce the high-frequency voltage oscillations and overshoot across the devices. The overshoot in the drain-to-source voltage measurements shown in Fig. 15 is always below 25%.

Even though differences in duty cycles or in the self-inductances between the two legs could cause unbalance, respectively, in the dc component [37], [38] and in the ac component [39] of the inductor currents, during the tests conducted on these prototypes, no significant current unbalance has been observed. From Fig. 15, the ripple currents in each POL present nearly identical slopes, thus confirming that the self-inductances of the coupled inductor do not present significant differences. In addition to that, it is possible to see that, for all the tested inductor in all the points of load, the drain-to-source voltages across the bottom devices of the two legs are in agreement. This confirms that both phases achieve soft-switching or partial soft switching, depending on the POL, which would not be possible under significant current unbalance. Additional tests, using a single Hall effect sensor, have been conducted to measure the dc unbalance between the phases, which confirmed to be negligible (always below 40 mA).

Fig. 16 summarizes the comparison between analytical model results and the experimentally measured converter losses in the current-inductor space. The analytically calculated device losses show a consistent trend that well agrees with the measurements in the whole load range. On the contrary, the inductor losses trend is not perfectly consistent with the predicted one. In particular, there are POLs at lower current and higher frequencies in which the model overestimates the losses, whereas at higher current and lower frequency, it underestimates. Taking into account the results obtained from the software validation, presented in Fig. 11, and considering that transient FEM simulation with appropriate mesh in the conductors is capable of describing the losses mechanisms in the winding (skin and proximity effect) with excellent accuracy, it is reasonable to conclude that the major source of error is the core loss model. Indeed, by using the iGSE approach to estimate the core losses during the design optimization, it is not possible to take into account dc bias, relaxation effects, and variation of SE coefficients with frequency. The mismatch between expected and measured core losses can be ascribed to these phenomena. Considering the gathered information throughout the simulation and experimental work, it is difficult to conclude if any of these phenomena contributes more than the others.

Fig. 17 summarizes the optimization results and the experimental measurements on the three prototyped inductors. Although there is a discrepancy between the expected and measured performance, the overall trend is respected, which implies that the optimality of the obtained solutions is guaranteed.

VIII. Conclusion

Automated design and MO optimization have been pictured as potential methodologies to meet the growing demand of more power dense power electronics. In this article, general analytical loss models have been presented and applied to a converter topology, which is particularly challenge to design being described by a relevant number of design variables affecting different physical domains. Each constituent component of the mutually coupled interleaved H-bridge has been modeled, carefully balancing the trade-off between accuracy of the performance evaluation and requested computational effort. Once built all the submodels, a comprehensive design optimization strategy has been proposed, which allows to fully consider the interaction among all the converter components, thus avoiding reaching suboptimal solutions typical of hierarchical (or component independent) design approach. In addition, the proposed optimization workflow permits to take into account different operating POLs during the search, thus guaranteeing optimal performance over a wide operating range. To achieve such ambitious aims, a nested optimization workflow has been implemented. On the one hand, the inner

optimization loop tries to identify the optimal modulation strategy for a given inductor geometry and POL to reduce the total converter loss. On the other hand, the outer optimization loop targets the minimization of both inductor volume and weighted total losses for each considered operating point, subject to the constraint on the maximum device and inductor temperatures.

This optimization routine has been applied to four POL dc–dc converter applications, using GaN-HEMT devices and operating at 200 V of input voltage and 48 V of output voltage.

Three optimal results with different inductor geometries and modulations have been selected to perform a validation of the model. At first, the optimization results have been compared to the results obtained using commercial software: LT spice for the device losses and Ansys Maxwell for the losses in the inductor. These commercial software are the standards in their specific field; however, they are too computationally expensive to be included in an optimization workflow. The software validation shows an average deviation of 7.7% on total losses between the presented model and the alternative commercial software. This confirms that the proposed model enables to carry out a multiobjective and multivariables optimization without compromising the accuracy of the results.

The prototype of the GaN based H-bridge has been built together with the three inductors that were considered for the software validation. Additional effort has been invested in a losses measurement technique that allows to measure separately the losses in the GaN devices and in the inductor. A calorimetric test setup has been built exclusively for the measurements of the inductor losses, while the total losses have been measured by means of a precision power analyzer.

By analyzing the voltage and current waveforms, it is clear that a modulation scheme with a phase shift of 180 combined with an optimal inductor geometry, providing a magnetic coupling of 0.3, results in an advantageous current waveform with an extend plateau.

While a hierarchical design approach would suggest to always adopt complete soft switching to minimize the switching losses, by considering simultaneously inductor and device losses, at higher load currents, full soft switching leaves place to partial soft switching to reduce the current ripple and inductor losses.

The losses measurements show that the main trend of the optimization Pareto-front is respected, confirming that the suggested method can be used to perform optimal design of converters when a large research space has to be investigated. Given the inevitable deviation between the estimated and measured losses, the optimization results can also be used to restrict the research space and perform a more detailed optimization.

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Andrea Stratta received the B.Eng. degree in energy engineering and the M.Eng. degree in electrical engineering from the University of Pisa, Pisa, Italy, in 2014 and 2017, respectively. He is currently working toward the Ph.D. degree with the Power Electronics, Machines and Control Group, University of Nottingham, Nottingham, U.K.

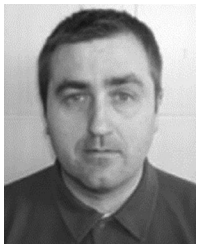
He was with the German Corporate Research Center of ABB AG, Ladenburg, Germany, in 2017. His research interests include soft magnetic materials, electromagnetic components integration, and high-power density energy conversion techniques.

Davide Gottardo received the B.Eng. and M.Eng. degrees in electrical engineering from the University of Pisa, Pisa, Italy, in 2012 and 2015 respectively, and the Ph.D. degree in power electronics from the University of Nottingham, Nottingham, U.K., in 2020.

In 2016, he joined the Power Electronics, Machines and Control (PEMC) Group, University of Nottingham, Nottingham, U.K. He is currently with the Thinking Pod Innovations Ltd. (TTPi), Nottingham. His research interests include design and control of novel topologies for grid-connected power converters for distributed generation and/or energy storage solutions.

Mauro Di Nardo received the M.Sc. (Hons.) degree in electrical engineering from the Polytechnic University of Bari, Bari, Italy, in 2012, and the Ph.D. degree in electrical machine design from the University of Nottingham, Nottingham, U.K., in 2017.

From 2017 to 2019, he was Head with the AROL R&D Team, Polytechnic University of Bari. Since 2019, he has been a Research Fellow with the Power Electronics and Machine Control Group, University of Nottingham. His research interests include the analysis, modeling, and design optimizations of permanent magnet and synchronous reluctance machines for automotive, aerospace and household sectors, induction motor for industrial applications, as well as niche machine topologies such as bearingless and hysteresis motor.



Jordi Espina received the M.Eng. and Ph.D. degrees in electrical and electronics engineering from the Universitat Politecnica de Catalunya, Catalonia, Spain, in 2005 and 2011, respectively.

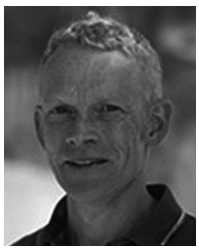
From 2013 to 2017, he was a Research Fellow with the Power Electronics Machines and Control Group (PEMC), University of Nottingham, Nottingham. From 2017 to 2020, he was a Senior Electronic Engineer with the Thinking Pod Innovations (TTPi), Nottingham. He is currently an R&D Electronic Team Leader with Circontrol s.a, Viladecavalls, Catalonia. His research interests include variable-speed drive systems, electromagnetic compatibility, power electronics converters, and smart electric vehicle charging.

Liliana de Lillo received the M.Eng. degree in electronic engineering from Politecnico di Bari, Bari, Italy, in 2001, and the Ph.D. degree in electrical engineering from Power Electronics, Machines and Control (PEMC) Group, University of Nottingham, Nottingham, U.K., in 2006.

She was a Research Fellow and Senior Research Fellow with the PEMC Group, University of Nottingham, in 2007 and 2012, respectively.

Lee Empringham (Member, IEEE) received the B.Eng. (Hons.) and Ph.D. degrees in electrical and electronic engineering from the University of Nottingham, Nottingham, U.K., in 1996 and 2000, respectively.

He was a Principal Research Fellow with the Power Electronics, Machines, and Control Group, University of Nottingham, in 2010, where he was a Full Professor in 2017, and is currently a Research Fellow. His research interests include direct ac–ac power conversion, variable-speed ac-motor drives using different circuit topologies, more-electric aircraft applications, power electronics integration, and high-power-density power conversion techniques.



Mark C. Johnson received the B.A. degree in engineering and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in 1986 and 1991, respectively.

From 1990 to 1992, he was a Research Associate with the University of Cambridge, and in 1992, he was a Lecturer with the University of Newcastle, Newcastle upon Tyne, U.K. From 1998 to 2001, he managed the U.K. national programme on silicon carbide electronics, and in 2000, he was a Reader of Power Electronics with the University of Newcastle. In 2003, he was a Rolls-Royce/RAEng Research Professor of Power Electronic Systems with the University of Sheffield, Sheffield, England, U.K., and in 2006, he was a Personal Chair with the University of Nottingham, Nottingham, U.K. He was the Director of the U.K. Engineering and Physical Sciences Research Council (EPSRC) Centre for Power Electronics, Swindon, U.K. He holds two patents.