Non-Isolated DC-DC Converters With Low Common-Mode Noise by Using Split-Winding Configuration

Lihong Xie, *Member, IEEE*, and Xibo Yuan, *Senior Member, IEEE*

***Abstract*—The common-mode (CM) noise in nonisolated dc-dc converters is mainly caused by the displacement current through the high *dv/dt* node in the circuit and the associated parasitic capacitance, and it may cause electromagnetic interference (EMI) to the surrounding equipments. To reduce the original CM noise and shrink the EMI filter size of non-isolated dc-dc converters, CM noise cancellation methods have been proposed, including the symmetry circuit, balancing technique, passive cancellation and CM voltage cancellation. In these methods, additional components or windings are required for reducing the CM noise. In this article, a new CM noise cancellation method in non-isolated dc–dc converters is proposed by adopting a split-winding configuration. Compared to the existing CM noise cancellation methods which require additional components, the proposed method in the buck, boost and single-ended primary-inductor converter (SEPIC) converters which runs in voltage step-up mode has the identical volume as their conventional circuit configurations. The proposed method is verified for a buck converter by experiment.**

***Index Terms*—Common-mode (CM) noise cancellation, CM noise, nonisolated dc–dc converter, split-winding (SW) configuration.**

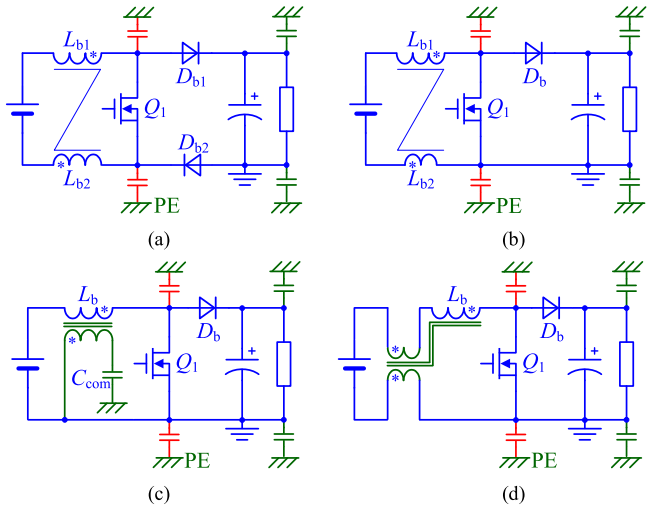

Fig. 1. Circuit implementation for the existing CM noise cancellation methods in the boost converter. (a) Symmetry circuit. (b) Balancing technique. (c) Passive cancellation. (d) The CMVC method.

I. Introduction

IN NONISOLATED dc–dc converters, the common-mode (CM) noise is mainly caused by the displacement current flowing through the high *dv/dt* nodes in the circuit and the associated parasitic capacitance between these nodes and the protective earth (PE) [1]–[4]. The CM noise of the converter propagates through both the power lines and returns from the PE, and may cause electromagnetic interference (EMI) to the electrical equipments nearby. To attenuate the CM noise, EMI filters are usually inserted in the input or output power cords, which usually take considerable volume and limit the system power density and efficiency [5]–[9].

In order to shrink the EMI filter size, CM noise cancellation methods are usually adopted to reduce the original CM noise, which is realized by generating out-of-phase compensation current (voltage) to cancel the CM current (voltage) of the converter [10]–[14]. As the configuration of conventional non-isolated converters is asymmetrical, the CM noise cannot be cancelled within the converter, so the circuit configuration of the power converter is modified for creating the branch with cancellation current (voltage) for enabling the CM noise cancellation capability. As a result, the symmetry circuit [10], [11], balancing technique [12], passive cancellation [13] and the CM voltage cancellation (CMVC) method [14] have been proposed to reduce the original CM noise of the converter.

Take the boost converter as an example, Fig. 1 shows the circuit implementation for the existing CM noise cancellation methods, where the CM parasitic capacitance between the circuit nodes and the PE are included. In Fig. 1(a), by adding active or passive components and making the circuit symmetrical, the symmetry circuit creates pairs of nodes with complementary *dv/dt*, so the CM current flowing from these nodes to the PE via the associated CM parasitic capacitance can be cancelled by each other. The symmetry circuit helps to create compensation voltage source in the circuit, and its major concern is the increased hardware cost and power losses. As shown in Fig. 1(b), instead of creating a symmetrical configuration, the balancing

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The authors are with the Department of Electrical and Electronic Engineering, University of Bristol, BS8 1UB Bristol, U.K. (e-mail: xie.lihong@bristol.ac.uk; xibo.yuan@bristol.ac.uk).

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technique reduces the CM noise by impedance balance [12]. The CM parasitic capacitance between the load and the PE needs to be concerned, as it is involved in the impedance balance for CM noise reduction.

As an alternative method, the passive cancellation shown in Fig. 1(c) reduces the CM noise by adding a branch to cancel the CM noise current of the converter [13]. The branch consists of a compensation capacitor and a compensation winding coupled with the inductor in the main circuit. As the duality scheme to the passive cancellation method, the CMVC method given in Fig. 1(d) cancels the CM voltage of the converter by injecting compensation voltage in the circuit [14], and the compensation voltage is implemented by CMVC winding coupled with the inductor in the main circuit. In these two methods, additional windings are required to induce the desired compensation voltage.

Since the CM noise propagates between the power cords and the PE, the CM current could appear at both the input and output sides [15]–[17]. Although the CM noise at the input side is mainly concerned for non-isolated dc–dc converters, the CM noise at the output side may also cause EMI to the equipment such as the devices with touch screen [16]. Therefore, the capability of CM noise reduction at both sides for the conventional CM noise cancellation methods needs to be further investigated. The symmetry circuit and passive cancellation method is capable of reducing the CM noise at both sides, because the noise current is confined within the converter rather than flowing into the input or output side. However, for the balancing technique and the CMVC method, only the CM noise at the input side can be reduced. In these two methods, a coupled winding is placed between the input source ground and the output load ground. As the voltage across this coupled winding has high *dv/dt* characteristics, there is still CM noise current flowing through the CM parasitic capacitance between the load and the PE, and the output side CM noise still exists.

In this article, a new CM noise cancellation method is proposed by using split-winding (SW) configuration. The inductor windings are split and redistributed at the input side, the ground side and the output side, which modulates the electric potential of the nodes in the circuit for cancelling the CM noise. The split windings for the proposed method can be integrated into the original filter inductor, and the total winding dimension in the buck, boost and SEPIC converter which runs in voltage step-up mode is the same as their conventional configurations. Moreover, the CM noise at both sides can be reduced simultaneously by the proposed method.

The rest of this article is organized as follows. In Section II, the CM noise model of the buck converter is derived, which considers the CM impedances at the input and output sides. In Section III, the derivation of the proposed method in the buck converter is given. The total winding dimension is calculated, and the current balance viewpoint is discussed. In Section IV, the CM noise reduction is studied by considering the effect of imperfect coupling between the windings. In Section V, the applications of the proposed method in other non-isolated power converters are discussed. In Section VI, a conventional buck converter and the buck converter with the SW configuration are built, and the CM noise current are measured and compared. Finally, Section VII concludes this article.

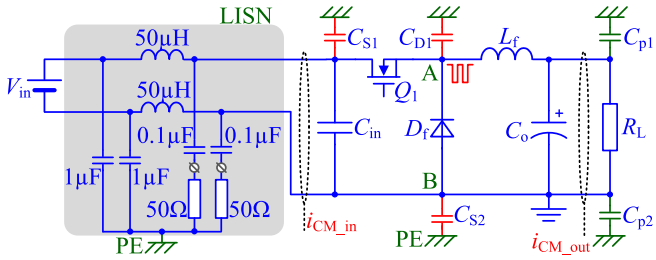

Fig. 2. Buck converter and its related CM parasitic capacitances.

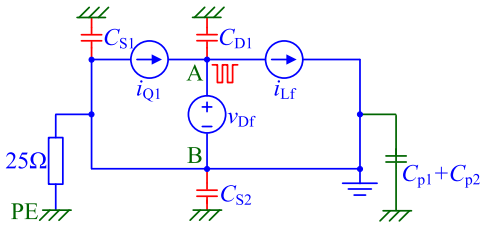

Fig. 3. CM noise circuit with substituted sources.

II. CM Noise Model of Buck Converter Considering CM Impedance at the Input and Output Sides

The buck converter is taken as an example for deriving the CM noise model, which includes the CM impedances at the input and output sides. As seen in Fig. 2, during the CM EMI test, line impedance stabilization network (LISN) is inserted between the input voltage source and the converter input side to provide specific impedance for the CM noise current [18]. The CM parasitic capacitances of the converter include C_{S1} between the drain of Q_1 and the PE, C_{D1} between the cathode of D_f and the PE, and C_{S2} between the power ground (PG) and the PE. In addition, the capacitance C_{p1} and C_{p2} represent the CM path between the load and the PE.

To derive the CM noise circuit of the buck converter, the freewheeling diode D_f is replaced with a voltage source that replicates its waveform, owing to the high *dv/dt* characteristics of node A in the circuit. The input capacitor $C_{\rm in}$ and output capacitor $C_{\rm o}$ is treated as short circuit, because the *dv/dt* of their voltage is much smaller than that of the voltage across D_f. The switch Q_1 and inductor L_f are replaced with current sources that replicate their waveform, for avoiding voltage loops or current nodes [12]. For the CM noise, the CM impedance at the LISN side can be simplified as a 25 Ω resistor, and the CM impedance at the output side is essentially the parallel of C_{p1} and C_{p2}. The resultant CM noise circuit with substituted sources is shown in Fig. 3.

Superposition theorem is applied to simplify the equivalent circuit in Fig. 3. First, the voltage source v_{DF} is shorted to only consider the excitation of current sources $i_{\rm Q1}$ and i_{Lf}. Since i_{Q1} and i_{Lf} are essentially shorted, the current sources do not cause CM noise. Second, by opening the current sources i_{Q1} and i_{Lf}, the resultant circuit is given in Fig. 4(a). By using Thevenin

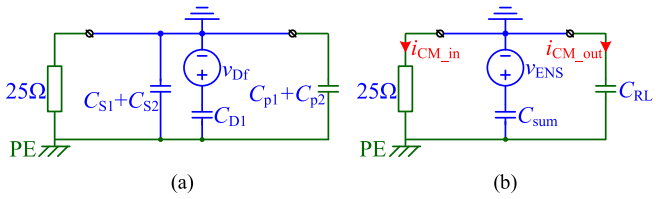

Fig. 4. Simplified CM noise circuit. (a) With v_{Df}. (b) With $v_{\rm ENS}$.

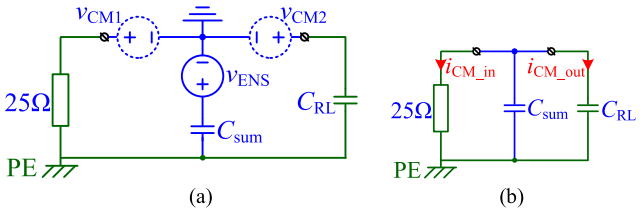

Fig. 5. Principle of CMVC for input and output sides. (a) Adding two voltage sources. (b) Circuit with voltage sources cancelled.

theorem to simplify the CM noise model of the buck converter, the CM noise circuit is simplified as a voltage source $v_{\rm ENS}$ which is the equivalent noise source (ENS) [19] of the buck converter and the capacitance $C_{\rm sum}$, as shown in Fig. 4(b). The terms $v_{\rm ENS}$, $C_{\rm sum}$, and C_{RL} are expressed as

$$v_{\rm ENS} = k_{\rm buck} v_{Df} \tag{1}$$

$$C_{\rm sum} = C_{D1} + C_{S1} + C_{S2} \tag{2}$$

$$C_{RL} = C_{p1} + C_{p2} \tag{3}$$

where the coefficient $k_{\rm buck}$ is given by

$$k_{\rm buck} = C_{D1}(C_{\rm sum})^{-1}. \tag{4}$$

As the voltage across D_f and L_f have the same ac component [13], the ENS of the buck converter can be also written as

$$v_{\rm ENS} = k_{\rm buck} v_{Lf}. \tag{5}$$

With the CM noise model of the buck converter in Fig. 4(b), the CM noise cancellation method will be discussed in the next section, which aims to reduce the CM noise $i_{\rm CM\_in}$ and $i_{\rm CM\_out}$ at the input and output sides simultaneously.

III. CM Noise Cancellation for Buck Converter

A. Derivation of the CM Noise Cancellation Method

According to Fig. 4(b), for eliminating the CM current $i_{\rm CM\_in}$ and $i_{\rm CM\_out}$, the voltage source $v_{\rm ENS}$ should be eliminated. The principle of eliminating the $v_{\rm ENS}$ in the circuit is given in Fig. 5(a), where two voltage sources $v_{\rm CM1}$ and $v_{\rm CM2}$ are inserted in the circuit. As long as $v_{\rm CM1} = v_{\rm CM2} = v_{\rm ENS}$, these voltage sources cancel each other because the positive terminals of these voltage sources are equipotential. By shorting these positive terminals, the voltage sources can be removed and zero

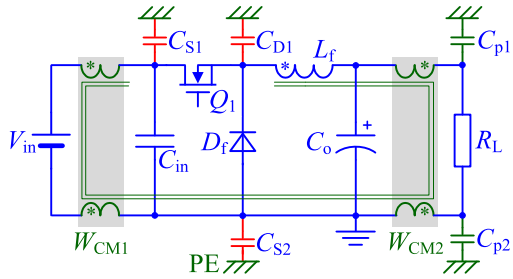

Fig. 6. Realization of CMVC for the input and output sides.

CM current can be anticipated. The resultant circuit of Fig. 5(a) is given in Fig. 5(b).

Referring to Fig. 5(a), the voltage sources $v_{\rm CM1}$ and $v_{\rm CM2}$ are located at the converter input and output side, respectively. In order to derive the corresponding circuit realization, $v_{\rm CM1}$ and $v_{\rm CM2}$ are implemented by CM windings [14] which are coupled with the inductor $L_{\rm f}$, as shown in Fig. 6. The turns $N_{\rm CM}$ of each winding in $W_{\rm CM1}$ and $W_{\rm CM2}$ are the same, which is equal to

$$N_{\rm CM} = k_{\rm buck} N_{Lf} \tag{6}$$

where N_{Lf} is the turns of inductor winding L_f.

The circuit in Fig. 6 can be simplified as follows. Firstly, the output capacitor $C_{\rm o}$ can be shifted to the right side of the CM winding $W_{\rm CM2}$, as shown in Fig. 7(a). This is because the voltage across $C_{\rm o}$ in Fig. 6 is the same as the voltage across R_L, when the leakage inductance for the windings in $W_{\rm CM2}$ is neglected. Secondly, the inductor winding of L_f and the upside winding in $W_{\rm CM2}$ in Fig. 7(a) can be combined into a single winding owing to their serial connection. The combined winding has $(1–k_{\rm buck})N_{Lf}$ turns as the original two windings are differentially coupled. Finally, according to Fig. 7(c), the dotted terminals in the downside windings have the same electric potential owing to the same turns. Therefore, these two dotted terminals can be connected together. By paralleling these two windings, the resultant circuit is given in Fig. 8. The operation principle of this converter is essentially the same as the conventional buck converter, as discussed below.

B. Operation Principle

In Fig. 8, the average voltage across each winding is zero when the converter runs at steady state, so the average voltage across the input filtering capacitor $C_{\rm in}$ is equal to $V_{\rm in}$ according to Kirchhoff's voltage law. The subcircuits with Q_1 turned on, D_f turned ON and Q_1 and D_f both turned OFF are given in Fig. 9(a)–(c). In the following analysis, the voltage ripple in the capacitors $C_{\rm in}$ and $C_{\rm o}$ is neglected as they are small compared to their respective dc component. In Fig. 9(a), the branches with $V_{\rm in}$ and $W_{\rm IN}$, $C_{\rm in}$ and $W_{\rm GND}$ are in parallel. Because the voltage across $C_{\rm in}$ is $V_{\rm in}$, by swapping the position of $C_{\rm in}$ and $W_{\rm GND}$, the windings $W_{\rm IN}$ and $W_{\rm GND}$ are essentially in parallel, as shown in Fig. 9(d). In Fig. 9(b), the branch with $V_{\rm in}$, $W_{\rm IN}$, and $C_{\rm in}$ can be simplified as a single winding $W_{\rm IN}$, because $V_{\rm in}$ cancels the voltage across $C_{\rm in}$. The resultant circuit is given in Fig. 9(e). In Fig. 9(c), as the switches are both turned OFF, the current through

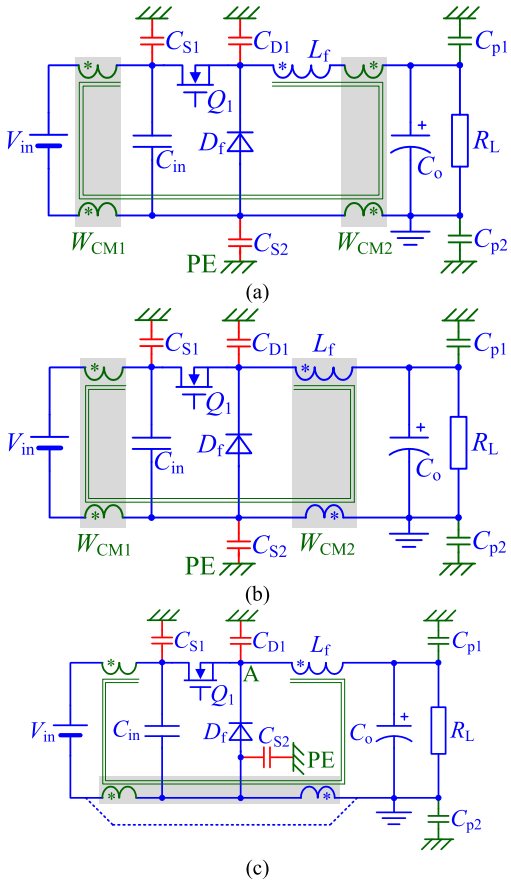

Fig. 7. Simplification of the circuit by. (a) Shifting C_o to the right side. (b) Combining the upside two windings. (c) Paralleling the downside windings.

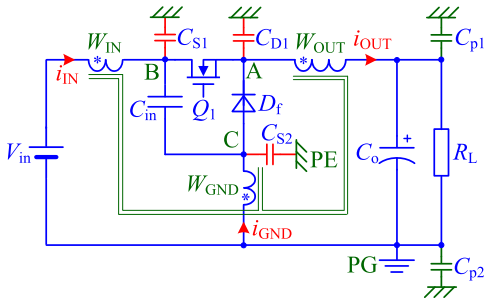

Fig. 8. SW buck converter for the CM noise reduction.

each winding is zero, Q_1 sustains the difference between input and output voltage and D_f sustains the output voltage as the conventional buck converter in discontinuous conduction mode. The lighter the load is, the longer this load dependant interval [20] will be.

As seen in Fig. 9(d) and (e), the windings $W_{\rm IN}$ and $W_{\rm GND}$ are in parallel and then in series with $W_{\rm OUT}$, which can be simplified into a single inductor by decoupling these windings. Noticed that $W_{\rm IN}$ and $W_{\rm GND}$ are in parallel and have the same turns number, their paralleled branch can be simplified into a single winding $W_{\rm IG}$ coupled with $W_{\rm OUT}$ to simplify the analysis, as shown in Fig. 9(f). Owing to the cumulative connection, the equivalent inductance of this branch is expressed as

$$L_{\rm eq} = L_{\rm IG} + L_{\rm OUT} + 2M_{\rm IG-O} \tag{7}$$

where $L_{\rm IG}$ and $L_{\rm OUT}$ are the self inductance of $W_{\rm IG}$ and $W_{\rm OUT}$, $M_{\rm IG\text{-}O}$ is the mutual inductance between $W_{\rm IG}$ and $W_{\rm OUT}$. These parameters can be obtained by paralleling $W_{\rm IN}$ and $W_{\rm GND}$, and measuring the self inductance by open circuit test and calculating the mutual inductance by cumulative connection of $W_{\rm IG}$ and $W_{\rm OUT}$.

After substituting the inter-connected coupled windings in Fig. 9(d) and (e) with an equivalent inductor $L_{\rm eq}$, it can be concluded that the operation principle of the proposed converter configuration is identical to the buck converter as their subcircuits are essentially the same.

C. Comparison of the Total Winding Dimension

Compared to the conventional buck converter with a single filtering winding, three windings appear in the proposed circuit shown in Fig. 8, which makes the winding structure complicated. Nevertheless, it can be proved that the total winding dimension which occupies the core window in these two cases is the same, as discussed below.

For the conventional buck converter, by assuming that the current ripple of the filter inductor is 20% with respect to its dc component $I_{\rm OUT}$ (the nominal load current), the root mean square (rms) value of the inductor current is very close to its dc value [20]. Therefore, the total winding dimension of the filter inductor $L_{\rm f}$ can be expressed as

$$A_W = N_{Lf} I_{\rm OUT} J^{-1} \tag{8}$$

where J is the current density.

For the buck converter with the proposed configuration in Fig. 8, the winding dimension ($A_{\rm WIN}$, $A_{\rm WGND}$, and $A_{\rm WOUT}$) of each winding ($W_{\rm IN}$, $W_{\rm GND}$, and $W_{\rm OUT}$) is given by

$$A_{\rm WIN} = k_{\rm buck} N_{\rm Lf} I_{\rm IN} J^{-1} \tag{9}$$

$$A_{\rm WGND} = k_{\rm buck} N_{\rm Lf} \left(I_{\rm OUT} - I_{\rm IN}\right) J^{-1} \tag{10}$$

$$A_{\rm WOUT} = \left(1 - k_{\rm buck}\right) N_{\rm Lf} I_{\rm OUT} J^{-1} \tag{11}$$

where $I_{\rm IN}$ is the input dc current of the converter.

By adding the winding dimension from (9) to (11), the total winding dimension is equal to the result in (8), so the total winding dimension is not increased. By using the same core for the original single winding to accommodate these split windings, the total volume of the inductor is not changed. An intuitive demonstration is given in Fig. 10 for a better understanding of the SW configuration.

D. Current Balance Viewpoint of the Proposed Method

To have a better understanding of the circuit in Fig. 8 for reducing the CM noise, the high *dv/dt* nodes in the circuit are plotted in Fig. 11. As seen, the electric potential v_A, v_B, and v_C

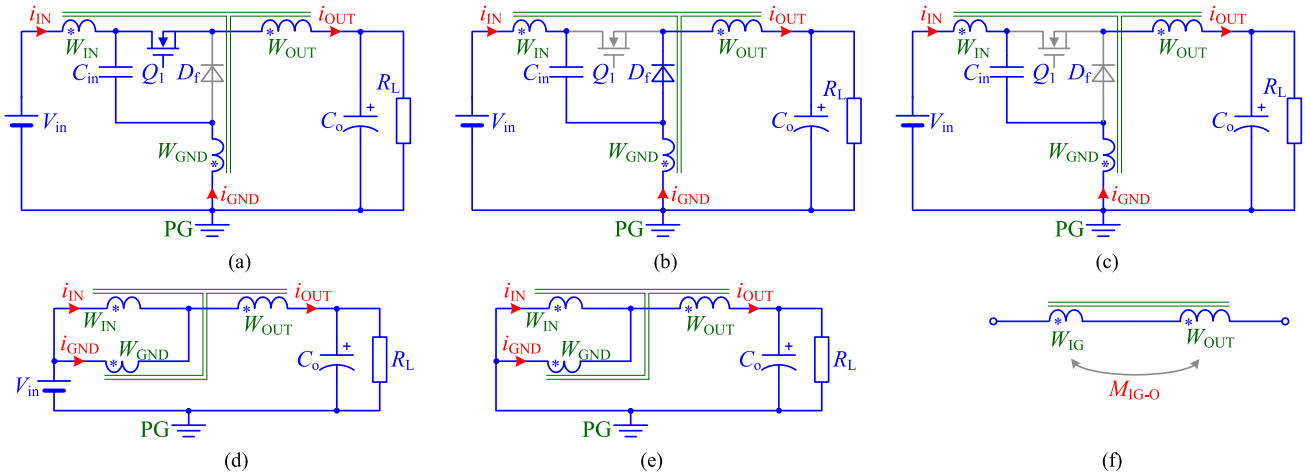

Fig. 9. Subcircuits of the proposed converter. (a) Q_1 is turned ON. (b) D_f is turned ON. (c) Q_1 and D_f are both turned OFF. (d) Equivalent circuit when Q_1 is turned ON. (e) Equivalent circuit when D_f is turned ON. (f) Equivalent circuit for the series-parallel connected coupled inductors.

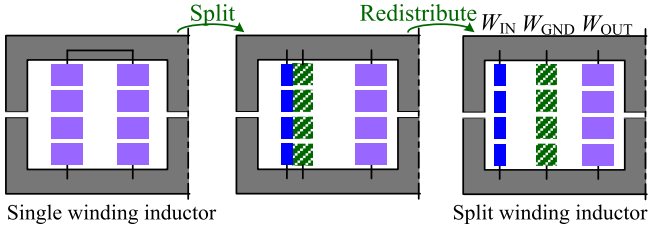

Fig. 10. Demonstration for understanding the SW configuration.

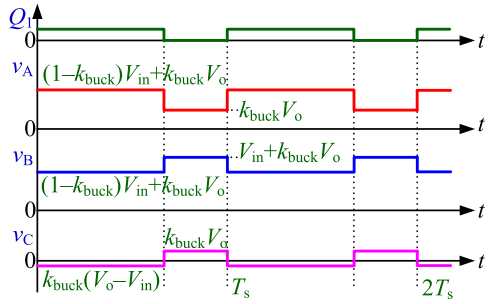

Fig. 11. Waveforms of v_A, v_B, and v_C in the circuit.

for the nodes *A*, *B,* and *C* in Fig. 8 with respect to the PG satisfies the following relationship:

$$\left(\frac{k_{\text{buck}}}{k_{\text{buck}}-1}\right)\frac{dv_A}{dt}=\frac{dv_B}{dt}=\frac{dv_C}{dt}. \tag{12}$$

By substituting (4) into the left coefficient in (12), yields

$$C_{D1}\frac{dv_A}{dt}+(C_{S1}+C_{S2})\frac{dv_B}{dt}=0. \tag{13}$$

Referring to the right part in (12), (13) is rewritten as

$$C_{D1}\frac{dv_A}{dt}+C_{S1}\frac{dv_B}{dt}+C_{S2}\frac{dv_C}{dt}=0. \tag{14}$$

As seen from (14) and Fig. 8, the displacement current flowing through the associated parasitic capacitances are canceled by each other, indicating that the CM noise is confined within the converter rather than propagating into the source or the load side. In this sense, the proposed CM noise cancellation method modifies the electric potential of the high *dv/dt* nodes in the circuit. By building out-of-phase *dv/dt* nodes and utilizing the parasitic capacitance in the circuit, the CM noise is reduced. This principle is similar with the symmetry circuit, while additional component is not required. For the convenience of discussion, the proposed configuration is denoted as the SW configuration.

IV. Balance Condition Considering Imperfect Coupling

For the SW buck converter in Fig. 8, three windings are coupled and their coupling would not be perfect in practical applications, which may influence the CM noise reduction. In this Section, the effect of imperfect coupling is discussed.

To derive the CM noise equivalent circuit for Fig. 8, the circuit with substituted sources is given in Fig. 12(a). By simplifying the circuit in Fig. 12(a), the resultant circuit is given in Fig. 12(b), which has a bridge circuit in the middle. As long as the bridge is balanced, the CM noise current at the converter input and output sides are both equal to zero.

To derive the balance condition for the circuit in Fig. 12(b), the windings W_{IG} and W_{OUT} are decoupled, and the circuit is given in Fig. 12(c). The balance condition is

$$\frac{L_{\text{IG}}+M_{\text{IG-O}}}{L_{\text{OUT}}+M_{\text{IG-O}}}=\frac{C_{D1}}{C_{S1}+C_{S2}}. \tag{15}$$

In practical applications, the parasitic capacitances C_{S1} and C_{D1} are dominant compared with C_{S2}, because C_{S1} and C_{D1} are formed between the switches and the heatsink which are typically larger than C_{S2}. In addition, C_{S1} and C_{D1} are nearly equal if the same type of insulation material with the equal thickness is used between the switches and the heatsink. Therefore, the coefficient k_{buck} is equal to 0.5 according to (4), so the turns number of W_{IN}, W_{GND}, and W_{OUT} are equal. For a compact design of magnetic component in the SW buck converter, the

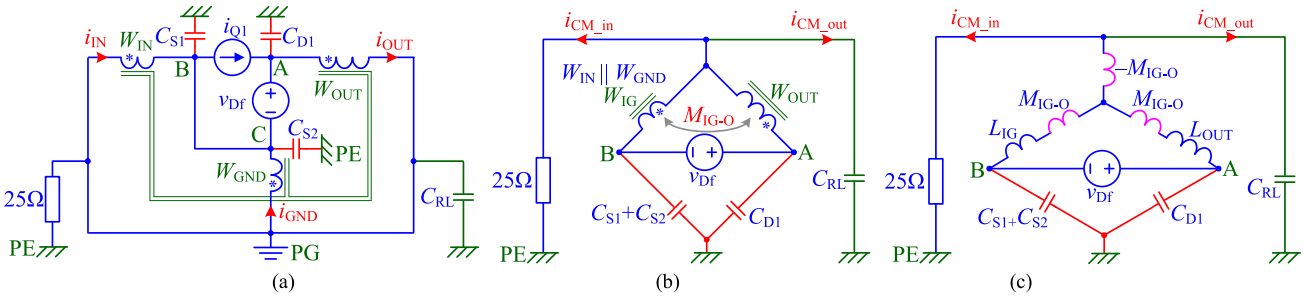

Fig. 12. CM noise circuit of the SW buck converter. (a) CM noise circuit with substituted sources. (b) Simplified circuit. (c) Decoupled circuit.

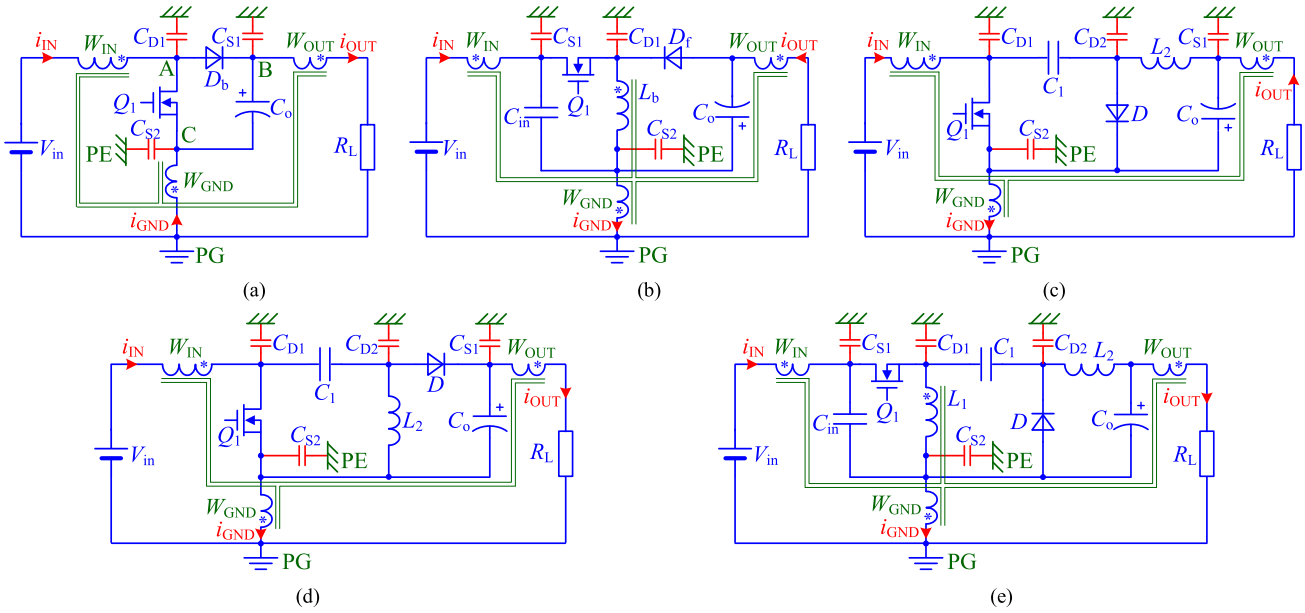

Fig. 13. Nonisolated SW converter. (a) Boost Converter. (b) Buck–boost converter. (c) Cuk converter. (d) SEPIC converter. (e) Zeta converter.

windings should be wound in the same core to achieve tight coupling. As a result, the self inductance $L_{\rm IG}$ and $L_{\rm OUT}$ are nearly the same, and the balance condition in (15) for CM noise reduction can be satisfied without adding external capacitor to achieve balance.

V. The Applications in Other Nonisolated Converters

Referring to the discussions in Sections II and III, the application of the proposed SW configuration in other nonisolated dc—dc converters can be derived, as given below.

The SW boost converter can be directly derived from the SW buck converter, as their power flow direction is reversed to each other. The related circuit is shown in Fig. 13(a). The winding turns of $W_{\rm IN}$, $W_{\rm GND}$ and $W_{\rm OUT}$ are

$$N_{\rm IN} = (1 - k_{\rm boost})\, N_{Lb} \tag{16}$$

$$N_{\rm GND} = N_{\rm OUT} = k_{\rm boost} N_{Lb} \tag{17}$$

where N_{Lb} is the turns of boost inductor winding, and $k_{\rm boost}$ is the same as (4).

For the other nonisolated dc–dc converters, the circuit using SW configuration are listed in Fig. 13(b)–(e). For the buck–boost converter in Fig. 13(b), the winding turns of $W_{\rm IN}$, $W_{\rm GND}$ and $W_{\rm OUT}$ are equal to $k_{bb}N_{Lb}$, where k_{bb} is the same as (4), and N_{Lb} is the turns of buck–boost inductor. For the Cuk converter in Fig. 13(c), the winding turns of $W_{\rm IN}$, $W_{\rm GND}$, and $W_{\rm OUT}$ are

$$N_{\rm IN} = (1 - k_{\rm Cuk})\, N_{L1} \tag{18}$$

$$N_{\rm GND} = N_{\rm OUT} = k_{\rm Cuk} N_{L1} \tag{19}$$

where $N_{\rm L1}$ is the turns of the inductor near the input voltage source, and $k_{\rm Cuk}$ is given by

$$k_{\rm Cuk} = (C_{D1} + C_{D2})\,(C_{D1} + C_{D2} + C_{S1} + C_{S2})^{-1}. \tag{20}$$

For the SEPIC converter in Fig. 13(d), the winding turns of $W_{\rm IN}$, $W_{\rm GND}$ and $W_{\rm OUT}$ are

$$N_{\rm IN} = (1 - k_{\rm SEPIC})\, N_{L1} \tag{21}$$

$$N_{\mathrm{GND}} = N_{\mathrm{OUT}} = k_{\mathrm{SEPIC}} N_{L1}. \tag{22}$$

where N_{L1} is the turns of the inductor near the input voltage source, and the coefficient k_{SEPIC} is the same as (20).

For the Zeta converter in Fig 13(e), the winding turns of W_{IN}, W_{GND}, and W_{OUT} are equal to $k_{\mathrm{Zeta}} N_{L1}$, where k_{Zeta} is the same as (20), and N_{L1} is the turns of the inductor L_1.

As seen, for the buck–boost converter and Zeta converter, the added CM windings cannot be combined with the inductor winding in the circuit, so the overall winding dimension is larger than that in the conventional circuit. For the Cuk converter, the average current in W_{GND} is larger than the input current, so the total winding dimension is also larger than that in the conventional circuit.

For the conventional SEPIC converter, the winding dimension of L_1 near the input voltage source is given by

$$A_{W\_\mathrm{SEPIC}} = N_{L1} I_{\mathrm{IN}} J^{-1}. \tag{23}$$

For the SW SEPIC converter, the winding dimension of each coupled winding is

$$A_{\mathrm{WIN\_SEPIC}} = (1 - k_{\mathrm{SEPIC}})\, N_{L1} I_{\mathrm{IN}} J^{-1} \tag{24}$$

$$A_{\mathrm{WGND\_SEPIC}} = k_{\mathrm{SEPIC}} N_{L1} \left| I_{\mathrm{OUT}} - I_{\mathrm{IN}} \right| J^{-1} \tag{25}$$

$$A_{\mathrm{WOUT\_SEPIC}} = k_{\mathrm{SEPIC}} N_{L1} I_{\mathrm{OUT}} J^{-1}. \tag{26}$$

By adding (24) to (26), the total winding dimension A_T is

$$A_T = N_{L1} I_{\mathrm{IN}} J^{-1},\ (I_{\mathrm{IN}} \geq I_{\mathrm{OUT}}) \tag{27}$$

$$A_T = \left[1 + 2k_{\mathrm{SEPIC}} \left(\frac{I_{\mathrm{OUT}} - I_{\mathrm{IN}}}{I_{\mathrm{IN}}}\right)\right] N_{L1} I_{\mathrm{IN}} J^{-1},\ (I_{\mathrm{IN}} < I_{\mathrm{OUT}}). \tag{28}$$

As seen, the total winding dimension of the inductor L_1 in the SW SEPIC converter is equal to that in the conventional SEPIC converter when the input current is higher than the output current (voltage step-up mode). Otherwise, the total winding dimension is larger than that in the conventional SEPIC converter.

VI. Experimental Verification

To verify the effectiveness of the proposed CM noise cancellation method, a buck converter and an SW buck converter are built, and the CM noise at the input and output sides are measured and compared.

Fig. 14 shows the SW buck converter prototype, the inductor with split windings and the inductor for the conventional buck converter. The printed circuit board in Fig. 14(a) is also compatible for building the conventional buck converter by simply shorting the through-holes for accommodating W_{IN} and W_{GND}, respectively. Table I gives the related main circuit parameters.

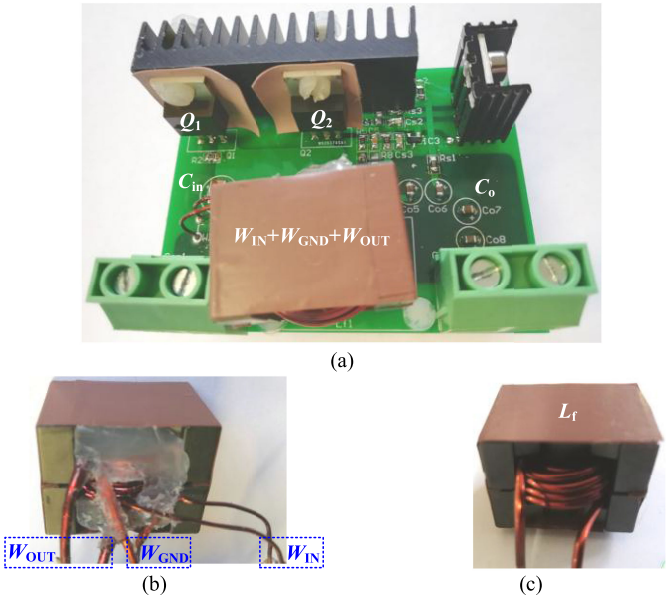

Fig. 14. Photo of the prototype. (a) SW buck converter. (b) Inductor with split windings. (c) Inductor in the conventional buck converter.

TABLE I
MAIN CIRCUIT PARAMETERS OF THE CONVERTER

Input voltage	48 V	Input capacitance C_{in}	180 μF
Output voltage	12 V	Filtering inductance L_{f}	25 μH
Load resistance	1.5 Ω	Output capacitance C_{o}	180 μF
Switching frequency	200 kHz	Capacitance C_{D1}, C_{S1}	27 pF

TABLE II
RELATED PARAMETERS OF THE MAGNETIC COMPONENT

	Inductor w/o split windings	Inductor with split windings		
		W_{IN}	W_{GND}	W_{OUT}
Turns number	14	7	7	7
Winding dimension	1.5 mm	0.7 mm	1.3 mm	1.5 mm
Self inductance	25.16 μH	Paralleled (W_{IG}): 6.54 μH		6.52 μH
Mutual inductance		W_{IG} and W_{OUT}: 6.05 μH		
Weight	45 g	44 g		
Dimension	27.3×19.3×21.6 mm (PQ 26/20 core)			

The capacitance C_{D1} and C_{S1} are measured by the impedance analyzer (WAYNE KERR 6500B) at the test frequency of 100 kHz, and the switches are disconnected from the circuit during the measurement. For the magnetic component in the buck and SW buck converter, the winding dimension and measured parameters are given in Table II. Single strand enameled wire is used for the windings in these inductors. The detailed arrangement and connection of the windings are shown in Fig. 15. The winding W_{IN} is connected between $C_{\mathrm{in}}(+)$ and $V_{\mathrm{in}}(+)$,

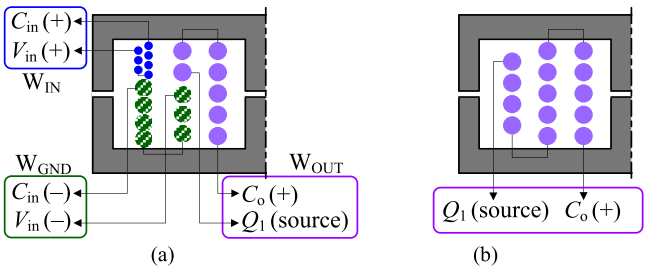

Fig. 15. Winding arrangement for the magnetic components. (a) Inductor with split windings. (b) Inductor in the conventional buck converter.

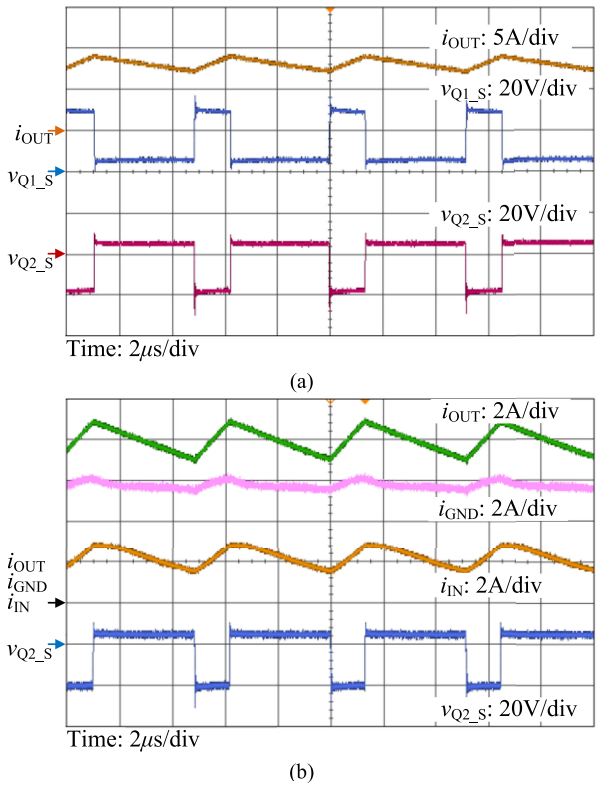

Fig. 16. Operation waveforms of the SW buck converter. (a) Current through W_{OUT} and the electric potential of the source terminals of each switch with respect to the PG. (b) Current through each winding.

which are the positive node of C_{in} and V_{in}, respectively. The winding W_{GND} is placed between $C_{in}(-)$ and $V_{in}(-)$, which are the negative node of C_{in} and V_{in}, respectively. The winding W_{OUT} interconnects the switching node Q_1(source) and the positive node of the output capacitor C_o, whose connection is the same as the inductor winding in the conventional buck converter.

Fig. 16 shows the operation waveforms of the SW buck converter, including the electric potential of the source of the switch Q_1, Q_2 with respect to the PG, the current flowing through the coupled windings. As seen in Fig. 16(a), the current through W_{OUT} is identical to the inductor current in conventional buck converter. Moreover, the electric potential of the observed nodes are complementary, which enables the CM noise cancellation for the SW configuration. In Fig. 16(b), the input current i_{IN} of the SW buck converter is continuous, which is another attractive feature of the SW configuration.

TABLE III
MEASURED RIPPLE CURRENT, DC RESISTANCE, EFFICIENCY AT FULL LOAD AND THE CALCULATED WINDING LOSSES

	Buck	SW buck		
		W_{IN}	W_{GND}	W_{OUT}
Ripple current (A)	2.00	1.30	0.70	2.00
DC resistance (mΩ)	6.81	24.70	5.88	3.15
Winding losses (mW)	406.92	106.86	197.80	191.65
Efficiency (%)	92.57	92.37		

Table III gives the measured ripple current, dc resistance, the total weight and the efficiency of two converters at full load condition, as well as the calculated winding losses of each winding. The dc resistance is measured by a dc milliohm meter (RS PRO RM-805), and the winding losses are calculated with the dc resistance and the dc current of each winding. The other losses for these two converters such as core loss, power semiconductor losses are the same, so it is not compared here. As seen, the total winding losses in the SW buck converter is around 0.1 W higher than that in the buck converter, so its efficiency is slightly lower than that of the buck converter.

When measuring the CM noise, the heatsink is connected to the PE. According to (15) and Table II, the left side in (15) is 1.0016, which means the capacitance C_{D1} should be 0.16% larger than C_{S1}. Considering that C_{S1} is 27 pF, C_{D1} should be 27.0432 pF to achieve balance. In this experiment, balancing capacitor is not added as the 0.0432 pF capacitance is not available. During the measurement of CM noise current, LISN (EMCO 3825/2) is inserted in the input power cord, and two 50 Ω resistors are connected to the radio frequency output of the LISN for providing the specific impedance. In addition, two capacitors C_{p1} and C_{p2} (both equal to 20 pF) are connected between the load positive and the PE, load negative and the PE, respectively. Instead of separating the noise with separators [21], the CM current at both sides is measured. As indicated in Fig. 2, the input and output CM current i_{CM_in} and i_{CM_out} are measured by clamping two high bandwidth current probes (Agilent 1147A) into the input and output power cable, respectively. The CM current data is collected by a digital oscilloscope (Agilent MSO-X 3054A), and the noise spectrum is obtained by fast Fourier transformation using the rectangular window with time length of 100 μs.

Fig. 17 compares the CM noise spectrum of these two buck converters. The input side CM current i_{CM_in} is converted into noise spectrum [22] in dBμV by taking the voltage across the 50 Ω equivalent resistance at the LISN side into account. In Fig. 17(a), the CM noise of the SW buck converter is still higher than the standard EN55022 class B [18] with quasi-peak limit and average (AV) limit, so additional filtering or CM noise

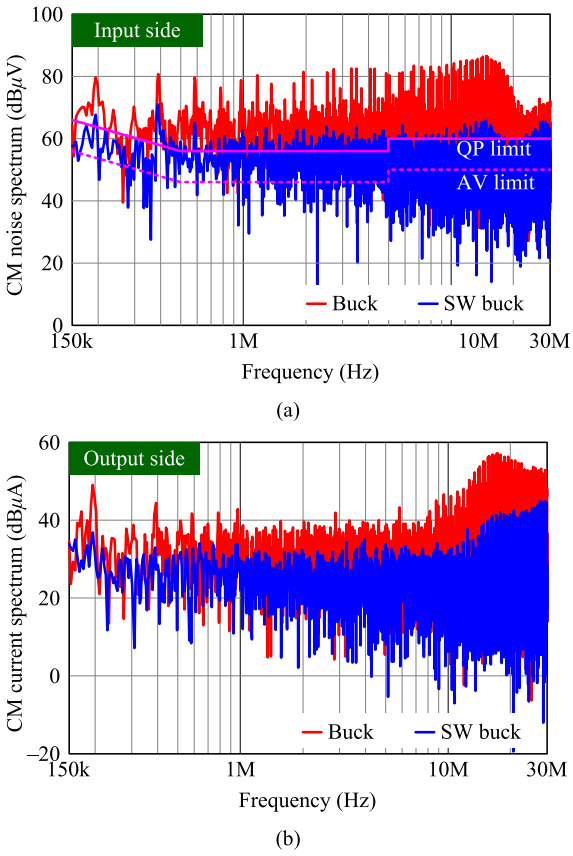

Fig. 17. Comparison of the CM noise of the buck converters. (a) Input side CM noise. (b) Output side CM current.

reduction techniques should be adopted to further suppress the CM noise. However, as seen in Fig. 17(a), 10 to 20 dB reduction for the input side CM noise is achieved when adopting the SW configuration, which is clear to help reduce the EMI filter size. In Fig. 17(b), for the output side CM current, 10 dB reduction can be observed when adopting the SW configuration. Therefore, the effectiveness of the proposed method is verified.

VII. Conclusion

In this article, a SW configuration is proposed to reduce the CM noise of nonisolated dc–dc converters at the input and output sides simultaneously. The inductor windings are split and redistributed at the input side, the ground side and the output side, which modulates the electric potential of the nodes in the circuit and creates CM noise cancellation capability. Specially, for the SW buck converter, SW boost converter and SW SEPIC converter which runs in voltage step-up mode, the total winding dimension is the same as their conventional configuration. Considering imperfect coupling between the split windings, the balance condition is derived. The proposed SW method is verified by a 100 W buck converter, where 10 to 20 dB reduction at the input side and 10 dB reduction at the output side for the CM noise are achieved, respectively. The experimental results demonstrate the effectiveness of the proposed method.

The following issues can be further investigated as future work considering the limited scope of this article.

1) Under different input voltages, the nonlinearity of the device's capacitance will affect the transient of the high *dv/dt* node, and the CM noise spectrum may be influenced. A quantitative analysis is worth figuring out how the CM noise spectrum will change under different input voltages by considering this nonlinearity effect.
2) Instead of coupling the split windings in a single core, three independent inductors can be placed at the input, ground and output sides as an alternative solution for spreading the power losses and improving the thermal performance. This configuration with independent inductors will be superior if the total volume or power losses of these inductors is proved to be less than that in the SW inductor with coupled windings in this article.

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Lihong Xie (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2012 and 2018, respectively.

Since November 2018, he was a Research Associate with the Electrical Energy Management Group, University of Bristol, Bristol, U.K., as part of its work with the EPSRC Centre for Power Electronics. His current research interests include transformer modeling, conducted EMI of SMPS and virtual prototyping of power converters.

Xibo Yuan (Senior Member, IEEE) received the B.S. degree from the China University of Mining and Technology, Xuzhou, China, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2005 and 2010, respectively, both in electrical engineering.

Since 2017, he has been a Professor with the Electrical Energy Management Group, Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K., where he became a Lecturer, a Senior Lecturer and a Reader in 2011, 2015 and 2016, respectively. He also holds the Royal Academy of Engineering/Safran Chair in Advanced Aircraft Power Generation Systems. He is the Director of the U.K. National Centre for Power Electronics and an Executive Committee Member of the IET Power Electronics, Machines and Drives Network. His research interests include power electronics and motor drives, wind power generation, multilevel converters, application of wide-bandgap devices, electric vehicles and more electric aircraft technologies.

Dr. Yuan is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is a fellow of IET and was the recipient of The Isao Takahashi Power Electronics Award in 2018.