Modular Bidirectional Differential Converter With Series Parallel Connected Output for Ultra-Wide-Voltage Applications: Control, Module Shedding, and Fail-Safe Operation

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***Abstract*—In this article, a modular output series-parallel series resonant converter (SRC) differential buck converter is analyzed for high-power, ultra-wide-voltage applications such as battery formation systems and bench-type power supplies where a zero voltage discharging function is required. An independent control method in one module is proposed to increase the efficiency of the converter compared to the conventional complementary control method. In the modular output-series connection, higher efficiency can be achieved by shedding needless modules in the low voltage range. Module shedding and activating techniques are proposed to eliminate current and voltage transients during a mode change under any load condition without the use of additional bypass switches. In addition, when a fault occurs in one module, its effect on the other module is analyzed. A practical solution involving turn-OFF processes for fail-safe operation is proposed, which reduces current stress and voltage spikes on devices and effect among modules without depending on the external signal from the central controller and the communication delay. A prototype of a modular series-parallel SRC- differential buck converter is implemented to verify the proposed concept.**

***Index Terms*—Current sharing, differential converter, fail-safe operation, module shedding, series-parallel connected output, ultrawide voltage, voltage sharing.**

I. Introduction

A BIDIRECTIONAL ultrawide voltage converter is required in many applications, such as battery formation systems, bench-type power supplies, plasma-sputtering systems, and propulsion systems [1], [2], [8]–[18]. In special cases during the formation process, batteries need to be discharged by a constant current until the voltage reaches zero [6], [9], [20], known as the zero-voltage discharge function.

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In general, the system consists of two conversion steps involving an ac–dc rectifier and a dc–dc stage. A single-stage dc–dc for a lower power battery formation with the zero-voltage discharge function was also published [6]; however, under high power, the efficiency is dramatically reduced due to the high rms current of transformer winding. A two-stage dc–dc structure is normally used to achieve high conversion efficiency and flexible output power control under a wide range of conversion gains. This two-stage structure includes an isolated bidirectional dc–dc converter with a fixed conversion gain (DCX), and a bidirectional buck converter to control the wide output voltage range is normally used [1], [6], [9], [13], [16], [17]. However, the buck converter cannot achieve the zero-voltage discharge function due to the voltage drop in the parasitic resistance of the inductors and the forward voltage drops of the switches [6], [20]. A differential buck converter, composed of two buck converters, is a capable solution for zero voltage operation [9], [20], [18]. The difference between the two outputs is the battery voltage. The conventional control method for a differential buck converter is termed *"complementary control,"* where the duty cycles of two converters are complementary (D and 1-D), as found in earlier work [9], [18]. The drawback of this control method is that all switches of the two converters operate in both power flow directions, resulting in low efficiency within a wide voltage range due to high switching and conduction losses. This article analyzes and proposes a control method to increase the efficiency of the differential buck converter.

To realize a wider range of output voltage and to increase the power of the converter, multiple standardized modules are connected in series and/or parallel on the output side. In the output-series connection, the converter can operate under a very wide voltage range, but the efficiency of the system may be low at lower voltage levels because all modules operate together. Therefore, needless modules should be turned OFF within the low voltage range. Two earlier studies [5] and [21] demonstrated that it is possible to shut down needless modules using additional current bypass switches; however, additional bypass switches can also make the system more complicated and more costly. Another study [4] shows a modular dc–dc converter with a collapsible input voltage of series-connected modules without the use of an additional bypass switch. However, the methods above depict the module shutdown and activation only in a zero-power state, which means that the power is controlled to zero, resulting in a large transient during the mode change.

In addition to the problems of the modular output series-parallel connection system, the reliability of the system when a fault occurs in one module and the effects on other modules should be considered. In general, to prevent faults, such as overcurrent and overvoltage caused by an overload, an out-of-control system, or sensing noise during operation, software protection is implemented in each module, which acts to turn OFF all switches and relays simultaneously; however, this method can result in high current stress and voltage spikes in the fault modules of the system. Moreover, due to communication delays, the slave and the master may not turn OFF at the same time, resulting in high current and voltage spikes due to interactions among the modules. It should be noted that the output capacitor has a low current rating for only bypassing the ripple of the output current component (around 5%–15% of the output current). Despite the fact that the film capacitor can allow a high pulse current, the high current tress most likely increases the chance of a capacitor failure during extended operation times [27] [28]. Therefore, the fail-safe operation should be considered to increase the reliability of modular output series-parallel systems. Studies of module shedding and fail-safe operation of the modular differential converter have rarely been discussed thus far.

In this article, a modular differential converter with series-parallel connected output is proposed with the following features.

1) The converter operates under an ultra-wide voltage range with a zero-voltage discharge function.
2) An independent control scheme is proposed to ensure higher efficiency under a wide voltage range compared to the conventional control method.
3) Output voltage and current sharing control are assured among the output series-parallel connected modules by means of a master-slave control scheme with a direct current sharing and an independent voltage sharing control loop.
4) In the output series connection, a control scheme for module shedding and activating is proposed to eliminate current and voltage transients regardless of the load condition and without the use of an additional bypass switch.
5) Through an analysis of a fault in one module and the corresponding interaction with other modules, a practical solution involving turn-OFF processes for fail-safe operation is proposed with low current stress, reduced voltage spikes of devices, and less effect on the other modules without depending on an external signal from a central controller.

Experimental results of a modular output series connection are provided to verify the proposed concepts.

II. Series Resonant Converter (SRC) Differential Buck Converter

A. Advantage of the SRC-Differential Buck Converter

Fig. 1 shows the configuration of a two-stage SRC differential buck converter for a battery formation system. The V_H is the output of a three-phase ac–dc converter. The output is supplied to charge and discharge the battery with the voltage range is from 0 to 100 V. A relay, *RL*, is required to prevent unwanted inrush current from different voltage sources during the start-up process and to isolate the converter and battery when a fault occurs.

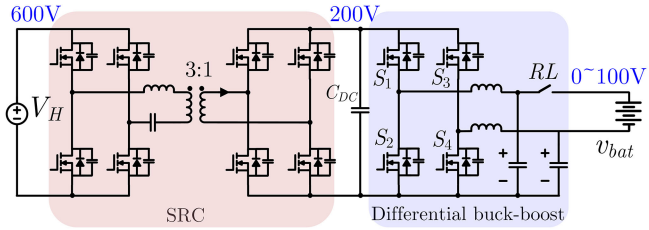

Fig. 1. Configuration of the two-stage series resonant-differential converter.

The main function of the SRC stage is to isolate the battery and grid side. This SRC operates at a fixed frequency with a series resonance tank for achieving ZCS turn-ON and turn-OFF regardless of the voltage or load variation. It is also insensitive to the tolerances of the resonant components, making it suitable for high-volume manufacturing compared to an *LLC* [19]. Moreover, this SRC achieves a natural bidirectional power flow for the isolation stage without an additional control scheme compared to an earlier method [1]; therefore, it is suitable for a pulse-test function in the formation/grading system. Also, the isolated converter helps to significantly reduce the common-mode noise between the battery and the earth.

The differential buck stage regulates the voltage and current of the battery with the zero discharge function. This converter can operate under an ultrawide voltage range in both power directions.

B. Proposed Control Method

The conventional control method for the differential buck converter is complementary control, as introduced in earlier work [18]. This control method is shown to be simple with only three sensors and one cascade control loop for the CC–constant voltage (CV) mode, as shown in Fig. 2(b), where the duty cycle of leg 1 is d_1 and the duty cycle of leg 2 is $d_2 = 1–d_1$. The drawback of this control method is shown to be its low efficiency in the low voltage range due to high switching and conduction losses.

To improve the efficiency, an independent control method is proposed in which the duty cycle of legs 1 and 2 can be controlled separately, as shown in Fig. 2(a). In the buck mode, only leg 1 operates while lower switch of leg 2 is bypassed. In the boost mode, the boost gain is limited due to the effect of the parasitic resistance [6], [18], therefore, when the battery voltage is low (less than 30 V), leg 2 controls the voltage v_{c2} to a certain value of 50 V and leg 1 can boost the voltage v_{c1} from $v_{c2}+v_{\rm bat}$ to $v_{\rm dc}$. By doing this, the battery can achieve a zero battery discharge function**.** Fig. 3 shows the results of a comparative analysis of the losses of the two switching methods. It should be noted that in the proposed control method, the switching loss and the core loss of the inductor are reduced by half when lower switch of leg 2 is bypassed, resulting in a significantly reduced total loss of 25%. Moreover, the proposed control method helps to reduce transients during the module shedding process, as detailed in Chapter IV. Current ripple analysis of two switching methods

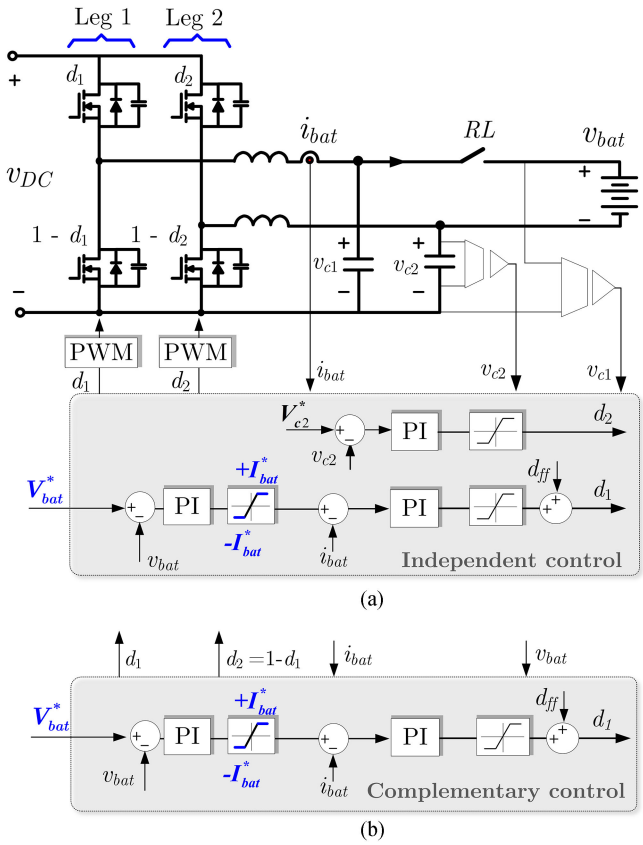

Fig. 2. Two types of control methods. (a) Independent control (*proposed*). (b) Complementary control (*conventional*) [18].

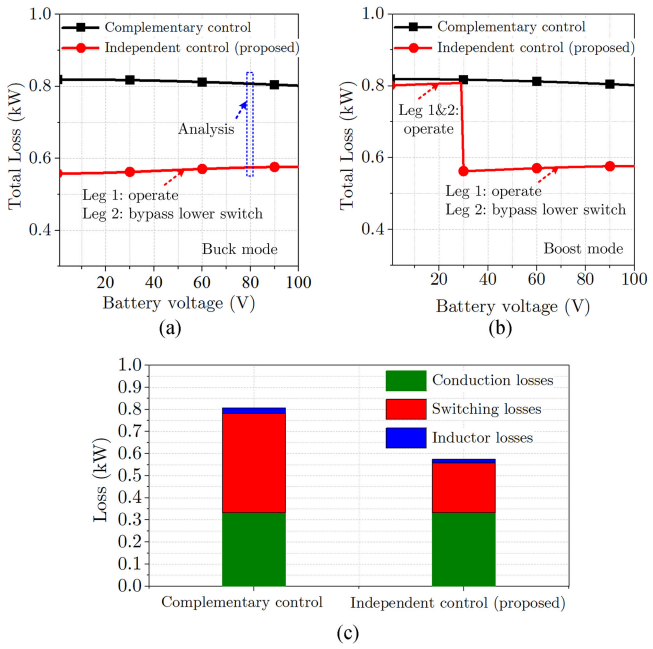

Fig. 3. Losses comparision analysis of two switching methods. (a) Total losses in the buck mode (b) Total losses in the boost mode. (c) Losses distribution (v_{DC} = 200 V, v_{bat} = 0∼100 *V*, f_s = 40 kHz, i_{bat} = 150 A, and $P_{\max}$ = 15 kW).

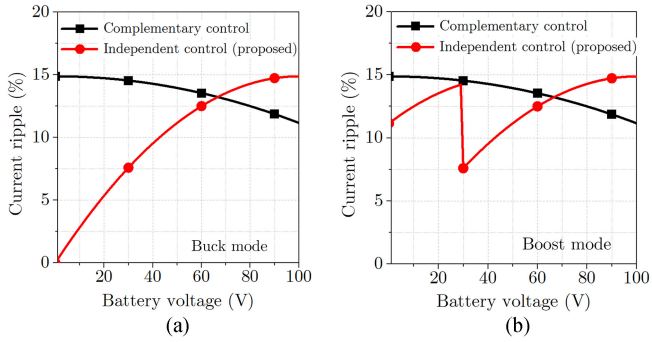

Fig. 4. Current ripple analysis of two switching methods. (a) In the buck mode. (b) In the boost mode.

TABLE I
COMPARISION OF TWO CONTROL METHODS

	Complementary control (Conventional) [18][9]	Independent control ***(Proposed)***
Control variables	Leg 1 : *d* Leg 2 : *1-d* (1 control variable)	Leg 1 : d_1 Leg 2 : d_2 (2 control variables)
Voltage gain	v_o= (2*d*-1)v_{in}	v_o= (d_1-d_2)v_{in}
d_{ff}	(v_{bat}+v_{dc})/(2v_{dc})	(v_{c2}+v_{bat})/v_{dc}
Number of control loop	2 control loop.	3 control loop.
Sensor	Just need 3 sensors: V_{bat}, v_{DC}, i_L.	Need 5 sensors: v_{C2}, v_{bat}, v_{DC}, i_L.
Effeciency	Lower	Higher
Protection level	Relative lower	Relative higher

are shown in Fig. 4. A summary of the comparative analysis of the two switching methods is given in Table I.

III. OUTPUT SERIES-PARALLEL CONNECTION

Fig. 5 shows the output series-parallel structure, including *m* submodules connected in parallel. Each submodule includes (*n*+1) SRC-differential buck converters connected in series. The goal of the proposed output series-parallel structure is to extend the voltage range of the system from *0* to $(n+1)V_{o,\max}$ *(V)* and to increase the maximum current to $mI_{o,\max}(A)$, where $V_{o\_\max}$ and $I_{o,\max}$ are the maximum voltage and current of one module, respectively. Each submodule is controlled by real-time commands from a central control interface.

A. Central Control Interface

The central control interface provides human interface functions, including the start-up, stop, CC, CV, and data management functions. Each submodule determines its operation depending on the command from the central control interface, as follows.

1) If the CC control is selected, each submodule operates with the command current value of *I*∗bat/*m*.
2) If the CV mode is selected, subm#1 operates as the master module while the other submodules are controlled to ensure current sharing among *m* submodules.

B. Submodule Local Control

The submodule local controls operate based on the commands from the central control interface, including the start-up, stop,

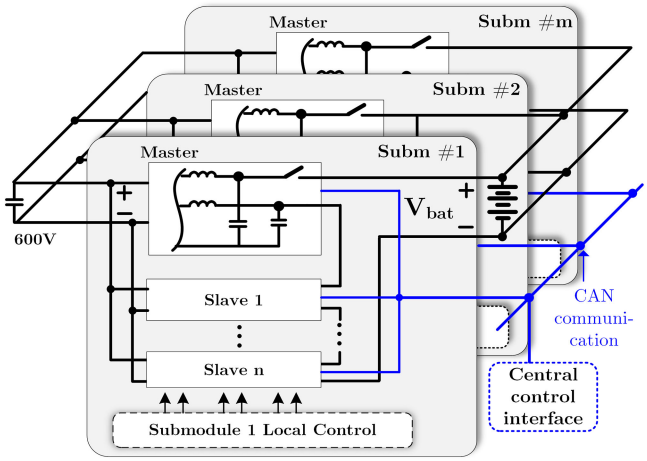

Fig. 5. Proposed output series-parallel structure for high-power, and ultrawide voltage operation.

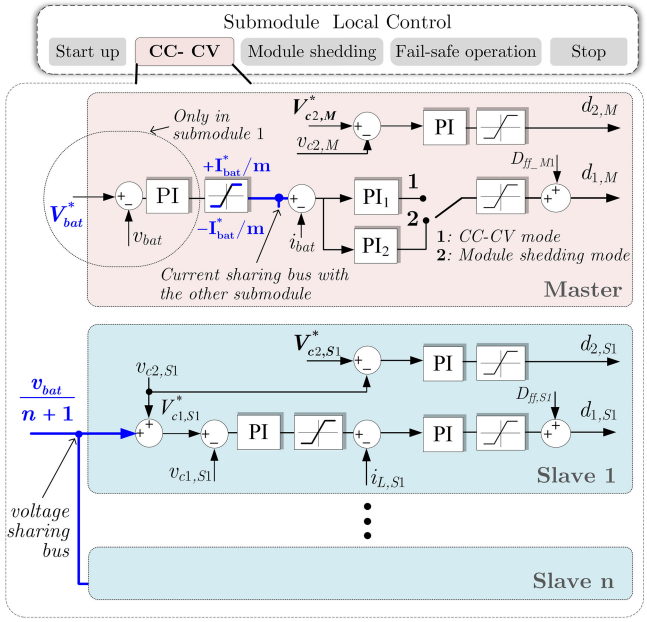

Fig. 6. CC–CV control block diagram with balancing control as part of submodule local control (a submodule includes 1 master and n slave modules).

CC–CV with balancing control, and module-shedding function comments. They also automatically turn OFF when an overcurrent or overvoltage is detected.

1) Safety Start-Up: After receiving the start-up command from the central control interface, the submodule performs the start-up operation by cooperation between master and slaves, where the relay of the master is turned ON only when all relays of slaves turn ON. This ensures the reliability of the system during the start-up process.

2) CC–CV Operation With Balancing Control: Fig. 6 shows the CC–CV control block diagram with balancing control as part of the submodule local control. For proper balance control among the submodules connected in the input parallel output parallel, direct current sharing through the current sharing bus is applied. The connection in one submodule can become an input parallel output series (IPOS) connection in the buck mode or an input series output parallel connection in the boost mode. For balancing between the modules in a submodule under both power flow directions, voltage sharing control on the battery side is used. Numerous studies have investigated a common duty control method [30]–[32], [36] in an effort to achieve inherent auto-balancing ability systems with the advantage of high modularity and redundancy. However, it requires high-speed (high bandwidth) communication to update the common duty cycle. To prevent the effect of communication delays in both the CC and CV modes, the master-slave method with independent voltage sharing control loops is recognized as a suitable control method with which to conduct the CC—CV and module shedding functions. The battery voltage (in the CV mode) or battery current (in the CC mode) are controlled by the master module, and the system-average input voltage $v_{\rm bat}/(n+1)$ is independently set as the voltage reference of the voltage-sharing loops of n slaves.

3) Module Shedding: In the output series connection, the converter can operate under a very wide voltage range; however, the efficiency of the system may be low at lower voltages because all modules are operated together. Therefore, in the low voltage range, needless modules are turned OFF. It is necessary to ensure low transient during the module shedding process while high current is still following through modules. The focus of this article is to maintain the current level during the module shutdown or activation processes without using additional bypass switches.

4) Fail-Safe Operation: To increase the system reliability during its operation, when a fault occurs in one module, it is necessary to have a turn-OFF process in each module with low current stress and low voltage spike on devices and less of an effect on the other modules without depending on an external signal from the central controller and a communication delay. A detailed analysis and the proposed fail-safe operation process are shown in Section V.

IV. Proposed Control Scheme for Module Shedding/Activation Process

A. Operating Principle

In order to realize a wider range of the output voltage of the battery, a submodule including two converters in a series connection is considered, as shown in Fig. 8. The output voltage $V_{\rm bat}$ is from 0 to 200 V. When the battery voltage $V_{\rm bat}$ <100 V, only the master module is operated, and the other module is shed by bypassing current through switches S_2 and S_4, and vice versa. However, during the shedding (or activation) process, a battery current transient and voltage ringing could result in the incorrect detection of the mode. Therefore, it is necessary to reduce the current transient during the module shedding (or activation) process while high current is maintained through both converters.

There are two important processes for reducing current transients and voltage ringing during the module shedding and activation process. First, the output voltage of the shed module must be controlled to zero, and the output capacitors of the shed module must be fully discharged before bypassing the switches. The simulation in Fig. 7(a) shows that before S_2 and S_4 are bypassed, the voltage existing in the resonant loop ($C_{1,S}$, $C_{2,S}$, and filter inductors) leads to voltage ringing. Therefore, $C_{1,S}$ and

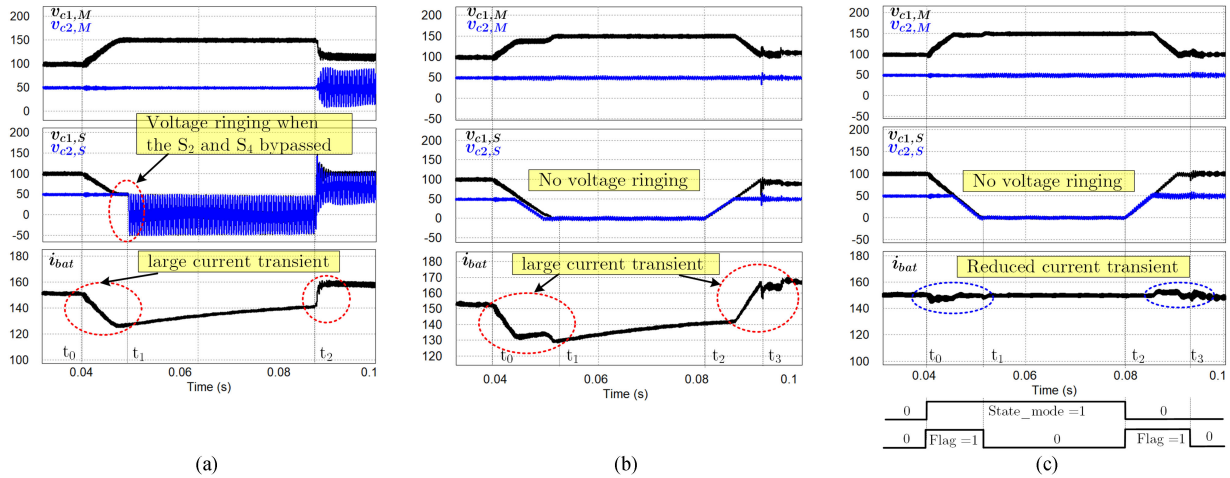

Fig. 7. Comparison simulation analysis during the module shedding process. (a) Without full capacitor discharge, (b) Without a change of the control gain in the master module. (c) Proposed control scheme with full capacitor discharge and a change in the control gain in the master. [t_0- t_1]: The interval of the slave module is shed, [t_2-t_3]: the slave module is operated again.

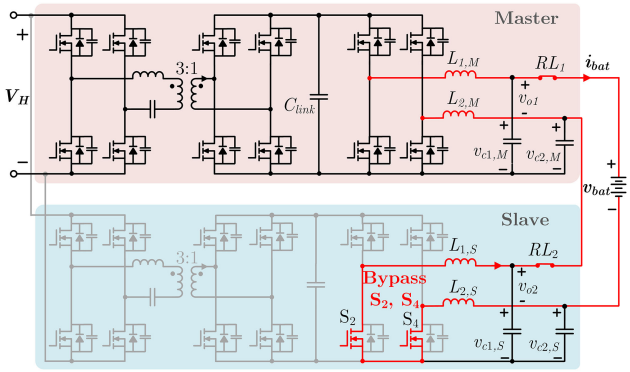

Fig. 8. Submodule includes two converters in a series (V_{bat} = 0–200 V; V_H = 600 V; $I_{\text{bat·max}}$ = 150 A). When V_{bat} <100 V, S_2 and S_4 are bypassed and the other switches of the slave module are in the OFF state.

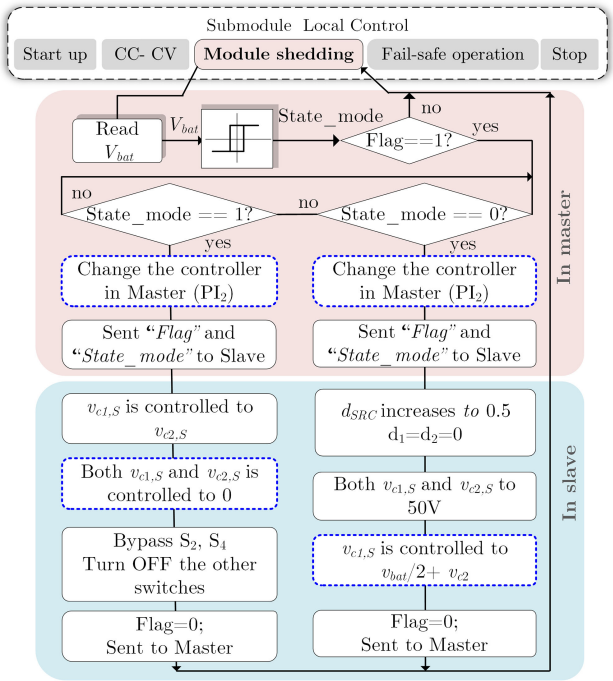

Fig. 9. Proposed control scheme for the module shedding activation process in a submodule including two modules in the out-series connection.

$C_{2,S}$ must be fully discharged before S_2 and S_4 are bypassed. Second, during the shedding or activation process, the output current control response of the master should be faster than in normal operation. The design of the control gain during the mode change is detailed in the next part of this section. Indeed, Fig. 7(b) shows a large current transient which arises when the current response of the master module is not increased during the mode change. Fig. 7(c) shows that there is no voltage ringing and only a small current transient during the module shedding and activation process with the proposed control scheme. The proposed control scheme is detailed as shown in Fig. 9 and described as below:

In the master module: the master will detect a mode change by measuring the value of V_{bat} and will set the *state_mode* value based on the battery voltage level (if v_{bat} <100, *State_mode = 0;* if v_{bat} >100, *state_mode = 1*). The mode change flag, *Flag*, becomes *1* if any change of *State_mode* is detected. The *PI* gain of the current controller of the master module changes with the gain of PI_2. The design of PI_2 is described in the next part of this section. The master will send the values of *Flag* and *State_mode* to the slave through Controller Area Network (CAN) communication.

In the Slave: Based on the received values of both *Flag* and *State_mode* from the master, the slave can recognize and provide the next operation precisely.

1) If *State_mode* = 0 and *Flag* = 1, the system is known to have to shut down the slave module. vc1,S is controlled to equal vc2,S to reduce vo_2 to zero. Then, both of these values are controlled at zero together before S2 and S_4 are bypassed, and the other switches of the slave module are turned OFF. *Flag* is set to 0 to indicate that the shedding process has finished.

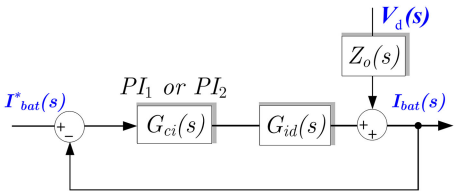

Fig. 10. Current control block diagram of the master module.

2) If *State_mode* $= 1$ and *Flag* $= 1$, the system is known to have reactivated the slave module. The SRC module gradually increases the duty cycle to 0.5. $v_{c1,S}$ and $v_{c2,S}$ are equally controlled to 50 V. Then, $v_{c1,S}$ is gradually controlled to $v_{c2,S} + v_{\rm bat}/2$. *Flag* is set to 0 again to indicate that the shedding process has finished.

In the simulation result shown in Fig. 7(c), t_0 to t_1 is the interval in which the slave module is shed, and from t_2 to t_3, the slave module is activated again.

B. Controller Design in the Transient Mode (When Flag = 1)

When the slave module is in the shedding process, the voltage of the slave module is controlled to 0 and the voltage of the master goes to $v_{\rm bat}$, the current undergoes a large transient due to the voltage change. The changing of the voltage in the master module can be considered as a disturbance source $V_d(s)$. Fig. 10 shows a current control block diagram of the master module considering the effect of V_d(s). The $G_{id}(s)$ and $Z_o(s)$ are the transfer function and output impedance of the buck converter, respectively, which are found in [18]

$$I_{\rm bat}(s) = \left(\frac{G_{ci}(s)G_{\rm id}(s)}{1+G_{ci}(s)G_{\rm id}(s)}\right) I^*_{\rm bat}(s) + \left(\frac{Z_o(s)}{1+G_{ci}(s)G_{\rm id}(s)}\right) V_d(s) \quad (1)$$

$$G_{ci}(s) = K\left(K_p + \frac{K_i}{s}\right) \quad (2)$$

$$G_{\rm id}(s) = V_{\rm in}\frac{R(1+r_{\rm esr}Cs)}{R+(L+r_{\rm esr}RC)s+RLCs^2} \quad (3)$$

$$Z_o(s) = \frac{R}{1+sRC}. \quad (4)$$

The target of this section is to design the controller $G_{ci}(s)$ to minimize the effects of $V_d(s)$ to the $I_{\rm bat}(s)$ during the transient time (when *Flag* $= 1$).

A well-known method is to multiply $G_{ci}(s)$ by a large K gain; this is intended to increase the magnitude of $T(s) = G_{ci}(s)G_{\rm id}(s)$ to infinity, with the ratio $V_d(s)/I_{\rm bat}(s)$ reaching zero while the ratio $I^*_{\rm bat}(s)/I_{\rm bat}(s)$ reaches 1, indicating the noneffect of a disturbance on the output current. However, an increase of K could result in instability of the main loop due to the increased bandwidth of the controller. A rule of thumb is to select the largest value of K to increase the bandwidth to an appropriate value (i.e., 5 kHz in this article), which depends on the switching frequency and the sampling period. Detailed discussions pertaining to this can be found in earlier work [18].

This article introduced a simple method by which to increase only the K_i gain. The Bode diagram analysis in Fig. 11 shows

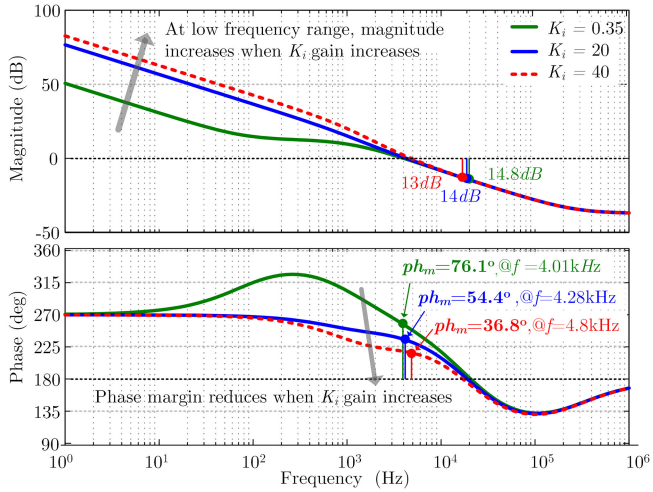

Fig. 11. Bode diagram of the open-loop $T(s)$ showing the effect of increasing the K_i gain to eliminate disturbances in the low-frequency range.

TABLE II
CONTROL GAIN IN NORMAL AND TRANSIENT MODES OF MODULE SHALDING (OR REACTIVATING)

	PI_1 (in CC-CV mode)	PI_2 (when *Flag* =1)
K_p	0.008	0.008
K_i	0.3	30

the effect of increasing the K_i gain. When K_i increases, the magnitude increases in the low-frequency range, which helps to eliminate the disturbance $V_d(s)$ without increasing the bandwidth of the controller (always less than 5 kHz). Despite the fact that the increase of K_i reduces the phase margin, in this transient mode, a small change of the current during a short time allows a lower phase margin of $T(s)$. An overly small phase margin creates high overshoot and oscillation when a small error of ($I^*_{\rm bat}$–$I_{\rm bat}$) appears. Thus, an appropriate K_i gain should be selected.

From Fig. 11, the phase margin is reduced from 76.1° to 36.7° when the K_i gain increases from 0.25 to 40. A suitable K_i of 30 is selected for this transient mode (when Flag $= 1$) as shown in Table II.

In addition, the voltage response of the slave module in the transient mode should be longer than 1/5 kHz (inside the bandwidth range of the controller of the master module). This condition is easily met by using a ramping function.

V. SYSTEM FAIL-SAFE OPERATION

A submodule including two converters in a series connection is considered, as shown in Fig. 12. The fault that occurs in the slave module becomes worse than that in the master. Thus, this section focuses on a fault in the slave module**.** If any fault including the overcurrent and overvoltage types occurs due to an overload or if the system goes out of control due to sensing noise, i.e., *Fault_flag* $= 1$, the converter enters the fault mode.

1) If the converter is in the buck mode (charging mode), a three-step fail-safe operation is applied, as shown in Fig. 12(b). In step 1, the SRC switches will turn OFF, the energy remaining in capacitor $C_{{\rm link},S}$ is discharged to

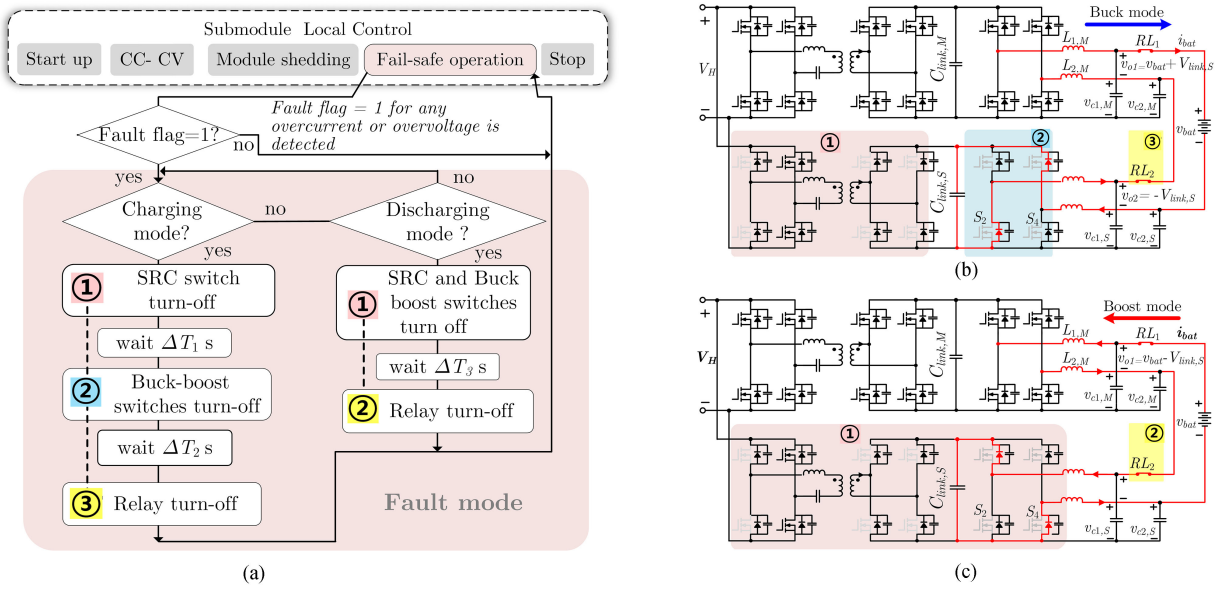

Fig. 12. Proposed fail-safe operation process during the charging and discharging processes to minimize the current stress and voltage spike on the devices without depending on control and communication processes. (a) Algorithm. (b) Three-step fail-safe operation in the buck mode. (c) Two-step fail-safe operation in the boost mode.

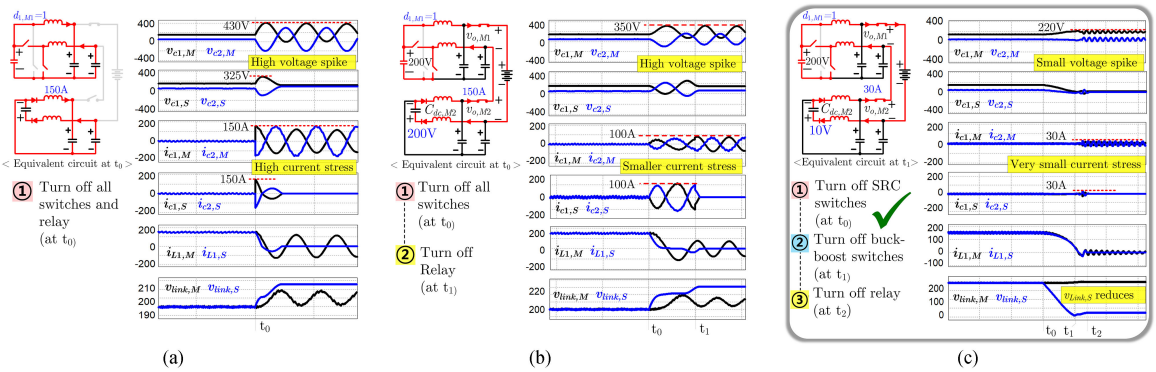

Fig. 13. Fail-safe operation analysis in case of one module has fault in the *buck mode*. (a) All switches and relay turns OFF at the same time. (b) Two-step fail-safe operation. (c) Proposed *three steps fail-safe operation in buck mode*.

nearly zero, while high current continues to flow through the battery. After time ΔT_1, in step 2, the buck switches turn OFF at time t_1, the fault module will be charged to $C_{\text{link},S}$ again with the remaining energy from the inductor, v_{o2} is forced to decrease to -$V_{\text{link},S}$, and v_{o1} is forced to increase to $v_{\text{bat}} + V_{\text{link},S}$. It should also be noted that if $V_{\text{link},S}$ is still high or ΔT_1 is not long enough to discharge $C_{\text{link},S}$ to nearly zero, the output capacitors $C_{1,S}$, $C_{2,S}$, $C_{1,M}$, and $C_{2,M}$ undergo large transients due to the large voltage change, resulting in high current tress on the capacitors. In step 3, the relay turns OFF at the time t_2 with a small amount of current stress in the capacitors.

2) If the converter is in the boost mode (discharging mode), the two-step fail-safe operation is applied. In step 1, both SRC switches and buck switches turn OFF initially and high current passes through battery because the relay is still in the ON state; also, v_{o2} is forced to $V_{\text{link},S}$. All of the remaining energy in the inductors is charged to the capacitor $C_{\text{link},S}$. After time ΔT_3, RL_2 turns OFF with a low current stress and low voltage spike in the capacitors. The simulation results in Fig. 12(c) show the proposed two-step fail-safe operation in the discharging mode.

The results of a comparison of several turn-OFF processes in the buck and boost mode are analyzed in Figs. 13 and Fig. 14, respectively. It was noted that the fail-safe process is aimed to reduce the effects among the modules before all the switches and relays are turned OFF to minimize the current stress and the voltage spike on the devices without depending on communication delay. The method by which all switches and relays are turned OFF at the same time, shown in Figs. 13(a) and(a), indicates that a high current of 150 A immediately charges and discharges through the capacitors, resulting in high current stress and low voltage spike on capacitor in both power flow directions. The method in Fig. 13(b) (in the buck mode) shows the less current stress on the device by bypassing the load current

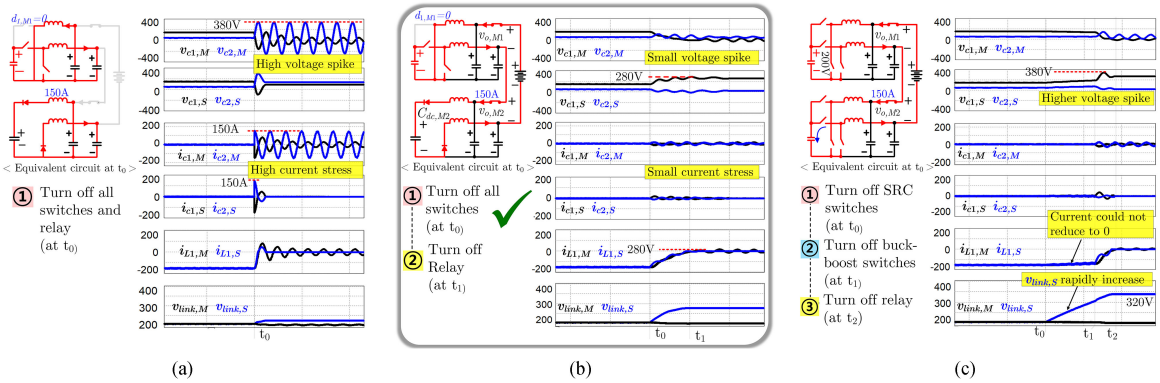

Fig. 14. Fail-safe operation analysis in case of one module has fault in the *boost mode*. (a) All switches and relay turns OFF at the same time. (b) Proposed *two steps fail-safe operation in boost mode.* (b) Three steps fail-safe operation.

through the load before the relay turns OFF; however, it shows some interaction between the modules. $v_{o,S}$ is forced to decrease from 100–200 V and $v_{o,M}$ is forced to increase from 100 V to $v_{\text{bat}} + v_{o,S} = 400$ V, which requires high charging and discharging current, resulting in high current stress and a high voltage spike. Therefore, in the charging mode, the three-step fail-safe operation is proposed. Fig. 14(c) (in the discharging mode) shows that the inductor current could not be reduced until the SRC switches are turned OFF, while the voltage $v_{\text{link},S}$ increases rapidly before the buck switches are turned OFF. Accordingly, this method should not be used in the reverse mode. Thus, in the boost mode, the two-step fail-safe operation is selected

$$\Delta T_1 > \frac{C_{\text{link}} V_{\text{link}}}{0.1 I_{\text{bat,max}}} = 10.7\,\text{ms} \tag{5}$$

$$\Delta T_2 = \Delta T_3 > \pi\sqrt{L_f C_{\text{link}}} = 0.6\ \text{ms}. \tag{6}$$

The delay time ΔT_1 is calculated so that the voltage in C_{link} is discharge to zero with a small amount of current of 0.1 times the maximum current $I_{\text{bat,max}}$. ΔT_2 and ΔT_3 are calculated so that the current through the inductor is reduced to zero when the voltage across the inductor is at its lowest point of V_{link}–$0.5V_{\text{bat}}$.

VI. Experimental Results

Fig. 15 shows a photograph of a submodule including two modules connected in an IPOS with a 33 V battery. Table III gives the main specifications, the designed parameters, and the selected prototype devices. Design values of filter inductors and capacitors can be obtained as

$$L_{f1} = L_{f2} = \frac{D(1-D)}{\Delta I_L \cdot f_{\text{sw}}} \cdot V_{\text{DC}} = 56\,\mu\text{H} \tag{7}$$

$$C_1 = C_2 = \frac{\Delta I_L}{8 \cdot \Delta V_C \cdot f_{\text{sw}}} = 83.3\,\mu\text{F} \tag{8}$$

where $\Delta I_L = 30$ A, $f_{\text{sw}} = 30$ kHz, $\Delta Vc = 1.5$ V, $V_{\text{DC}} = 200$ V, and $D = 0.5$.

The experiment is implemented using the microprocessor DSP TMS320F28377, and using CAN for communicating between modules and the user interface.

The experimental results including the start-up operation, CC, CC–CV mode control, module shedding and activation, and fail-safe operation are presented to verify the proposed concepts.

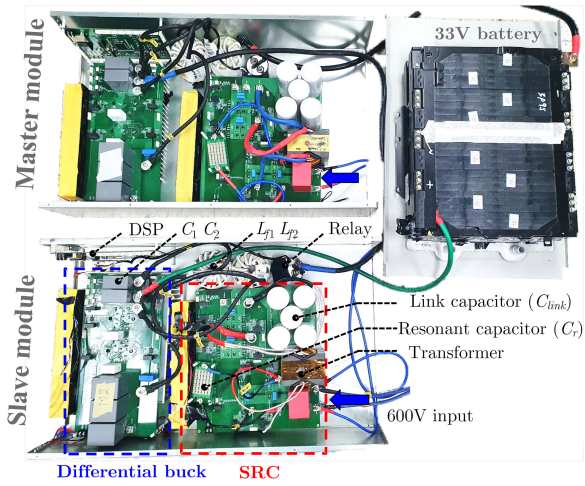

Fig. 15. Photograph of a submodule including two modules connected in an IPOS.

TABLE III
Experimental Specifications of a SRC Differential Buck Module

Items		Value		Selected devices
Output voltage		0~ 100V		-
Input voltage		600V		-
Maximum current		150A		-
SRC converter	Switching frequency	f_s	40kHz	-
	Transformer turn ratio	N_p / N_s	3:1	PM7/ PQ987
	Resonance tank	L_r C_r	7μH 1.8μF	- GR355XD72E105KW05(x66ea)
	Switches	-	-	SCT50N120 (x4ea) SCTW90N65G2V(x8ea)
Buck converter	Link capacitor	C_{link}	800μF	E61.G95-204P3C (x5ea) C4AQLEW6210(x3EA)
	Switching frequency	f_s	30kHz	-
	Switches	-	-	FF6MR12W2M1 (x2ea)
	Filter inductors	L_{f1}, L_{f2}	56μH	CH740125 (x2ea)
	Output capacitors	c_1, c_2	100μF	C4AQLBW6100A3MK (x2ea)
	Relay	-		EVR250 (YMtech)

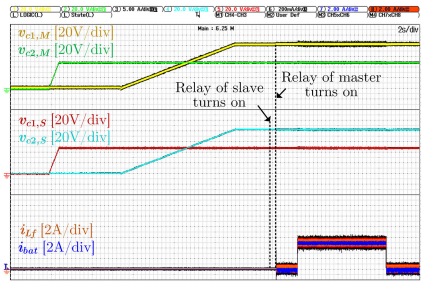

Fig. 16. Experimental result of the start-up operation of the output-series connection system.

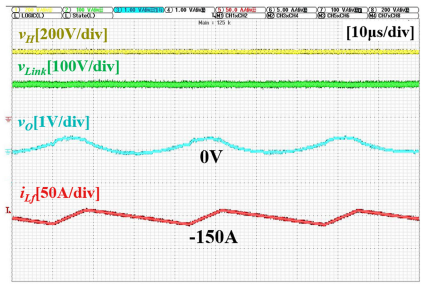

Fig. 17. Experimental results of zero voltage discharge with the maximum current.

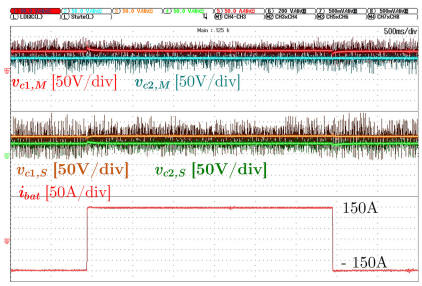

Fig. 18. Bidirectional operation with output voltage balancing of two modules in a series.

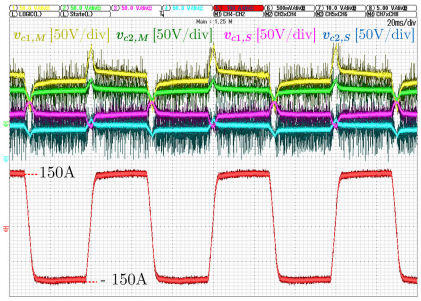

Fig. 19. Experimental result of the current pulse charge/discharge function.

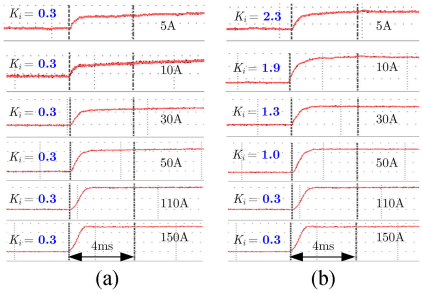

Fig. 20. Experimental results of the current response at different current levels. (a) Without changing K_i. (b) With an increase in the K_i gain under low current.

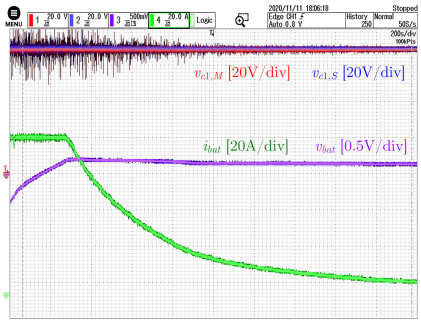

Fig. 21. Experimental result of the CC–CV operation.

Fig. 16 demonstrates the start-up operation of the submodule. First, $v_{c2,M,}$ $v_{c2,S}$ of both modules are controlled to 50 V, after which $v_{c1,M}$, $v_{c1,S}$ are controlled 50V + $v_{\rm bat}$/2. The start-up process ends when the relay of the master module turns ON after turning on the relay of the slave module. Fig. 17 shows the zero discharge function of one module with a maximum discharge current of −150 A. Fig. 18 shows the bidirectional operation of the system. The battery current changes from 150 to −150 A with a small voltage transient. The output voltages of the two modules are always balanced. Fig. 19 shows the experimental waveform of the pulse charge/discharge function with the fast current response, which is used to assess the battery characteristics by observing the voltage change during the pulse duration.

In battery formation applications, a fast current response time is required when simulating rapidly changing current and power states. Fig. 20(a) shows that the current response of the converter becomes low when the converter reaches the Discontinuous Conduction (DCM) mode (<30 A). In order to maintain a current response of 4 ms under a low current level, the control gain K_i should increase, as shown in Fig. 20(b), which can easily be done by the lookup table method. Fig. 21 shows the CC–CV operation of the converter. Fig. 22 shows the ZCS turn-ON and turn-OFF points of the SRC module.

Fig. 23 shows the experimental result of two submodules in a parallel connection. It should be noted that the currents of the two submodules ($i_{o,\mathrm{subm}\,1}$ and $i_{o,\mathrm{subm}\,2}$) are balanced.

There is high-frequency ringing component in the experiment results, which appeared due to high *di/dt* of the switching regulator, parasitic capacitances of filter inductor, parasitic inductances of PCB layout, and error of measurement tool. This could be reduced by the use of a proper Electromagnetic Interference (EMI) filter at the input of the buck converter.

Fig. 24 shows the experimental results of the module shedding process with and without the proposed control method. When the master module detects the module shedding process, the mode change flag, *Flag*, becomes *1*. The master will send the values of *Flag* to the slave. In the slave module, both $v_{c1,S}$ and $v_{c2,S}$

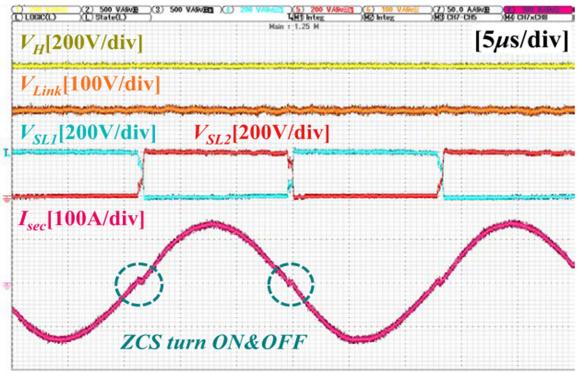

Fig. 22. Experimental result showing the ZCS turn-ON and turn-OFF processes of the SRC module.

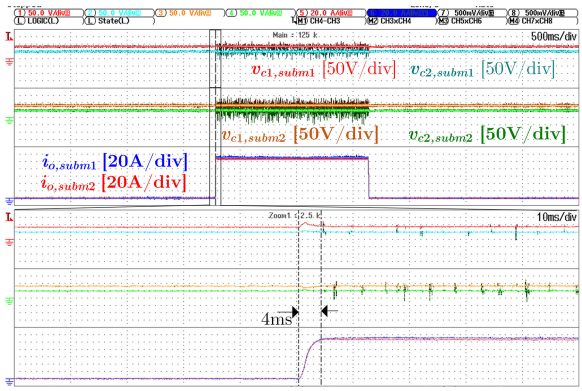

Fig. 23. Experimental result of two submodules in parallel connected output showing a balanced output current.

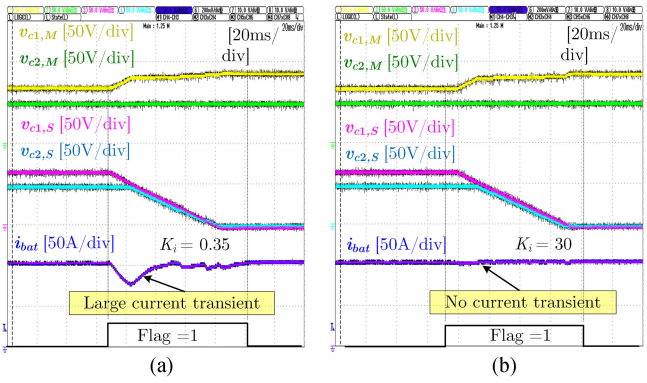

Fig. 24. Experimental results of the module shedding process. (a) Without a change of the control gain in the master module, $K_i = 0.35$. (b) With the proposed control scheme with a change of the control gain in the master module, $K_i = 30$.

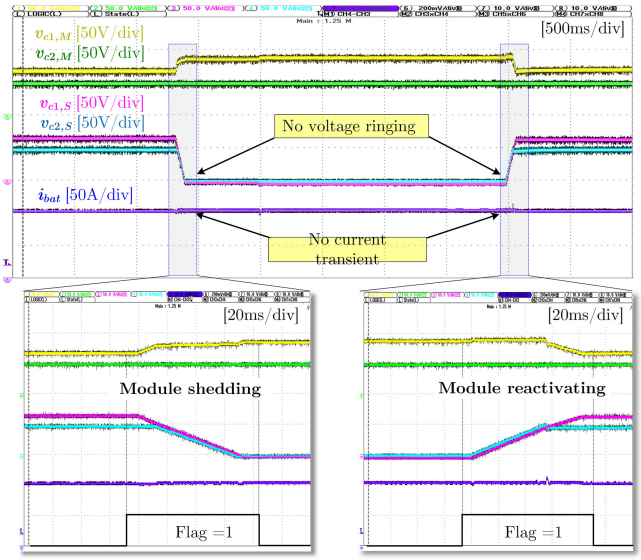

Fig. 25. Experimental results showing that there are no voltage-ringing current transient during module shedding and activation processes.

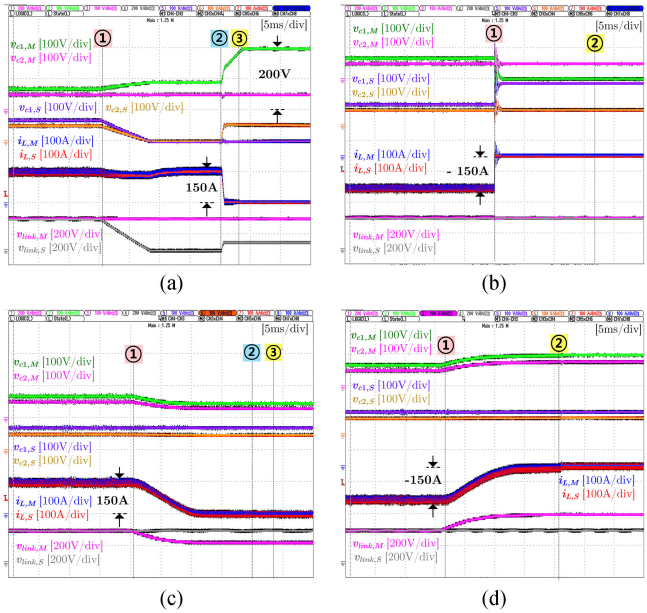

Fig. 26. (a) Fault in the slave module in the buck mode. (b) Fault in the slave module in the boost mode. (c) Fault in the master module in the buck mode. (d) Fault in the master module in the boost mode.

are controlled to zero before S_2 and S_4 are bypassed, and the other switches of the slave module are turned OFF. *Flag* is set to zero again to indicate that the shedding process is finished. There is no voltage ringing because the voltages of capacitors of the slave are already discharged. During the mode change (*Flag* = 1), if K_i is kept at 0.3, there is a large current transient, as shown in Fig. 24(a). When K_i increases to 20, there is no current transient during the mode change. Fig. 25 shows that the experimental results of the mode change of module shedding and activation without voltage and current transient, which verifies the performance of the proposed control scheme concept.

Fig. 26 shows the transient waveforms of the system when a fault occurs in one module in both the buck and boost modes with the proposed turn-OFF process for fail-safe operation. When a fault occurs in slave module under the buck mode, the three-step turn-OFF process is applied, as shown in Fig. 26(a). When the SRC switches turn OFF, the remaining energy in capacitor $C_{\text{link},S}$ is discharged to zero and the voltages $v_{c1,S}$ and $v_{c2,S}$ are naturally reduced to nearly zero. Therefore, there is no effect

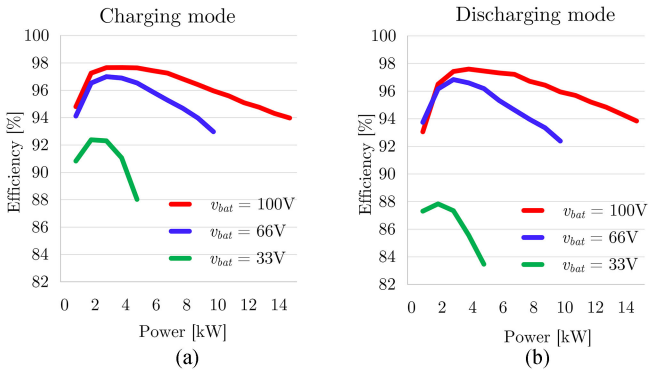

Fig. 27. Measured efficiency rates of one module as a function of the output power with different voltage levels. (a) Buck mode. (b) Boost mode.

on the other modules. When the buck switches are turned OFF, the remaining energy in the inductors is charged to the $C_{\text{link},S}$ of the fault module again and the current is naturally reduced to zero before the relay turns OFF in step 3, resulting in small current stress in the capacitors. When a fault occurs in slave module under the boost mode, the two-step turn-OFF process is applied, as shown in Fig. 26(b). v_{o2} is forced to equal $\text{v}_{\text{link},S}$ when the SRC switches and the buck switches turn OFF in step 1. The current is reduced to zero before the relay turns ON in step 2. The current stress on switches of the fault module is always smaller than the rated current of 150 A, which is shown to be safe when a fault occurs. The voltage tresses on switches are equal to the voltage across the link capacitor, V_{link} which is increased from 200 to 300 V when the fault occurs in the boost mode as shown in Fig. 26(d). This voltage can easily be calculated and is ensured to be smaller than the rated voltage of switches.

It was also noted that when a fault occurs in any module, there is small current stress and low voltage spike due to the reduced interaction with the other modules without depending on the communication delay. The experimental results are in close agreement with the analysis results.

Fig. 27 shows the efficiency curves of one module under different battery voltages, as measured using a Yokogawa WT3000 device. The maximum efficiency is 97.5% at 3.5 kW when $v_{\text{bat}} = 100$ V. When $v_{\text{bat}} = 33$ V, the efficiency of the buck mode is significantly increased compared to the boost mode due to only one leg is operated and the other leg is bypassed.

VII. Conclusion

In this article, a modular output series-parallel SRC-differential buck converter is analyzed for high-power, ultrawide-voltage applications with a zero voltage discharging function. An independent control method is proposed to increase the efficiency, where two legs of the converter are operated together only when the voltage of the battery is less than the value of 30 V in the boost mode, which helps to reduce the switching loss and core loss in the other mode and voltage range. With a modular output-series connection, a module shedding control scheme is proposed to eliminate current and voltage transients during the shedding process of needless modules at a low voltage range. In addition, through an analysis of a single module fault and its effect on the other module, three- and two-step turn-OFF processes are proposed for use during the buck and boost operations, respectively. These methods result in low current stress and low voltage spike in devices and have less of an effect on the other modules without depending on an external signal from the central controller or a communication delay.

Experimental results from a prototype including the start-up operation, CC, CC–CV mode control, module shedding, and activation, and fail-safe operation verified the proposed concepts.

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