Modified Z-Source DC Circuit Breaker With Enhanced Performance During Commissioning and Reclosing

Venkata Raghavendra I, *Student Member, IEEE*, Satish Naik Banavath, *Senior Member, IEEE*, and Sreekanth Thamballa, *Member, IEEE*

***Abstract*—Solid-state dc circuit breaker (SSCB) plays a very important role in the dc system protection against fast rising overload and short-circuit faults. Among various SSCB topologies, z-source dc circuit breakers (ZSCBs) have a great ability to interrupt the fault at a much faster rate, without even using a fault sensing circuit. However, ZSCBs suffer from various issues such as: 1) high starting current in the main thyristor (SCR), 2) unwanted power flow in the load during commissioning and reclosing of ZSCBs, and 3) negative current flow through the load at starting/reclosing of the ZSCB. These problems arise due to the fact that the z-source series capacitor stays charged even after the fault is interrupted or cleared. Unwanted power flow, negative current circulation in the load needs special attention especially in unidirectional loads and also in electromechanical systems. Hence, this article proposes a modified ZSCB to address the aforementioned problems. The proposed topology employs power semiconductor devices such as IGBTs to discharge the capacitor before the next interruption cycle. Initially, a detailed analysis, with simulation and experimental validation showing the issues with the existing ZSCB is presented. Later, a detailed analysis of the proposed modified ZSCB is presented, followed by an extensive simulation and experimental validation on a laboratory scale 120-V/3.5-A (400 W) prototype.**

***Index Terms*—DC circuit breaker (dcCB), dc microgrid, fault protection, solid-state circuit breaker (SSCB), z-source dc circuit breaker (ZSCB).**

I. Introduction

IN RECENT years, electric power transfer by direct current (dc) means finds its way in various applications such as microgrids, data centers, subsea, electric vehicle, energy storage, and electric ships [1]–[4]. DC power transmission and/or distribution is growing very rapidly as there is an urgent need for integration of a large number of renewable energy resources. Electric power transfer in the dc form offers several advantages over the conventional three-phase ac systems in terms of reduced number of conductors, asynchronous operation, efficiency, and flexibility [5], [6]. Despite several advantages, electric power transmission/distribution in the dc form is not very successful especially for low to medium power levels and also in multiterminal dc system architectures due to the nonavailability of a fast and reliable fault protection system [7], [8]. The absence of natural current zero-crossing and steep rise of fault currents in the dc system are the technical barriers in designing a reliable and fast dc circuit breaker (dcCB).

Though dc distribution is not standardized due to the unavailability of standards and operating duties, it is a good practice to consider following factors while designing a dcCB:

1) fault current interruption time;
2) maximum fault current breaking capability;
3) ON-state power losses;
4) maximum dissipated energy in metal oxide varistor;
5) dc current limiting reactor;
6) overvoltage protection.

Conventional ac system employs an arc-based CB for protection, that interrupts and clears fault at the current zero-crossing. These CBs produce an arc between the mechanical contacts during the fault interruption process. Performance improvements on these types of CB's are achieved by either employing arc lengthening techniques or by cooling [9], that further improves arc extinction in the consecutive current zero crossings. DC systems on the other hand lacks with natural current zero-crossing, which makes arc-based CB more difficult to extinguish the arc. On these lines, several dcCB topologies have been proposed in the literature for low voltage dc (LVdc), medium-voltage dc (MVdc), and high-voltage dc (HVdc) systems for fast and reliable fault interruption [10]–[12].

DCCBs in literature are broadly classified into three categories, namely: 1) modified mechanical switch-based CBs (MCBs), 2) solid-state CBs (SSCBs), and 3) hybrid dc CBs (HCBs) [12]. Initial proposals focus on creating an artificial current zero-crossing in the already existing ac CB (ACCBs) by adding an auxiliary branch consisting of inductors and capacitors. Yet, these topologies take longer fault interruption time and are also bulkier in size [13], [14]. Power semiconductor-based

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Venkata Raghavendra I and Satish Naik Banavath are with the Department of Electrical Engineering, Indian Institute of Technology Dharwad, Dharwad, Karnataka 580011, India (e-mail: raghavendra.iv@gmail.com; satti.naik7@gmail.com).

Sreekanth Thamballa is with the Department of Electrical and Computer Engineering, University of Minnesota Twin Cities, Minneapolis, MN 55455 USA (e-mail: tsreekan@umn.edu).

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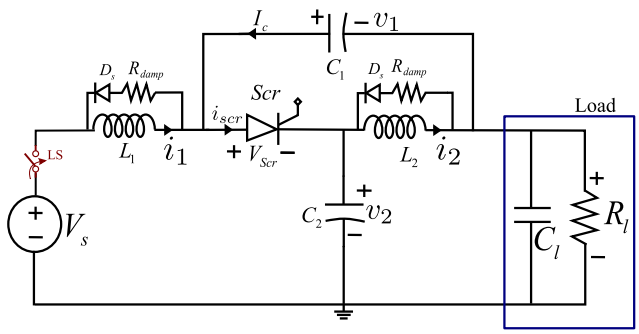


Fig. 1. Conventional series z-source dc circuit breaker (ZSCB).

solid-state dc circuit breakers (SSCBs) are alternative to the modified mechanical CBs in applications which require faster fault interruption. SSCBs use semiconductor devices such as IGBT/MOSFETs, IGCTs, and SCRs, etc., either in series or parallel depending upon the voltage and current rating of the dc system, device rating, and breaker configuration. Moreover, semiconductor devices do not have moving parts, as a result fast and arcless fault interruption could be achieved thereby improveing the reliability and life span of the CB [11], [15]. Despite the above advantages, SSCBs poses several issues such as higher ON-state power loss, lack of galvanic isolation, and requirement of additional sensing and control circuitry. The efficiency of SSCBs could be improved significantly by adopting wideband gap devices as given in [10]. These devices are very expensive at least for now, and their availability at a high power level also limits their widespread application in DCCBs. HCB operation falls in between the MCB and SSCB. HCBs are another class of dcCBs that provide better performance over MCBs in terms of fault interruption time, and also very efficient when compared to SSCBs. The main constraint with this class of dcCBs is the mechanical time constant of the ultrafast disconnector [16], [17].

Z-source dc circuit breaker (ZSCB) is a class of SSCBs that respond autonomously to the faults. The main advantage of ZSCB is that it does not employ any sensing or control circuit to interrupt the fault [18], [19]. An improved version of ZSCB with faster fault response, simple control, and bidirectional power flow capability is proposed in [20]. Furthermore, an attempt to reduce ON-state power losses in ZSCB by integrating SiC devices is given in [21]. The ZSCB proposed in [18] and [19] have led to several advancements in the series ZSCB topologies [22]. The key advantages of ZSCB given in [22] are the common ground connection between the source and load side, and inbuilt low-pass filter integration. A modification to the series ZSCB is proposed in [23] which differentiates by itself between the load changes and the fault. Circuit schematic of a series ZSCB proposed in [23] is illustrated in Fig. 1. Authors in [24] also propose a modified series ZSCB (MZSCB) with a target to design the ZSCB more compactly by employing mutually coupled inductors.

The dc microgrid structures with battery energy storage are growing very rapidly. These systems are capable of delivering power on both sides, that is, bidirectional power flow. However, the dc load takes power only in one direction. Employing a conventional series ZSCBs for the protection in dc microgrid poses several issues especially on the load. They are as follows.

1) A negative current flow in the load for a short period during commissioning or after reclosure of series ZSCB.
2) The series capacitor (C_1) as shown in Fig. 1 keeps charging during fault interruption and discharges through the main SCR during reclosure. This leads to high peak currents in the main SCR.
3) Unwanted power flow in the load during the commissioning of the series ZSCB.

All the above listed issues as a whole disturb the operation of load and may also create serious problems especially in unidirectional loads such as traction systems with dc motors, process manufacturing, household dc loads, end use dc loads of submarine and naval ships, and finally may damage the loads.

This article introduces a MZSCB topology to address the above listed problems. Application of the proposed series ZSCB can be extended to even MVdc systems with reduced size using coupled inductors and also bidirectional power flow capability can be provided by using bidirectional switch configuration. The proposed MZSCB retains the advantages of series ZSCB which includes, a common ground connection between input and output, and inbuilt low-pass filter integration. Rest of the article is structured as follows. Section II reviews the operation of conventional series ZSCB and also highlights the problems that exist in series ZSCBs with experimental validation. Section III presents the proposed MZSCB topology along with a description of its operation. This section also provides a theoretical analysis of MZSCB concerning various fault conditions. Simulation and experimental validation of the proposed ZSCB are illustrated in Section IV. Section V presents the performance comparison of the proposed dcCB with the existing ZSCBs reported in the literature. Finally, Section VI concludes this article.

II. Series Z-Source DC Circuit Breaker

In this section, a discussion on series ZSCB proposed in [23] is presented. This section also highlights various issues resulted in the series ZSCBs during commissioning and/or reclosing of the CB. From the literature, it is envisaged that there are no attempts on the analysis of the ZSCBs especially at its commissioning in field or reclosing after the fault. Moreover, an extensive study is presented in the literature on the analysis of ZSCBs during the fault. But, when we analyze operation of several ZSCBs such as classical ZSCB, parallel connected ZSCB, and series ZSCB at starting/reclosing, it is found that, various issues arise such as high starting current in SCR, negative current flow, and unwanted power flow in the load during reclosing.

A. Issues in Series ZSCB

To illustrate the issues a series ZSCB is considered and analyzed for a rating of 120-V/3.5-A dc system having an approximate power capacity of 400 W. The system parameters considered are shown in Table I.

TABLE I
SYSTEM PARAMETERS

S. No	Parameter	Value
1	Source Voltage (Vs)	120V
2	Z-Source Inductors (L_1, L_2)	1.2mH
3	Z-Source Capacitors(C_1, C_2)	63μF
4	Load Resistance	35Ω

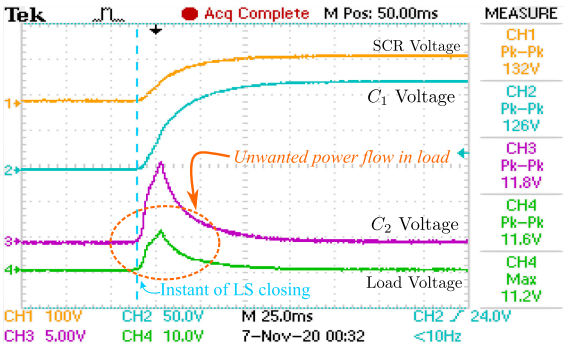


Fig. 2. Voltage waveforms of the series ZSCB showing unwanted power flow in the load during commissioning.

Consider a series ZSCB as shown in Fig. 1. The switch LS is kept open and gate pulse to the SCR is also OFF before commissioning. Now to bring the CB into operation, a turn ON command for switch LS is given. As a result, current flows through L_1, capacitor C_1, and the load. Though, the main SCR is kept in OFF state which means ideally there should not be any power flow from source to the load, however, in this case there exists some power flow in the load during this initial commissioning. In this process, capacitor C_1 charges to dc grid source voltage. Experimental waveforms pertaining to unwanted power flow in the load and initial C_1 charging is elucidated in Fig. 2. Now, gate pulse to the SCR is issued which enables power flow between source and the load. Exactly at the SCR turn ON instant, there are observed to be two current components flowing in the SCR, first component is the source current, while the other component is the discharge current of capacitor C_1. Capacitor C_1 discharges through the path consisting of $C1$ - SCR - C_2 - load R_l. It may be noted that, the current flowing in load is in the opposite direction (negative) to the normal operation. It may also be observed that, the peak current flowing through SCR during starting is very high as the capacitor current is very high due to lower resistance in the discharge path.

Analytical expressions for current and voltage in various components of the series ZSCB during starting transient is derived as follows. Consider state variables i_1, i_2, v_1, and v_2, where, i_1 and i_2 are the currents flowing through inductors L_1 and L_2, respectively. Similarly, v_1 and v_2 are the voltages across capacitors C_1 and C_2, respectively. The state equations that govern the dcCB are as follows:

$$\begin{bmatrix} \dot{i_1} \\ \dot{i_2} \\ \dot{v_1} \\ \dot{v_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & \frac{-1}{C_1} & \frac{-1}{R_l C_1} & \frac{1}{R_l C_1} \\ \frac{1}{C_2} & 0 & \frac{1}{R_l C_2} & \frac{-1}{R_l C_2} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_s \end{bmatrix}. \tag{1}$$

The time domain solution of state variables is found by applying Laplace transform as

$$\dot{X} = AX + BU$$
$$X(S) = [sI - A]^{-1}x(0) + [sI - A]^{-1}BU(s). \tag{2}$$

For simplifying the analysis, consider $L_1 = L_2 = L$ and $C_1 = C_2 = C$. With these assumptions, the time domain solution to state variables is obtained as

$$i_1 = \frac{V_s}{R_l} - \frac{V_s}{R_l} e^{-\frac{t}{R_l C}} \cosh\left(\frac{t\sqrt{1-CR_l^2}}{R_l C\sqrt{L}}\right) \tag{3}$$

$$+ -\frac{V_s}{R_l} e^{-\frac{t}{R_l C}} \frac{\sqrt{L}}{\sqrt{1-CR_l^2}} \sinh\left(\frac{t\sqrt{1-CR_l^2}}{R_l C\sqrt{L}}\right) \tag{4}$$

$$i_2 = \frac{V_s}{R_l}\left[1 - e^{-\frac{t}{R_l C}} \cosh\left(\frac{t\sqrt{1-CR_l^2}}{R_l C\sqrt{L}}\right)\right. \tag{5}$$

$$\left. - e^{-\frac{t}{R_l C}} \frac{\sqrt{L}}{\sqrt{1-CR_l^2}} \sinh\left(\frac{t\sqrt{1-CR_l^2}}{R_l C\sqrt{L}}\right)\right] \tag{6}$$

$$v_1 = \frac{V_s\sqrt{L}}{\sqrt{1-CR_l^2}} e^{-\frac{t}{R_l C}} \sinh\left(\frac{t\sqrt{1-CR_l^2}}{R_l C\sqrt{L}}\right) \tag{7}$$

$$v_2 = V_s - \frac{V_s\sqrt{L}}{\sqrt{1-CR_l^2}} e^{-\frac{t}{R_l C}} \sinh\left(\frac{t\sqrt{1-CR_l^2}}{R_l C\sqrt{L}}\right). \tag{8}$$

The expression for current flowing through the SCR is obtained by applying KCL at anode node of SCR

$$i_{\text{scr}} = i_1 - C\frac{dv_1}{dt} \tag{9}$$

substituting (3) and (8) in (11), we get

$$i_{\text{scr}} = \frac{V_s}{R_l} - \frac{2V_s}{R_l} e^{-\frac{t}{R_l C}} \left[\cosh\left(\frac{t\sqrt{1-CR_l^2}}{R_l C\sqrt{L}}\right)\right]. \tag{10}$$

Additionally, during every reclosure of the CB, capacitor C_1 discharges and takes a path through the SCR - C_2 - load (current in the opposite direction). The expression for entire current flowing through SCR during those reclosing instances is shown in (12). The negative current in load during every reclosure disturbs the operation of unidirectional dc loads. Extensive simulation and experimental validation is carried on the series ZSCB with the system parameters as listed in Table I. The simulation and experimental voltage and current waveforms of various elements of the ZSCB under consideration showing the negative current circulation in the load, high peak current in the SCR are illustrated in Figs. 3(a)–4(b). Following sections discusses on how these issues are resolved by a MZSCB topology.

III. PROPOSED MZSCB

The proposed MZSCB topology that eliminates the issues associated with the existing series ZSCB is illustrated in Fig. 5, where C_1, C_2, L_1, and L_2 are the z-source capacitors and inductors, respectively. The z-source inductors consists of a parallel snubber branch which helps to dissipate trapped energy in the inductors. SCR is used as the main fault current interruption

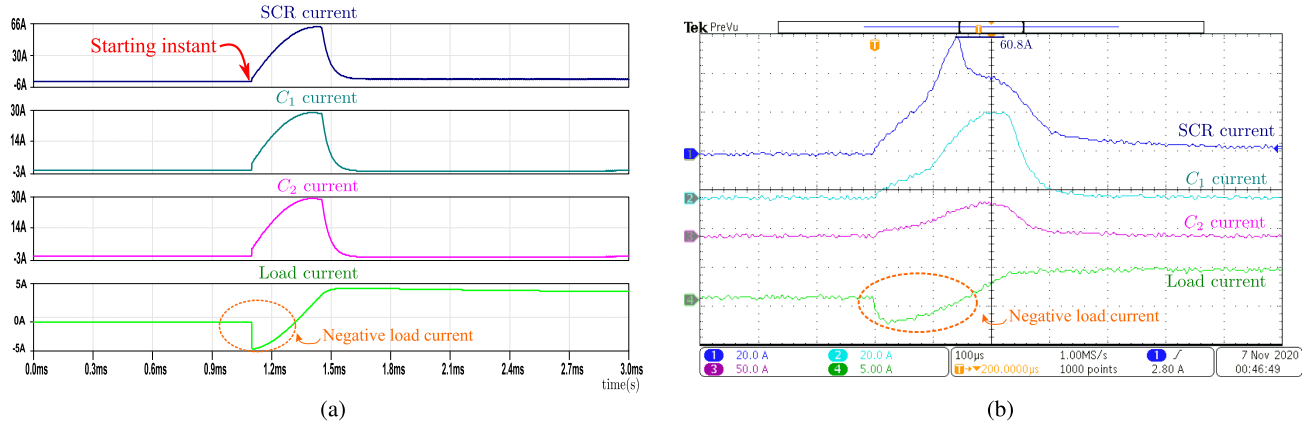


Fig. 3. Simulation and experimental current waveforms of a series ZSCB showing negative current in the load during starting/reclosing. (a) Simulation results. (b) Experimental results.

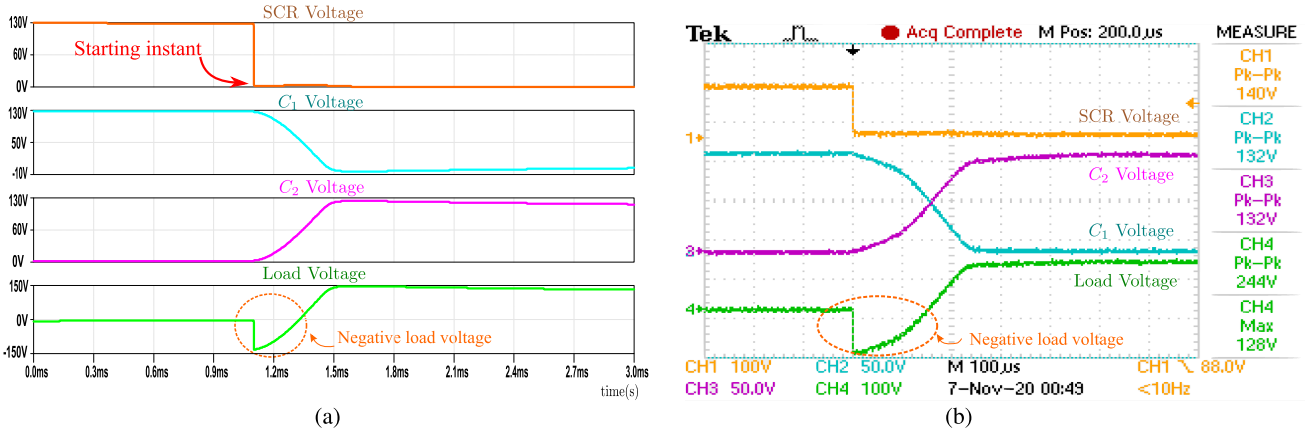


Fig. 4. Simulation and experimental voltage waveforms of a series ZSCB showing negative current in the load during starting/reclosing. (a) Simulation results. (b) Experimental results.

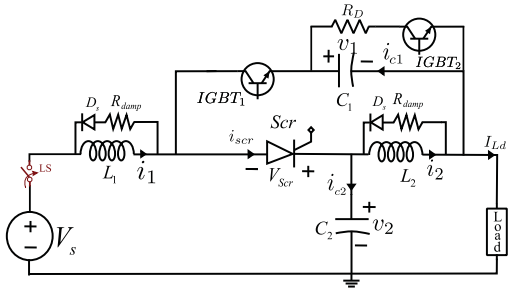


Fig. 5. Schematic of proposed series ZSCB.

device. The SCR is turned OFF by creating an artificial zero current crossing through it by using z-source elements. Power semiconductor devices such as $IGBT_1$ and $IGBT_2$ are used to control the charging and discharging profile of the capacitor C_1. These IGBTs are operated in a mutually complimentary manner. Under normal operation, that is, when there is no fault, $IGBT_1$ is kept in ON state to provide a path for current in the event of fault. During this period $IGBT_2$ is kept in the OFF state. When the dc system is not energized, $IGBT_2$ is kept in ON state, such that the stored energy in capacitor C_1 is completely discharged and keep the capacitor ready for the next fault interruption. Switch LS is used to provide galvanic isolation between the source and load which is very essential for maintenance activity.

A. Operating Modes

The proposed ZSCB operation is divided into three modes as follows.

1) *Mode - 1:* In this mode the dc system is considered to be in the normal or steady-state operation, wherein there is a power flow from source to the load side. During this mode switches LS, SCR, and $IGBT_1$ are kept in ON state while $IGBT_2$ is kept in OFF state. Keeping the $IGBT_1$ in ON position helps in providing a high-frequency path for the fault current. During this mode, capacitor C_1 is kept uncharged while the capacitor C_2 is charged to dc grid voltage (V_s). Circuit schematic showing the current path during this interval is elucidated in Fig. 6(a).

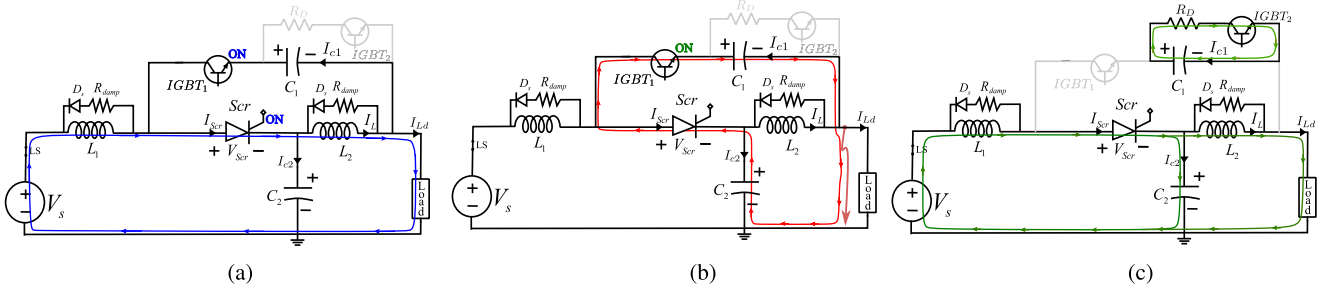


Fig. 6. Proposed modified circuit breaker operation during various modes. (a) Mode - 1. (b) Mode - 2. (c) Mode - 3.

2) *Mode - 2:* Circuit schematic pertaining to this mode is illustrated in Fig. 6(b). In this mode a short-circuit fault is created on a steady operating system. Soon after the short-circuit fault, a high frequency closed path is formed and current instantly flows through this path which is in opposite direction to the SCR main current as shown in Fig. 6(b). As a result, the net current flowing through the SCR reaches to zero and makes the SCR to go into OFF state. Now, the source current takes a path through L_1 - IGBT$_1$ - C_1 - fault, and charges C_1 to the grid voltage. On the other hand, C_2 discharges through L_2 and fault. The instant at which C_1 voltage reaches just above the grid voltage and C_2 voltage is near to zero, snubber diode D_s gets forward biased and dissipates the trapped energy in inductors through the corresponding damping resistors R_{damp}. This makes the net fault current to zero. In this whole process, capacitor C_1 voltage is sensed continuously and when it reaches to grid voltage a command to turn OFF IGBT$_1$ and turn ON IGBT$_2$ is issued. In case if there is a severe maintenance requirement then LS is opened to provide galvanic isolation.
3) *Mode - 3:* This mode discusses about the circuit operation during reclosure of the CB as shown in Fig. 6(c). This mode starts after the short-circuit fault is cleared and dc system is ready for the power transfer. CB is *reclosed* to reestablish the power flow between the source and load. CB operation during reclosure is as follows: Initially the switch LS is closed, and IGBT$_2$ is kept in ON state that helps in discharging the capacitor C_1 through the resistor R_D. In this process C_1 voltage is sensed, and when it reaches to zero, then a command to turnOFF IGBT$_2$ and turn ON IGBT$_1$ is issued. SCR is triggered just before the turn ON of IGBT$_1$, may be a few microseconds prior. Now, SCR conducts two components of currents, one would flow through C_2 and helps it to charge to grid voltage, and the other component is the load current. Major advantages of using this topology can be seen during reclosing. Unlike in the series ZSCB, capacitor C_1 current during its discharge does not take a path through the SCR, this reduces the peak current in SCR. Also consider a case where the switch LS is in ON state and SCR is not yet triggered; there exist no unwanted power flow in the load unlike in series ZSCBs. It may also be noted that, the negative current circulation in the load during reclosing is eliminated as the capacitor C_1 is discharged independently in a separate circuit.

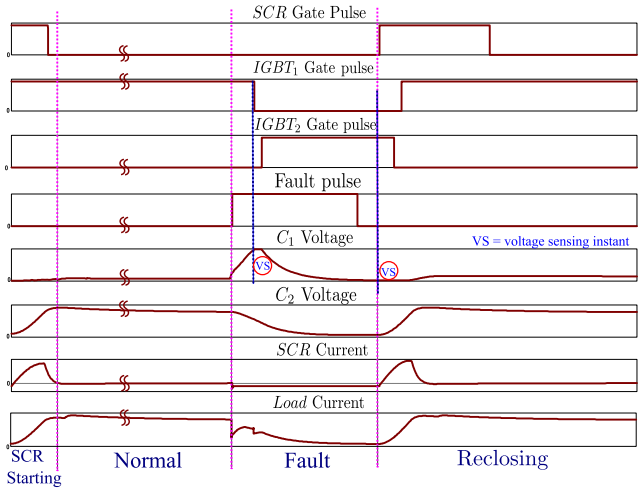


Fig. 7. Timing sequence of switches and corresponding voltage and current waveforms.

Fig. 7 shows the turn ON and turn OFF sequence of various switches used in the proposed converter along with their corresponding voltage and current waveforms.

B. Marginal Fault Conductance

The ZSCB operation greatly depends on the type of load, load transients, and also on type of fault and its characteristics. These parameters play a key role in the fault current interruption process. On the other hand, these parameters greatly control the SCR current and its corresponding zero crossing. Hence, this section deals about a design methodology for finding a marginal value of fault conductance beyond which any changes in the load are considered as a fault and system is interrupted. Consider a faulty case with fault conductance G_f as shown in Fig. 8, in which the capacitor C_2 discharges and takes a path through C_2 - SCR - IGBT$_1$ - C_1 - G_f. If the load side is considered to have a voltage fed power electronic converter, then its input capacitance C_l will also act as a load capacitance and this capacitor would also discharge through the fault conductance G_f.

The fault current can be written in two forms. Equation (13) is derived with respect to the fault conductance; where as (14)

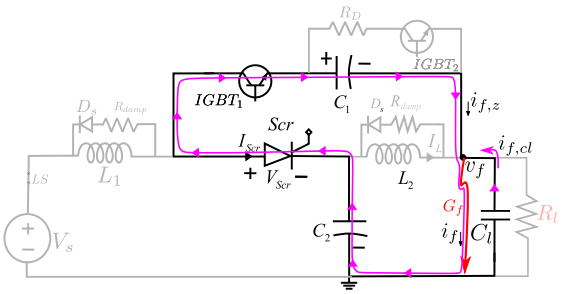


Fig. 8. Fault current flow through the capacitors.

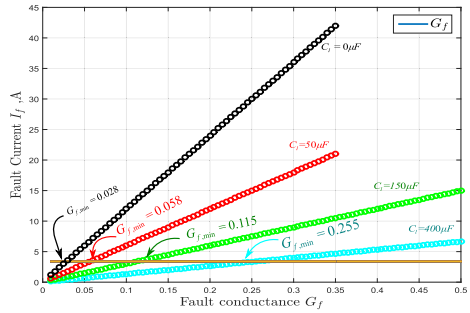


Fig. 9. Plot showing marginal fault conductance with different values of load capacitance.

is with respect to the current injected into the fault by z-source capacitors and the load side converter input capacitance

$$i_f(t) = v_f(t)G_f \tag{11}$$

$$i_f(t) = i_{f,z}(t) + i_{f,cl}(t) \tag{12}$$

where i_f is the fault current, and v_f is the voltage across fault conductance. For simplicity and design symmetry consider, $C_1 = C_2 = C_z$, and also by neglecting the ON-state voltage drop of thyristor and R_{on} of IGBT_1, we get (15) by performing mathematical deductions on (13) and (14)

$$G_f v_f(t) = -\frac{C_z}{2}\frac{dv_f(t)}{dt} - C_l\frac{dv_f(t)}{dt}. \tag{13}$$

At the fault instant, the initial state of fault node voltage $V_f(0)$ is V_s, by solving the first-order differential (15) for fault node voltage $v_f(t)$ we get

$$v_f(t) = Vs\ \ e^{-\frac{2G_f}{C_z+2C_l}t}. \tag{14}$$

The fault current injected by the z-source capacitors is found to be

$$i_{f,z}(t) = V_s\frac{C_zG_f}{C_z+2C_l}\ \ e^{-\frac{2G_f}{C_z+2C_l}t}. \tag{15}$$

From (17), we can say that $i_{f,z}(t)$ is exponentially decaying with a peak magnitude of $I_{f,\text{zmax}}$

$$I_{f,\text{zmax}} = V_s\frac{C_zG_f}{C_z+2C_l}. \tag{16}$$

For i_{scr} to become zero, $I_{f,\text{zmax}}$ must be greater than the steady-state current

$$V_s\frac{C_zG_f}{C_z+2C_l} \gg \frac{V_s}{R_l}. \tag{17}$$

From (19), the marginal value of fault conductance is found and expressed in (20). It may be noted that, the fault conductance is a function of load capacitance, z-source capacitor, and the load resistance. Fig. 9 shows the fault conductance variation for a given set of system parameters, $V_s = 120$ V, and $I_L = 3.5$ A with z-source capacitance of $C_z = 100$ μF and load capacitance C_l is varied from 0–400 μF.

$$G_{f,\text{min}} = \left(1+\frac{2C_l}{C_z}\right)\cdot\frac{1}{R_l}. \tag{18}$$

From (20), it can be inferred that the value of $G_{f,\text{min}}$ decreases with reduction in load side dc link capacitance. It may also be noted that the minimal fault conductance is inversely proportional to the load resistance (R_l).

C. Design Considerations

Voltage and current rating of the selected components in the proposed MZSCB are chosen from the following design analysis. State equation that governs the proposed MZSCB is

$$\begin{bmatrix}\dot{i_1}\\ \dot{i_2}\\ \dot{v_2}\end{bmatrix} = \begin{bmatrix}0 & 0 & \frac{-1}{L_1}\\ 0 & -\frac{R_l}{L_1} & \frac{1}{L_1}\\ \frac{1}{C_2} & -\frac{1}{C_2} & 0\end{bmatrix}\begin{bmatrix}i_1\\ i_2\\ v_2\end{bmatrix} + \begin{bmatrix}\frac{1}{L_1}\\ 0\\ 0\end{bmatrix}\begin{bmatrix}V_s\end{bmatrix}. \tag{19}$$

For simplicity, consider $L_1 = L_2 = L$ and $C_1 = C_2 = C$. Solving for time domain expressions of state variables results in

$$i_1 = \frac{V_s}{R_l} - \frac{V_s(2L - R_l^2\,C)}{R_l\sqrt{L}\sqrt{1-R_l^2\,C}}\,e^{-\frac{t}{R_l}} \sinh\left(\frac{t\sqrt{1-CR_l^2}}{R_lC\sqrt{L}}\right). \tag{20}$$

The current i_1 flows through the SCR during starting/reclosing transient

$$i_2 = \frac{V_s}{R_l}\left[1 - e^{-\frac{t}{R_lC}}\cosh\left(\frac{t\sqrt{1-CR_l^2}}{R_lC\sqrt{L}}\right) - e^{-\frac{t}{R_lC}}\frac{\sqrt{L}}{\sqrt{1-CR_l^2}}\sinh\left(\frac{t\sqrt{1-CR_l^2}}{R_lC\sqrt{L}}\right)\right] \tag{21}$$

$$v_2 = V_s - V_s\,e^{-\frac{t}{R_lC}}\cosh\left(\frac{t\sqrt{1-CR_l^2}}{R_lC\sqrt{L}}\right). \tag{22}$$

Comparing the thyristor current expressed in (12) with that of thyristor current expression in (22), with same system parameters, it is observed that the current flowing through SCR in proposed ZSCB is very less compared to the existing series ZSCB, same can be observed in experimental results. By using (22)–(26), maximum current and voltage rating of SCR, IGBT's, capacitors, and inductors are found, accordingly the practical components are selected.

During commissioning of ZSCB, capacitor C_1 and its corresponding discharge resistor R_D forms an independent loop. Design of resistance R_D completely depends on capacitor C_1's

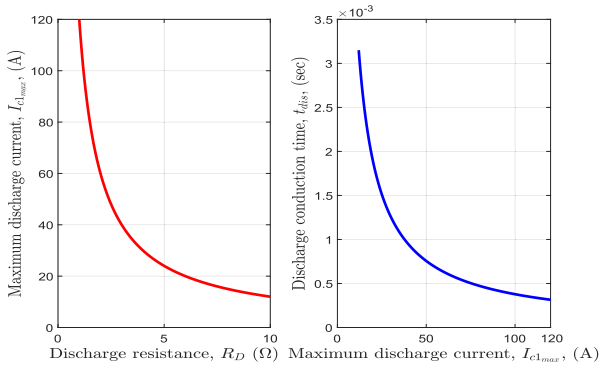


Fig. 10. Design of discharge resistance.

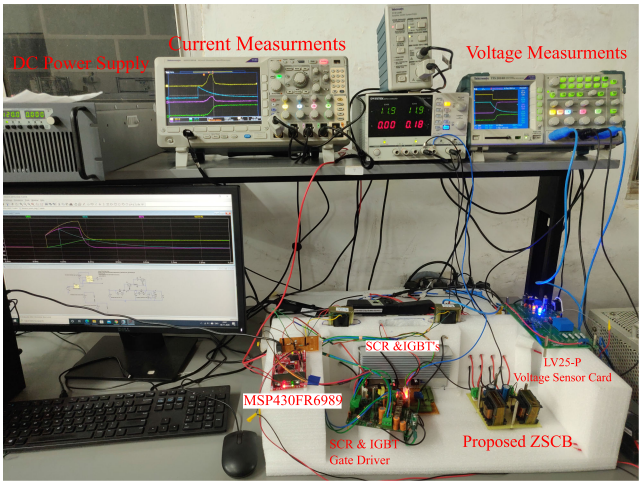


Fig. 11. Photograph of the proposed ZSCB experimental setup.

maximum current capability and its discharge rate. Voltage and current expressions of capacitor C_1 during its discharge period are as follows:

$$v_{c1} = V_s e^{-\frac{t}{R_D C_1}} \tag{23}$$

$$i_{c1} = \frac{V_s}{R_D} e^{-\frac{t}{R_D C_1}}. \tag{24}$$

For the system parameters given in Table I, the value of R_D is chosen from Fig. 10. Once we are done with selecting IGBT_2, and know its peak current capability then the corresponding R_D value can be chosen. With the selected value of resistance the discharge duration can be found from Fig. 10.

IV. Simulation and Experimental Validation of the Proposed ZSCB

To validate the performance of proposed concept, an experimental prototype along with simulation study in LTspice software platform with manufacturers datasheet models is developed. A photograph of the developed prototype is shown in Fig. 11, the corresponding system parameters are listed in Table I. Due to limitations in the laboratory, the prototype is developed for only 400 W, with dc system voltage/currents as 120 V/3.5 A. Main interruption device that is SCR is of $40TPS12\,A$ Vishay Siliconix make. While, IGBTs devices used are $H20R1203$ and corresponding gate drivers are custom made for our lab inverter systems. The dc system is emulated using a high power regulated dc source of rating 400 V/25 A from M/s. enArka. Inductors are wound on available ferrite cores (EE 42/21/20) in the laboratory, while the capacitors are selected from M/s. TDK Electronics. Gating pulses for IGBT and SCR are generated from $MSP430FR6989$ microcontroller. All the waveforms are captured using Tektronix oscilloscopes.

Experimental validation of the proposed MZSCB is performed considering two distinct situations on the dc system as follows.

A. Proposed ZSCB Validation During—Fault Interruption

In this case, the proposed dc circuit breaker is turned ON by providing firing pulses to the SCR and also allowed the dc system to operate in steady state. Steady-state current flowing in the load (resistive) is observed to be 3.5 A. Now, a fault is created on load side with a fault conductance of $G_f = 0.0555\,\mho$ which is more than the $G_{f,\text{min}} = 0.028\mho$. As a result, dc circuit breaker detects the fault, and automatically a tripping command is initiated. This process instantly results in capacitor C_2 discharge and further creates a zero current flow through the SCR. This way SCR is turned OFF. Simulation and experimental results pertaining to the above condition are elucidated in Figs. 12 and 13. Wherein, Fig. 12(a) and (b) shows the current waveforms, while Fig. 13(a) and (b) shows voltage waveforms during the fault interruption process. It may be noted that, the simulation and experimental results are in close agreement with each other.

As shown in the above results, the capacitor C_2 starts discharging soon after the fault, through a path consisting of C_2 - SCR - IGBT_1 - C_1 - fault. In this process capacitor C_1 starts charging and eventually it reaches to dc system voltage, on the other hand capacitor C_2 discharges completely and reaches to zero voltage.

B. Proposed ZSCB Validation During—Reclosing

After the fault is cleared and system is fully recovered, CB now needs to be closed again to restore the dc grid. In the reclosing process, first switch LS is closed. Later, a command to turn OFF IGBT_1 and turn ON IGBT_2 is issued simultaneously. After that, a gate triggering pulse for the SCR in given which further enables power flow in the dc system. In this process, capacitor C_2 starts charging and reaches to dc grid voltage while the capacitor C_1 discharges its energy completely through R_D and makes itself ready for the next fault interruption. As soon as capacitor C_1 voltage V_{c1} reaches to zero, then gate pulses for IGBT_1 and IGBT_2 are altered, such that IGBT_1 is ON and IGBT_2 is OFF. Simulation and experimental results pertaining to reclosure of proposed series ZSCB are presented in Figs. 14 and 15. Wherein, Fig. 14(a) and (b) shows CB current waveforms during its reclosure, while Fig. 15(a) and (b) shows the corresponding voltage waveforms.

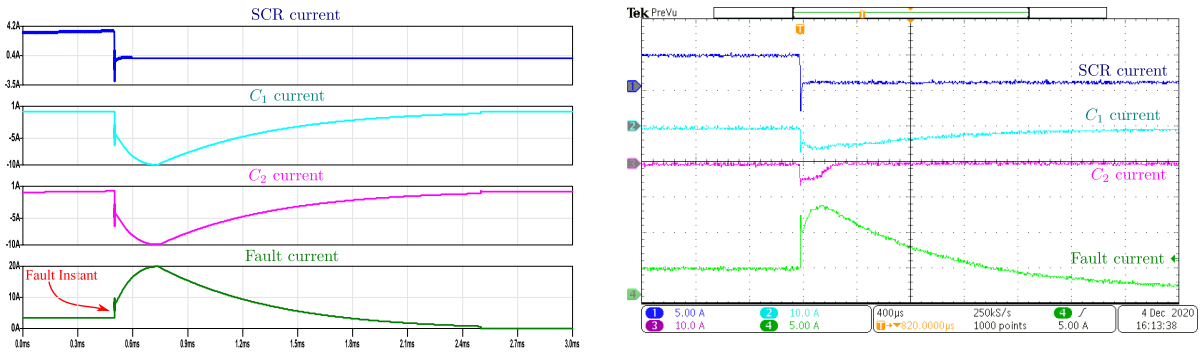


Fig. 12. Current waveforms of the proposed series ZSCB during fault interruption. (a) Simulation results. (b) Experimental results.

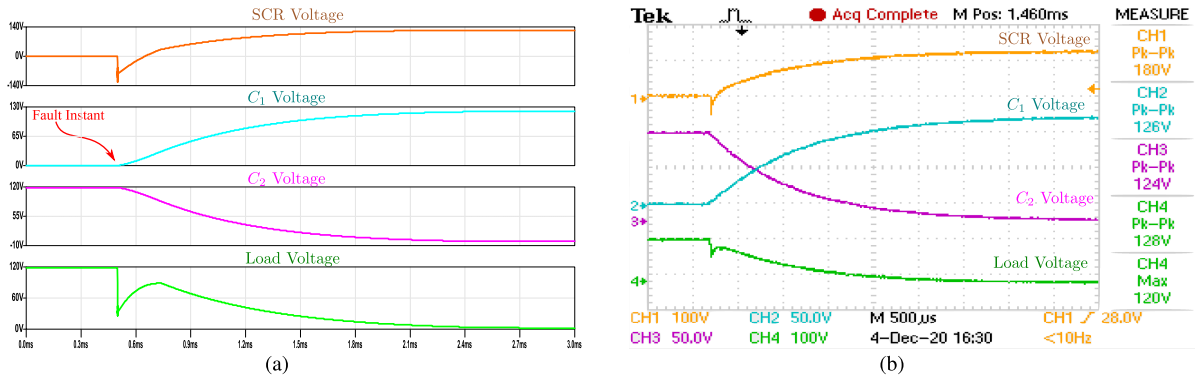


Fig. 13. Voltage waveforms of the proposed series ZSCB during fault interruption. (a) Simulation results. (b) Experimental results.

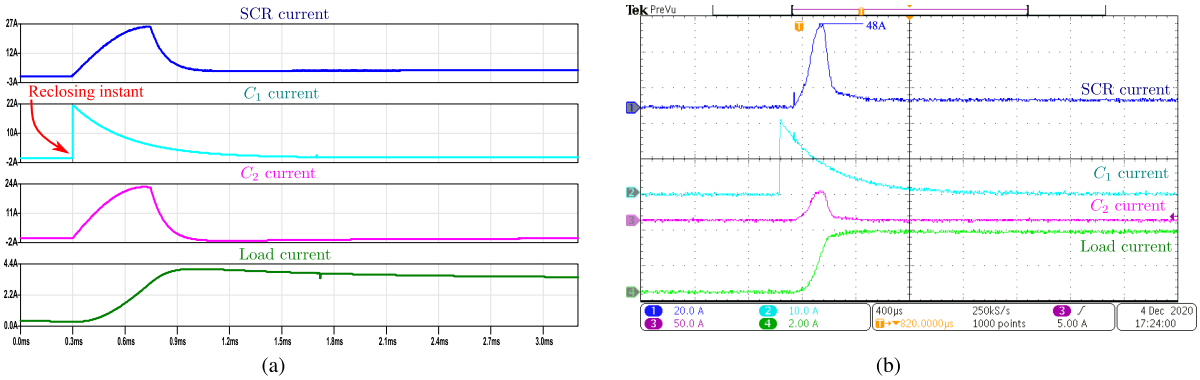
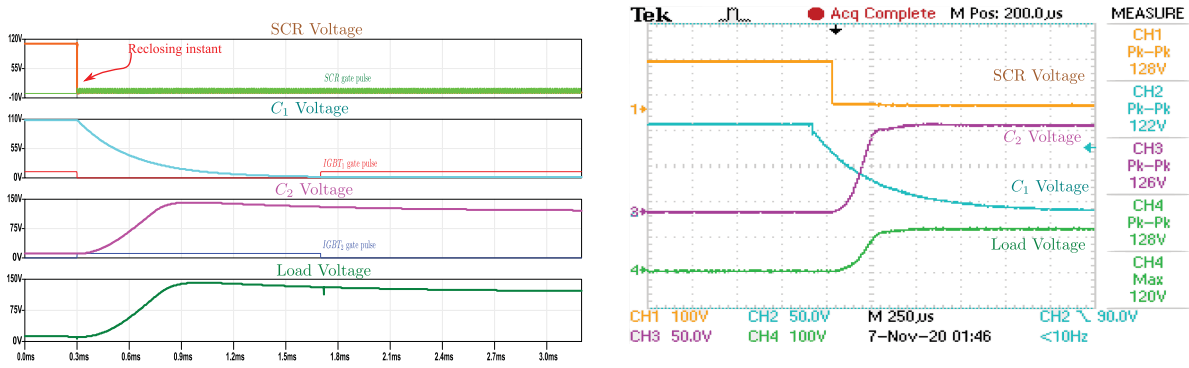


Fig. 14. Current waveforms of the proposed series ZSCB during reclosing process. (a) Simulation results. (b) Experimental results.

It may be noted from Fig. 14(a) and (b) that the starting current (48 A) in SCR during the reclosing process of the proposed concept is less when compared to the conventional series ZSCB (60.8 A) as given in Fig. 3(b). It may also be noted that there is no negative current flow in the load and also no unwanted power flow during reclosing/commissioning of the proposed series ZSCB. In voltage waveforms shown in Fig. 15(a) and (b), capacitor C_2 is charged to grid voltage, while capacitor C_1 discharges to zero independently in a loop consisting of C_1 - IGBT$_2$ - R_D. The energy in C_1 is dissipated as heat in R_D, which may be neglected as this energy is small in magnitude compared to the power transfer levels.

V. Comparison and Inferences

In this section, performance of the proposed MZSCBs is compared with various ZSCB reported in the literature. The features under consideration for the comparison are as follows.



(a) (b)

Fig. 15. Voltage waveforms of the proposed series ZSCB during reclosing process. (a) Simulation results. (b) Experimental results.

TABLE II
COMPARISON OF VARIOUS DC Z-SOURCE CIRCUIT BREAKERS

Features	Z-source DC Circuit Breaker Topology				
	Crossed [18]	Parallel [19]	Series [23]	Coupled [24]	Proposed
Common Ground	No	Yes	Yes	Yes	Yes
Fault current from source	I_{scr}	I_L+I_C	I_L	-	I_L
Z-source Transfer Function	Resonator	notch filter	low-pass	low-pass	low-pass
Input Filter integration	No	No	Yes	Yes	Yes
Fault current stress on Inductor	Medium	Medium	Medium	High	Medium
Negative current in load at reclosing	Yes	Yes	Yes	No	No
Starting current in SCR	High	High	High	Medium	Medium
SCR restriking possibility (tradeoff with capacitor size)	No	No	No	Yes	No
Number of Switches (SCRs, Diodes, IGBTs)	(1, 2, 0)	(1, 2, 0)	(1, 2, 0)	(1, 2, 0)	(1, 2, 2)

Ability of the breaker to provide common ground connection for source and the load, effect of fault current on the source, and type of transfer function, the proposed MZSCB retains the low-pass filtering action and thereby aids removing high-frequency components under normal operation, stress created on the inductor by the fault current, negative current flow in the load during the reclosing of the CB, starting current magnitude in the CB which decides the choice of SCR, and finally the SCR capability to interrupt the fault current efficiently without any restriking, and the number of switches used in the topology. The comparison is illustrated in Table II. It may be noted from the Table II that the proposed dc CB has similar performance characteristics when compared to [24], however, the proposed topology shows superior performance especially during fault interruption in terms of zero restriking possibility and lower magnitude of inductor current. Though the proposed dc CB uses higher number of components when compared to the existing topologies in the literature, it outperforms especially in terms of no-negative current in the load, low starting currents, and eliminates restriking possibility during a fault.

VI. CONCLUSION

This article presents a MZSCB. The proposed MZSCB addresses several challenges that exists in the conventional ZSCBs. They are as follows: 1) negative current circulation in the load during reclosing and commissioning, 2) unwanted power flow in the load during commissioning, and 3) high starting current flowing through the main SCR during reclosing and commissioning. This article also presents an exhaustive experimental and simulation analysis highlighting above listed problems in the conventional series ZSCBs. Later, a detailed design methodology for the proposed series ZSCB followed by an exhaustive simulation and experimental validation on a prototype with a voltage/current rating of 120 V/3.5 A is elucidated. The proposed topology is tested against faults and also during reclosing process to demonstrate its ability to interrupt faults with better performance.

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Venkata Raghavendra I. (Student Member, IEEE) received the bachelor's degree in electrical engineering from Acharya Nagarjuna University, Guntur, India, in 2010, and the master's degree in electrical engineering from the Indian Institute of Technology (IIT) Madras, Chennai, India, in 2012. He is currently working toward the Ph.D degree with the Department of Electrical Engineering with IIT Dharwad, Karnataka, India.

From 2012 to 2019, he was an Assistant Professor with the Department of Electrical Engineering, Bapatla Engineering College, Bapatla, Andhra Pradesh, India. His research interests include multilevel inverters, dc circuit breakers, and power converter applications in renewable energy systems and electric vehicles.

Satish Naik Banavath (Senior Member, IEEE) received the B.Tech. degree in electrical and electronics engineering from Acharya Nagarjuna University, Guntur, India, in 2010, the M.E. and Ph.D. degrees in electrical engineering from the Indian Institute of Science, Bengaluru, India, in 2012 and 2018, respectively.

From 2012 to 2014, he was with the Defence Research and Development Organization (DRDO), Ministry of Defence, Government of India, Bengaluru, India. He was a Postdoctoral Fellow with the University of Houston, Houston, TX, USA, from September 2017 to May 2018. Later, he joined Mahindra Electric Mobility Limited, Bengaluru, India, where he served as a Research and Development Manager, from July 2018 to January 2019. In February 2019, he joined the Indian Institute of Technology (IIT) Dharwad, Dharwad, Karnataka, where is currently an Assistant Professor with the Department of Electrical Engineering. His research interests include multilevel power converters, power converters for renewable energy conversion, electric vehicles, and dc circuit breakers.

Sreekanth Thamballa (Member, IEEE) received the bachelor's degree in electrical engineering from Acharya Nagarjuna University, Guntur, India, in 2010, the master's degree in power electronics and drives from the National Institute of Technology, Tiruchirapalli, India, in 2013, and the Ph.D degree in electrical engineering from the Indian Institute of Technology Madras, Chennai, India.

He is currently working as a Postdoctoral Associate with the University of Minnesota, Minneapolis, MN, USA. His research interests include single-stage inverters design and control, topologies and control schemes for multilevel inverters in renewable energy systems and electric vehicles.