Modeling, Design, and Evaluation of Active $\mathrm{d}v/\mathrm{d}t$ Balancing for Series-Connected SiC MOSFETs

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***Abstract*—Series connection of SiC MOSFETs provides an effective alternative to achieving higher blocking voltage with simpler circuit topologies. However, the voltage imbalance during the switching transient remains a critical issue. Recently, an active $\mathrm{d}v/\mathrm{d}t$ control approach utilizing a controllable equivalent Miller capacitor has been proved to be an effective, low-loss, and compact solution. This article renders an improved control circuit with comprehensive modeling and analysis. First, the original circuit is modified with an additional bipolar-junction-transistor and pulsed control signal so that the external capacitor can be fully reset every switching cycle. Second, a simplified model of the active $\mathrm{d}v/\mathrm{d}t$ control is derived to unveil the linear correlation between the control voltage and the device $\mathrm{d}v/\mathrm{d}t$ during the turn-OFF transient. Third, a feedback control model is described by difference equations for stability analysis, offering parameter selection guidelines for the control process. Fourth, experimental results with two series-connected SiC MOSFETs under 1.5-kV dc-link voltage are demonstrated to validate the open-loop control model and closed-loop stability. Finally, the control method is expanded to eight series-connected devices under 6 kV to prove its scalability and potential for medium-voltage high-current applications.**

***Index Terms*—Active $\mathrm{d}v/\mathrm{d}t$ control, series connection, silicon carbide (SiC) MOSFET.**

I. Introduction

THE emergence of wide-bandgap semiconductors, including silicon carbide (SiC) devices, enables significantly improved efficiency and power density of power electronic systems, thanks to their characteristics superiority [1], [2]. Although the available voltage level of SiC MOSFET devices has been gradually increasing [3], [4], to pursue higher system voltages for less conductor weight and losses, direct device stacking can further help to break the limit of a single device voltage-blocking capability. Nevertheless, static and dynamic voltage imbalance between devices is inevitably caused by several factors: tolerance in device parameters [5], gate signal timing mismatch, package and layout parasitics [6], etc. The imbalance becomes more challenging with the device switching speed as high as 100 V/ns if SiC MOSFETs are brought into play. The unbalanced voltages can result in system failures due to device breakdown or unbalanced thermal stresses. Therefore, different types of balancing techniques [7], which mainly fall into three categories, have been investigated to ensure voltage balancing for both the steady state and the switching transient.

The first category of balancing methods is to add additional components connected to the drain side. Passive resistor–capacitor–diode (RCD) snubber or clamping circuit is the most intuitive method with minimized cost and control effort [8]–[15]. To reduce the size of the snubber circuit, a concentrated method [16] is proposed so that the snubber circuit is not necessarily required by each device. To reduce the losses of the snubber circuit, an active switch is added so that the energy stored during the balancing process can be reused to reduce the losses [17], [18]. A hybrid method utilizing clamping circuit and gate control is proposed in [19] and [20] to optimize the system performance. These balancing methods, especially for solutions only utilizing passive components, are usually simple and robust. However, the size and losses added to the main circuit especially for high-voltage high-current applications are not negligible. With the same RCD snubber circuit in use, the super-cascode structure proposed in [21] and [22] provides a simple and robust solution to increase total blocking voltage by series connection of several high-voltage normally ON SiC JFETs and one controlled MOSFET. However, devices are turned ON and OFF sequentially, resulting in an unavoidable unbalance of device losses, which limits its power capability.

The second category of balancing methods is to add additional components connected to the gate side. For the passive gate coupling method, many works have been done to drive multiple series-connected devices with one set of driving circuit to minimize the system complexity [23]–[28]. These methods minimized the cost and number of components to drive multiple devices in series. However, accurate voltage balancing cannot

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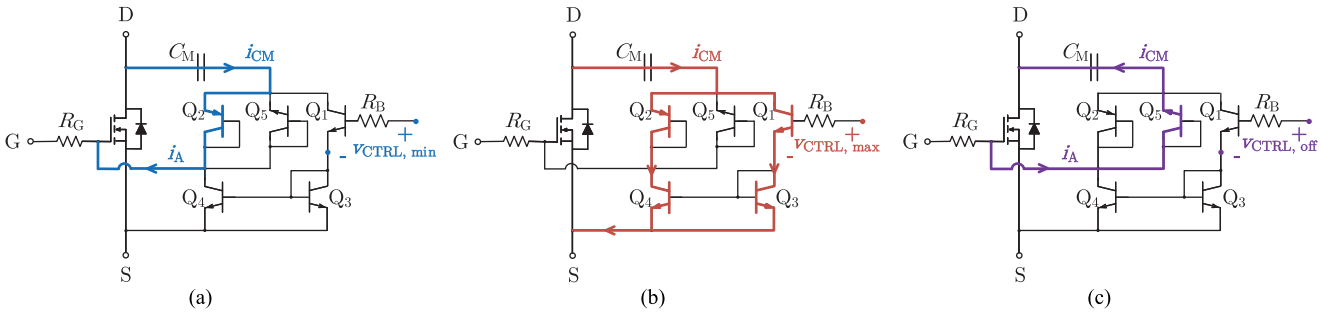

Fig. 1. Working principles of the VCCS. (a) BJT network current flow when v_{CTRL} has the minimum value. (b) BJT network current flow when v_{CTRL} has the maximum value. (c) BJT network current flow when C_{M} is discharging.

be guaranteed, especially in applications where high switching speed is required. Furthermore, the complex parasitic effects also limit the number of devices that can be series connected. Different from utilizing capacitive coupling, another approach in [29] uses magnetizing coupling to clamp gate voltage. However, this method will lead to higher gate loop inductance, and the size is not small.

In order to have a more flexible and accurate balancing behavior, the active gate control is the third category although the system complexity is increased. One straightforward method is to control gate delays [30]–[33]. With this method, if the unbalance is caused by different switching speeds, the faster device has to be turned OFF later to balance the voltage, which leads to lower switching loss. Therefore, potential thermal management is more difficult because of the unbalanced losses. Also, considering the cases with more than two devices in series, the control for gate delay may conflict against one another. Another active gate control method is to tune the device switching speed directly including active gate resistance control [34]–[36], active gate current control [37]–[39], and active gate–drain compensation [40], [41]. The idea of adding a controllable equivalent Miller capacitor using a bipolar-junction-transistor (BJT) network to inject gate current for active $\mathrm{d}v/\mathrm{d}t$ control was originally proposed for electromagnetic interference optimization purpose in [42] and later leveraged for SiC MOSFET voltage balancing [40]. The method was verified to be compact, efficient, and accurate for balancing series-connected SiC MOSFETs, but many aspects remained to be addressed.

As a continuation of the work in [40], the contributions of this article reside in the following aspects. First, the original circuit is modified with an additional BJT and pulsed control signal so that the externally added capacitor can be fully discharged (reset) every switching cycle. Second, an analytical model for active $\mathrm{d}v/\mathrm{d}t$ control is derived unveiling the linear correlation between the control voltage v_{CTRL} and the device turn-OFF $\mathrm{d}v/\mathrm{d}t$. Third, stability analysis of the closed-loop feedback control is carried out providing a proper parameter selection for a stable control process. Finally, the control method is validated in the cases with multiple devices in series, including four switches under 2 kV and eight switches under 6 kV, to demonstrate the scalability and potential of the proposed active $\mathrm{d}v/\mathrm{d}t$ balancing in medium-voltage applications.

The remaining sections of this article are organized as follows. Section II introduces the working principles of the modified balancing circuit, including the design of the open-loop voltage-controlled current source (VCCS) and the closed-loop feedback control circuit. Subsequently, modeling and quantitative analysis of the BJT network, the VCCS, and the MOSFET turn-OFF transient behavior is derived in Section III. After the open-loop analysis, in Section IV, the stability analysis is done for the feedback control to find out how circuit parameters will affect the stability/convergence of the balancing circuit. Section V introduces the hardware prototype design and implementation of the system up to 6 kV. Experimental results and validations of the system are demonstrated in Section VI. Finally, Section VII concludes this article.

II. Working Principles of the Active $\mathrm{d}v/\mathrm{d}t$ Control

A. Voltage-Controlled Current Source

In Fig. 1, the VCCS added to the main power MOSFET includes an external capacitor C_{M}, five BJTs from Q_1 to Q_5, and a current limiting resistor R_{B} connected to the base of Q_1. When the MOSFET is switching, an induced current i_{CM} will be generated and guided to the gate or source of the MOSFET depending on v_{CTRL}. Assuming that v_{GS} and the BJTs' conduction voltages are negligible compared to v_{DS} during switching transients, we have

$$i_{\mathrm{CM}} = C_{\mathrm{M}} \frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}. \tag{1}$$

For the BJT network, Q_1 is in series with Q_3. At the same time, Q_3 and Q_4 form a current mirror, so

$$i_{\mathrm{Q1}} = i_{\mathrm{Q3}} = i_{\mathrm{Q4}}. \tag{2}$$

During the MOSFET turn-OFF transient, when v_{CTRL} is at its minimum value and Q_1 is turned OFF, all the induced current i_{CM} has to flow via Q_2 to the gate of the MOSFET [cf. Fig. 1(a)], which leads to the lowest MOSFET turn-OFF $\mathrm{d}v/\mathrm{d}t$. In this case, the active current i_{A} injecting into the gate is

$$i_{\mathrm{A,max}} = i_{\mathrm{CM}}. \tag{3}$$

When v_{CTRL} is at its maximum value and Q_1 is fully turned ON, for the ideal case, the induced current i_{CM} will be evenly shared between Q_1 and Q_2, so there is no current injecting into the gate

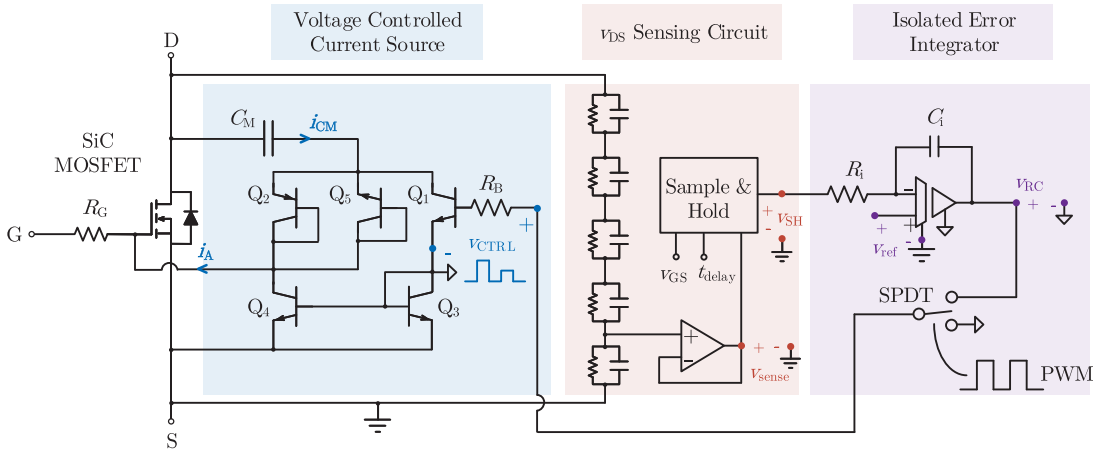

Fig. 2. Schematics of the closed-loop feedback control.

of the MOSFET [cf. Fig. 1(b)], which leads to the highest MOSFET turn-OFF $\mathrm{d}v/\mathrm{d}t$. In this case, the active current i_A injecting into the gate is

$$i_{A,\min} = 0. \tag{4}$$

Therefore, by controlling the v_{CTRL}, i.e., the base current of Q_1, different amount of i_A can be injected into the gate of MOSFET to control the device turn-OFF speed, where

$$i_A \in [0, 1] \cdot i_{CM}. \tag{5}$$

Transistor Q_5 works during the turn-ON transient of the MOSFET [cf., Fig. 1(c)] like a diode so that the external capacitor C_M can be fully discharged.

B. Feedback Control of the Active dv/dt Balancing

With the help of the VCCS, the gate injection current i_A can control the $\mathrm{d}v/\mathrm{d}t$ of a single MOSFET. Therefore, a closed-loop feedback control can serve to adjust v_{CTRL} automatically to a proper value balancing the voltage between two MOSFETs according to the comparison result between the sensed MOSFET v_{DS} and a reference voltage v_{ref}. The full schematic of the closed-loop control method in Fig. 2 falls into three parts: the VCCS, the v_{DS} sensing circuit, and the isolated error integrator. In this section, it is assumed that there are only two devices in series, and only the top device is under control. Fig. 3 presents essential operating waveforms of variables labeled in Fig. 2 during the control process. Device switching sequence is synchronized with the system pulsewidth modulation (PWM) signal presented in the first row of Fig. 3. When the MOSFET turns OFF at t_{off}, the top device v_{DS} starts to increase. This voltage information is sensed by a voltage divider with resistors and capacitors in parallel to increase sensing bandwidth. Multiple RC pairs are series connected to increase sensing circuit insulation capability. Following the voltage divider, the buffered signal v_{sense} is sent to a sample-and-hold (S&H) block. The sampling instant t_{SH} is synchronized with PWM falling edge with a delay t_{delay} to sample the steady-state value other than the oscillation interval of v_{DS}. This v_{SH} value will be held for the entire switching cycle

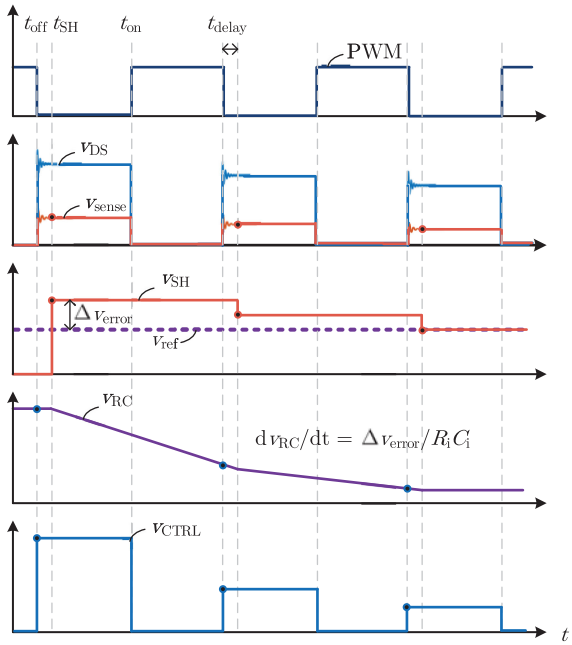

Fig. 3. Operating waveforms of the closed-loop control.

until the S&H circuit is triggered by the next PWM falling edge and updates the new v_{SH} value. Subsequently, v_{SH} is compared with a reference value v_{ref} as the input to the isolated error integrator. The output of the integrator v_{RC} will keep changing until the error between the sampled value and the reference value is eliminated. Finally, the sampled output of the integrator is modulated by an S&H single-pole double-throw (SPDT) switch to generate a pulsed v_{CTRL} as the control voltage, which is synchronized with the system PWM signal. The purpose of such design is to ensure that C_M is fully discharged by Q_5 when the MOSFET is turned ON. Since the reference point of v_{CTRL}, i.e., the emitter of Q_1, is different from the MOSFET source voltage potential, an isolation barrier is required for the error integrator. The voltage difference of two isolated grounds is the

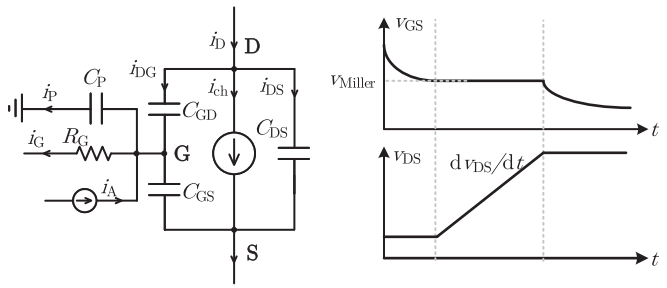

Fig. 4. Equivalent circuit model of MOSFET during turn-OFF transient.

collector–emitter voltage of a BJT. Detailed voltage sampling circuit design and power isolation schemes can be found in [40].

III. Analytical Model of the Open-Loop Active $\mathrm{d}v/\mathrm{d}t$ Control

A. Modeling of the VCCS

A single BJT is a current-controlled device. By adding a base resistor R_B, the BJT can be controlled by a voltage source. The emitter current of Q_1 can be calculated by

$$i_{\mathrm{Q1}} = \beta \cdot \frac{v_{\mathrm{CTRL}} - V_{\mathrm{BE,on}}}{R_\mathrm{B}} \tag{6}$$

where β is the common-base current gain of the BJT, and $V_{\mathrm{BE,on}}$ is the voltage drop from base to emitter that is typically around 0.7 V. The active current injecting into the power MOSFET gate i_A can be calculated by

$$\begin{aligned} i_A &= i_{\mathrm{Q2}} - i_{\mathrm{Q4}} = i_{\mathrm{CM}} - i_{\mathrm{Q1}} - i_{\mathrm{Q4}} \\ &= C_\mathrm{M}\frac{dv_\mathrm{DS}}{dt} - 2 \cdot i_{\mathrm{Q1}} \\ &= C_\mathrm{M}\frac{dv_\mathrm{DS}}{dt} - 2\beta \cdot \frac{v_{\mathrm{CTRL}} - V_{\mathrm{BE,on}}}{R_\mathrm{B}}. \end{aligned} \tag{7}$$

It is noted that this equation is only valid when the BJT is working in the forward-active region. If v_{CTRL} is smaller than $V_{\mathrm{BE,on}}$, I_{Q1} will be 0. Also, the current i_A cannot be negative regardless of the v_{CTRL} value.

B. Modeling of the SiC MOSFET During Turn-OFF Transient

With the correlation between the control voltage v_{CTRL} and the injected active current i_A, there is still one step missing to calculate device switching speed. Therefore, a MOSFET turn-OFF transient model is herein derived step by step with an equivalent turn-OFF model presented in Fig. 4.

1) Calculation of the Bottom Device dv/dt: For the bottom MOSFET, there is neither active current injection nor induced current through a parasitic capacitor to the ground. During the Miller plateau region, the channel current i_{ch} can be calculated by the linearized approximation equation

$$i_{\mathrm{ch}} \approx g_\mathrm{m}\left(v_{\mathrm{miller}} - V_{\mathrm{th}}\right) \tag{8}$$

where g_m is the transconductance of the MOSFET, v_{miller} is the Miller plateau voltage, and V_{th} is the threshold voltage of the MOSFET. From the circuit model, we have

$$i_{\mathrm{DG}} = i_\mathrm{G} = \frac{v_{\mathrm{miller}} - V_{\mathrm{GS,off}}}{R_\mathrm{G}} \tag{9}$$

$$\frac{\mathrm{d}v_{\mathrm{DS,bot}}}{\mathrm{d}t} = \frac{i_{\mathrm{DG}}}{C_{\mathrm{GD}}} = \frac{i_\mathrm{D} - i_{\mathrm{ch}}}{C_{\mathrm{oss}}} \tag{10}$$

where $V_{\mathrm{GS,off}}$ is the gate driver turn-OFF voltage for the gate, and C_{oss} is the sum of C_{GD} and C_{DS}. Therefore, the bottom device turn-OFF speed is

$$\frac{\mathrm{d}v_{\mathrm{DS,bot}}}{\mathrm{d}t} = \frac{g_\mathrm{m}\left(V_{\mathrm{th}} - V_{\mathrm{GS,off}}\right) + i_\mathrm{D}}{\left(g_\mathrm{m}R_\mathrm{G} + 1\right)C_{\mathrm{GD}} + C_{\mathrm{DS}}}. \tag{11}$$

2) Calculation of Top Device $\mathrm{d}v/\mathrm{d}t$: For the top device, since the bottom device is switching, there will be an induced current i_P flowing through the parasitic capacitor C_p to the ground. For this case, we have

$$i_{\mathrm{DG}} = i_\mathrm{G} + i_\mathrm{P} = \frac{v_{\mathrm{miller}} - V_{\mathrm{GS,off}}}{R_\mathrm{G}} + C_\mathrm{P}\frac{\mathrm{d}v_{\mathrm{DS,bot}}}{\mathrm{d}t} \tag{12}$$

$$\frac{\mathrm{d}v_{\mathrm{DS,top}}}{\mathrm{d}t} = \frac{g_\mathrm{m}\left(V_{\mathrm{th}} - V_{\mathrm{GS,off}}\right) + i_\mathrm{D} + g_\mathrm{m}R_\mathrm{G}C_\mathrm{P}\dfrac{\mathrm{d}v_{\mathrm{DS,bot}}}{\mathrm{d}t}}{\left(g_\mathrm{m}R_\mathrm{G} + 1\right)C_{\mathrm{GD}} + C_{\mathrm{DS}}}. \tag{13}$$

By comparing (11) and (13), it can be found that C_p is an important factor that will cause the top device switching faster than the bottom during the turn-OFF transient. Also, there will be parasitic capacitance from the drain side to the ground, but this capacitor will be equivalently in parallel with, and much smaller than, the C_{DS} of the MOSFET. Therefore, only the gate-side parasitic capacitor to ground is considered.

3) Calculation of Top Device $\mathrm{d}v/\mathrm{d}t$ With Active Control: With the active current taken into account, we have

$$i_{\mathrm{DG}} = i_\mathrm{G} + i_P - i_A. \tag{14}$$

The top device switching speed can be defined by

$$\frac{\mathrm{d}v_{\mathrm{DS,top,ctrl}}}{\mathrm{d}t} = A \cdot v_{\mathrm{CTRL}} + B \tag{15}$$

where

$$\begin{cases} A = \dfrac{2g_\mathrm{m}R_\mathrm{G}\beta/R_\mathrm{B}}{g_\mathrm{m}R_\mathrm{G}\left(C_{\mathrm{GD}} + C_\mathrm{M}\right) + C_{\mathrm{GD}} + C_{\mathrm{DS}}} \\ B = \dfrac{g_\mathrm{m}\left(V_{\mathrm{th}} - V_{\mathrm{GS,off}}\right) + i_\mathrm{D} + \Delta}{g_\mathrm{m}R_\mathrm{G}\left(C_{\mathrm{GD}} + C_\mathrm{M}\right) + C_{\mathrm{GD}} + C_{\mathrm{DS}}} \\ \Delta = g_\mathrm{m}R_\mathrm{G}\left(C_\mathrm{P}\dfrac{\mathrm{d}v_{\mathrm{DS,bot}}}{\mathrm{d}t} - 2\beta\dfrac{V_{\mathrm{BE,on}}}{R_\mathrm{B}}\right). \end{cases} \tag{16}$$

For (15), if $v_{\mathrm{CTRL}} = V_{\mathrm{BE,on}}$, i.e., its minimum effective value,

$$\frac{\mathrm{d}v_{\mathrm{DS,top,ctrl}}}{\mathrm{d}t} = \frac{g_\mathrm{m}\left(V_{\mathrm{th}} - V_{\mathrm{GS,off}}\right) + i_\mathrm{D} + g_\mathrm{m}R_\mathrm{G}C_\mathrm{P}\dfrac{\mathrm{d}v_{\mathrm{DS,bot}}}{\mathrm{d}t}}{g_\mathrm{m}R_\mathrm{G}\left(C_{\mathrm{GD}} + C_\mathrm{M}\right) + C_{\mathrm{GD}} + C_{\mathrm{DS}}}. \tag{17}$$

Compared with (13), the equivalent Miller capacitor becomes $C_{\mathrm{GD}} + C_\mathrm{M}$, which means that the added external capacitor C_M is now in parallel with C_{DG} to slow down the top device. From

(16), parameter A, which presents the sensitivity of the active control, is highly related to the VCCS component selection, including β and $R_{\rm B}$ but not related to some system operation parameters such as $i_{\rm D}$ or $C_{\rm P}$.

IV. Analytical Model of the Closed-Loop Feedback Control

With the linear correlation between the control voltage $v_{\rm CTRL}$ and $\mathrm{d}v/\mathrm{d}t$ of the MOSFET under derived control, the next important step is to quantify the closed-loop feedback control scheme and analyze its stability. Although $v_{\rm CTRL}$ and $v_{\rm DS}$ are pulsating, the values during the turn-OFF steady state are the only important factors for this model. In addition, the transient procedure during the device turn-OFF, specifically, the Miller plateau region, is usually at a tens-of-nanoseconds level, which is negligible compared to the switching period in a tens-of-microsecond range or even higher. Therefore, many variables such as $v_{\rm DS}$, $v_{\rm SH}$, and $v_{\rm CTRL}$ in Fig. 3 can be treated as constant values, which are updated once per switching cycle. With this assumption, the overall modeling work is largely simplified so that the system can be described by discrete difference equations instead of continuous differential equations.

A. Functional Blocks of the Feedback Control Schematics

Since the top and bottom devices are in series, their $v_{\rm DS}$ is determined by how fast they are switching during the turn-OFF transient if there is no obvious switching delay mismatch. The drain-to-source voltage of the controlled top device during the OFF-state is calculated by

$$v_{\rm DS,top,ctrl} = V_{\rm bus} \cdot \frac{\dfrac{\mathrm{d}v_{\rm DS,top,ctrl}}{\mathrm{d}t}}{\dfrac{\mathrm{d}v_{\rm DS,top,ctrl}}{\mathrm{d}t} + \dfrac{\mathrm{d}v_{\rm DS,bot}}{\mathrm{d}t}} \tag{18}$$

where $V_{\rm bus}$ is the total dc-link voltage. The top device voltage is sensed by a voltage divider with a $k_{\rm d}:1$ ratio; then, we have

$$v_{\rm SH} = \frac{v_{\rm DS,top,ctrl}}{k_{\rm d}}. \tag{19}$$

For each switching cycle, the output of the isolated error integrator keeps changing linearly proportional to the input error, where $R_{\rm i}$ and $C_{\rm i}$ determine the time constant and $T_{\rm s}$ is the switching period. Therefore, the voltage change of $v_{\rm RC}$ per switching period is

$$\Delta v_{\rm RC} = \frac{V_{\rm ref} - v_{\rm SH}}{R_{\rm i}C_{\rm i}} \cdot T_{\rm s} \tag{20}$$

where

$$V_{\rm ref} = \frac{1}{2} V_{\rm bus}/k_{\rm d} \tag{21}$$

when there are two devices in series connection.

B. Closed-Loop Convergence and Stability Analysis

As mentioned before, the closed-loop feedback system is simplified to be described by difference equations. The $v_{\rm CTRL}$ value of the $(n+1)$th iteration can be calculated with the $v_{\rm CTRL}$ value of the nth iteration from the result of (20), as

$$v_{\rm CTRL,n+1} = v_{\rm CTRL,n} + \frac{V_{\rm ref} - v_{\rm SH,n}}{R_{\rm i}C_{\rm i}} \cdot T_{\rm s}. \tag{22}$$

The S&H value $v_{\rm SH}$ of the nth iteration can be calculated by combining (15), (16), (18), and (19) as

$$\begin{aligned} v_{\rm SH,n} &= \frac{V_{\rm bus}}{k_{\rm d}} \cdot \frac{\dfrac{\mathrm{d}v_{\rm DS,top,ctrl}}{\mathrm{d}t}}{\dfrac{\mathrm{d}v_{\rm DS,top,ctrl}}{\mathrm{d}t} + \dfrac{\mathrm{d}v_{\rm DS,bot}}{\mathrm{d}t}} \\ &= \frac{V_{\rm bus}}{k_{\rm d}} \cdot \frac{Av_{\rm CTRL,n} + B}{Av_{\rm CTRL,n} + B + k_{\rm bot}} \\ &= \frac{V_{\rm bus}}{k_{\rm d}} \cdot \frac{v_{\rm CTRL,n} + B/A}{v_{\rm CTRL,n} + (B + k_{\rm bot})/A} \end{aligned} \tag{23}$$

where $k_{\rm bot}$ is a simplified representation of $\mathrm{d}v_{\rm DS,bot}/\mathrm{d}t$. Therefore, the $v_{\rm CTRL}$ value of the $(n+1)$th iteration can be calculated from (22) and (23) as

$$v_{\rm CTLR,n+1} = \frac{{v_{\rm CTRL,n}}^2 + E \cdot v_{\rm CTRL,n} + F}{v_{\rm CTRL,n} + G} = f\left(v_{\rm CTRL,n}\right) \tag{24}$$

where

$$\begin{cases} E = \dfrac{2BR_{\rm i}C_{\rm i}k_{\rm d} + 2R_{\rm i}C_{\rm i}k_{\rm d}k_{\rm bot} - AT_{\rm s}V_{\rm bus}}{2AR_{\rm i}C_{\rm i}k_{\rm d}} \\ F = \dfrac{T_{\rm s}V_{\rm bus}k_{\rm bot} - BT_{\rm s}V_{\rm bus}}{2AR_{\rm i}C_{\rm i}k_{\rm d}} \\ G = \dfrac{BR_{\rm i}C_{\rm i}k_{\rm d} + R_{\rm i}C_{\rm i}k_{\rm d}k_{\rm bot}}{AR_{\rm i}C_{\rm i}k_{\rm d}}. \end{cases} \tag{25}$$

Now, $v_{\rm CTRL}$ is described by a first-order nonlinear difference equation. As such, the stability of the closed-loop control scheme can be transferred to the question whether the steady-state solution of the difference equation is stable. At the steady state, the controlled top device has the same switching speed as the bottom device, giving

$$\frac{\mathrm{d}v_{\rm DS,top,ctrl}}{\mathrm{d}t} = A \cdot v_{\rm CTRL} + B = k_{\rm bot} \tag{26}$$

to which the steady-state solution is

$$\bar{v}_{\rm CTRL} = \frac{k_{\rm bot} - B}{A}. \tag{27}$$

To let the steady-state solution of (24) be asymptotically stable, the following condition must be met [43]:

$$\left| \frac{\mathrm{d}f(\bar{v}_{\rm CTRL})}{\mathrm{d}v_{\rm CTRL}} \right| < 1. \tag{28}$$

The proof of this theorem is attached in the Appendix. Combining (24), (25), and (27), we obtain

$$\frac{\mathrm{d}f(\bar{v}_{CTRL})}{\mathrm{d}v_{\rm CTRL}} = 1 - \frac{AV_{\rm bus}k_{\rm bot}}{k_{\rm d}(B + k_{\rm bot} + A\bar{v}_{\rm CTRL})^2} \cdot \frac{T_{\rm s}}{R_{\rm i}C_{\rm i}}. \tag{29}$$

Therefore, from (28) and (29), the system steady-state solution $\bar{v}_{\rm CTRL}$ is stable, i.e., the control system leads to convergence

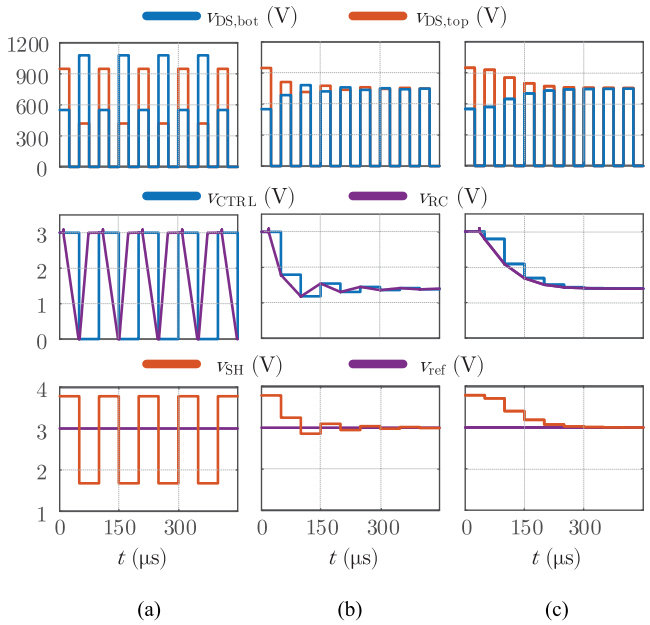

Fig. 5. Simulation waveforms of the closed-loop feedback control with result of (a) divergence when $R_iC_i = 10\,\mu$s, (b) oscillatory convergence when $R_iC_i = 20\,\mu$s, and (c) monotonic convergence when $R_iC_i = 50\,\mu$s.

when

$$R_iC_i > \frac{AV_{bus}T_s}{8k_dk_{bot}}. \tag{30}$$

Specifically, if

$$0 < \frac{df(\bar{v}_{CTRL})}{dv_{CTRL}} < 1 \tag{31}$$

the system leads to monotonic convergence when

$$R_iC_i > \frac{AV_{bus}T_s}{4k_dk_{bot}}. \tag{32}$$

C. Simulation and Discussion of the Closed-Loop Control

To present the detailed operating waveforms and validate the analysis of the convergence criteria, simulations with different R_iC_i are done as displayed in Fig. 5. In the simulation, two devices are connected in series with the active dv/dt control circuit for the top device, where $A = 4\,\text{ns}^{-1}$, $k_{bot} = 9.5$ V/ns, $V_{bus} = 1500$ V, $T_s = 50\,\mu$s, and $k_d = 250$. For each simulation result, device voltage v_{DS}, sampling and hold voltage v_{SH}, and control voltage v_{CTRL} are all recorded and compared. According to (30) and (32), the system should converge when $R_iC_i > 15.79\,\mu$s. Also, the system should have a monotonic converge when $R_iC_i > 31.58\,\mu$s. Simulation result in Fig. 5 lists three conditions when the system is diverging, oscillatorilly converging, and monotonically converging, which matches the mathematical analysis.

To release the concern on the dynamic performance of the proposed dv/dt control and the closed-loop control method, a simulation is done with results presented in Fig. 6. In the simulation, the real application condition is simulated that the dc-link bus will have a start-up procedure and ripple at the steady state. Also, the step response is added to compare with the later

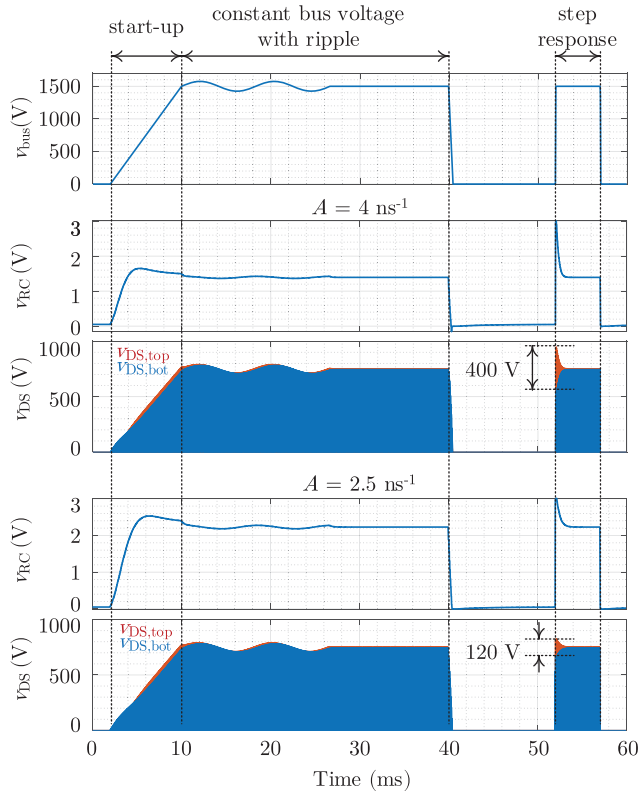

Fig. 6. Simulation waveforms of the closed-loop control dynamic performance.

test results. In Fig. 6, the bus voltage v_{bus}, error integrator output voltage v_{RC}, and two devices' v_{DS} are plotted. From the simulation, the control method can accurately balance two devices' voltage during the dynamic changing of the bus voltage during the ramp-up and bus ripple with low voltage difference between two devices. To reduce the step-response mismatch of two devices, resistor R_B can be increased to reduce A value of the loop gain. As presented in Fig. 6, when $A = 4\,\text{ns}^{-1}$, the mismatch of two device v_{DS} during the step response is 400 V, while the voltage is reduced to 120 V if $A = 2.5$ ns^{-1}. At the same time, with the model derived in this article, the required balancing point can be calculated; if a digital control system is implemented, there will be more flexibility for the control with better dynamic performance.

V. Hardware Design and Implementation

A. Prototype of a Phase-Leg Configuration

A phase-leg configuration test bed is built to verify the working principle of the proposed active dv/dt control method with schematics presented in Fig. 7 and a hardware prototype displayed in Fig. 8. The devices under test are four 1.7-kV SiC MOSFET power modules. Each module consists of two MOSFET switches in series to have eight stacked SiC MOSFET devices S_1–S_8. The synchronized eight switches function equivalently as a 13.6-kV switch. The active dv/dt control circuit is enabled on the gate drivers of MOSFETs S_2–S_8, while it is disabled on S_1. This design ensures the voltages of S_2–S_8 to follow the reference

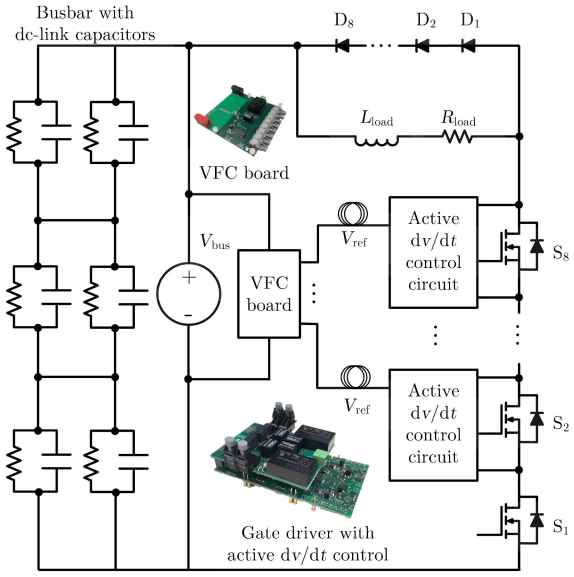

Fig. 7. Schematics of the test setup.

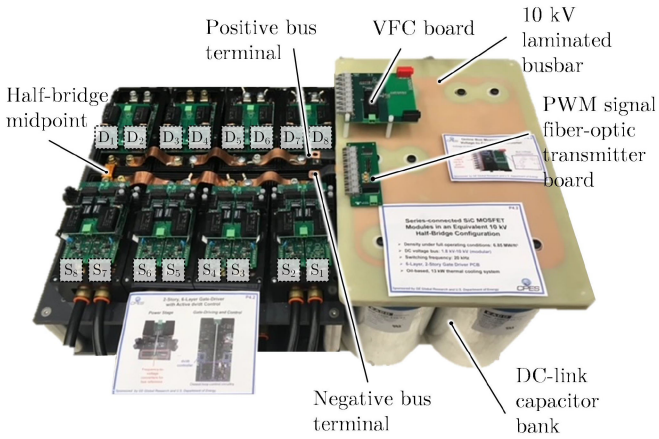

Fig. 8. Prototype of the 6-kV phase-leg configuration.

and allows the bottom device S_1 to take the remaining dc voltage; conflicting among controllers is, hence, avoided.

Serving as freewheeling diodes D_1–D_8, eight additional devices (four additional 1.5-kV MOSFET modules) are connected in series with each device gate-to-source clamped to a negative biased voltage. To perform the multiple-pulse test, the switching current is tuned and limited by the load inductor L_{load} and resistor R_{load}. To provide a stable voltage source during the test, a laminated busbar with a dc-link capacitor bank is also designed. The laminated busbar is tested to be partial discharge free up to 10 kV. For the capacitor bank, 3 kV, 125-µF capacitors are connected in series and parallel, as displayed in Fig. 7, to increase voltage level and total capacitance. For each capacitor, a bleeding resistor is connected in parallel to balance the voltage and dissipate stored energy after the test. The major components for the test setup are summarized in Table I.

TABLE I
COMPONENTS OF THE 6-kV PHASE-LEG SETUP

S_1∼S_8 1.7 kV SiC MOSFET	QJD1740001
D_1∼D_8 1.5 kV SiC MOSFET	QJD1520001
dc-link capacitor	3 kV, 125 µF (each)
dc-link bleeding resistor	100 kΩ (each)
device static balancing resistor	200 kΩ (each)
load inductor L_{load}	1 mH
load resistor R_{load}	0-30 Ω (tunable)
active control capacitor C_{M}	82 pF
BJT base resistor R_{B}	200 Ω
Device gate resistor R_{G}	5.1 Ω

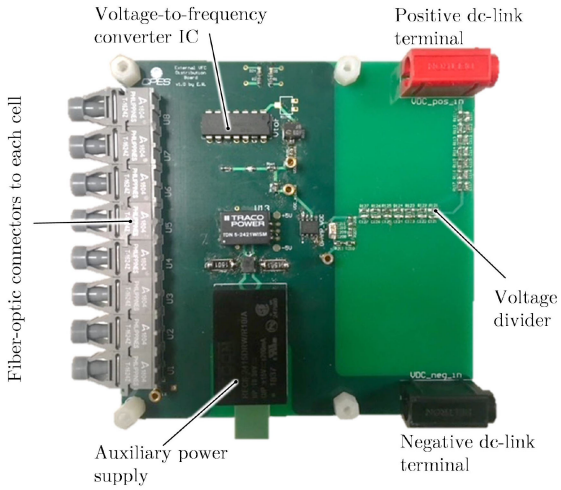

Fig. 9. Hardware prototype of the VFC board.

B. Voltage-to-Frequency Conversion (VFC) Board

The VFC board enables the real-time sensing of the dc-link voltage V_{bus}, transfers the voltage signal to frequency signal, and sends this information to each gate driver through optical fibers. In Fig. 9, the dc-link voltage is first scaled down through the voltage divider. Similar to the voltage divider in the active gate driver, a resistor–capacitor string is implemented to guarantee the sensing bandwidth. This scaled-down voltage signal is then sent through a voltage follower circuit. After the snubber, the voltage signal is converted to a frequency signal using a VFC converter IC (part number VFC320 from Texas Instruments). In order to provide isolation from the online bus voltage measurement board and each gate driver, fiber-optic communication is implemented. Once each gate driver receives the frequency signal that corresponds to the bus voltage reference, the same converter IC is used as a frequency-to-voltage converter (FVC) on each gate driver board. The reference voltage V_{ref} for the error integrator is then generated from the output of the FVC.

C. Gate Driver With Active dv/dt Control

The gate driver prototype with active dv/dt control is shown in Fig. 10. Each gate driver is symmetrical, and each half of it drives one device of the same module. For the two-level design of the gate driver, the top board includes the isolated auxiliary

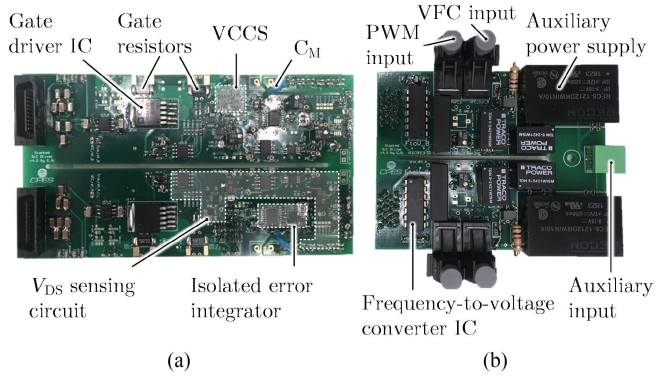

Fig. 10. (a) and (b) Hardware prototype of the active gate driver.

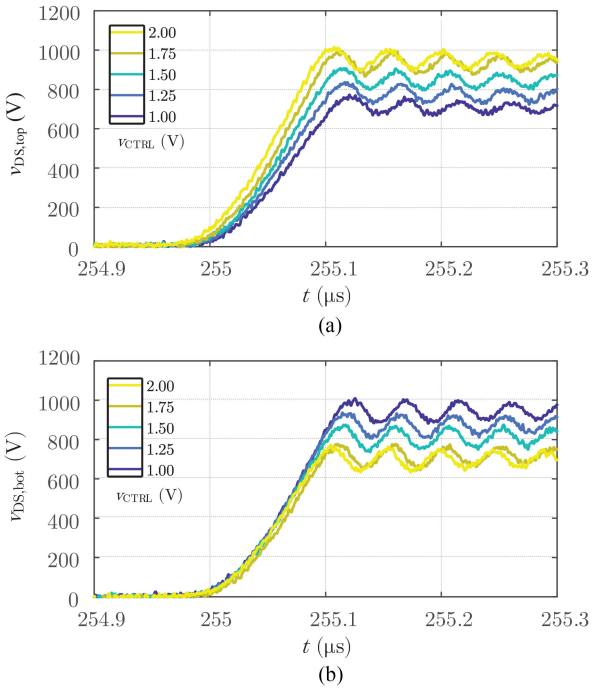

Fig. 11. Turn-OFF transient waveforms of a MOSFET half-bridge with active dv/dt control under 1.5-kV dc-link voltage. (a) Top device turn-OFF waveforms with different v_{CTRL} values. (b) Bottom device turn-OFF waveforms without active dv/dt control.

power supplies, PWM gate signal receiving optic connector, VFC reference voltage signal receiving optic connector, and the FVC circuit. The bottom board includes the main gate-driving circuitry, including gate driver IC, gate resistors, and the active control circuit. The VCCS, the external capacitor C_M, the v_{DS} sensing circuit, and the isolated error integrator are all labeled in Fig. 10.

VI. Experimental Verification

A. Open-Loop Test Results

In order to verify the analysis derived in Section III, two devices in series connection under 1.5-kV dc-link voltage are tested. Open-loop test results of two devices v_{DS} during the turn-OFF transient are presented in Fig. 11. The dv/dt control is only enabled for the top switch. The result illustrates that

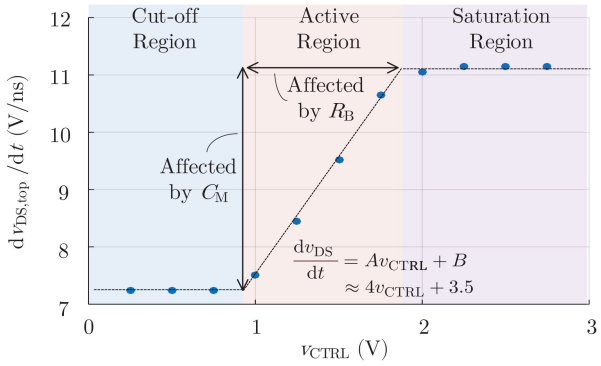

Fig. 12. Correlation between v_{CTRL} and dv/dt for different operation regions. ($A = 4.0$, $B = 3.5$, and $V_{bus} = 1500$ V.)

the top device dv/dt increases with v_{CTRL}, while the bottom device dv/dt remains the same, which proves the active dv/dt controllability of the proposed circuit.

Furthermore, the value of the top device turn-OFF speed is summarized in Fig. 12 as a function of the control voltage v_{CTRL}. Each blue dot is an experimental test result, while the dashed line is the curve fitting of all the dots. Three different operation regions are also defined for the active dv/dt control. The first region is the cutoff region. When $v_{CTRL} < v_{BE,on}$, transistor Q_1 is always OFF, all the induced current flows into the gate and the MOSFET has the lowest dv/dt. The second region is the linear active region, where the controlled device dv/dt will increase with v_{CTRL} linearly, which validates the correlation described by (15). The third region is the saturation region, where Q_1 is fully turned ON and no more current can be drawn even with higher v_{CTRL}. In this region, the MOSFET is operating as if there is no active control to slow it down.

There are mainly three important components in the VCCS circuit, including the externally added capacitor C_M, the base current limiting resistor R_B, and BJTs. The effect of different C_M and R_B parameters is presented in Fig. 13 with test results. Fig. 13(a) illustrates that higher C_M value means wider tunable range of the controlled dv/dt because higher C_M will generate larger current injecting into the gate of MOSFET during turn-OFF transient, which will slow it down more. Since this capacitor has high voltage across it, to have a consistent and accurate control, NP0/C0G-type high voltage capacitor is required. Different from C_M, R_B cannot change the tunable range of the MOSFET dv/dt. However, it can help to tune the sensitivity of the control loop. When R_B is small, the system will be more sensitive to v_{CTRL} (i.e., A is larger) so that as long as the v_{CTRL} is a little bit larger than $V_{BE,on}$, the dv/dt will change a lot and the VCCS will enter saturation region with relative low v_{CTRL} value, i.e., the width of the active region in Fig. 12 is narrower. For BJT, the maximum current flowing through it will be equal to $C_M \cdot dv/dt$. However, this current only exists during the switching transient of the power MOSFET. As for the voltage rating, since there is always at least one BJT conducting, as presented in Fig. 1, during the switching transient, and C_M will hold the voltage during the steady state, there is no special requirement for the breakdown voltage of the BJT. In this work, BJT with

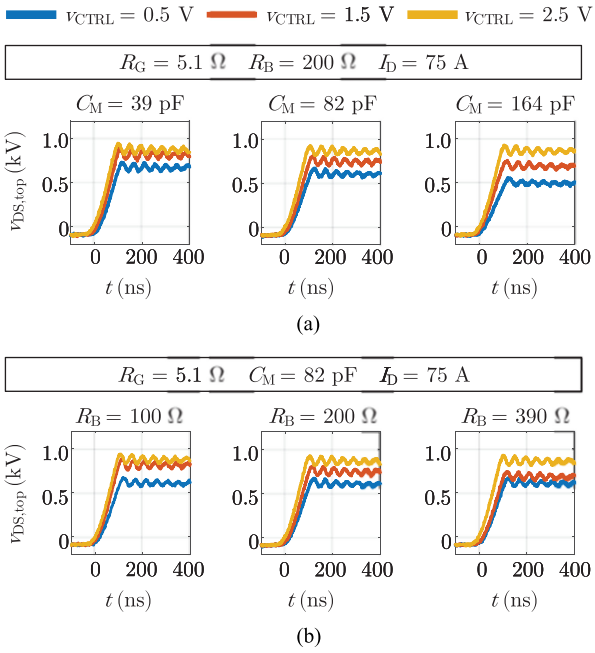

Fig. 13. (a) and (b) Effect of different circuit parameters on active dv/dt control.

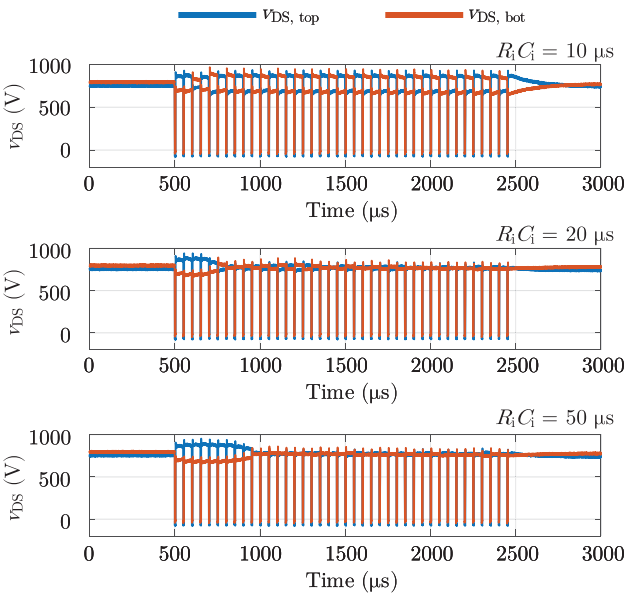

Fig. 14. Closed-loop test result of balancing two devices in series under 1.5-kV dc link with different R_iC_i values. ($A = 4\,\text{ns}^{-1}$, $D = 0.1$, $k_{bot} = 9.5$ V/ns, $V_{bus} = 1500$ V, $T_s = 50\,\mu$s, and $k_d = 250$.)

40-V breakdown voltage is selected. The last parameter, current gain β, should be selected considering the required system gain and the selection of C_M and R_B, as shown in (15) and (16).

B. Closed-Loop Test Results With Feedback Control

In order to verify the derivation in Section IV, tests using same parameters with the simulation (cf., Fig. 5) are conducted. Fig. 14 presents balancing waveforms of two devices in series connection. From the real test result, the derivations of (30) and (32) are verified again. When $R_iC_i = 10\,\mu$s, the control is not stable causing the top and bottom devices voltage diverging and ringing. When $R_iC_i = 20\,\mu$s, the system control is converging and the voltages are balanced. When $R_iC_i = 50\,\mu$s, the MOSFET voltage is converging monotonically, but the converging speed is lower compared to the oscillatory converging condition.

A brief parameter design procedure for stacked MOSFET active dv/dt control can be summarized here. First, the operation condition and device under control should be selected. With this step, bus voltage v_{bus}, switching current i_D, switching period T_s, and parameters related to device such as C_{GD}, V_{th}, etc., are fixed. The second step is the design of the open-loop parameters, i.e., parameters of the VCCS. The open-loop gain should be tuned by changing the value of R_B and C_M, which can be calculated by (15) with trend presented in Figs. 12 and 13. The third step is to design the value of closed-loop parameters R_iC_i for a stable control, whose design guideline is given in (30) and (32).

C. Multiple Devices in Series Connection

To prove the scalability and potential for medium-voltage high-current applications of the proposed method, hardware experimental tests are done with multiple devices in series with higher dc-link voltage and switching current.

Fig. 15 displays the balancing waveforms of four devices in series under 2-kV dc-link voltage and 42-A switching current. The result illustrates an accurate balancing for four devices in series with only 4% voltage difference. Fig. 16 displays the balancing waveforms of eight devices in series under 6-kV dc-link voltage and 125-A switching current. For this medium-voltage high-current condition, the balancing quality is not as perfect as previous tests due to several reasons. First, with more devices in series, much larger loop inductance exists in the system, which will cause higher turn-OFF ringing of devices. At the same time, the switching current is increased from 42 to 125 A, which also intensifies this trend. The proposed method is to make sure that all the devices have the same dv/dt during the turn-OFF transient, but the turn-OFF ringing amplitude and frequency are affected by the commutation loop parasitics, which cannot be compensated by the active dv/dt control. As shown in the zoomed-in turn-OFF switching transient in Figs. 15 and 16, although the dv/dt is always accurately controlled, there is some mismatch during the ringing procedure especially for the eight-device condition. To alleviate the ringing, commutation loop inductance can be reduced by improving the busbar design, minimizing connector inductance between modules, etc. The second reason is the tolerance introduced by voltage sensing. With higher bus voltage and more devices under control, accurately sampling and controlling the devices voltage becomes more challenging due to higher sensitivity of the system. For example, in the test of four-device condition, the v_{DS} of 500 V will be transferred to 2 V v_{sense} in the control circuit, for the test of eight-device condition, the v_{DS} of 750 V will be transferred to 2 V, so the resolution of the sensing network is reduced by

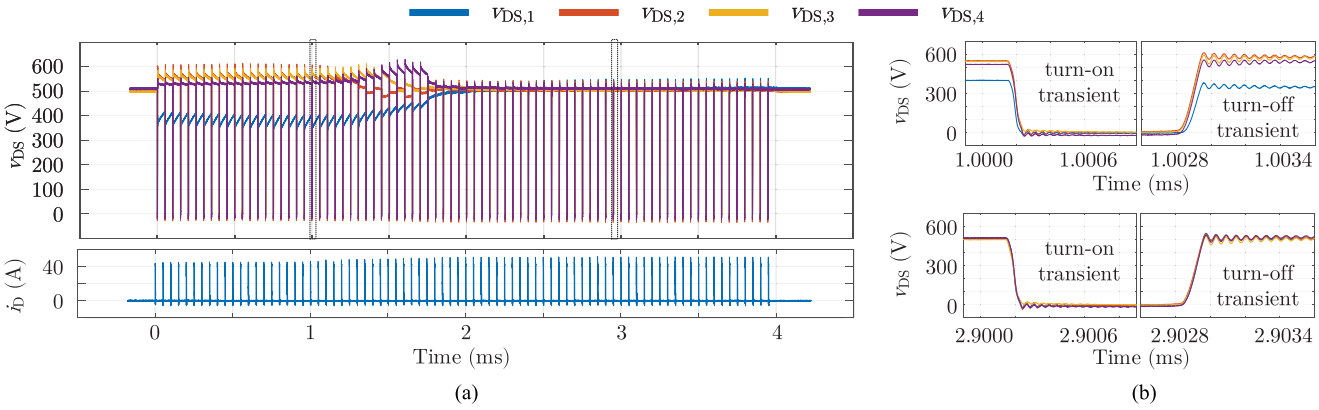

Fig. 15. (a) Closed-loop test result of balancing four devices in series under 2-kV dc link. (b) Device turn-ON and turn-OFF transient waveforms before and after the voltages are balanced. ($V_{\rm bus} = 2000$ V, $k_d = 250$, $T_{\rm s} = 50\,\mu$s, $D = 0.05$, $I_{\rm D} = 42$ A, $R_{\rm load} = 5\,\Omega$, and $R_{\rm i}C_{\rm i} = 150\,\mu$s.)

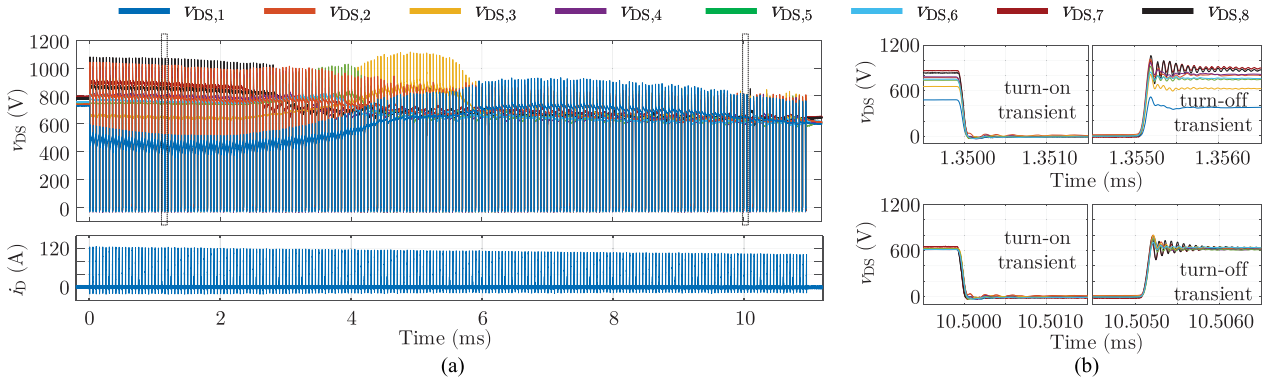

Fig. 16. (a) Closed-loop test result of balancing four devices in series under 6-kV dc link. (b) Device turn-ON and turn-OFF transient waveforms before and after the voltages are balanced. ($V_{\rm bus} = 6000$ V, $k_d = 400$, $T_{\rm s} = 50\,\mu$s, $D = 0.1$, $I_{\rm D} = 125$ A, $R_{\rm load} = 18\,\Omega$, $R_{\rm i}C_{\rm i} = 500\,\mu$s.)

1/3. Meanwhile, since all the switches are affecting each other, with more devices in series connection, the system is also more sensitive.

Concerning thermal drift, first, all the control-gain-related components, such as $C_{\rm M}$ and $R_{\rm B}$, should be chosen with low temperature coefficient. Second, for the BJT, the common-base current gain β will increase with higher junction temperature. For a typical BJT, the β value will increase by 20% if the junction temperature is increased from 25 to 75 °C, considering the low rms current flowing through the BJT (current only conducted during the switching transient), the thermal drift will not be high, and thus, the effect of BJT temperature to the system gain will be limited even lower than the range of 20%. Taken the thermal drift into account, the design of the closed-loop parameters $R_{\rm i}$ and $C_{\rm i}$ should have some margin to make sure that the system is always stable. Also, for the printed circuit board layout, the active $\mathrm{d}v/\mathrm{d}t$ circuit should stay away from heat generating components such as gate resistor $R_{\rm G}$, etc. To improve the performance, the accuracy and resolution of the sensing circuit should be further improved, e.g., selecting components with very low tolerance and thermal drift. Also, the system control sensitivity can be reduced by increasing $R_{\rm B}$. Admittedly, there are still some aspects not covered by this work such as balancing for ac operation conditions, as shown in [44], or diode voltage balancing; however, this research proves that the active $\mathrm{d}v/\mathrm{d}t$ control technique for series-connected SiC MOSFETs has potential to be a competitive alternative in medium-voltage high-current applications.

VII. Conclusion

This article presented the modeling, design, and evaluation of the active $\mathrm{d}v/\mathrm{d}t$ balancing for series-connected SiC MOSFETs. The working principles of the VCCS, analytical model of open-loop control, and feedback control stability were all analyzed. A 6-kV half-bridge prototype with eight SiC MOSFETs in series connection was built. Experimental results have verified the theoretical analysis and proved the proposed method's scalability and potential for medium-voltage high-current applications.

Appendix

Theorem 1: For first-order nonlinear difference equations, considering the scalar equation

$$x_{\rm n+1} = f(x_n), \qquad f(x) \in C^1 \tag{33}$$

we say $\bar{x}$ is a steady-state solution of (33) if $\bar{x} = f(\bar{x})$. The steady-state solution $\bar{x}$ of (33) is asymptotically stable if $|\mathrm{d}f(\overline{x})/\mathrm{d}x| < 1$ [43], [45].

Proof: Since $f(x) \in C^1$ and $|\mathrm{d}f(\overline{x})/\mathrm{d}x| < 1$, there is a $\varepsilon_1 > 0$ such that $|x_0 - \overline{x}| \leq \varepsilon_1$ ensures that $|\mathrm{d}f(\overline{x}_0)/\mathrm{d}x| < 1$. Then, we have

$$\lambda \equiv \max\{|df(x_0)/dx| : |x_0 - \overline{x}| \leq \varepsilon_1\} < 1. \tag{34}$$

Given $\varepsilon > 0$, let $\delta = \min\{\varepsilon/2, \varepsilon_1/2\}$. By the mean value theorem, we have

$$f(x_0) = f(\overline{x}) + f'(\xi)(x_0 - \overline{x}) \tag{35}$$

for some ξ in between x_0 and $\bar{x}$. Since $\bar{x} = f(\bar{x})$

$$|x_1 - \overline{x}| = |f(x_0) - \overline{x}| = |f'(\xi)(x_0 - \overline{x})| \leq \lambda\,|x_0 - \overline{x}| < \delta. \tag{36}$$

Continuing in this way, we have

$$|x_n - \overline{x}| \leq \lambda^n\,|x_0 - \overline{x}| < \delta. \tag{37}$$

Therefore, we have

$$\lim_{n\to\infty} x_n = \overline{x}. \tag{38}$$

■

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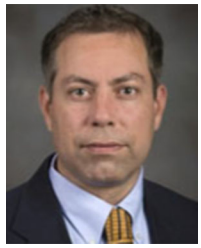

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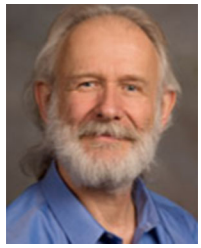

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