Low Complexity Finite-Control-Set MPC Based on Discrete Space Vector Modulation for T-Type Three-Phase Three-Level Converters

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***Abstract*—In this article, a low complexity finite-control-set model predictive control (FCS-MPC) based on the discrete space vector modulation (DSVM) is proposed for T-type three-phase three-level (3P-3L) converters. Different from the conventional FCS-MPC, 48 virtual voltage vectors (VVs) of the converter are constructed by real VVs based on the DSVM. Thus, the performance of 3P-3L converters is significantly improved and the peak amplitude of high-order harmonics concentrates at the sampling frequency. Furthermore, two-stage FCS-MPC based on virtual VVs is proposed to reduce the computation burden. Its first stage selects one of six virtual VVs that minimizes the current tracking error. Then, these candidate VVs located in the same sector as the optimal virtual VV selected in the first stage are evaluated in the second-stage optimization. Thus, the computational efficiency has been greatly improved. To verify the validity of the proposed control method and show its superiority over the conventional FCS-MPC, experimental results are presented.**

***Index Terms*—Discrete space vector modulation (DSVM), model predictive control, multilevel converters, virtual voltage vector (VV).**

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I. Introduction

THREE-PHASE three-level (3P-3L) converters have many advantages compared to three-phase two-level (3P-2L) converters, such as lower output voltage/current harmonics, alleviated power device voltage stress, decreased electromagnetic interference, and higher efficiency. Therefore, the 3P-3L converter has been widely used for industry applications such as renewable generation systems and motor drives [1]–[5]. Compared with the conventional diode neutral point clamped (NPC) 3P-3L converter, the T-type 3P-3L converter has fewer power electronic devices, lower cost, and better efficiency with the switching frequency ranging from 4 to 30 kHz [6]. Thus, the T-type 3P-3L converter is studied in this article.

One of the key challenges for 3P-3L converter regulation is the control design. The commonly employed controllers include proportional-integral (PI) control, proportional-resonant (PR) control, and deadbeat control [7]–[10]. However, the PI controller suffers from the difficulty of balancing steady-state and transient performance, and the PR controller has degraded performance when the frequency of output current changes. As for the deadbeat control, it is heavily dependent on system parameters. Poor control performance can be experienced when system parameter varies.

Finite-control-set model predictive control (FCS-MPC) is a widely used real-time optimal control approach that is capable of handling multiple control objectives and constraints [11]–[16]. Therefore, it is highly recommended for power electronic applications. The conventional FCS-MPC iteratively evaluates all the possible voltage vectors (VVs) in the cost function to determine the optimal VV. This mechanism works well for 3P-2L converter. Nevertheless, for three-phase multilevel converters, it will result in very high computational burden due to the availability of too many VVs.

In recent years, a considerable amount of research works have been carried out to enhance the computational efficiency of FCS-MPC for multilevel converters [17], [18]. For instance, in [17], a hexagon candidate region FCS-MPC and a triangle candidate region FCS-MPC have been proposed to reduce the number of candidate VVs. Similarly, by following the same logic, only some of the VVs are selected for evaluation in FCS-MPC for induction motor drives based on the angular

position and amplitude of stator flux linkage [18]. However, these two efficient FCS-MPC approaches require the fine tuning of weighting factor associated with the NP voltage balancing in the cost function, which complicates the control design because there are no theoretical guidelines on the tuning of weighting factors in FCS-MPC.

In order to eliminate the weight factors and simultaneously improve the computational efficiency, some enhanced FCS-MPC algorithms for 3P-3L converters are proposed [19]–[21]. In [19], a novel FCS-MPC based on "S" factor is proposed. It effectively controls the output current with balanced NP voltage and eliminated weight factors. In [20], the number of candidate VVs to be evaluated in FCS-MPC is effectively reduced by only selecting the VVs adjacent to the reference VV. Then, its NP voltage is balanced by selecting proper redundant small VVs, which eliminates weighting factors. For the 3P-3L converter fed induction motor drives, a computationally efficient FCS-MPC without weighing factors is presented in [21]. However, all the aforementioned FCS-MPC algorithms for 3P-3L converters apply only one VV in one entire control cycle, which leads to high current ripples. In addition, it also generates variable switching frequency, increasing the difficulty of filter design.

To enhance the overall converter performance with fixed switching frequency, various MPC algorithms have been presented. In [22], for 3P-2L converters, a duty cycle MPC is proposed to minimize the current tracking error. It applies multiple VVs in each control cycle with fixed switching frequency. Similarly, model predictive power control with multiple VV action has been proposed for 3P-2L converters in [23] and four-switch rectifiers in [24], which achieves good steady-state and dynamic performance. Recently, modulated MPC that makes use of the numerical values of cost functions has been proposed for power converters [25]–[27]. However, these MPC approaches are computationally complicated, especially when applied to multilevel converters.

To improve the converter performance while reducing the computational burden, FCS-MPC methods based on discrete space vector modulation (DSVM) are investigated [28]–[34]. The essence of these FCS-MPC approaches is to integrate FCS-MPC with DSVM technique. Unfortunately, these FCS-MPC approaches cannot be directly applied to multilevel converters such as three-level converters. In fact, to obtain superior performance, virtual VVs need to be employed in the FCS-MPC for three-level converters. In [35], an improved FCS-MPC based on DSVM for 3P-3L converter has been presented, which achieves the reduction in the output current ripples. However, the balancing of NP voltage is not taken into consideration. Similarly, an enhanced FCS-MPC based on DSVM is proposed in [36], which simultaneously achieves a lower output current total harmonic distortion (THD) and a balanced NP voltage. However, it only explores six virtual VVs, producing limited overall performance improvement compared to the conventional FCS-MPC. To simultaneously achieve fixed switching frequency performance and reducing computational burden for multilevel converters, two-stage optimization MPC algorithms for the three-level converter-fed PMSM in [37] and the 5L-ANPC converter-fed PMSM in [38] have been proposed, which achieve good steady-stage and dynamic performance.

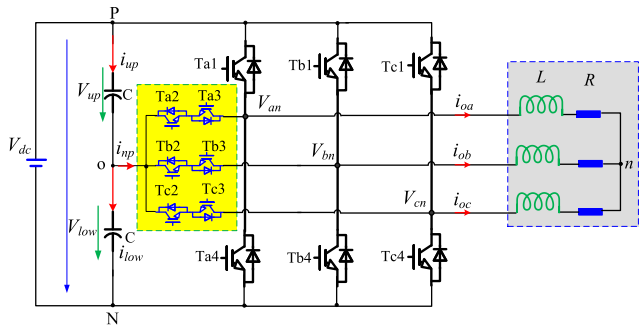

Fig. 1. Topology of the T-type three-phase three-level converter.

To address the drawbacks of the aforementioned MPC algorithms, a low complexity FCS-MPC based on DSVM is proposed in the article. The main novelty and contributions of the article are listed as follows.

1) To further improve the performance of 3P-3L converters, 48 virtual VVs of the converter are constructed by real VVs based on the DSVM. Thus, the performance of 3P-3L converters can be significantly improved and the peak amplitude of high-order harmonics will concentrate at the sampling frequency. Therefore, the proposed FCS-MPC is desirable from the perspective of *LC* filter design for dc/ac converters.
2) Two-stage FCS-MPC based on virtual VVs is proposed to reduce the computation burden. Its first stage selects one of six virtual VVs that minimizes the current tracking error. Then, these candidate VVs located in the same sector as the optimal virtual VV selected in the first stage are evaluated in the second-stage optimization. Then, one of the VVs with the minimum cost function value is selected as the best VV.
3) Balancing dc-link upper and lower capacitor voltages is achieved by utilizing small VVs and virtual VVs.
4) Comprehensive experimental results are presented to show the superior performance of the proposed FCS-MPC algorithm over the conventional FCS-MPC for T-type 3P-3L converter.

II. System Modeling and Conventional FCS-MPC

The topology of T-type 3P-3L converter is depicted in Fig. 1. $V_{\rm dc}$ represents the input voltage of the converter, $V_{\rm up}$ and $V_{\rm low}$ represent the dc-link upper and lower capacitor voltages, respectively, $i_{\rm up}$ and $i_{\rm low}$ denote capacitor currents across the upper and lower capacitors, respectively, $\rm i_{np}$ is the neutral point (NP) current, L means the load inductance, and R is the load resistance.

As shown in Fig. 1, the dynamic output currents of the converter in the stationary *abc* reference frame are obtained as

$$\begin{cases} V_{an} = V_{ao} + V_{\rm on} = L di_{oa}/dt + R i_{oa} \\ V_{bn} = V_{bo} + V_{\rm on} = L di_{ob}/dt + R i_{ob} \\ V_{cn} = V_{co} + V_{\rm on} = L di_{oc}/dt + R i_{oc} \end{cases} \tag{1}$$

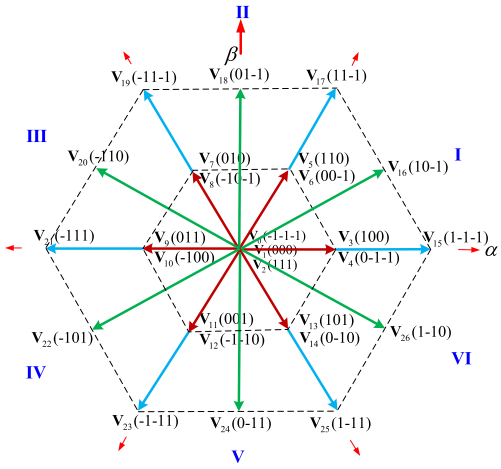

Fig. 2. Twenty-seven voltage vectors of 3P-3L converters.

where $V_{xn}(x=a,b,c)$ indicates the phase-x output voltage, $i_{ox}(x=a,b,c)$ means the phase-x output current.

By transforming (1) from the stationary abc reference frame to the stationary $\alpha\beta$ reference frame, we have

$$\begin{cases} V_\alpha = Ldi_{o\alpha}/dt + Ri_{o\alpha} \\ V_\beta = Ldi_{o\beta}/dt + Ri_{o\beta} \end{cases} \tag{2}$$

where V_α and V_β stand for the α-axis and the β-axis components of the converter output voltage, respectively. $i_{o\alpha}$ and $i_{o\beta}$ represent the α-axis and the β-axis components of the converter output current, respectively.

Suppose the NP voltage is well controlled at half of the dc-link voltage. Each leg generates three different output voltages that are denoted as $V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$ with respect to the NP. Thus, the converter generates 27 switching states, which are displayed in Fig. 2. In Fig. 2, "1," "0," and "-1" represents the converter output voltage $V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$, respectively.

Define the switching function T_i as

$$T_i = \begin{cases} 1 & T_{i1} \text{ and } T_{i2} \text{ on, } T_{i3} \text{ and } T_{i4} \text{ off} \\ 0 & T_{i2} \text{ and } T_{i3} \text{ on, } T_{i1} \text{ and } T_{i4} \text{ off} \\ -1 & T_{i3} \text{ and } T_{i4} \text{ on, } T_{i1} \text{ and } T_{i2} \text{ off} \end{cases} \quad (i=a,b,c)\ . \tag{3}$$

Then, the converter output voltages are expressed as

$$\begin{cases} V_\alpha = V_{\rm dc}(2T_a - T_b - T_c)/3 \\ V_\beta = \sqrt{3}V_{\rm dc}(T_b - T_c)/3\ . \end{cases} \tag{4}$$

By using forward Euler approximation, the predicted output currents at the $(k+1)$th sampling instant are derived as

$$\begin{cases} i_{o\alpha}(k+1) = i_{o\alpha}(k) + \frac{T_s}{L}(V_\alpha(k) - Ri_{o\alpha}(k)) \\ i_{o\beta}(k+1) = i_{o\beta}(k) + \frac{T_s}{L}(V_\beta(k) - Ri_{o\beta}(k)) \end{cases} \tag{5}$$

where T_s is the sampling period.

As depicted in Fig. 1, the currents flowing through dc-link capacitors are obtained as

$$\begin{cases} i_{\rm up} = C\frac{dV_{\rm up}}{dt} \\ i_{\rm low} = C\frac{dV_{\rm low}}{dt}. \end{cases} \tag{6}$$

By using forward Euler approximation, the dc-link upper and lower capacitor voltages are predicted as

$$\begin{cases} V_{\rm up}(k+1) = V_{\rm up}(k) + \frac{T_S}{C}i_{\rm up}(k) \\ V_{\rm low}(k+1) = V_{\rm low}(k) + \frac{T_S}{C}i_{\rm low}(k). \end{cases} \tag{7}$$

Subsequently, the currents flowing through the upper and lower capacitors can be expressed as

$$\begin{cases} i_{\rm up} = i_{\rm dc} - (T_a + {T_a}^2)/2 - (T_b + {T_b}^2)/2 - (T_c + {T_c}^2)/2 \\ i_{\rm low} = i_{\rm dc} + (T_a + {T_a}^2)/2 + (T_b + {T_b}^2)/2 + (T_c + {T_c}^2)/2 \end{cases} \tag{8}$$

where $i_{\rm dc}$ is the converter dc-link input current.

Substituting (8) into (7), the predicted dc-link upper and lower capacitor voltages are derived as

$$\begin{cases} V_{\rm up}(k+1) = V_{\rm up}(k) + \frac{T_S}{C}(i_{\rm dc} - \sum\limits_{x=a,b,c}(T_x + {T_x}^2)/2) \\ V_{\rm low}(k+1) = V_{\rm low}(k) + \frac{T_S}{C}(i_{\rm dc} + \sum\limits_{x=a,b,c}(T_x + {T_x}^2)/2). \end{cases} \tag{9}$$

According to (9), the predicted voltage difference $\Delta V_{\rm dc}(k+1)$ are written as

$$\begin{aligned} \Delta V_{\rm dc}(k+1) &= V_{\rm up}(k+1) - V_{\rm low}(k+1) \\ &= V_{\rm up}(k) - V_{\rm low}(k) - \frac{T_S}{4C}\sum_{x=a,b,c}(T_x + {T_x}^2). \end{aligned} \tag{10}$$

To track current references and simultaneously balance dc-link capacitor voltages, the cost function of the conventional FCS-MPC method is defined as

$$\begin{cases} G(j) = |i^*_{o\alpha}(k+1) - i_{o\alpha}(k+1)| + \left|i^*_{o\beta}(k+1) - i_{o\beta}(k+1)\right| \\ \quad +\lambda_{\rm np}\left|\Delta V_{\rm dc}(k+1)\right| \\ V_{\rm opt} = \arg\min\limits_{j=0,1,\ldots,26}(G(j)) \end{cases} \tag{11}$$

where $\lambda_{\rm np}$ is the weighing factor. ${i^*}_{o\alpha}(k+1)$ and ${i^*}_{o\beta}(k+1)$ represent the converter output current references at the $(k+1)$th instant, and they are calculated by the third-order Lagrange extrapolation as

$$\begin{cases} i^*_{o\alpha}(k+1) = 4i^*_{o\alpha}(k) - 6i^*_{o\alpha}(k-1) + 4i^*_{o\alpha}(k-2) \\ \qquad\qquad -i^*_{o\alpha}(k-3) \\ i^*_{o\beta}(k+1) = 4i^*_{o\beta}(k) - 6i^*_{o\beta}(k-1) + 4i^*_{o\beta}(k-2) \\ \qquad\qquad -i^*_{o\beta}(k-3). \end{cases} \tag{12}$$

The cost function (11) is used to determine the optimal VV.

III. FCS-MPC Based on DSVM

A. FCS-MPC Without Weighting Factors

For the conventional FCS-MPC, there is only one VV applied in the entire sampling period, which results in high current harmonics and variable switching frequency. To greatly diminish the current harmonics while maintaining a constant switching frequency, DSVM is adopted. If the sampling period is equally divided into N intervals, the virtual VV $\mathbf{V}_{\rm vir}$ can be synthesized by the real VVs $\mathbf{V}_i^{\rm real}$ and is expressed as

$$\mathbf{V}_{\rm vir} = \sum_{i=1}^{N} t_i \mathbf{V}_i^{\rm real} \tag{13}$$

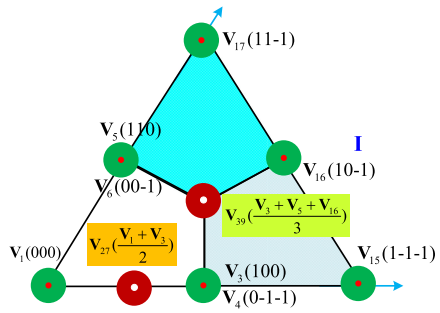

Fig. 3. Virtual voltage vectors $\mathbf{V}_{27}$ and $\mathbf{V}_{39}$.

TABLE I
VIRTUAL VVS OF 3P-3L CONVERTERS

Virtual VVs	Synthesized by real VVs	Virtual VVs	Synthesized by real VVs
$\mathbf{V}_{27}$	$(\mathbf{V}_1+\mathbf{V}_3)/2$	$\mathbf{V}_{28}$	$(\mathbf{V}_1+\mathbf{V}_4)/2$
$\mathbf{V}_{29}$	$(\mathbf{V}_1+\mathbf{V}_5)/2$	$\mathbf{V}_{30}$	$(\mathbf{V}_1+\mathbf{V}_6)/2$
$\mathbf{V}_{31}$	$(\mathbf{V}_1+\mathbf{V}_7)/2$	$\mathbf{V}_{32}$	$(\mathbf{V}_1+\mathbf{V}_8)/2$
$\mathbf{V}_{33}$	$(\mathbf{V}_1+\mathbf{V}_9)/2$	$\mathbf{V}_{34}$	$(\mathbf{V}_1+\mathbf{V}_{10})/2$
$\mathbf{V}_{35}$	$(\mathbf{V}_1+\mathbf{V}_{11})/2$	$\mathbf{V}_{36}$	$(\mathbf{V}_1+\mathbf{V}_{12})/2$
$\mathbf{V}_{37}$	$(\mathbf{V}_1+\mathbf{V}_{13})/2$	$\mathbf{V}_{38}$	$(\mathbf{V}_1+\mathbf{V}_{14})/2$
$\mathbf{V}_{39}$	$(\mathbf{V}_3+\mathbf{V}_5+\mathbf{V}_{16})/3$	$\mathbf{V}_{40}$	$(\mathbf{V}_4+\mathbf{V}_6+\mathbf{V}_{16})/3$
$\mathbf{V}_{41}$	$(\mathbf{V}_5+\mathbf{V}_7+\mathbf{V}_{18})/3$	$\mathbf{V}_{42}$	$(\mathbf{V}_6+\mathbf{V}_8+\mathbf{V}_{18})/3$
$\mathbf{V}_{43}$	$(\mathbf{V}_7+\mathbf{V}_9+\mathbf{V}_{20})/3$	$\mathbf{V}_{44}$	$(\mathbf{V}_8+\mathbf{V}_{10}+\mathbf{V}_{20})/3$
$\mathbf{V}_{45}$	$(\mathbf{V}_9+\mathbf{V}_{11}+\mathbf{V}_{22})/3$	$\mathbf{V}_{46}$	$(\mathbf{V}_{10}+\mathbf{V}_{12}+\mathbf{V}_{22})/3$
$\mathbf{V}_{47}$	$(\mathbf{V}_{11}+\mathbf{V}_{13}+\mathbf{V}_{24})/3$	$\mathbf{V}_{48}$	$(\mathbf{V}_{11}+\mathbf{V}_{13}+\mathbf{V}_{24})/3$
$\mathbf{V}_{49}$	$(\mathbf{V}_3+\mathbf{V}_{13}+\mathbf{V}_{26})/3$	$\mathbf{V}_{50}$	$(\mathbf{V}_4+\mathbf{V}_{14}+\mathbf{V}_{26})/3$
$\mathbf{V}_{51}$	$(\mathbf{V}_3+\mathbf{V}_{15})/2$	$\mathbf{V}_{52}$	$(\mathbf{V}_4+\mathbf{V}_{15})/2$
$\mathbf{V}_{53}$	$(\mathbf{V}_5+\mathbf{V}_{17})/2$	$\mathbf{V}_{54}$	$(\mathbf{V}_6+\mathbf{V}_{17})/2$
$\mathbf{V}_{55}$	$(\mathbf{V}_7+\mathbf{V}_{19})/2$	$\mathbf{V}_{56}$	$(\mathbf{V}_9+\mathbf{V}_{19})/2$
$\mathbf{V}_{57}$	$(\mathbf{V}_9+\mathbf{V}_{21})/2$	$\mathbf{V}_{58}$	$(\mathbf{V}_{10}+\mathbf{V}_{21})/2$
$\mathbf{V}_{59}$	$(\mathbf{V}_{11}+\mathbf{V}_{23})/2$	$\mathbf{V}_{60}$	$(\mathbf{V}_{12}+\mathbf{V}_{23})/2$
$\mathbf{V}_{61}$	$(\mathbf{V}_{13}+\mathbf{V}_{25})/2$	$\mathbf{V}_{62}$	$(\mathbf{V}_{14}+\mathbf{V}_{25})/2$
$\mathbf{V}_{63}$	$(\mathbf{V}_{15}+\mathbf{V}_{16})/2$	$\mathbf{V}_{64}$	$(\mathbf{V}_{16}+\mathbf{V}_{17})/2$
$\mathbf{V}_{65}$	$(\mathbf{V}_{17}+\mathbf{V}_{18})/2$	$\mathbf{V}_{66}$	$(\mathbf{V}_{18}+\mathbf{V}_{19})/2$
$\mathbf{V}_{67}$	$(\mathbf{V}_{19}+\mathbf{V}_{20})/2$	$\mathbf{V}_{68}$	$(\mathbf{V}_{20}+\mathbf{V}_{21})/2$
$\mathbf{V}_{69}$	$(\mathbf{V}_{21}+\mathbf{V}_{22})/2$	$\mathbf{V}_{70}$	$(\mathbf{V}_{22}+\mathbf{V}_{23})/2$
$\mathbf{V}_{71}$	$(\mathbf{V}_{23}+\mathbf{V}_{24})/2$	$\mathbf{V}_{72}$	$(\mathbf{V}_{24}+\mathbf{V}_{25})/2$
$\mathbf{V}_{73}$	$(\mathbf{V}_{25}+\mathbf{V}_{26})/2$	$\mathbf{V}_{74}$	$(\mathbf{V}_{26}+\mathbf{V}_{15})/2$

$$t_1 + t_2 + \ldots + t_N = T_S \tag{14}$$

$$\mathbf{V}_i^{\text{real}} \in \{\mathbf{V}_0, \mathbf{V}_1, \ldots, \mathbf{V}_{26}\}. \tag{15}$$

For example, when N is set to 2 or 3, the virtual VVs $\mathbf{V}_{27}$ and $\mathbf{V}_{39}$ can be obtained as

$$\begin{cases} \mathbf{V}_{27} = (\mathbf{V}_1 + \mathbf{V}_3)/2 \\ \mathbf{V}_{39} = (\mathbf{V}_3 + \mathbf{V}_5 + \mathbf{V}_{16})/3. \end{cases} \tag{16}$$

Thus, the virtual VVs $\mathbf{V}_{27}$ and $\mathbf{V}_{39}$ are shown in Fig. 3.

Similarly, other virtual VVs can be obtained. All the virtual VVs are listed in Table I, and all the virtual VVs and the real VVs of the 3P-3L converter are depicted in Fig. 4.

As listed in Table I, two or three real VVs are used to synthesize one virtual VV. Duty ratios of different power switches are shown in Fig. 5 when the virtual VVs $\mathbf{V}_{27}$ and $\mathbf{V}_{39}$ are applied to

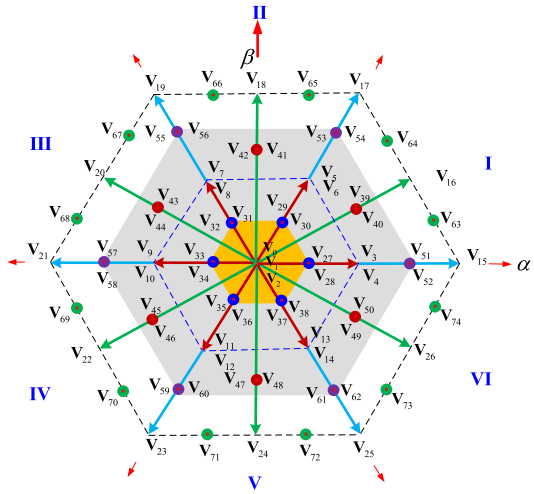

Fig. 4. Real voltage vectors and virtual VVs.

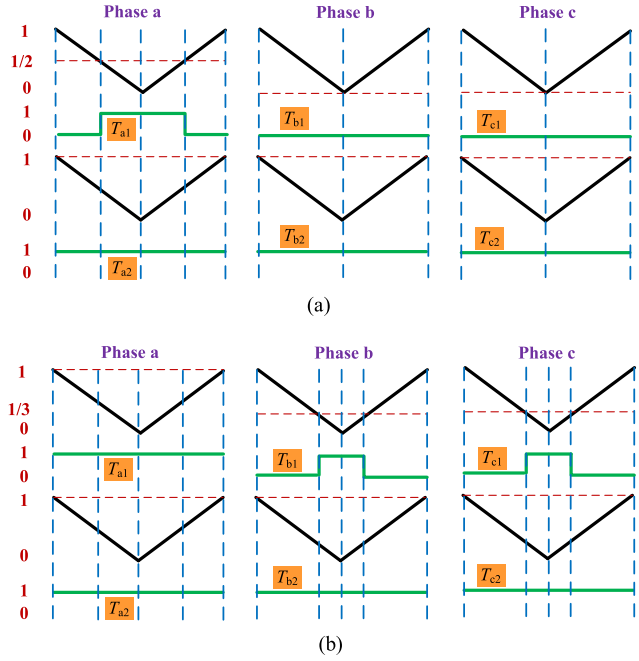

Fig. 5. Duty ratios of virtual VVs $\mathbf{V}_{27}$ and $\mathbf{V}_{39}$. (a) $\mathbf{V}_{27}$. (a) $\mathbf{V}_{39}$.

the 3P-3L converter. Similarly, duty ratios of other virtual VVs can be obtained.

As displayed in Fig. 5, multiple VVs are applied per control cycle, which leads to fixed switching frequency and lower current harmonics compared to the conventional FCS-MPC.

Based on the expressions in (4), (5), (10), (11), and (12), it is noted that 27 iterative calculations and 75 iterative calculations are required for the conventional FCS-MPC and the FCS-MPC based on DSVM, respectively. Hence, it is time consuming to implement these FCS-MPC algorithms using digital signal processors (DSP). Furthermore, as shown in (11), there is a weighting factor, which is tedious for the tuning of this weighting factor. In order to avoid the tuning process, the cost function

TABLE II
CANDIDATE REAL AND VIRTUAL VVS

Optimal virtual VV	Candidate real and virtual VVs
$\mathbf{V}_{39}$	$\mathbf{V}_1$, $\mathbf{V}_3$, $\mathbf{V}_4$, $\mathbf{V}_5$, $\mathbf{V}_6$, $\mathbf{V}_{15}$, $\mathbf{V}_{16}$, $\mathbf{V}_{17}$, $\mathbf{V}_{27}$, $\mathbf{V}_{28}$, $\mathbf{V}_{29}$, $\mathbf{V}_{30}$, $\mathbf{V}_{39}$, $\mathbf{V}_{40}$, $\mathbf{V}_{51}$, $\mathbf{V}_{52}$, $\mathbf{V}_{53}$, $\mathbf{V}_{54}$, $\mathbf{V}_{63}$, $\mathbf{V}_{64}$
$\mathbf{V}_{41}$	$\mathbf{V}_1$, $\mathbf{V}_5$, $\mathbf{V}_6$, $\mathbf{V}_7$, $\mathbf{V}_8$, $\mathbf{V}_{17}$, $\mathbf{V}_{18}$, $\mathbf{V}_{19}$, $\mathbf{V}_{29}$, $\mathbf{V}_{30}$, $\mathbf{V}_{31}$, $\mathbf{V}_{32}$, $\mathbf{V}_{41}$, $\mathbf{V}_{42}$, $\mathbf{V}_{53}$, $\mathbf{V}_{54}$, $\mathbf{V}_{55}$, $\mathbf{V}_{56}$, $\mathbf{V}_{65}$, $\mathbf{V}_{66}$
$\mathbf{V}_{43}$	$\mathbf{V}_1$, $\mathbf{V}_7$, $\mathbf{V}_8$, $\mathbf{V}_9$, $\mathbf{V}_{10}$, $\mathbf{V}_{19}$, $\mathbf{V}_{20}$, $\mathbf{V}_{21}$, $\mathbf{V}_{31}$, $\mathbf{V}_{32}$,$\mathbf{V}_{33}$, $\mathbf{V}_{34}$, $\mathbf{V}_{43}$, $\mathbf{V}_{44}$, $\mathbf{V}_{55}$, $\mathbf{V}_{56}$, $\mathbf{V}_{57}$, $\mathbf{V}_{58}$, $\mathbf{V}_{67}$, $\mathbf{V}_{68}$
$\mathbf{V}_{45}$	$\mathbf{V}_1$, $\mathbf{V}_9$, $\mathbf{V}_{10}$, $\mathbf{V}_{11}$, $\mathbf{V}_{12}$, $\mathbf{V}_{21}$, $\mathbf{V}_{22}$, $\mathbf{V}_{23}$, $\mathbf{V}_{33}$, $\mathbf{V}_{34}$, $\mathbf{V}_{35}$,$\mathbf{V}_{36}$, $\mathbf{V}_{45}$, $\mathbf{V}_{46}$, $\mathbf{V}_{57}$, $\mathbf{V}_{58}$, $\mathbf{V}_{59}$, $\mathbf{V}_{60}$, $\mathbf{V}_{69}$, $\mathbf{V}_{70}$
$\mathbf{V}_{47}$	$\mathbf{V}_1$, $\mathbf{V}_{11}$, $\mathbf{V}_{12}$, $\mathbf{V}_{13}$, $\mathbf{V}_{14}$, $\mathbf{V}_{23}$, $\mathbf{V}_{24}$, $\mathbf{V}_{25}$, $\mathbf{V}_{35}$, $\mathbf{V}_{36}$, $\mathbf{V}_{37}$,$\mathbf{V}_{38}$, $\mathbf{V}_{47}$, $\mathbf{V}_{48}$, $\mathbf{V}_{59}$, $\mathbf{V}_{60}$, $\mathbf{V}_{61}$, $\mathbf{V}_{62}$, $\mathbf{V}_{71}$, $\mathbf{V}_{72}$
$\mathbf{V}_{49}$	$\mathbf{V}_1$, $\mathbf{V}_3$, $\mathbf{V}_4$, $\mathbf{V}_{13}$, $\mathbf{V}_{14}$, $\mathbf{V}_{15}$, $\mathbf{V}_{25}$, $\mathbf{V}_{26}$, $\mathbf{V}_{27}$, $\mathbf{V}_{28}$, $\mathbf{V}_{37}$, $\mathbf{V}_{38}$, $\mathbf{V}_{49}$, $\mathbf{V}_{50}$, $\mathbf{V}_{51}$, $\mathbf{V}_{52}$, $\mathbf{V}_{61}$, $\mathbf{V}_{62}$, $\mathbf{V}_{73}$, $\mathbf{V}_{74}$

without weighting factors is constructed as

$$\begin{cases} G_s(j) = |i^*_{o\alpha}(k+1) - i_{o\alpha}(k+1)| \\ \quad + \left|i^*_{o\beta}(k+1) - i_{o\beta}(k+1)\right| \\ V_{\text{opt}} = \arg\min\limits_{j=0,1,\ldots,74}(G_s(j)). \end{cases} \tag{17}$$

To lessen the execution time implementing FCS-MPC, a two-stage FCS-MPC based on virtual VVs is proposed. The first stage evaluates six virtual VVs ($\mathbf{V}_{39}$, $\mathbf{V}_{41}$, $\mathbf{V}_{43}$, $\mathbf{V}_{45}$, $\mathbf{V}_{47}$, and $\mathbf{V}_{49}$ shown in Fig. 4) to find out the VV with minimum cost function (17). Then, the VVs located in the same sector as the first stage are chosen to take part in the second-stage optimization. For example, when the virtual VV $\mathbf{V}_{39}$ is selected as the optimal VV in the first stage, the candidate VVs in the second stage include $\mathbf{V}_1$, $\mathbf{V}_3$,$\mathbf{V}_4$, $\mathbf{V}_5$, $\mathbf{V}_6$, $\mathbf{V}_{15}$, $\mathbf{V}_{16}$, $\mathbf{V}_{27}$, $\mathbf{V}_{28}$, $\mathbf{V}_{29}$, $\mathbf{V}_{30}$, $\mathbf{V}_{39}$, $\mathbf{V}_{51}$, $\mathbf{V}_{52}$, $\mathbf{V}_{53}$, $\mathbf{V}_{54}$, $\mathbf{V}_{63}$, and $\mathbf{V}_{64}$. Candidate VVs in the other sectors can be obtained in the same way. All candidate VVs in different sectors are listed in Table II.

It can be clearly seen from Table II that the number of candidate VVs for the proposed FCS-MPC is reduced from 75 to 20, which greatly reduces the computational burden.

B. Balancing NP Voltage

The NP voltage balancing is an important issue for the 3P-3L converter. Unbalanced NP voltage will degrade the converter performance. As shown in Fig. 2, there are redundant VVs that generate the same output voltages but with different influences on the NP voltage. Thus, redundant VVs are utilized to balance the NP voltage. In terms of their influence on the NP voltage, the real VVs are divided into positive small VVs and negative small VVs. To select proper virtual VVs for balancing the NP voltage, virtual VVs are analyzed as follows:

Define a virtual VV $\mathbf{V}_{\text{V1}}$ as

$$\mathbf{V}_{\text{V1}} = (\mathbf{V}_4 + \mathbf{V}_5 + \mathbf{V}_{16})/3. \tag{18}$$

When the virtual VV $\mathbf{V}_{\text{V1}}$ is applied in one entire control cycle, the average NP current i_{np} in this control cycle is calculated as

$$i_{\text{np}} = (i_{oa} + i_{ob} + i_{oc})/3 = 0. \tag{19}$$

TABLE III
CANDIDATE VOLTAGE VECTORS SELECTION

Optimal sector	Conditions	Candidate voltage vectors
I	$V_{up} \geq V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_3$, $\mathbf{V}_5$, $\mathbf{V}_{15}$, $\mathbf{V}_{16}$, $\mathbf{V}_{17}$, $\mathbf{V}_{27}$, $\mathbf{V}_{29}$, $\mathbf{V}_{39}$, $\mathbf{V}_{51}$, $\mathbf{V}_{53}$, $\mathbf{V}_{63}$, $\mathbf{V}_{64}$
	$V_{up} < V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_4$, $\mathbf{V}_6$, $\mathbf{V}_{15}$, $\mathbf{V}_{16}$, $\mathbf{V}_{17}$, $\mathbf{V}_{28}$, $\mathbf{V}_{30}$, $\mathbf{V}_{40}$, $\mathbf{V}_{52}$, $\mathbf{V}_{54}$, $\mathbf{V}_{63}$, $\mathbf{V}_{64}$
II	$V_{up} \geq V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_5$, $\mathbf{V}_7$, $\mathbf{V}_{17}$, $\mathbf{V}_{18}$, $\mathbf{V}_{19}$, $\mathbf{V}_{29}$, $\mathbf{V}_{31}$, $\mathbf{V}_{41}$, $\mathbf{V}_{53}$, $\mathbf{V}_{55}$, $\mathbf{V}_{65}$, $\mathbf{V}_{66}$
	$V_{up} < V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_6$, $\mathbf{V}_8$, $\mathbf{V}_{17}$, $\mathbf{V}_{18}$, $\mathbf{V}_{19}$, $\mathbf{V}_{30}$, $\mathbf{V}_{32}$, $\mathbf{V}_{42}$, $\mathbf{V}_{54}$, $\mathbf{V}_{56}$, $\mathbf{V}_{65}$, $\mathbf{V}_{66}$
III	$V_{up} \geq V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_7$, $\mathbf{V}_9$, $\mathbf{V}_{19}$, $\mathbf{V}_{20}$, $\mathbf{V}_{21}$, $\mathbf{V}_{31}$, $\mathbf{V}_{33}$, $\mathbf{V}_{43}$, $\mathbf{V}_{55}$, $\mathbf{V}_{57}$, $\mathbf{V}_{67}$, $\mathbf{V}_{68}$
	$V_{up} < V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_8$, $\mathbf{V}_{10}$, $\mathbf{V}_{19}$, $\mathbf{V}_{20}$, $\mathbf{V}_{21}$, $\mathbf{V}_{32}$, $\mathbf{V}_{34}$, $\mathbf{V}_{44}$, $\mathbf{V}_{56}$, $\mathbf{V}_{58}$, $\mathbf{V}_{67}$, $\mathbf{V}_{68}$
IV	$V_{up} \geq V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_9$, $\mathbf{V}_{11}$, $\mathbf{V}_{21}$, $\mathbf{V}_{22}$, $\mathbf{V}_{23}$, $\mathbf{V}_{33}$, $\mathbf{V}_{35}$, $\mathbf{V}_{45}$, $\mathbf{V}_{57}$, $\mathbf{V}_{59}$, $\mathbf{V}_{69}$, $\mathbf{V}_{70}$
	$V_{up} < V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_{10}$, $\mathbf{V}_{12}$, $\mathbf{V}_{21}$, $\mathbf{V}_{22}$, $\mathbf{V}_{23}$, $\mathbf{V}_{34}$, $\mathbf{V}_{36}$, $\mathbf{V}_{46}$, $\mathbf{V}_{58}$, $\mathbf{V}_{60}$, $\mathbf{V}_{69}$, $\mathbf{V}_{70}$
V	$V_{up} \geq V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_{11}$, $\mathbf{V}_{13}$, $\mathbf{V}_{23}$, $\mathbf{V}_{24}$, $\mathbf{V}_{25}$, $\mathbf{V}_{35}$, $\mathbf{V}_{37}$, $\mathbf{V}_{47}$, $\mathbf{V}_{59}$, $\mathbf{V}_{61}$, $\mathbf{V}_{71}$, $\mathbf{V}_{72}$
	$V_{up} < V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_{12}$, $\mathbf{V}_{14}$, $\mathbf{V}_{23}$, $\mathbf{V}_{24}$, $\mathbf{V}_{25}$, $\mathbf{V}_{36}$, $\mathbf{V}_{38}$, $\mathbf{V}_{48}$, $\mathbf{V}_{60}$, $\mathbf{V}_{62}$, $\mathbf{V}_{71}$, $\mathbf{V}_{72}$
VI	$V_{up} \geq V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_3$, $\mathbf{V}_{13}$, $\mathbf{V}_{15}$, $\mathbf{V}_{25}$, $\mathbf{V}_{26}$, $\mathbf{V}_{27}$, $\mathbf{V}_{37}$, $\mathbf{V}_{49}$, $\mathbf{V}_{51}$, $\mathbf{V}_{61}$, $\mathbf{V}_{73}$, $\mathbf{V}_{74}$
	$V_{up} < V_{low}$	$\mathbf{V}_1$, $\mathbf{V}_4$, $\mathbf{V}_{14}$, $\mathbf{V}_{15}$, $\mathbf{V}_{25}$, $\mathbf{V}_{26}$, $\mathbf{V}_{28}$, $\mathbf{V}_{38}$, $\mathbf{V}_{50}$, $\mathbf{V}_{52}$, $\mathbf{V}_{62}$, $\mathbf{V}_{73}$, $\mathbf{V}_{74}$

From (19), it can be found that the virtual VV $\mathbf{V}_{\text{V1}}$ has no influence on the NP voltage.

The virtual VVs $\mathbf{V}_{39}$ and $\mathbf{V}_{40}$ are defined as

$$\begin{cases} \mathbf{V}_{39} = (\mathbf{V}_3 + \mathbf{V}_5 + \mathbf{V}_{16})/3 \\ \mathbf{V}_{40} = (\mathbf{V}_4 + \mathbf{V}_6 + \mathbf{V}_{16})/3. \end{cases} \tag{20}$$

Subtracting (18) from (20), the following expressions can be obtained:

$$\begin{cases} \mathbf{V}_{39} - \mathbf{V}_{\text{V1}} = (\mathbf{V}_3 - \mathbf{V}_4)/3 = (\mathbf{V}_3 + \mathbf{V}_9)/3 \\ \mathbf{V}_{40} - \mathbf{V}_{\text{V1}} = (\mathbf{V}_6 - \mathbf{V}_5)/3 = (\mathbf{V}_6 + \mathbf{V}_{12})/3. \end{cases} \tag{21}$$

Suppose the 3P-3L converter works with unity power factor, positive/negative small VVs will decrease/increase the upper capacitor voltage and increase/decrease the lower capacitor voltage. As shown in (18) and (21), it can be observed that: 1) tree virtual VVs generate the same output voltage; 2) the virtual VV $\mathbf{V}_{39}$ will decrease the dc-link upper capacitor voltage and increase the dc-link lower capacitor voltage, which is denoted as a positive virtual VV; and 3) virtual VV $\mathbf{V}_{40}$ is capable of increasing the dc-link upper capacitor voltage and decreasing the dc-link lower capacitor voltage, which is denoted as a negative virtual VV. Thus, the balancing of dc-link upper and lower capacitor voltages is achieved by utilizing small VVs and virtual VVs. The candidate real and virtual VVs employed in the proposed FCS-MPC algorithm are listed in Table III.

From Table III, it is found that the number of candidate VVs to be evaluated in FCS-MPC is greatly reduced from 75 to 13 by the proposed method. Furthermore, as shown in (17), weighting factors are eliminated, and the NP voltage is controlled by selecting small and virtual VVs. In terms of above analysis, the control block diagram of FCS-MPC based on DSVM is shown in

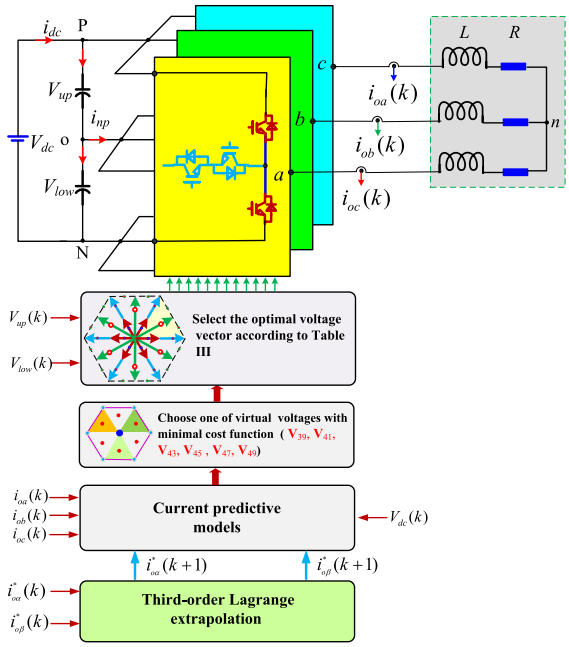

Fig. 6. Control block diagram of FCS-MPC based on DSVM.

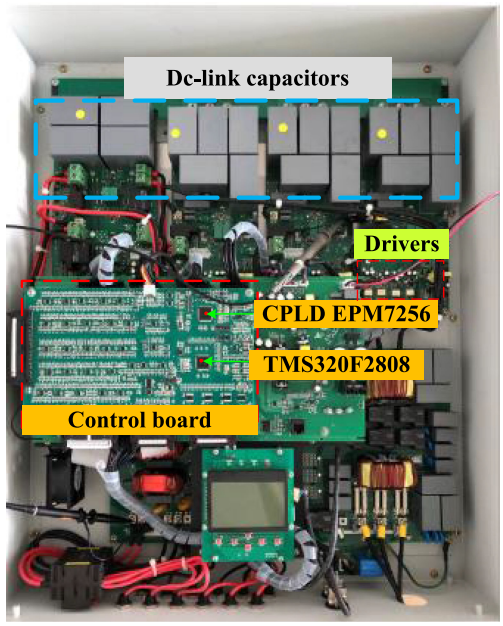

Fig. 7. Experimental platform of the 3P-3L converter.

TABLE IV
EXPERIMENT PARAMETERS

Name	Description	Value
V_{dc}	Dc-link voltage	180 V
C	Dc-link capacitors	500 μF
L	Load inductance	10 mH
R	Load resistance	18 Ω
f_s	Sampling frequency	10 kHz
λ_{np}	Weighing factor	0.015

TABLE V
TEST CONDITIONS

Condition	I^*_o	f^*_o
Test 1	2.5 A	50 Hz
Test 2	5 A	50 Hz
Test 3	Step from 2.5 A to 5 A	50 Hz
Test 4	Step from 5 A to 2.5 A	50 Hz

TABLE VI
EXECUTION TIME

FCS-MPC approaches	A/D and other tasks	FCS-MPC time	Total time
Conventional FCS-MPC	10.4 μs	56.8 μs	67.2μs
Proposed FCS-MPC	10.4 μs	47.2 μs	57.6 μs

Fig. 6. As displayed in Fig. 6, the proposed FCS-MPC algorithm is implemented in two stages. The first stage selects a virtual VV that minimizes cost function (17). Then, some candidate VVs located in the same sector are involved in the second-stage FCS-MPC iterative calculation according to Table III. Finally, duty ratios of the 3P-3L converter are generated using the conventional pulsewidth modulation (PWM) technique.

IV. EXPERIMENT EVALUATIONS

To verify the proposed FCS-MPC based on DSVM, an experimental platform based on DSP (TMS320F2808) and complex programmable logic device (CPLD) (EMP7256) is built. The DSP is utilized to implement FCS-MPC algorithms, and the CPLD is adopted to generate gate pulses for 3P-3L converters. The experimental platform is depicted in Fig. 7 and its key parameters are listed in Table IV.

There is a digital control delay when implementing FCS-MPC by DPSs. Thus, the two-step forward prediction is required and adopted in this article [39].

For conciseness, the experimental test conditions are summarized in Table V. In Table V, I^*_o and f^*_o represent the amplitude reference and the frequency reference of converter output currents, respectively.

A. Execution Time

To compare the computational efficiency of the conventional and the proposed FCS-MPC, their execution time is evaluated in experiments. In this article, the FCS-MPC approach in [40] is taken as the conventional FCS-MPC. Input/output (I/O) ports of the DSP TMS320F2808 are utilized to evaluate execution time. The level of I/O ports is set to high level once the algorithm runs and reset to low level when the FCS-MPC algorithm is completed. The execution time of different FCS-MPC approaches is depicted in Fig. 8 and summarized in Table VI. In the system, the control period is equal to the sampling period of 100 μs. As shown in Table VI, it is clearly observed that the proposed FCS-MPC algorithm has less execution time although there are 75 candidate VVs instead of 27 VVs for the conventional FCS-MPC algorithm. Therefore, the proposed FCS-MPC algorithm is computationally more efficient.

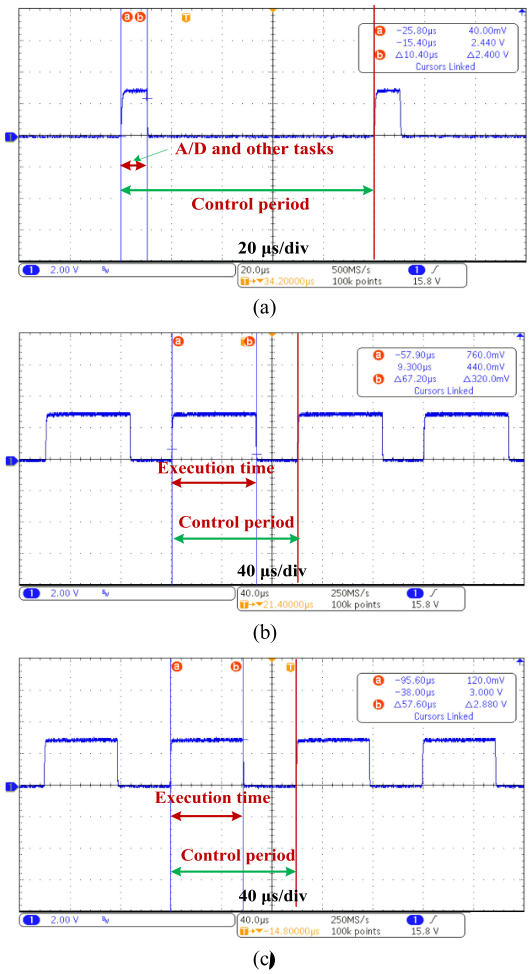

Fig. 8. Execution time. (a) A/D and other tasks. (b) Conventional FCS-MPC algorithm. (c) Proposed FCS-MPC algorithm.

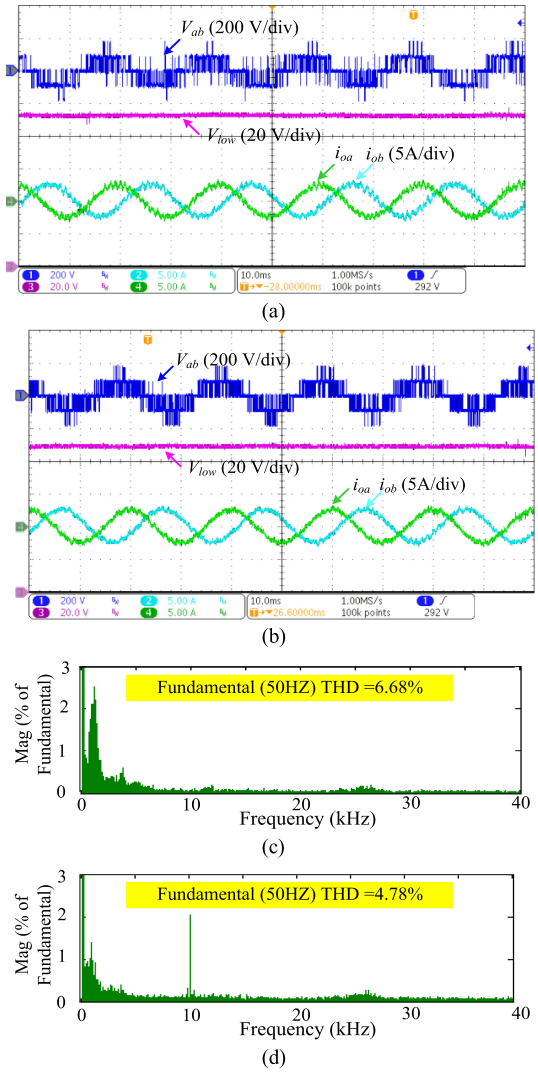

Fig. 9. Steady-state experimental results under Test 1 condition. (a) and (c) for the conventional FCS-MPC in [40]. (b) and (d) for the proposed FCS-MPC.

B. Steady-State Performance Evaluation

As shown in (17), the weighting factor of NP voltage balancing will directly affect the ripples of the NP voltage. The larger $\lambda_{\rm np}$ is, the higher priority NP voltage balancing obtains. In this article, the weighting factor $\lambda_{\rm np}$ is set to 0.015, which results in very similar peak-to-peak NP voltage ripple for both FCS-MPC algorithms. To compare the steady-state performance of the conventional and the presented FCS-MPC, Test 1 and Test 2 are carried out. Fig. 9 displays the main experimental results, including the output line–line voltage V_{ab}, dc-link lower capacitor voltage $V_{\rm low}$, phase-a and phase-b output currents (i_{oa}, i_{ob}), and fast Fourier transform of phase-a output current under Test 1 condition for both FCS-MPC methods. Fig. 10 shows the corresponding experimental waveforms under Test 2 condition.

From Figs. 9 and 10, the following aspects are clearly observed.

1) The output line–line voltage of the converter has five levels compared to the two levels of classical 3P-2L converter.
2) Output currents for both FCS-MPC algorithms are sinusoidal. THDs for the conventional FCS-MPC approach are 6.68% and 3.88% under Test 1 and Test 2, respectively, and the corresponding THDs for the proposed FCS-MPC algorithm are only 4.78% and 2.87%. The quality of output currents for the proposed FCS-MPC approach is significantly improved due to the employment of DSVM.
3) Harmonics of output currents in the conventional FCS-MPC approach spread over a wide frequency range, which is very undesirable for filter design. In comparison, current harmonics in the proposed FCS-MPC mainly concentrate at the sampling frequency (10 kHz), which is similar to the conventional space vector modulation. This significantly simplifies the filter design.
4) The dc-link lower capacitor voltage of both FCS-MPC methods is well controlled around 90 V (half of the dc-link input voltage), and its peak–peak voltage ripple keeps within 3 V. From these comparative results shown in Figs. 9 and 10, it can be concluded that the presented FCS-MPC has low current harmonics and good NP voltage balancing capability.

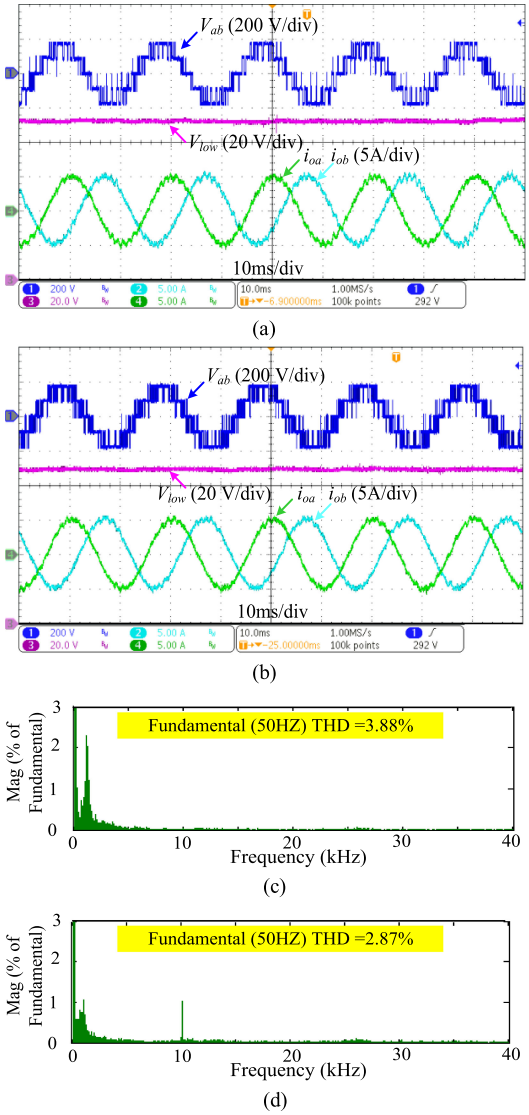

Fig. 10. Steady-state experimental results under Test 2 condition. (a) and (c) for the conventional FCS-MPC. (b) and (d) for the proposed FCS-MPC.

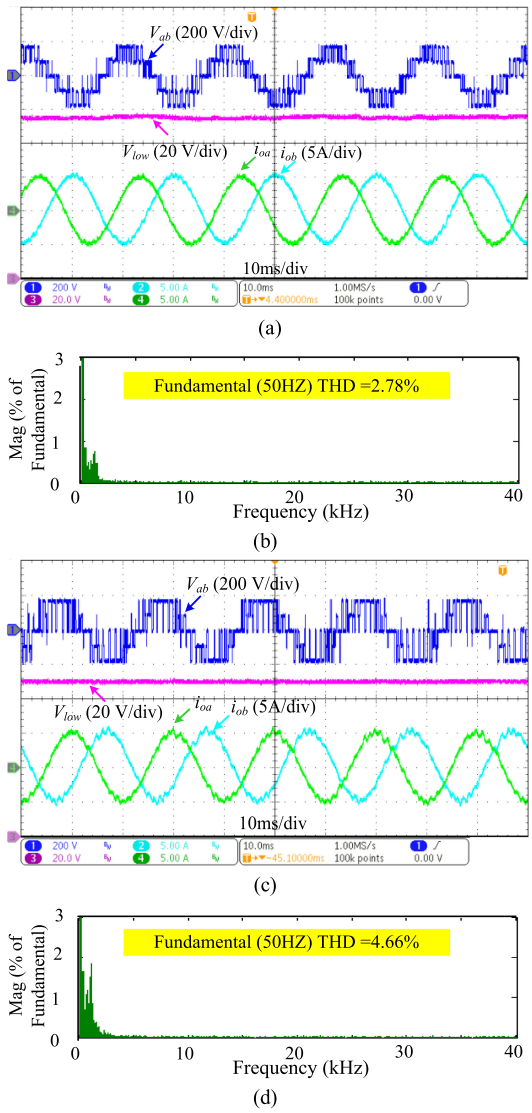

Fig. 11. Experimental results with different weighting factors $\lambda_{\rm np}$. (a) and (b) with $\lambda_{\rm np} = 0.0015$. (c) and (d) with $\lambda_{\rm np} = 0.15$.

C. Performance Evaluation for Different Weighting Factors

As seen in (11), there is a weighing factor $\lambda_{\rm np}$. The larger the weighing factor $\lambda_{\rm np}$ is, the more priority is given to the control of NP voltage. Fig. 11 displays the experimental results under Test 2 with different weighting factors. From Fig. 11, it can be clearly observed that, first, the dc-link lower capacitor voltage $V_{\rm low}$ cannot be effectively controlled and is about 96 V with $\lambda_{\rm np} = 0.0015$. However, the dc-link lower capacitor voltage $V_{\rm low}$ is well controlled around 90 V with the peak–peak ripple less than 2 V when $\lambda_{\rm np} = 0.15$. The performance of NP balancing becomes worse when the weighting factor $\lambda_{\rm np}$ decreases. And second, the THD value is 2.78% with $\lambda_{\rm np} = 0.0015$, and the corresponding THD value is 4.66% with $\lambda_{\rm np} = 0.15$. The quality of output currents becomes better with the decrease of weighting factor $\lambda_{\rm np}$.

From the above analysis, it can be concluded that there is trade-off between the THD value and the NP balancing by adjusting the weighting factor $\lambda_{\rm np}$ for the conventional FCS-MPC. However, choosing a proper weighting factor $\lambda_{\rm np}$ requires tedious tuning procedures, which are really time consuming.

D. Performance Evaluation for the Same Average Switching Frequency

To fairly compare the steady-state performances of different control methods, the average switching frequency needs to be set equal [41], [42]. The average switching frequency $f_{\rm avs}$ for the 3P-3L converter can be defined as

$$f_{\rm avs} = \frac{1}{12T_{\rm sw}} \sum_{x=a}^{c} N_x \tag{22}$$

where $T_{\rm sw}$ represents the measurement time and it is set to 600 ms in the system. N_x $(x = a,b,c)$ means switching times of power switches in phase-x.

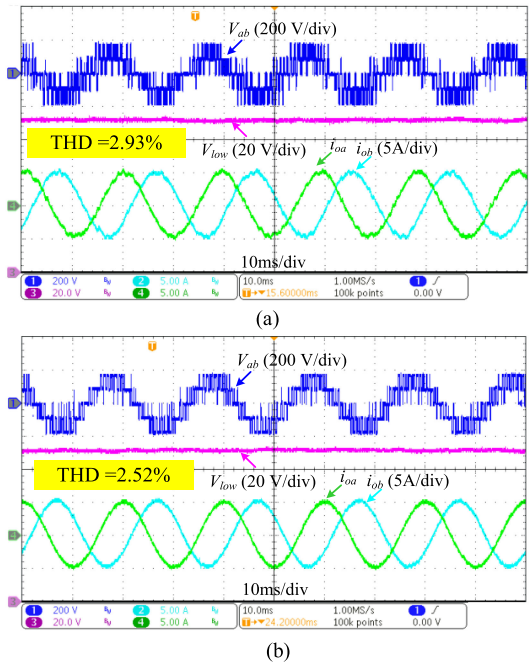

Fig. 12. Steady-state experimental results with the same average switching frequency. (a) Conventional FCS-MPC. (b) Deadbeat control with SVPWM.

TABLE VII
PERFORMANCE COMPARISION FOR DIFFERENT METHODS

Control schemes	f_s (kHz)	f_{av} (kHz)	THD
Deadbeat control	3.50	3.50	2.52%
Conventional FCS-MPC	20	3.50	2.93%
Proposed FCS-MPC	10	3.50	2.87%

In the article, three methods will be evaluated, including the conventional FCS-MPC in [40], the deadbeat control with space vector PWM (SVPWM) in [43], and the proposed FCS-MPC algorithm. Fig. 12 shows experimental results for different methods with the same average switching frequency under Test 2. To give a clear comparison, the sampling frequency, the switching frequency, and the THD of these three control schemes are listed in Table VII. The following phenomena can be observed from Table VII. First, the conventional FCS-MPC has the highest sampling frequency with the same average switching frequency. However, it has the largest THD value due to the application of only one VV in each control cycle. Second, the conventional deadbeat control has the lowest sampling frequency and the best quality of output currents. However, the deadbeat control requires the conventional SVPWM technique to achieve the fixed switching frequency. For the proposed MPC, it can easily include nonlinearities and constraints in the cost function. Thus, the proposed FCS-MPC is regarded as a promising control scheme for the 3P-3L converter.

E. Dynamic Performance Evaluation

To further compare the dynamic performance of the two FCS-MPC approaches, Test 3 and Test 4 conditions are conducted. Fig. 13 depicts the experimental waveforms of output line–line voltage V_{ab}, dc-link upper lower capacitor voltage V_{low}, and phase-a and phase-b output currents (i_{oa}, i_{ob}). The following facts can be clearly seen from Fig. 13. First, it takes less than 1 ms for both FCS-MPC methods to track current references. Second. the system for both FCS-MPC algorithms stays stability and works well when a 100% current reference change occurs, which illustrates that the proposed FCS-MPC has strong robustness. Third, the dc-link bottom capacitor voltage

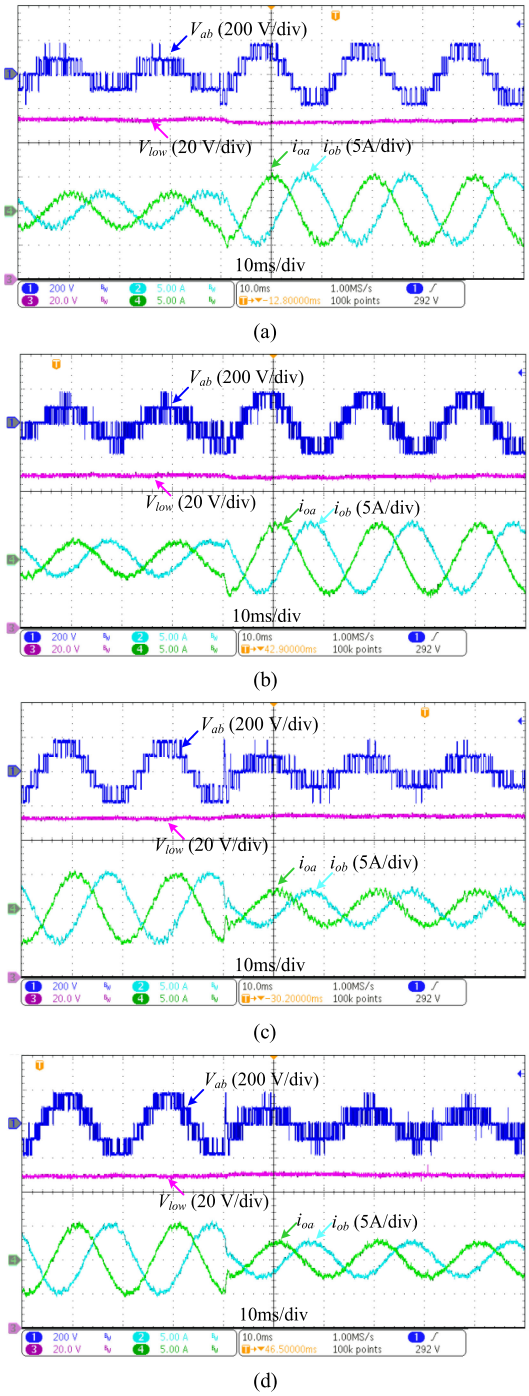

Fig. 13. Dynamic experimental results under Test 3 and Test 4 conditions. (a) and (c) for the conventional FCS-MPC. (b) and (d) for the proposed FCS-MPC.

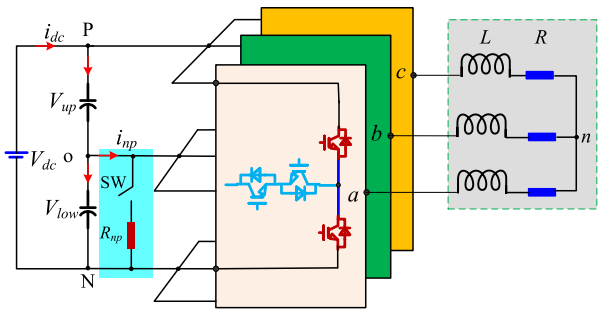

Fig. 14. Configuration of evaluating the NP capacitor voltage.

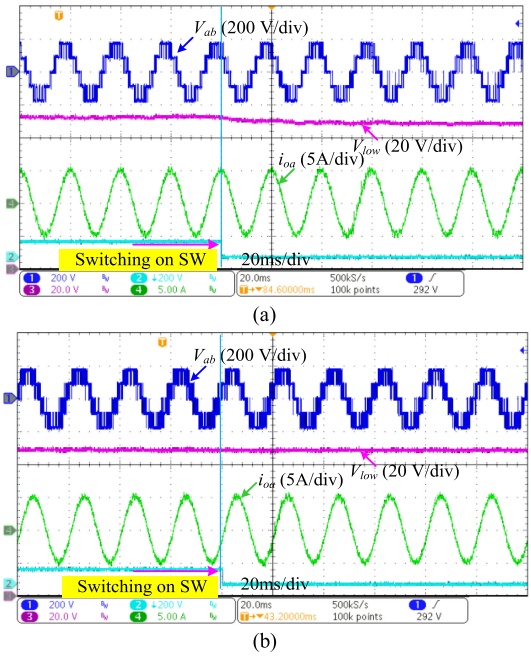

Fig. 15. Balancing NP voltage evaluation. (a) Conventional FCS-MPC. (b) Proposed FCS-MPC.

keeps almost unchanged even with 100% current reference step change for both FCS-MPC approaches. The experimental results demonstrate the fast dynamics of the proposed FCS-MPC.

F. Balancing NP Voltage Evaluation

To further verify the proposed FCS-MPC based on DSVM in balancing the NP voltage, a switch SW in series with a resistor $R_{\rm np}$ is added to the dc-link bottom capacitor voltage. The configuration is depicted in Fig. 14. As shown in Fig. 14, the resistor $R_{\rm np}$ is in parallel with the bottom capacitor when SW is turned ON. Then, the current will flow through the resistor which creates the NP voltage imbalance.

In the system, the resistance of $R_{\rm np}$ is selected to be 100 Ω. The test condition is given as follows.

Test 5: The amplitude and frequency of output current references are set to 5 A and 50 Hz, respectively. In addition, $R_{\rm np}$ is in parallel with the bottom capacitor by turning on the switch SW.

Fig. 15 shows experimental results under Test 5. The results in Fig. 15 can be summarized as follows:

1) The dc-link bottom capacitor voltage for the conventional FCS-MPC approach is stable. However, it becomes a bit lower than half of the dc-link voltage when SW is turned ON.
2) The bottom capacitor voltage $V_{\rm low}$ for the proposed FCS-MPC is nearly unaffected when SW is turned ON, which demonstrates the excellent NP voltage balancing capacity of the proposed FCS-MPC.

V. Conclusion

In the article, a low complexity FCS-MPC based on DSVM for 3P-3L converter has been proposed. Comparative experimental results for the conventional and proposed MPC approaches are presented, and some conclusions for these results are summarized as follows.

1) The proposed MPC produces excellent steady-state performance, and the quality of output current is significantly improved compared to the conventional MPC.
2) The peak amplitude of high-order harmonics concentrates at the sampling frequency.
3) Two-stage optimization is employed to reduce the computational burden. The execution time of the proposed MPC using the DSP TMS320F2808 is approximately 83% of that of the conventional FCS-MPC.
4) There is no weighting factor for the proposed MPC, which eliminates the tedious weighting factor tuning process required by the conventional MPC.
5) The proposed MPC exhibits very fast reference current tracking response.
6) The proposed MPC possesses excellent capacity in balancing the NP voltage with peak–peak ripple kept within 3 V.

In summary, the presented FCS-MPC overcomes disadvantages of the conventional FCS-MPC approach such as heavy computational burden, variable frequency of output currents, and the requirement of weighting factor tuning. Thus, the presented MPC exhibits a promising application prospects in 3P-3L converters.

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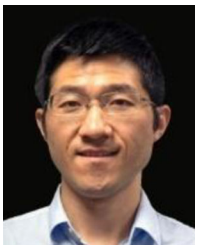

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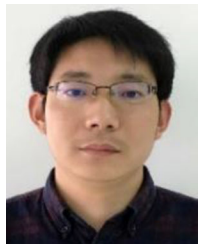

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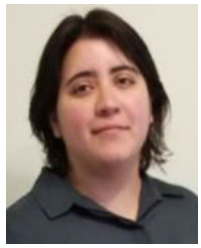

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