Four Novel Embedded Z-Source DC–DC Converters

Guidong Zhang, *Member, IEEE*, Ziyang Wu, Shenglong S. Yu, *Member, IEEE*, Hieu Trinh, and Yun Zhang

***Abstract*—This article develops a series of improved Z-source dc–dc converters to realize additional voltage pumping and high power density through two propositions. Proposition 1 develops two improved positive- and negative-connected Z-source dc–dc converters (IPZSC and INZSC), using the same number of components as in the existing voltage pumping Z-source converter. Based on Proposition 1, Proposition 2 proposes four novel embedded Z-source dc–dc converters (EZSCs) by placing the source in a specifically designed position, which realizes lower voltage stresses across capacitors. Various technical aspects of the proposed EZSCs, including operations, power losses, and small signal stability analyses are detailed in this paper. Besides, comparisons between the proposed series of improved Z-source dc–dc converters and other existing Z-source dc–dc converters are thoroughly made to demonstrate the better performance of the EZSCs. Finally, experiments are conducted to well validate the effectiveness and superiority of the proposed converter circuits.**

***Index Terms*—Capacitor voltage stresses, high-power density, high-step-up converters, Z-source dc–dc converter.**

I. Introduction

In RECENT years, air pollution and energy shortage have become major concerns in the international community, affecting all people living on the planet. To resolve or delay these problems, renewable energy (RE) installation capacity has experienced substantial increases due to the decreasing cost and maturity of RE technologies [1], [2]. Among the key power electronics technologies, multistage converters are employed in the RE generation systems like photovoltaic arrays or fuel cells to realize grid integration [3], [4]. For example, the two-stage inverter can be applied to a high-step-up dc–dc converter to minimize the required high power rating of the system and to boost low voltages to high voltages before being fed into the utility grid [5]–[7].

To design high step-up dc–dc converters, great research effort has been devoted. The main research findings include the coupled-inductor [8], switched inductor [9], switched capacitor [10], hybrid switched-inductor-capacitor [11], [12], voltage multiplier [13], and voltage lifter [14]. However, in all these topologies, the high voltage gain is achieved at the expense of increased sizes, higher costs, and complicated structures, which prevent the system from having high power density [15]–[17].

Limited by the parasitic parameters of the capacitor, inductor, and semiconductor switch, the conventional boost converter can only reach a maximum voltage gain of 5 or 6. Moreover, an extremely high duty cycle operation may cause serious reverse-recovery problem of the rectifier diode and large current ripples, which aggravate conduction losses [18]. To cope with this issue, cascaded boost converters have been developed and can provide high voltage gains without having an extreme high duty cycle. But this structure has many switches and high switch voltage stresses [19], [20].

The Z-source network, i.e., impedance network with power source, was first invented in 2003 by the researchers in [21], which consists of two identical capacitors and two identical inductors, forming an X-shape, which can be applied for dc–dc, dc–ac, ac–dc, and ac–ac power conversion. With this unique impedance network, the Z-source inverter (ZSI) bears a range of new attractive advantages like realizing voltage step-up and step-down, requiring minimum number of components and having high efficiency and low costs [21]. Despite being so, the ZSI also has some disadvantages. For example, the capacitors' voltage stresses are higher than the input voltage, which increases its cost and size. Besides, the discontinuous input current limits dc voltage utilization. Moreover, the boost factor is limited by $1/(1-2d)$ (d is the shoot-through duty ratio). To resolve these drawbacks, some improved ZSI and quasi-ZSI have been proposed. For instance, Tang *et al.* [22] proposed an improved ZSI with lower capacitor voltage stresses. Through exchanging the positions of the inverter bridge and diode and rearranging their connection directions, the capacitor voltage stress can be reduced significantly. Nguyen *et al.* [23] added one more inductor and one more capacitor to the traditional ZSI, resulting in another improved ZSI, which can provide continuous input current and a higher inverted voltage boost.

Owing to the buck–boost inversion ability, Z-source network is suitable for dc–dc converters as well. Cao and Peng [24] proposed a family of Z-source and quasi-Z-source dc–dc converters. With two active switches, these converters can provide four quadrant operations and obtain higher voltage gains than the boost converter. However, the voltage gain is limited by $(1-d)/(1-2d)$, which is relatively low even when a high duty cycle is used for driving the switches. In order to realize higher

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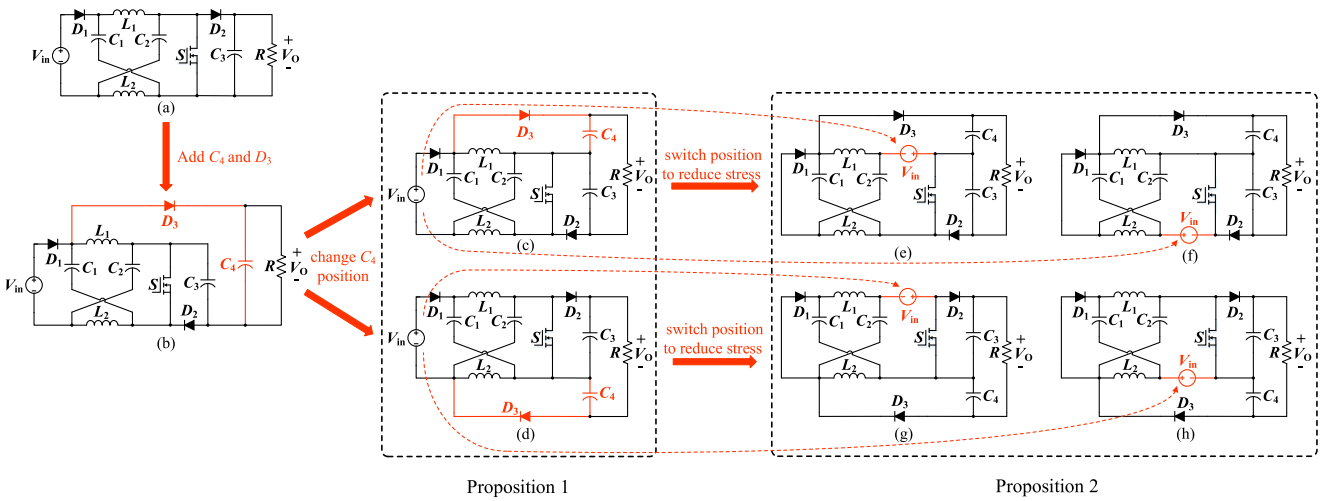


Fig. 1. Derivations of Z-source converters. (a) Conventional Z-source dc–dc converter. (b) Voltage pumping Z-source converter [28]. (c) Improved positive-connected Z-source dc–dc converter. (d) Improved negative-connected Z-source dc–dc converter. (e) Quasi positive-connected embedded Z-source converter. (f) Positive-connected embedded Z-source converter. (g) Negative-connected embedded Z-source converter. (h) Quasi negative-connected embedded Z-source converter.

voltage gains, Torkan and Ehsani [25] presented a high step-up dc–dc converter using Z-source network, flyback, and voltage multiplier concepts. However, the combination of several cells leads to complex circuitry and complicated control. In addition, the use of the coupled inductor in this converter may cause stability problems and low efficiency because of the leakage inductance. The cascaded topology with multiple switched-capacitor cells is presented in [26] in Z-source converter wherein the voltage gain of the converter achieves $(3-4d)/(1-4d)$, with d being the switchs duty cycle. However, an increased number of the switches lead to higher costs and low circuit reliability, which is not widely suitable for practical applications. Takiguchi and Koizumi [27] introduced a quasi-Z-source dc–dc converter with the voltage-lift technique. In this proposed circuit, a capacitor, an inductor, and two diodes were added to the conventional quasi-Z-source network. Compared with the Z-source dc–dc converter proposed in [24], this converter can not only obtain a higher voltage conversion ratio but can also reduce the capacitor voltage stress. However, this improvement was achieved at the expense of additional electronics components, which increases cost and reduces power density.

To achieve higher power density, a higher voltage gain with lower component stress is required, and the minimum number of additional electronics components are desired. Therefore, in this study, we propose a series of improved Z-source dc–dc converters with single-switch active impedance network. Two design propositions are detailed in this study—two improved Z-source dc–dc converters (IZSCs) and further to the IZSC, four embedded Z-source dc–dc converters. Particularly, two IZSCs are developed based on the voltage pumping Z-source converter in [28] and have identical electronics components. Then, by placing the input source at designated positions, four EZSCs are proposed. Through extensive theoretical study and derivations, power loss, efficiency, and system stability are investigated and presented, which show that the proposed EZSCs can all achieve a lower components voltage stresses and higher voltage gain than their existing counterparts. A 100-W positive-connected EZSC prototype is built in this work and experiments are conducted, which further verifies the advantages of the EZSC design.

II. Derivations of Z-Source Converters

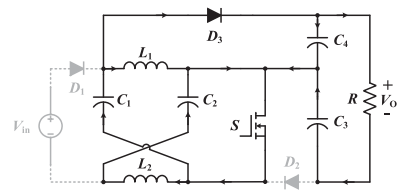
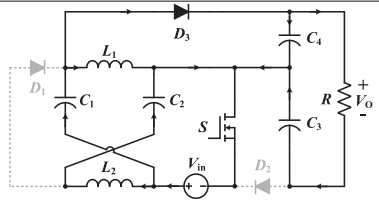
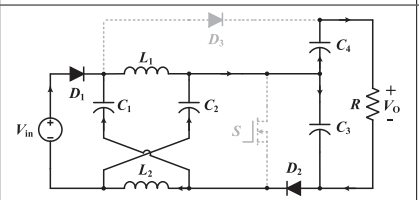
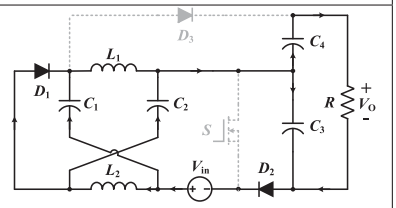
A. Conventional Z-Source DC–DC Converter

The conventional Z-source dc–dc converter (ZSC) is shown in Fig. 1(a). Compared with the traditional boost converter, its voltage conversion ratio can achieve as high as $1/(1-2d)$. However, the ZSC has the drawback of high capacitor voltage stress and, meanwhile, its voltage gain is still relatively low.

B. Proposition 1: Improved Z-Source DC–DC Converters

In order to realize higher voltage gains, Zhang *et al.* [28] proposed a voltage-pumping Z-source converter (VPZSC) with only one additional diode D_3 and capacitor C_4 than the conventional ZSC as shown in Fig. 1(b). It has a higher voltage conversion ratio and can reduce the input current ripple. Inspired by the VPZSC, an improved Z-source dc–dc converter, or IZSC, is proposed by changing the positions of the additional diode and capacitor in this study, i.e., Proposition 1. Fig. 1(c) and (d) depicts the two different IZSCs. The improved Z-source dc–dc converter has the same voltage gain as the VPZSC. However, the voltage stress on C_4 is lower, because the output capacitor is composed of capacitors C_3 and C_4. Since the voltage stresses on other capacitors can be further reduced, we consider this IZSC as an intermediary converter, which helps us design the four EZSCs in this article.

TABLE I
EQUIVALENT CIRCUITS OF IPZSC AND PEZSC

State	IPZSC	PEZSC
0		
1		

C. Proposition 2: Embedded Z-Source DC–DC Converter

Through setting the input-source at an appropriate position between the Z-network and switch based on the IZSC, embedded Z-source dc–dc converters are proposed. According to different connections and the position of the input source, four topologies are shown in Fig. 1(e)–(h). It can be seen that the voltage stresses on capacitors C_1 and C_2 decrease. Different performances of the boost ability can be achieved by different connections. Only when the input source is placed as shown in Fig. 1(f) and (g), the voltage gain remains the same as in the IZSC. Therefore, the negative-connected embedded Z-source dc–dc converter, or NESZC, and the positive-connected embedded Z-source dc–dc converter, or PEZSC, can not only reduce the voltage stresses on capacitors C_1, C_2, and C_4 but can also realize higher voltage gains, thus achieving higher power density.

III. OPERATIONAL ANALYSIS AND COMPARISON STUDY

Positive-connected converters, IPZSC and PEZSC, are analyzed in detail as two examples in this section, and negative-connected converters can be analyzed with the same method. Some assumptions are made as follows: 1) All electronics components are ideal. 2) $L_1 = L_2 = L, C_1 = C_2 = C_3 = C_4 = C$. Currents flowing through L_1, L_2 and voltages across C_1, C_2, C_3, C_4 increase and decrease linearly.

A. Operational Analysis

The operations of both the IPZSC and PEZSC can be divided into two states: State 0 and State 1. Table I shows the equivalent circuits of operation modes and relevant parameters are summarized in Table II.

B. Comparison Study

Table II presents a comprehensive comparison between the proposed and other Z-source-network-based converters. Meanwhile, a graphical comparison of the voltage gains of these converters is illustrated in Fig. 2. The conventional ZSC has a voltage gain of $1/(1-2d)$, and the numbers of L/C/D/S are

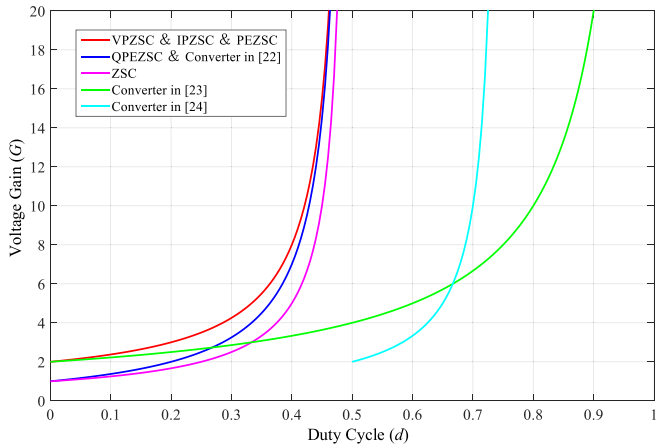


Fig. 2. Comparison of voltage gains between proposed and other Z-source-network-based converters.

2/3/2/1. Converter in [29] is a novel quasi-ZSC by adding a switched-capacitor branch to the existing quadratic boost converter. This quasi-ZSC has a boost factor of $2/(1-d)$, which may require extreme duty cycle (when $d = 0.8 \sim 0.9$) when high voltage gain is needed. This can damage the converter circuit. A three-level dc–dc converter with a diode-rectified quasi-Z source is proposed in [30]. With an additional switch than the converter in [29], its voltage gain achieves $2/(3-4d)$, with the duty cycle ranging from 0.5 to 0.75. However, the use of two switches increases the complexity of control; besides, the improvement of the boost factor is not significant. Research in [31] describes a ZSC with cascaded switched-capacitor, whose voltage gain can reach $(1+d)/(1-2d)$. Moreover, this converter has a lower duty cycle ranges similar to the conventional ZSC (i.e., $d = 0 \sim 0.5$). However, the numbers of L/C/D/S in this converter are 3/5/3/1, which leads to a bigger size, higher cost, and higher complexity. Compared with the conventional ZSC and three converters mentioned above, the VPZSC and the proposed IPZSC and PEZSC can realize higher voltage gains, and quasi-PEZSC has the voltage gain

TABLE II
COMPARISONS AMONG THE CONVENTIONAL ZSC, OTHER Z-SOURCE-NETWORK-BASED CONVERTERS, AND THE SERIES OF PROPOSED IMPROVED Z-SOURCE CONVERTERS

Topologies	No. of L/C/D/S	Voltage gain	Voltage stresses of capacitors	Voltage stresses of diodes and switches	Remarks
ZSC	2/3/2/1	$G=\frac{1}{1-2d}$ $(0<d<0.5)$	$V_{C_1}=V_{C_2}=\frac{1-d}{1-2d}V_{\rm in}$ $V_{C_3}=\frac{1}{1-2d}V_{\rm in}$	$V_{D_1}=V_{D_2}=\frac{1}{1-2d}V_{\rm in}$ $V_S=\frac{1}{1-2d}V_{\rm in}$	• Limited voltage gain • High voltage stresses on capacitors and semiconductors • Discontinuous input current
Converter in [29]	2/4/3/1	$G=\frac{2}{1-d}$ $(0<d<1)$	$V_{C_1}=V_{C_2}=\frac{d}{1-d}V_{\rm in}$ $V_{C_3}=\frac{1+d}{1-d}V_{\rm in}$ $V_{C_4}=\frac{2}{1-d}V_{\rm in}$	$V_{D_1}=V_{D_2}=V_{D_{\rm o}}=\frac{1}{1-d}V_{\rm in}$ $V_S=\frac{1}{1-d}V_{\rm in}$	• Extreme duty cycle when high voltage gain is needed • High voltage stresses on capacitors • Continuous input current
Converter in [30]	2/4/3/2	$G=\frac{2}{3-4d}$ $(0.5<d<0.75)$	$V_{C_1}=\frac{2d-1}{3-4d}V_{\rm in}$ $V_{C_2}=\frac{2-2d}{3-4d}V_{\rm in}$ $V_{C_3}=\frac{1}{3-4d}V_{\rm in}$ $V_{C_4}=\frac{2}{3-4d}V_{\rm in}$	$V_{D_1}=V_{D_2}=V_{D_3}=\frac{1}{3-4d}V_{\rm in}$ $V_{S_1}=V_{S_2}=\frac{1}{3-4d}V_{\rm in}$	• Additional switch • Limited voltage gain • High cost • Discontinuous input current
Converter in [31]	3/5/3/1	$G=\frac{1+d}{1-2d}$ $(0<d<0.5)$	$V_{C_1}=V_{C_2}=\frac{1-d}{1-2d}V_{\rm in}$ $V_{C_3}=V_{C_4}=\frac{1}{1-2d}V_{\rm in}$ $V_{C_{\rm f}}=\frac{1+d}{1-2d}V_{\rm in}$	$V_{D_1}=V_{D_2}=V_{D_3}=\frac{1}{1-2d}V_{\rm in}$ $V_S=\frac{1}{1-2d}V_{\rm in}$	• Lots of passive elements • Circuit complexity • Large volume • Discontinuous input current
VPZSC	2/4/3/1	$G=\frac{2-d}{1-2d}$ $(0<d<0.5)$	$V_{C_1}=V_{C_2}=\frac{1-d}{1-2d}V_{\rm in}$ $V_{C_3}=\frac{1}{1-2d}V_{\rm in}$ $V_{C_4}=\frac{2-d}{1-2d}V_{\rm in}$	$V_{D_1}=V_{D_2}=V_{D_3}=\frac{1}{1-2d}V_{\rm in}$ $V_S=\frac{1}{1-2d}V_{\rm in}$	• High voltage stresses on capacitors in Z-source network and C_4 • Discontinuous input current
IPZSC	2/4/3/1	$G=\frac{2-d}{1-2d}$ $(0<d<0.5)$	$V_{C_1}=V_{C_2}=\frac{1-d}{1-2d}V_{\rm in}$ $V_{C_3}=\frac{1}{1-2d}V_{\rm in}$ $V_{C_4}=\frac{1-d}{1-2d}V_{\rm in}$	$V_{D_1}=V_{D_2}=V_{D_3}=\frac{1}{1-2d}V_{\rm in}$ $V_S=\frac{1}{1-2d}V_{\rm in}$	• High voltage stresses on capacitors in Z-source network • Discontinuous input current
QPEZSC	2/4/3/1	$G=\frac{1+d}{1-2d}$ $(0<d<0.5)$	$V_{C_1}=V_{C_2}=\frac{d}{1-2d}V_{\rm in}$ $V_{C_3}=\frac{1}{1-2d}V_{\rm in}$ $V_{C_4}=\frac{d}{1-2d}V_{\rm in}$	$V_{D_1}=V_{D_2}=V_{D_3}=\frac{1}{1-2d}V_{\rm in}$ $V_S=\frac{1}{1-2d}V_{\rm in}$	• Medium voltage gain • Low voltage stresses on capacitors • Discontinuous input current
PEZSC	2/4/3/1	$G=\frac{2-d}{1-2d}$ $(0<d<0.5)$	$V_{C_1}=V_{C_2}=\frac{d}{1-2d}V_{\rm in}$ $V_{C_3}=\frac{1}{1-2d}V_{\rm in}$ $V_{C_4}=\frac{1-d}{1-2d}V_{\rm in}$	$V_{D_1}=V_{D_2}=V_{D_3}=\frac{1}{1-2d}V_{\rm in}$ $V_S=\frac{1}{1-2d}V_{\rm in}$	• High voltage gain • Low voltage stresses on capacitors • High efficiency • Discontinuous input current

curve between the two groups. The numbers of L/C/D/S in the VPZSC and proposed converters are both 2/4/3/1, which have only one additional diode and capacitor than the conventional ZSC. The voltage gain of the PEZSC rises from $1/(1-2d)$ to $(2-d)/(1-2d)$. Moreover, the PEZSC achieves the lowest components voltage stresses among all the converters in the table. Figs. 3 and 4 show the comparison of voltage stresses on capacitors among the conventional ZSC, the VPZSC, and the proposed PEZSC. In the PEZSC, the voltage stress on the capacitor in the Z-source network drops to $1/9 \sim 2/3$ of that in the VPZSC, while the voltage stress on the output capacitor drops to $3/8 \sim 5/8$ of that in the VPZSC (with duty cycle ranging from $0.1 \sim 0.4$). This reduces the converter size and cost and enhances its power density. In addition, according to the formulas presented in Table II, when all the converters have the same voltage gain, the semiconductors in conventional Z-source converter suffer the highest voltage stresses because of the use of a high duty cycle, while the voltage stresses on the semiconductors of the proposed improved Z-source converters are lower.

Note that among all the derived Z-source converters in Fig. 1, the input and output do not share a common ground, which is the inherent problem of all Z-source network-based converters.

IV. SMALL-SIGNAL MODELING AND ANALYSIS

To obtain the small-signal model of the PEZSC, the state vector is composed of the currents flowing through the inductors and the voltages across the capacitors, and input variable is defined the input voltage, i.e.,

$$x(t)=\begin{bmatrix} i_{L_1} & i_{L_2} & v_{C_1} & v_{C_2} & v_{C_3} & v_{C_4}\end{bmatrix}^T \tag{1}$$

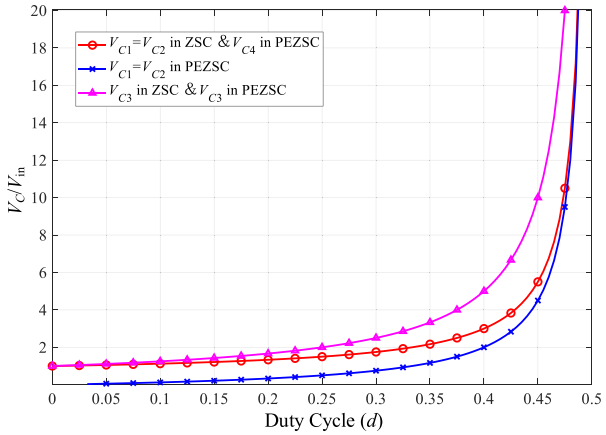


Fig. 3. Comparisons of capacitor voltages between the conventional ZSC and PEZSC.

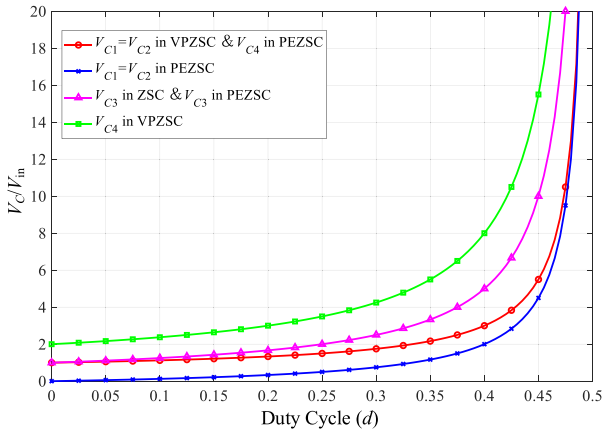


Fig. 4. Comparisons of capacitor voltages between the VPZSC and PEZSC.

$$u(t) = \left[v_{\text{in}}\right]. \tag{2}$$

When $0 \le t \le dT$, the converter works in State 0 and the following equations can be derived:

$$\begin{cases} L_1\frac{di_{L_1}}{dt} = v_{\text{in}} + v_{C_1}, L_2\frac{di_{L_2}}{dt} = v_{\text{in}} + v_{C_2} \\ C_1\frac{dv_{C_1}}{dt} = i_{\text{in}} - i_{L_2}, C_2\frac{dv_{C_2}}{dt} = i_{L_2} \\ C_3\frac{dv_{C_3}}{dt} = i_{\text{o}}, C_4\frac{dv_{C_4}}{dt} = i_{\text{o}} - i_{L_1} - i_{L_2} - i_{\text{in}} \end{cases}. \tag{3}$$

Meanwhile, the corresponding state-space model and output function for the PEZSC in State 0 can be derived

$$\begin{cases} \dot{x}(t) = A_1x(t) + B_1u(t) \\ y(t) = E_1x(t) + F_1u(t) \end{cases}. \tag{4}$$

According to the (3) and (4), matrices A_1, B_1, E_1, and F_1 can be obtained.

When $dT \le t \le T$, the converter works in State 1 and the following equations can be derived:

$$\begin{cases} L_1\frac{di_{L_1}}{dt} = -v_{C_2}, & L_2\frac{di_{L_2}}{dt} = -v_{C_1} \\ C_1\frac{dv_{C_1}}{dt} = i_{L_2} - i_{\text{in}}, & C_2\frac{dv_{C_2}}{dt} = i_{\text{in}} - i_{L_1}. \\ C_3\frac{dv_{C_3}}{dt} = i_{\text{in}} - i_{\text{o}}, & C_4\frac{dv_{C_4}}{dt} = i_{\text{o}} \end{cases} \tag{5}$$

TABLE III
COMPONENTS' VOLTAGE STRESSES

Component	Voltage Stress
C_1/C_2	$\frac{d}{1-2d}V_{\text{in}}$
C_3	$\frac{1}{1-2d}V_{\text{in}}$
C_4	$\frac{1-d}{1-2d}V_{\text{in}}$
S	$\frac{1}{1-2d}V_{\text{in}}$
$D_1/D_2/D_3$	$\frac{1}{1-2d}V_{\text{in}}$

TABLE IV
COMPONENTS' CURRENT STRESSES

Component	Current Stress
L_1	$\frac{V_{\text{o}}}{R_{\text{o}}}\cdot\frac{1+d}{1-2d}$
L_2	$\frac{V_{\text{o}}}{R_{\text{o}}}\cdot\frac{2-d}{1-2d}$
D_1/D_3	$\frac{V_{\text{o}}}{R_{\text{o}}}\cdot\frac{1+d}{1-2d}$
D_2	$\frac{V_{\text{o}}}{R_{\text{o}}}\cdot\frac{2-d}{1-2d}$
S	$\frac{V_{\text{o}}}{R_{\text{o}}}\cdot\frac{2-d}{1-2d}$

Meanwhile, the corresponding state-space model and output function for the PEZSC in State 1 can be derived,

$$\begin{cases} \dot{x}(t) = A_2x(t) + B_2u(t) \\ y(t) = E_2x(t) + F_2u(t) \end{cases}. \tag{6}$$

According to (5) and (10), matrices A_2, B_2, E_2, and F_2 can be obtained.

In a switching period T, the complete state transition matrices can be obtained by taking the average equation (4) and (6) as (7)–(10)

$$\begin{aligned} A &= dA_1 + (1-d)A_2 \\ &= \begin{bmatrix} 0 & 0 & \frac{d}{L_1} & -\frac{1-d}{L_1} & 0 & 0 \\ 0 & 0 & -\frac{1-d}{L_2} & \frac{d}{L_2} & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 & \frac{\epsilon}{C_1} & \frac{\epsilon}{C_1} \\ -\frac{1-d}{C_2} & \frac{d}{C_2} & 0 & 0 & \frac{\zeta}{C_2} & \frac{\zeta}{C_2} \\ 0 & 0 & 0 & 0 & \frac{\kappa}{C_3} & \frac{\kappa}{C_3} \\ -\frac{d}{C_4} & -\frac{d}{C_4} & 0 & 0 & \frac{\rho}{C_4} & \frac{\rho}{C_4} \end{bmatrix} \end{aligned} \tag{7}$$

$$[\text{Note}: \epsilon = \tfrac{2-d}{R(1-2d)}; \zeta = \tfrac{2-3d+d^2}{R(1-2d)}; \kappa = \tfrac{1+d-3d^2}{R(1-2d)}; \rho = \tfrac{1-2d+3d^2}{R}]$$

$$B = dB_1 + (1-d)B_2 = \begin{bmatrix} \frac{d}{L_1} & \frac{d}{L_2} & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{8}$$

$$E = dE_1 + (1-d)E_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}^T \tag{9}$$

$$F = dF_1 + (1-d)F_2 = \begin{bmatrix} 0 \end{bmatrix}. \tag{10}$$

TABLE V
EXPERIMENTAL PARAMETERS OF THE PEZSC

Parameters	Values
Input voltage V_{in}	20V
Output voltage V_{on}	140V
Rated power P_{o}	100W
Diodes D_1, D_2 and D_3	SS5200
Mosfet S	IPB117N20NFD
Inductors L_1 and L_2	330μH/6A
Capacitors C_1 and C_2	100μF/63V
Capacitors C_3 and C_4	100μF/100V
Switching frequency f	$50k$Hz
Load R_{o}	200Ω

State variables, input variables, output variables and control variable can be expressed as the sum of an average and a disturbance as shown below:

$$\begin{cases} \langle i_{L_1}\rangle_{\text{T}} = I_{L_1} + \hat{i}_{L_1} \\ \langle i_{L_2}\rangle_{\text{T}} = I_{L_2} + \hat{i}_{L_2} \\ \langle v_{C_1}\rangle_{\text{T}} = V_{C_1} + \hat{v}_{C_1} \\ \langle v_{C_2}\rangle_{\text{T}} = V_{C_2} + \hat{v}_{C_2} \\ \langle v_{C_3}\rangle_{\text{T}} = V_{C_3} + \hat{v}_{C_3} \\ \langle v_{C_4}\rangle_{\text{T}} = V_{C_4} + \hat{v}_{C_4} \\ \langle v_{\text{in}}\rangle_{\text{T}} = V_{\text{in}} + \hat{v}_{\text{in}} \\ d' = d + \hat{d} \end{cases} \tag{11}$$

where $\langle i_{L_1}\rangle_{\text{T}}$, $\langle i_{L_2}\rangle_{\text{T}}$, $\langle v_{C_1}\rangle_{\text{T}}$, $\langle v_{C_2}\rangle_{\text{T}}$, $\langle v_{C_3}\rangle_{\text{T}}$, $\langle v_{C_4}\rangle_{\text{T}}$, $\langle v_{\text{in}}\rangle_{\text{T}}$ is the average of $i_{L_1}, i_{L_2}, v_{C_1}, v_{C_2}, v_{C_3}, v_{C_4}, v_{\text{in}}$ in one switching cycle, respectively. d' is the variable quantity of the duty cycle of the switch.

When duty cycle $d = 0.4$, using the experimental parameters in Table V, the control-to-output transfer function can be obtained as (12) shown at the bottom of this page, for the simulation system. The bode diagram of the transfer function is shown in Fig. 5. In order to achieve stable operation, a voltage loop PI(propotional integrate) controller is used. The expression of the PI controller is $G_{\text{PI}}(s) = k_{\text{p}} + \frac{k_{\text{i}}}{s}$, where $k_{\text{p}} = 0.006$ and $k_{\text{i}} = 0.00065$ are selected. Using this voltage loop PI controller, the bode diagram of the proposed converter voltage loop is shown in Fig. 5. The phase margin is 47.8° when the gain is 0 dB, so this control strategy can ensure stable operations of the system.

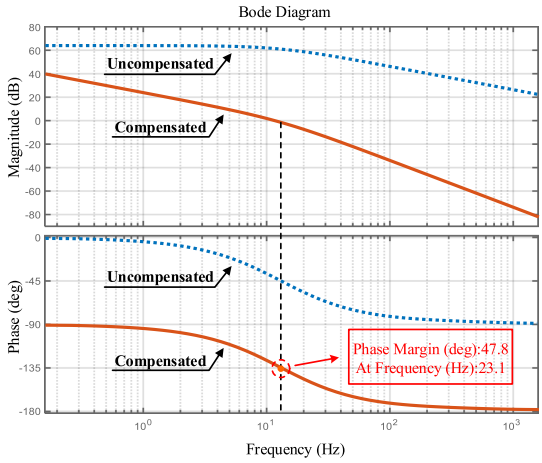


Fig. 5. Bode plot of the control-to-output transfer function of the PEZSC.

V. PARAMETERS DESIGN OF THE PEZSC

A. Voltage Stresses of Components

Through Table II, the maximum voltage of capacitors in the PEZSC are shown below:

$$V_{C_1} = V_{C_2} = \frac{d}{1-2d} V_{\text{in}} \tag{13}$$

$$V_{C_3} = \frac{1}{1-2d} V_{\text{in}} \tag{14}$$

$$V_{C_4} = \frac{1-d}{1-2d} V_{\text{in}}. \tag{15}$$

During State 0, diodes D_1 and D_2 are OFF, and the maximum voltages of D_1 and D_2 can be obtained as

$$V_{D_1} = V_{C_1} + V_{L_2} \tag{16}$$

$$V_{L_2} = V_{\text{in}} + V_{C_2}. \tag{17}$$

Substituting (13) and (17) into (16) leads to

$$V_{D_1} = \frac{1}{1-2d} V_{\text{in}} \tag{18}$$

$$V_{D_2} = V_{C_3} = \frac{1}{1-2d} V_{\text{in}}. \tag{19}$$

During State 1, diode D_3 and switch S are OFF, and the maximum voltages of D_3 and S can be obtained as

$$V_{D_3} = V_{C_4} - V_{L_1} \tag{20}$$

$$V_{L_1} = -V_{C_2}. \tag{21}$$

Substituting (13), (15), and (21) into (20) yields

$$V_{D_3} = \frac{1}{1-2d} V_{\text{in}} \tag{22}$$

$$G_{\text{do}}(s) = \frac{\hat{v}_{\text{o}}(s)}{\hat{d}(s)}\bigg|_{\hat{v}_{\text{in}}(s)=0} = \frac{1.377e05s^5 - 1.212e07s^4 - 3.414e12s^3 + 2.755e14s^2 + 7.361e18s}{s^6 + 80s^5 - 2.485e07s^4 - 1.996e09s^3 + 5.51e13s^2 + 4.599e15s}. \tag{12}$$

$$V_S = V_{C_3} = \frac{1}{1-2d} V_{\text{in}}. \tag{23}$$

Based on the derivations above, the voltage stresses of components are summarized in Table III.

B. Current Stresses of Components

In ideal cases, the effects of parasitic parameters of each device are ignored. According to the principle of power conservation, the input power of the converter is equal to the output power, and then the following relation can be obtained:

$$\frac{V_{\text{o}}^2}{R} = V_{\text{in}} I_{\text{in}}. \tag{24}$$

Thus, the maximum currents flowing through inductors L_1 and L_2 can be obtained as follows:

$$I_{L_1} = \frac{V_{\text{o}}}{R_{\text{o}}} \cdot \frac{1+d}{1-2d} \tag{25}$$

$$I_{L_2} = \frac{V_{\text{o}}}{R_{\text{o}}} \cdot \frac{2-d}{1-2d}. \tag{26}$$

During State 1, diodes D_1 and D_2 are ON, and the maximum currents flowing through D_1 and D_2 can be obtained as

$$I_{D_1} = I_{L_1} + I_{L_2} - I_{\text{in}} = \frac{V_{\text{o}}}{R_{\text{o}}} \cdot \frac{1+d}{1-2d} \tag{27}$$

$$I_{D_2} = I_{\text{in}} = \frac{V_{\text{o}}}{R_{\text{o}}} \cdot \frac{2-d}{1-2d}. \tag{28}$$

During State 0, diode D_3 is ON, and according the KCL, the maximum current flowing through D_3 is

$$I_{D_3} = I_{\text{in}} - I_{L_1} - I_{L_2} = \frac{V_{\text{o}}}{R_{\text{o}}} \cdot \frac{1+d}{1-2d}. \tag{29}$$

During State 0, switch S is ON. The maximum current flowing through S is

$$I_S = I_{\text{in}} = \frac{V_{\text{o}}}{R_{\text{o}}} \cdot \frac{2-d}{1-2d}. \tag{30}$$

Based on the derivations above, the current stresses of components are summarized in Table IV.

C. Inductors

The inductance of L_1 is selected according to the inter-peak current of L_1, the inductance by a given permitted fluctuation range $x_L\%$, inductor voltage V_{L_1}, duty cycle d, switching period T, and switch conduction time $T_{\text{on}} = dT$, which is shown as follows:

$$I_{L_{1\text{pp}}} = \int_{T_{\text{on}}}^{T} \frac{V_{L_1}}{L_1} dt = \frac{dV_{\text{in}}}{1-2d} \cdot \frac{1}{L_1} \cdot (T - T_{\text{on}}) \tag{31}$$

and

$$I_{L_{1\text{pp}}} = x_L\% I_{L_1}. \tag{32}$$

According to Table IV, (31), and (32), the derivation of L_1 can be obtained as

$$L_1 = \frac{d(1-d)^2 R}{(2-d)^2 x_L\% f_{\text{s}}}. \tag{33}$$

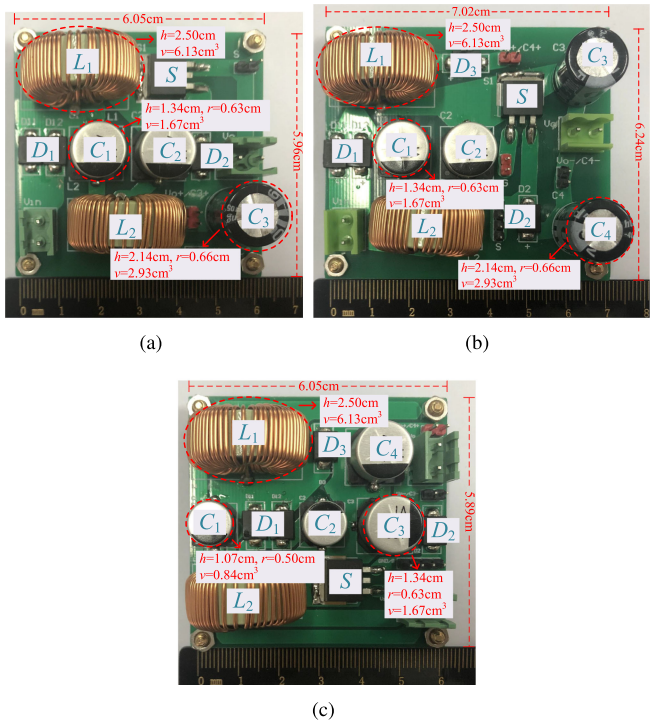


Fig. 6. Experimental prototype. (a) Conventional Z-source dc–dc converter. (b) Voltage pumping Z-source converter [28]. (c) Positive-connected embedded Z-source converter.

The inductance of L_2 is chosen to be the same as the L_1.

D. Capacitors

The capacitance of C_2 is determined according to the inter-peak voltage of C_2, the capacitance by a given permitted fluctuation range $x_C\%$, capacitor voltage V_{C_2}, duty cycle d, switching period T, and switch conduction time $T_{\text{on}} = dT$, which is shown as follows:

$$V_{C_{2\text{pp}}} = \int_{T_{\text{on}}}^{T} \frac{I_{C_2}}{C_2} dt = \frac{I_{\text{o}}}{C_2} \cdot (T - T_{\text{on}}) \tag{34}$$

and

$$V_{C_{2\text{pp}}} = x_C\% V_{C_2}. \tag{35}$$

According to Table III, (34), and (35), the expression of C_2 can be obtained as

$$C_2 = \frac{(1-d)(2-d)}{dRx_C\% f_{\text{s}}}. \tag{36}$$

The capacitance of C_1 is chosen to be the same as C_2.

The capacitance of C_3 and C_4 can be obtained with a similar method as follows:

$$C_3 = \frac{(1+d)(1-d)(2-d)}{(1-2d)Rx_C\% f_{\text{s}}} \tag{37}$$

$$C_4 = \frac{2-d}{Rx_C\% f_{\text{s}}}. \tag{38}$$

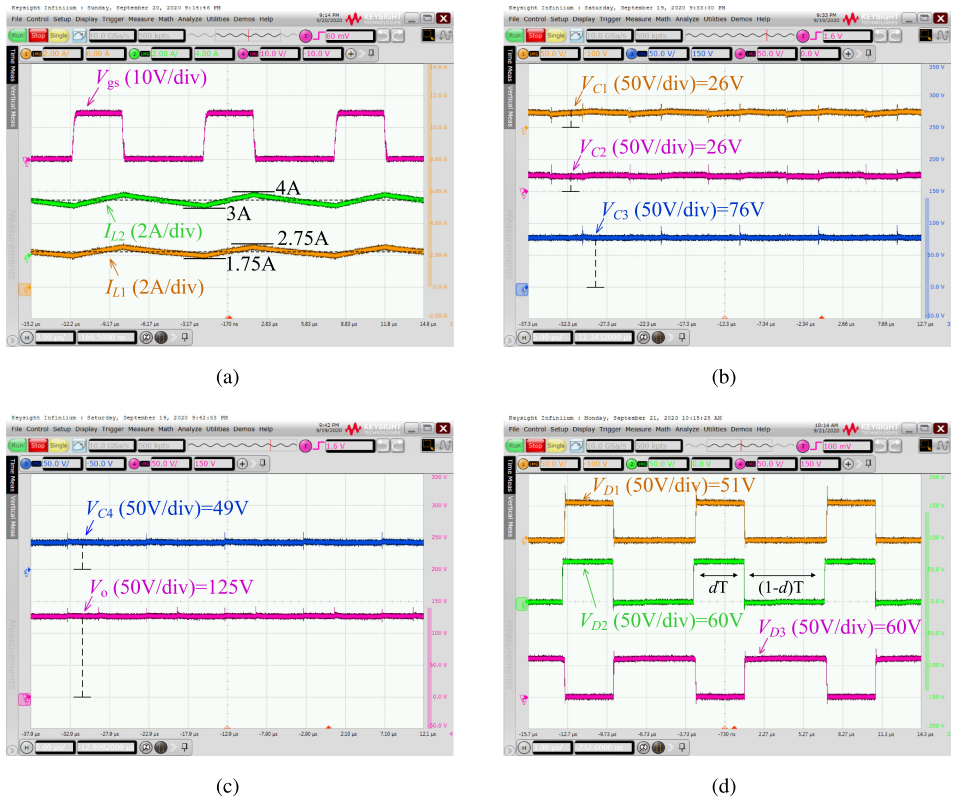


Fig. 7. Open-loop experimental results of the PEZSC. (a) Driving signal and the currents flowing through inductors I_{L_1} and I_{L_2}. (b) V_{C_1}, V_{C_2}, and V_{C_3}. (c) V_{C_4} and output voltage V_o. (d) V_{D_1}, V_{D_2}, and V_{D_3}.

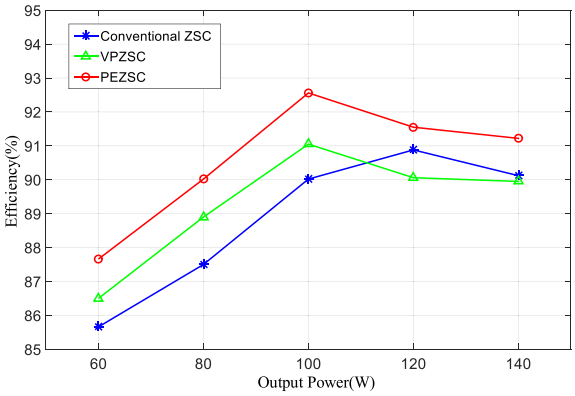


Fig. 8. Efficiency curves.

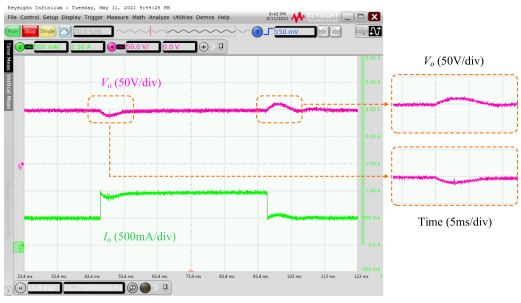


Fig. 9. Experimental waveforms for time-varying loads (output power is approximately 100 W).

TABLE VI
COMPARISONS OF SIZES, POWER DENSITY, AND COSTS AMONG THE CONVENTIONAL ZSC, THE VPZSC, THE IPZSC, THE QPEZSC, AND THE PEZSC

Topologies	Size(cm^3)	Power density	Cost
ZSC	$6.05 \times 5.96 \times 2.50$	$18.18\text{W}/\text{in}^3$	\$7.50
VPZSC	$7.02 \times 6.24 \times 2.50$	$14.97\text{W}/\text{in}^3$	\$8.29
IPZSC	$7.02 \times 6.24 \times 2.50$	$14.97\text{W}/\text{in}^3$	\$8.29
QPEZSC	$6.05 \times 5.89 \times 2.50$	$18.38\text{W}/\text{in}^3$	\$7.95
PEZSC	$6.05 \times 5.89 \times 2.50$	$18.38\text{W}/\text{in}^3$	\$7.95

E. Parameters of Switching Devices and Diodes

The voltage and current stresses are the key constraints for selecting switching devices and diodes. According to Tables III and IV, we can choose appropriate switches and diodes within the safety margin.

VI. EXPERIMENTAL VERIFICATION

To verify the proposed PEZSC, a hardware prototype is built in this study as shown in Fig. 6(c). In addition, to reveal the superiority of the PEZSC, hardware prototypes of conventional ZSC and VPZSC are also built as shown in Fig. 6(a) and (b). The experimental parameters and important specifications of power devices of the PEZSC are listed in Table V.

TABLE VII
LOSS ANALYSIS OF THE PEZSC

P_{L_1}		$R_{L_1} I^2_{L_1\mathrm{RMS}}$	0.51W
P_{L_2}		$R_{L_2} I^2_{L_2\mathrm{RMS}}$	0.72W
P_{D_1}	$P_{V_{F_1}}$	$V_{\mathrm{F}_1} I_{D_1\mathrm{avg}}$	0.50W
	$P_{R_{F_1}}$	$R_{\mathrm{F}_1} I^2_{D_1\mathrm{RMS}}$	0.46W
P_{D_2}	$P_{V_{F_2}}$	$V_{\mathrm{F}_2} I_{D_2\mathrm{avg}}$	0.50W
	$P_{R_{F_2}}$	$R_{\mathrm{F}_2} I^2_{D_2\mathrm{RMS}}$	0.46W
P_{D_3}	$P_{V_{F_3}}$	$V_{\mathrm{F}_3} I_{D_3\mathrm{avg}}$	0.50W
	$P_{R_{F_3}}$	$R_{\mathrm{F}_3} I^2_{D_3\mathrm{RMS}}$	0.46W
P_S	P_{con}	$R_{DS} I^2_{S\mathrm{RMS}}$	0.53W
	P_{sw}	$\frac{V_{DS(\mathrm{off})} I_{S(\mathrm{on})} (t_{\mathrm{on}} + t_{\mathrm{off}}) f_S}{6}$	0.80W
$P_{C_1} + P_{C_2}$ $+P_{C_3} + P_{C_4}$		$r_{C_1} I^2_{C_1\mathrm{RMS}} + r_{C_2} I^2_{C_2\mathrm{RMS}}$ $+r_{C_3} I^2_{C_3\mathrm{RMS}} + r_{C_4} I^2_{C_4\mathrm{RMS}}$	1.69W

Table VI shows the comparisons of power density, sizes, and costs among the conventional Z-source dc–dc converter, the VPZSC, the IPZSC, the proposed QPEZSC, and PEZSC. It can be seen that the PEZSC has the smallest size with the use of smaller capacitors due to the lower voltage stresses on capacitors, while the power density of the PEZSC is the highest among these converters. The cost of the PEZSC is between that of the conventional ZSC and VPZSC, but the PEZSC has achieved the highest voltage gain with low-voltage stresses on capacitors.

Fig. 7 shows the open-loop experimental results of the PEZSC. The driving signal and currents flowing through inductors I_{L_1} and I_{L_2}, voltages of capacitors V_{C_1}, V_{C_2}, and V_{C_3}, output voltage V_{o} and V_{C_4}, voltages of diodes V_{D_1}, V_{D_2}, and V_{D_3} are shown in each subfigures, respectively. In this experiment, the actual output voltage is 125 V, whereas the theoretical value is 140 V. This discrepancy is expected and acceptable. The power loss of PEZSC at 100 W is shown in Table VII when the load is 200Ω, wherein the loss of diodes accounts for 46% of the total loss. The efficiency curves of the conventional ZSC, the VPZSC, and the proposed PEZSC are shown in Fig. 8. It is obvious that the PEZSC has higher efficiency than the conventional ZSC and the VPZSC, and its highest efficiency reaches 92.68%.

Fig. 9 shows the closed-loop experimental results of the PEZSC. The input voltage V_{in} maintains at 15 V and the output resistance R changes from 200 to 100Ω, and then back to 200Ω. The parameters of the PI controller are set as $k_{\mathrm{p}} = 0.0015$, $k_{\mathrm{i}} = 0.0004$. It can be seen that the output voltage V_{o} restores to 100 V in 10 ms after the load changes, and the output voltage is not significantly affected by the load change.

VII. CONCLUSION

In this article, we have developed a series of improved Z-source dc–dc converters aiming to realize high voltage gain and high power density. Specifically, inspired by the voltage pumping Z-source converters in [28], an improved Z-source dc–dc converter with additional voltage pumping was proposed. Then, four embedded Z-source dc–dc converters based on the IZSC were proposed through circuit manipulations, which have higher voltage gains yet with lower component stresses. Through extensive theoretical analyses and experiments, the proposed positive-connected EZSC has been proven to attest a higher voltage gain than the existing Z-source network-based converters, while having low component stresses. To conclude, the proposed converter circuits are able to realize higher power density and voltage gains with lower sizes and costs, leading to their wide applicability in today's power electronics applications.

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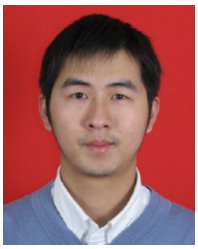

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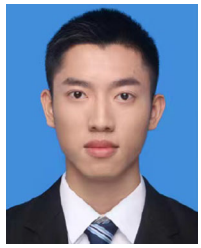

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