Feedback Noise Propagation in Multisampled DC–DC Power Electronic Converters

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***Abstract*—This article analyzes the propagation of feedback noise in multisampled dc–dc power converters. The analytical calculations for noise attenuation, strictly valid for linear time-invariant systems, are found to offer good predictions for power converters, after suppressing the decimation effects of the digital pulsewidth modulator (DPWM). For control systems that employ a proportional-integral controller, without any digital low-pass filters, the nonlinearity caused by the DPWM decimation is found to saturate the noise attenuation properties, as the multisampling factor N is increased. Strong noise attenuation is enabled using antialiasing digital filters, with a small impact on the dynamic response. For control systems that employ a proportional-integral-derivative controller, increase of the multisampling factor, without any digital filters, causes the amplification of the noise power. Therefore, a greater attenuation of high-frequency components is required to provide a significant noise reduction in the control bandwidth. Even with these antialiasing digital filters, the dynamic response of multisampled control systems is improved compared to double-update. This is proven by the analytical and experimental comparison of various multisampled control strategies in terms of dynamic response and noise attenuation capabilities. The experimental results, from a buck-type converter, match well with simulations and analytical calculations.**

***Index Terms*—Digital pulsewidth modulators (DPWM), feedback noise attenuation, multisampled pulsewidth modulators (MS-PWM).**

I. Introduction

In POWER electronics systems (PESs), digital signal processors (DSPs), and field-programmable gate array (FPGA) systems are nowadays standard solutions for control, due to their strong processing capabilities and decreasing cost. Digital control offers much higher flexibility compared to analog control circuits; this is especially important for applications that require various monitoring tasks, controller tuning, communications, additional protection levels, and similar [1]. For digitally controlled PESs with high dynamic performance, attention must be paid to the analysis of delays that are added, due to the analog-to-digital conversion (ADC), algorithm computation, and phase lag introduced by the digital pulsewidth modulator (DPWM) [1]. In standard digital control applications for power electronics, feedback acquisition and modulating waveform update are performed once (single-sampled, single-update method) or twice [double-sampled, double-update (DS-DU-PWM) method] per switching period [1]. The motivation for using single- or double-update of the modulating waveform is that the DPWM can adjust its output pulsewidth once (leading and trailing edge modulators) or twice (triangular modulator) per switching period. An often mentioned advantage of single-sampled and double-sampled methods is that the sampling itself acts as a finite impulse response filter for the switching ripple component. However, if the sampling instant of the inductor current is not perfectly aligned with the middle of the applied voltage impulse, this kind of sampling is seen to introduce severe errors for certain operating modes [2]. For voltage loops, the synchronization between the sampling instant and the average value is hardly achieved [1].

A step toward overcoming the bandwidth limitations of digital control loops is made by adopting the multisampled, multiupdate (MS-MU-PWM) control, in which the feedback is sampled and the modulating waveform is updated with a rate higher than double the switching frequency [3]. It has been thoroughly analyzed in the literature that the multisampled control reduces the digital control delays, improving both small-signal [3] and large-signal [4] responses. Due to these and other potential benefits, multisampling is gaining high interest for grid-connected converters [5]–[12]. Furthermore, the application of multisampling in predictive controllers is being investigated as well [13]–[15]. However, the MS-MU-PWM control introduces several drawbacks, mainly induced by the discontinuities of the digital modulating waveform [3], [16], [17]. Oversampling the feedback signal is also used in combination with single-update (MS-SU-PWM) and double-update (MS-DU-PWM) methods, for achieving the error-free acquisition (in terms of the actual average value) and strong noise attenuation [2], [8], [18], [19]. These strategies can be relatively easily implemented in DSPs as well, by exploiting the direct memory access (DMA) module, in order to highly oversample the signal and then average it over one switching period at a decreased control rate. In [8], it is shown that oversampling the signal and subsequently using a moving average filter (MAF), before reducing to single- or

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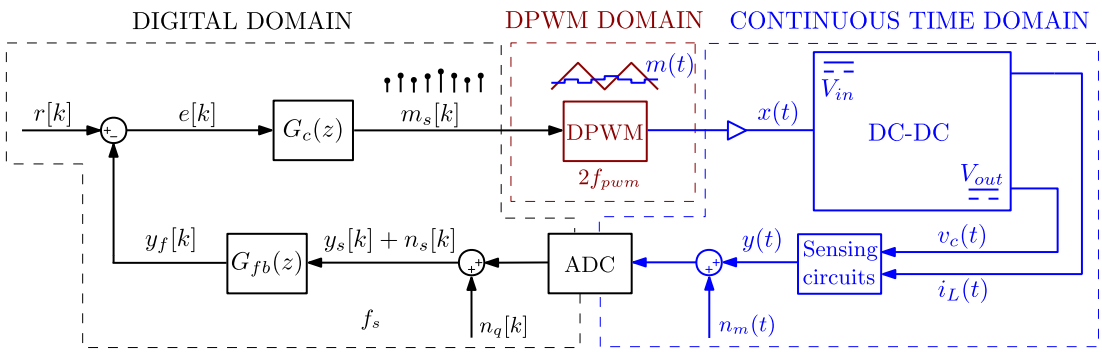

Fig. 1. Multisampled control loop of a dc–dc power converter with emphasis on its multirate structure.

double-update rate, can significantly reduce the output jitter. These methods rely on oversampling purely for filtering purposes, without exploiting the dynamic benefits.

This article, as an extension of [20], investigates the capability of MS-MU-PWM control to reduce the impact of white noise over control performance. Attention is dedicated to analyze whether multisampled systems can increase the noise attenuation, while maintaining the dynamic benefits. In [20], it is shown that the DPWM "resampling" action is the main limiting factor for white noise attenuation in multisampled PESs. This article further demonstrates that, for strong noise attenuation, some digital filtration above the switching frequency is required to suppress the DPWM decimation effects. Experimental results are given for a buck-type converter's single-stage current loop, with a proportional-integral (PI) controller, and for a single-stage voltage loop, with a proportional-integral-derivative (PID) controller. It is important to notice that this article investigates and models the attenuation of generally uncorrelated, white noise, which is why the feedback signal should not be dominantly affected by transistor switching noise and other PWM correlated noises. The key contributions of this article are as follows:

1) the analysis of single-stage current loops with PI controllers;
2) the analysis of single-stage voltage loops with PID controllers;
3) the analysis of control loops that use MAFs, as often used in industry for oversampled feedback filtering (MS-DU-PWM);
4) comparisons in terms of the dynamic performance and noise attenuation of the MS-MU-PWM method with two commonly used industrial approaches: the DS-DU-PWM method and oversampling applications that may be implemented on standard DSPs (MS-DU-PWM).
5) a guideline for the design of antialiasing digital filters for suppression of the DPWM decimation effect;
6) experimental validations of analytical results for a wide range of operating points;

The rest of this article is organized as follows. Section II presents the structure and small-signal modeling of multisampled dc–dc power converters. Section III discusses sources of errors in feedback acquisition and introduces an analytical procedure for calculation of white noise attenuation. In Section IV, PI and PID controllers are designed for current and voltage loops, respectively. The effect of the DPWM decimation is introduced and illustrated by providing simulation results. In the end, feedback filters are designed to suppress such negative effect. In Section V, extensive experimental verification of noise attenuation is performed on a buck-type converter. The results are compared with simulations and analytically obtained values. Section VI discusses and provides experimental results for different strategies that use multisampling, comparing them in terms of dynamics and noise attenuation. Finally, Section VII concludes this article.

II. Multisampled DC–DC Power Converters

An example of a dc–dc power converter, with MS-MU-PWM control stage, is shown in Fig. 1. The presented control system is of a multirate nature and can be separated in three sections, based on their operating frequency. The sampling and control frequency is labeled $f_s = Nf_{\text{pwm}}$, where f_{pwm} is the switching frequency and N is the oversampling factor. An ADC is used to sample the continuous time output variable, transforming it into the digital domain. After the sampling process, the ADC output is summed with $n_q(k)$, which models the quantization noise due to finite ADC resolution. The digital domain, which operates with the frequency f_s, consists of a digital feedback filter $G_{fb}(z)$ and a digital controller $G_c(z)$. The DPWM block transforms its digital input into an analog output. The modulating impulse train $m_s[k]$, which is the output of the digital controller, is held constant over one sampling period $T_s = \frac{1}{f_s}$, as the modulating waveform $m(t)$. It is compared with the DPWM counter, which results in a square-wave transistor gate signal $x(t)$ with period $T_{\text{pwm}} = \frac{1}{f_{\text{pwm}}}$. In this article, triangular DPWM is used due to its favorable characteristics for multisampled control [3]. The triangular DPWM adjusts its output based on the value of $m(t)$ twice per PWM period, which is why the DPWM domain is labeled with $2f_{\text{pwm}}$. The power stage and sensing circuits belong to the continuous time domain. The converter output $y(t)$ is summed with the measurement noise $n_m(t)$ resulting from sensing circuits.

A simplified block-diagram of a multisampled dc–dc converter is shown in Fig. 2, where all modeled noise sources are analyzed as a unique source $n(t)$. Note that the function of the interpolator is inherent to the DPWM, because that is the block where the conversion from the digital to analog domain takes

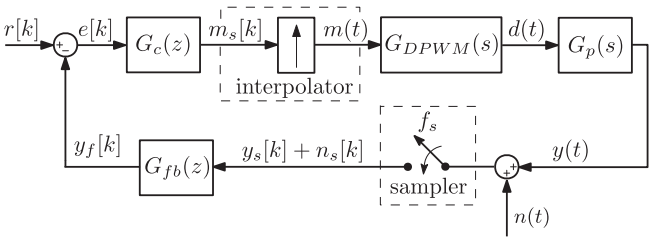

Fig. 2. Block diagram of the control loop in Fig. 1.

TABLE I
PARAMETERS OF THE ANALYZED BUCK-TYPE CONVERTER

Converter hardware parameters	label	value	unit
Nominal input voltage	V_{in}	400	V
Switching frequency	f_{pwm}	20	kHz
Filter inductance	L	1.2	mH
Filter capacitance	C	20	μF
Load resistor	R	47	Ω
Nominal power	P_n	3	kW

place [1]. Regarding its phase response, the DPWM with the triangular carrier can be well approximated in continuous-time domain with a pure delay independently of the operating point [1], [3]

$$G_{\text{DPWM}}(s) = \frac{d(s)}{m(s)} \approx e^{-s\frac{T_s}{2}} \tag{1}$$

where d is the continuous-time duty-cycle of $x(t)$, used in averaged modeling [1], and s is the complex variable of the Laplace transform.

For the subsequent small-signal analysis, the interpolator and the sampler feature unity gains. The analyzed converter operates in single-stage control-loop configuration, where the converter output $y(t)$ (either the inductor current $i_L(t)$ or the output capacitor voltage $v_c(t)$) is directly controlled by modifying the duty-cycle. The single-stage loops are used in order to examine the DPWM impact on the noise attenuation.

In this article, the experimental setup consists of a buck-type converter with resistive load, which is why it is used for the subsequent modeling. The experimentally used buck converter consists of an industrial half-bridge configuration, compatible with applications as a bidirectional dc–dc or dc–ac converter. The passive component sizing is a tradeoff between these possible applications. The switching frequency is fixed by design, based on the inductor and power switch technology. The parameters of the analyzed converter are shown in Table I.

The transfer function from d to y is obtained using averaging technique. For the current loop, it is equal to

$$G_{p,i}(s) = \frac{i_L(s)}{d(s)} = \frac{V_{\text{in}}}{R}\frac{sRC+1}{s^2LC + s\frac{L}{R}+1} \tag{2}$$

where V_{in} is the input voltage of the converter, R is the output load resistor, L is the filter inductor, and C is the filter capacitor.

For the voltage loop, it is equal to

$$G_{p,v}(s) = \frac{v_c(s)}{d(s)} = V_{\text{in}}\frac{1}{s^2LC + s\frac{L}{R}+1}. \tag{3}$$

III. Noise Modeling and Analytical Calculations

A. Sources of Errors in Feedback Acquisition

Some of the most relevant sources of errors in feedback acquisition, present in digitally controlled power converter systems, can be classified as follows.

1) Switching noise, resulting from high dv/dt and di/dt during commutations of the converter. This type of noise is strongly correlated with the feedback signal. It cannot be modeled as white noise and, because of that, is hard to treat analytically. In multisampled PWM control, for certain operating points, sampling of the switching noise cannot be avoided. This can cause undesired response of the controller to noise corrupted samples of the feedback signal. The switching noise is strongly dependent on the hardware design, and the undesired effects depend also on the oversampling factor, the duty cycle, and the filter and controller design. The effect of the switching noise is mentioned in [2] for the application of MS-DU-PWM, and its propagation in MS-MU-PWM control needs to be independently analyzed. The conclusions drawn in this article are valid for hardware systems that do not feature excessive propagation of switching noise. In cases when the feedback signal contains switching noise with high energy spread over the switching period, its content is sampled across all operating points, which makes the white noise attenuation properties masked [20].
2) Synchronous sampling errors. For acquisition of the inductor current, designers often rely on acquiring feedback samples at instants where the DPWM carrier is equal to zero or to its maximum value. Theoretically, for single-update methods, this instant coincides with the middle of the applied voltage impulse and the average value is sampled [1]. However, this is hardly achieved in practice, due to the deadtime in the driver signals, analog low-pass filters in the signal feedback path, limited bandwidth of the sensors, and other disturbances. This type of acquisition error can cause a significant impact on the system and can, therefore, be one of the motivations for oversampling the feedback signal and averaging it over the switching period [2]. It should be mentioned that in current industrial practice, these errors are often reduced simply by delaying the sampling instant.
3) Quantization noise, which results from ADC and DPWM operations. In modern processors, DPWM clocks have several hundreds of MHz rate, and the effect of DPWM quantization has a small impact on the system if the switching frequencies are not extremely high. Hence, only the effect of the ADC noise $n_q(t)$ is discussed. The quantization noise depends on the full-scale feedback signal range and the number of ADC bits. For the analysis, the quantization noise is represented as an additive white noise

superimposed to the sampled signal, which is a strong assumption for feedback systems [1].

4) Measurement noise $n_m(t)$, which propagates due to measurement and conditioning electronic circuits, and other sources of electromagnetic interference present at the converter's location [21]. For the analytical considerations presented in this article, this type of noise is also considered to be random and additive to the feedback signal.

For analytical purposes, the quantization and measurement noises are analyzed jointly, with the assumption of them being wide-sense stationary (WSS) random signals (white noise) [22]. In this way, a simple analytical procedure can be used to estimate the noise attenuation depending on the sampling frequency and small-signal models.

B. Analytical Calculation of White Noise Attenuation

The analysis is performed by studying the effect of processing a random discrete-time signal by a linear time-invariant (LTI) discrete-time system with a transfer function $H_n(z)$, where z is the complex variable of the Z transform corresponding to the sampling frequency f_s. From the statistical properties of a WSS random signal, the following formula can be used to calculate the attenuation of the noise variance of the output variable y [22]

$$\frac{\sigma_y^2}{\sigma_n^2} = \frac{2}{f_s}\int_0^{f_x} |H_n(e^{jf})|^2 df \tag{4}$$

where σ_y^2 is the variance of the analyzed output variable, σ_n^2 is the input noise variance, and f_x is the upper frequency limit for the calculation. In order to obtain the magnitude response $|H_n(e^{jf})|$, the small-signal transfer function is obtained by transforming the entire multirate system from Fig. 2 into the digital domain

$$H_n(z) = \frac{y_s(z)}{n_s(z)} = -\frac{L(z)}{1+L(z)} \tag{5}$$

where $y_s(z)$ and $n_s(z)$ are discrete-time variables corresponding to y and n. The loop gain $L(z)$ of the system shown in Fig. 2 is obtained by using the inverse Laplace transform $\mathcal{L}^{-1}$ and subsequently applying the Z transform $\mathcal{Z}$ to the continuous time domain part of the system [8]

$$L(z) = G_{fb}(z)G_c(z)\mathcal{Z}\left\{\mathcal{L}^{-1}\left\{G_{\text{DPWM}}(s)G_p(s)\right\}\right\}. \tag{6}$$

In sampled systems, the white noise spectral power is spread across the Nyquist frequency window, leaving lower spectral power density in the bandwidth of interest as the sampling frequency is increased [22]. This spreading is determined by the factor $\frac{2}{f_s}$ in (4). The integral in (4) determines the impact of the magnitude response of the system on the noise attenuation. An intuitive way of decreasing the noise power, even without multisampling, is to design control loops with lower bandwidths, providing a higher filtering action by $H_n(z)$. These two mechanisms jointly impact the total white noise attenuation of multisampled systems.

The Nyquist frequency of multisampled systems surpasses the switching frequency of the converter. As the small-signal plant models $G_{p,i}(s)$ and $G_{p,v}(s)$ are obtained using averaging technique, they are only valid up to a fraction of the switching frequency. Hence, in order to correctly estimate the variance attenuation, frequency window in (4) must be limited below f_{pwm}. In this article, the upper frequency limit is arbitrarily chosen as $f_x = 0.4 f_{\text{pwm}}$, which is anyway well-above the feasible bandwidths of state-of-the-art PWM control loops.

IV. Control Loop Design

In this section, controller structures for single-stage current and voltage loops of a buck-type converter are given. Subsequently, the effect of the DPWM decimation, which is found to be a limiting factor regarding white noise attenuation, is explained. In the end, digital feedback low-pass filters are designed to suppress the DPWM decimation effects.

A. Controller Design

Without loss of generality, the controllers analyzed in this article feature one step computation delay. The crossover frequency f_c of the control loops is chosen to be near $\frac{f_{\text{pwm}}}{10}$. For single-stage current loops, this is feasible using a PI controller $G_{c,i}$

$$zG_{c,i}(z) = k_{p,i} + k_{i,i}T_s\frac{1}{1-z^{-1}}. \tag{7}$$

For voltage loops, in order to achieve crossover frequencies above the LC resonance, a PID controller must be employed. Typically, this kind of controller also features a low-pass filter for the derivative gain, G_d

$$zG_{c,v}(z) = k_{p,v} + k_{i,v}T_s\frac{1}{1-z^{-1}} + \frac{k_d}{T_s}(1-z^{-1})G_d(z). \tag{8}$$

In this article, $G_d(z)$ is chosen to be a first order low-pass filter with cut-off frequency equal to $\frac{f_{\text{pwm}}}{2}$, discretized using the bilinear transform.

The controller parameters are designed according to the lowest tested N, after which they are kept constant. In this way, the crossover frequency remains the same, and the phase margin is increased for higher oversampling factors. This allows us to examine the noise properties with different multisampling factors in relative terms, without significantly altering the DPWM nonlinearity, resulting from modulating waveform discontinuity [3], [17]. Furthermore, by having significantly variable phase margins for lower values of N, the presented results are expected to show emphasized impact on noise attenuation of the closed-loop system $|H_n(z)|$. For higher values of N, where the phase margin is almost constant, the only expected impact on noise attenuation is, instead, the white noise spreading across the Nyquist frequency window.

For the voltage loop, in order to achieve satisfactory phase margin near $\frac{f_{\text{pwm}}}{10}$, analysis is performed starting from $N = 2$. The parameters of the controllers used in this article are shown in Table II.

B. Nonlinearity Caused by the DPWM Decimation

The analytical method for quantification of the white noise attenuation, shown in (4), is strictly valid only for LTI systems.

TABLE II
CONTROLLER PARAMETERS

Current loop	label	value	unit
Controller configuration	$G_{c,i}$	PI	/
Relative proportional gain	$\frac{V_{in}}{R}k_{p,i}$	0.2344	/
Relative integral gain	$\frac{V_{in}}{R}k_{i,i}$	585	$\frac{1}{\text{s}}$
Crossover frequency	$f_{c,i}$	2000	Hz
Tested oversampling factors	N	$[1, 2, 4, 8, 16, 32]$	/
Voltage loop	**label**	**value**	**unit**
Controller configuration	$G_{c,v}$	PID	/
Relative proportional gain	$V_{in}k_{p,v}$	1.3294	/
Relative Integral gain	$V_{in}k_{i,v}$	709	$\frac{1}{\text{s}}$
Relative Derivative gain	$V_{in}k_{d,v}$	$1.4 \cdot 10^{-4}$	s
Cut-off frequency of $G_d(z)$	$f_{c,d}$	10	kHz
Crossover frequency	$f_{c,v}$	1850	Hz
Tested oversampling factors	N	$[2, 4, 8, 16, 32]$	/

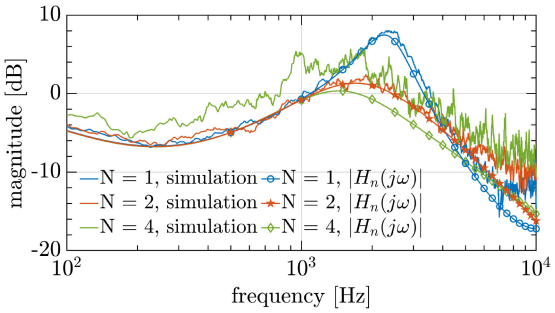

Fig. 3. Comparison between the simulated magnitude response from n_s to i_L and $|H_n(z)|$, for the converter described in Table I and the PI controller described in Table II. The spectra are averaged over 100 Hz. The simulation settings are described in Section V.

The multirate structure of a multisampled PES exhibits highly nonlinear properties, due to the DPWM. The impact of the triangular DPWM on noise attenuation can be estimated by modeling it as a resampler of $m_s[k]$ with the frequency $2f_{\text{pwm}}$. The nonlinear impact of the DPWM can be examined by simulating the magnitude response from individually sampled noise n_s to the inductor current i_L, and comparing it with $|H_n(e^{jw})|$. This kind of test cannot be performed experimentally due to existence of a unique ADC. The result of this simulation is shown in Fig. 3 for the current loop with parameters shown in Table II, up to $\frac{f_{\text{pwm}}}{2}$. The spectral content is averaged over 100 Hz, for clarity. As it can be seen, for $N = 1$ and $N = 2$, the simulated magnitude response matches very well to the response of the small-signal model, which shows that the linear analysis from (4) is a good approximation for single- and double-update DPWM. However, for $N = 4$, when the sampled feedback contains noise components at $f > f_{\text{pwm}}$, the simulated magnitude response shows a significant mismatch from the small-signal model. This difference is even higher as N increases further. The most-likely

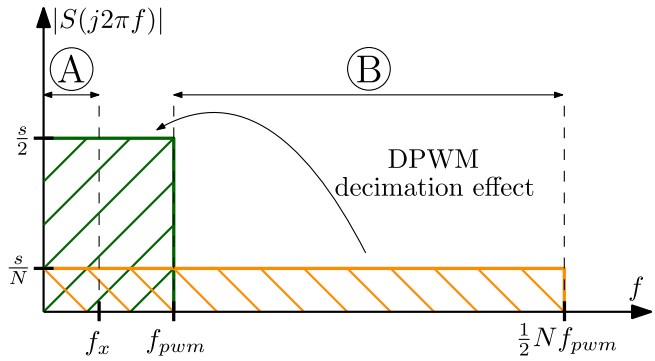

Fig. 4. Illustration of oversampling impact on white noise power spectral density $|S|$ for a triangular PWM carrier. Zone A represents the frequency window of interest for noise calculations. Zone B represents frequency window that must be filtered in digital domain to suppress the DPWM decimation effect.

reason behind this is that the aliasing of noise spectral components at $f > f_{\text{pwm}}$ is occurring due to "resampling" process introduced by the triangular DPWM.

In order to reduce the spectral fold-back and make noise attenuation properties closer to the values predicted by (4), some digital filtering is required. The required action of the digital low-pass filters (DLPFs) is to attenuate noise components above f_{pwm}, so that less noise power is folded back to low frequencies by the DPWM decimation. As shown in [20], for current loops with a PI controller, this DLPF can be designed to have a negligible impact on the system dynamic response, as its cut-off frequency is placed well-above the bandwidth of interest for noise calculations. In that way, the spectral aliasing is reduced, and the improvement of noise attenuation is expected on frequencies well-below f_{pwm}, where the DLPF does not have a direct impact.

The frequency regions of interest for noise attenuation in MS-PWM power converters are summarized in Fig. 4, by comparing a double-sampled system with an eight-sampled system. By oversampling the feedback, white noise spectral power is spread up to $\frac{1}{2}Nf_{\text{pwm}}$. This results in the power spectral density S being lower for the case with $N = 8$ than for the double-sampled case, $s_8 = \frac{2}{8}s_2$. The region of interest for noise attenuation $f < f_x$, is marked as A. The zone B marks the region in which the spectral components are folded back due to the DPWM decimation. Without any digital filtering, aliasing due to DPWM decimation limits the achievable power spectral density to the value determined by the double-sampling case. Regarding noise attenuation, this can be considered equivalent to the implementation of MS-MU-PWM with the controller output being decimated to $N = 2$, without any prior filtering. In order to achieve the power spectral density equal to $\frac{s}{N}$ in zone A, spectral components in zone B must be completely filtered-out in digital domain, prior to entering the DPWM. Hence, values predicted by (4) are expected to provide exact measure of noise attenuation for MS-PWM only if the entire spectral content of zone B is removed.

The triangular carrier is already proven to be most suitable for MS-PWM considering modulator dead-bands [3]. This section points to another possible advantage. Namely, the trailing and

leading edge modulators compare their counters with $m_s[k]$ (resample) only once per T_{pwm}. Therefore, digital filtering for noise attenuation should be performed in region $f > \frac{f_{\text{pwm}}}{2}$, which would imply a significant deterioration of the system dynamics.

C. Feedback Filter Design

In this section, digital feedback filters are designed in order to suppress the DPWM decimation effect. The design goal is to obtain filtering at $f > f_{\text{pwm}}$ (zone B in Fig. 4), while not imposing a too high impact on the dynamic performance. At frequencies much higher than bandwidth ($f > f_{\text{pwm}}$), the attenuation from noise to the DPWM input can be analyzed using a transfer function obtained with open-loop gains [8]. Based on Fig. 2, the transfer function from n_s to m_s, labeled as $H_{nm}(z)$, at frequencies where $|L(z)| \ll 1$ can be considered equal to

$$H_{nm}(z) = \frac{m_s(z)}{n_s(z)} = -G_{fb}(z)G_c(z). \tag{9}$$

Note that the feedback filter can also be added to the controller structure, which would result in a single design procedure. However, in this article, the filter is placed in the feedback path to more clearly represent its function. For current loops with a PI controller, the suppression of the DPWM decimation is tested by introducing a single first-order DLPF with the cut-off frequency equal to the switching frequency. This filter, labeled as $G_{\text{DLPF}}(z)$, is implemented in the following form using the Bilinear transform:

$$G_{\text{DLPF}}(z) = a\frac{z+1}{z+b} \tag{10}$$

where $a = \frac{\pi}{\pi+N}$ and $b = \frac{\pi-N}{\pi+N}$. This filter results in a small impact on the system dynamics as the phase lag introduced by it is nearly 6 degrees at $\frac{f_{\text{pwm}}}{10}$. For the current loop, the frequency responses of $H_{nm,i}(z)$ are shown in Fig. 5(a). For control loops that employ a PI controller, gain of $G_c(z)$ is practically constant above the bandwidth, determined by the value of k_p. Hence, the total noise power above the bandwidth practically does not change as the sampling frequency is increased. For voltage loops that require a PID controller, the situation is different. Due to the derivative action (comprising also a low-pass filter), gain of $H_{nm}(z)$ rises at high frequencies, and also with the increase of N. For this reason, with the increase of N, the total noise power being folded back by the DPWM decimation increases, which results in the amplification of the related spectral aliasing. Therefore, it is expected that higher attenuation at $f > f_{\text{pwm}}$ is required for the loops that employ a PID compared to the ones that employ a PI controller. Hence, for the voltage loop with a PID controller, the results are given for the $G_{\text{DLPF}}(z)$, and also for a third-order filter, equivalent to a cascade of three $G_{\text{DLPF}}(z)$, labeled $G^3_{\text{DLPF}}(z)$. Note that the $G^3_{\text{DLPF}}(z)$ introduces approximately 16° phase lag at the crossover frequency of the voltage loop, which results in a nonnegligible impact on the dynamic response. For the voltage loop, the frequency responses of $H_{nm,v}(z)$ are shown in Fig. 5(b). The results in Fig. 5 are given for $N = 8$.

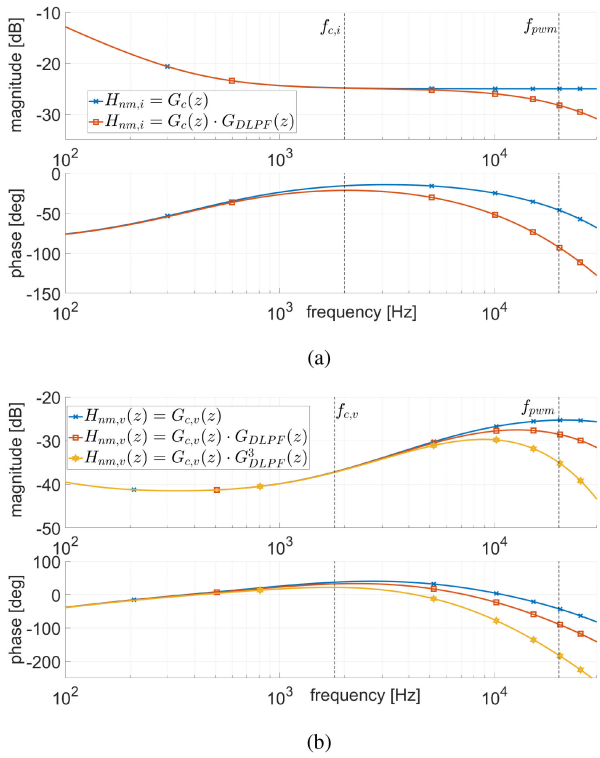

Fig. 5. Frequency responses of cascades of the controller $G_c(z)$ and the feedback filter $G_{fb}(z)$ for (a) current loop with the PI controller and (b) voltage loop with the PID controller. The controller parameters are shown in Table II and the plots are given for $N = 8$.

Finally, the impact of MAFs on noise attenuation is tested as well

$$G_{\text{MAF}}(z) = \frac{1}{N}\sum_{k=0}^{N-1} z^{-k}. \tag{11}$$

The phase lag of the $G_{\text{MAF}}(z)$ at the crossover frequency of the voltage loop is approximately 15°.

Note that for all results presented in this article, digital feedback filters are used only for oversampling factors $N > 2$ as their sole purpose is the attenuation of the aliasing effect due to the DPWM decimation, and not the direct attenuation of the spectral content up to f_x.

V. Verification of the Noise Attenuation

The noise attenuation properties are verified experimentally on a buck-type converter, described in Section II. The hardware parameters are equal to those in Table I and the controller parameters are equal to those in Table II.

The control system is implemented on an NI sbRIO-9606, which is based on a Xilinix Zynq 7020 all programmable system on chip (AP-SoC). The inductor current i_L and capacitor voltage v_c are sensed by a custom interfacing board, based on shunt-resistor and voltage divider, respectively [23]. The boards use conditioning circuits, 12 b ADC module AD9226 by Analog Devices, and digital isolators that enable FPGA platform to read digital signal values at very high rates. The ADC quantization in the experimental setup corresponds to $\text{LSB}_i = 17$ mA for

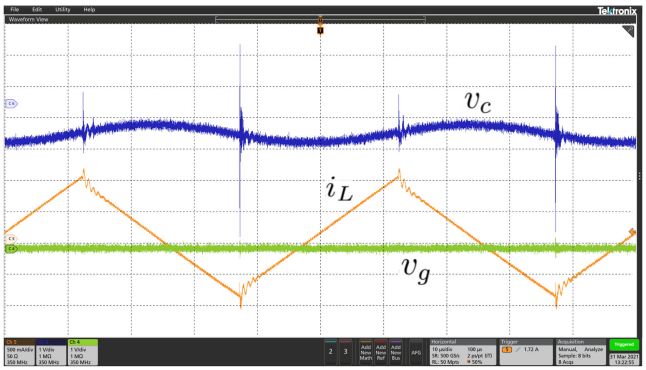

Fig. 6. Oscilloscope screen capture showing switching components over $2T_{\text{pwm}}$, with channel offsets. The blue trace features 1 V/div scale and corresponds to $v_c(t)$. The orange trace features 500 mA/div scale and corresponds to $i_L(t)$. The green trace features 1 V/div scale and corresponds to the voltage measured by connecting both probe leads to the capacitor ground connection, $v_g(t)$.

the current loop, and $\text{LSB}_v = 75$ mV for the voltage loop. The DPWM clock runs at 160 MHz rate.

For postprocessing, 50 ms of data is acquired with a 250 MS/s rate, using the high-resolution mode (15 b) of Tektronix MS056 oscilloscope with channel bandwidths set to 20 MHz. The inductor current is sensed using Tektronix TCP202 current probe, and the capacitor voltage is sensed using Rohde & Schwarz RT-ZD01 differential voltage probe, with attenuation set to 100. Signal offsets and scales that result in highest possible resolution are set on the oscilloscope.

Measurements are conducted for steady-state duty cycles equal to $D = [0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8]$. By covering a wide range of operating points, the sensitivity of noise attenuation properties can be examined. This is especially important as in experimental prototypes certain amount of switching noise is always present. All presented measurements were repeated multiple times, in order to verify that they do not significantly vary from one measurement to another. The input voltage for the voltage loop tests is set to $V_{in} = 160$ V, so that the voltage probe attenuation would not have to be changed to 1000, which would increase the noise resulting from the probe. For the current loop tests, the input voltage is set to $V_{in} = 200$ V, in order to have a comparable switching noise content. The variance is calculated up to $f_x = 8$ kHz.

Two switching periods of i_L and v_c are shown in Fig. 6, for the highest possible sampling rate of the oscilloscope, without bandwidth limitations on input channels. The presence of the switching noise is clearly seen, and its magnitude compared to the switching ripple component is much higher in the capacitor voltage than in the inductor current. In order to verify that the spikes are an actual differential voltage across the capacitor terminals, both leads of the probe were connected to the negative capacitor terminal. This ground voltage measurement is also shown in Fig. 6 as v_g and it can be seen that its value is negligible.

A. Benchmark Simulation Settings

Simulations are performed in MATLAB/Simulink (using PLECS Blockset) by injecting a random signal into the feedback.

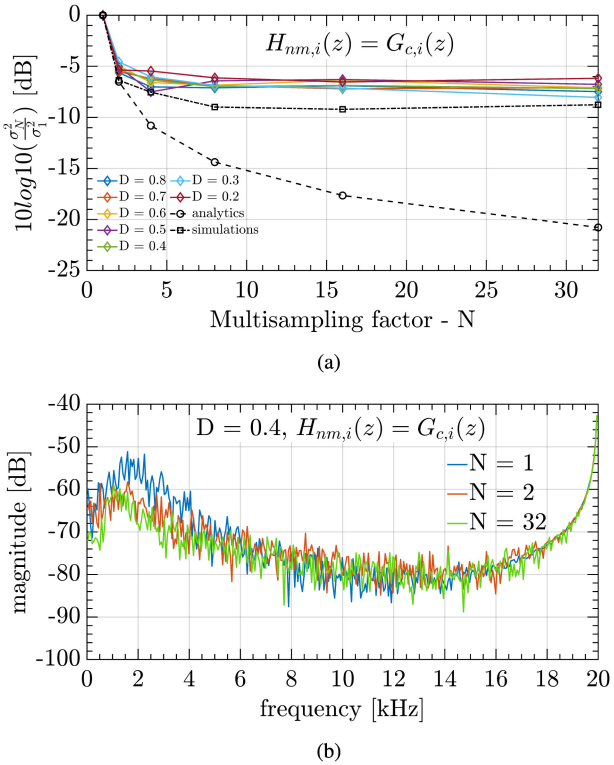

Fig. 7. Comparison between experiments, simulations, and analytics for the current loop without feedback filters: (a) variance results, (b) spectral results.

The injected signal features high enough bandwidth, so that it can be considered as white noise for all examined sampling frequencies. In simulations, data acquisition, ADC and DPWM quantization effects match those in the experimentally tested prototype. The motivation for these simulation results is to compare the noise attenuation in MS-MU-PWM power converters, with ideal white noise in the feedback, and the results predicted by (4). The switching noise is not simulated, as it is strongly dependent on hardware realization and operating points; hence, the results would lack generality in conclusions. These results serve as a benchmark for subsequent experimental verifications. The simulations were performed for many operating points, variances of the injected noise, and controller gains. The relative noise attenuation results did not change, hence, experimental results are compared with simulations for $D = 0.4$ and injected noise variance $\sigma^2_{nm,i,v} = 10^{-3}$ [A^2, V^2].

B. Results for the PI Current Loop

Variances of measured i_L, simulation results, and analytical values obtained using (4) are given in Figs. 7(a) and 8(a). Variance results are given relative to the lowest tested oversampling factor ($N = 1$ for the current loop), in logarithmic scale.

In Fig. 7(a), results are given for the control loop without any digital feedback filter, where $H_{nm,i}(z) = G_{c,i}(z)$. A great mismatch from analytical values is obtained both in simulations and experimental measurements. This is due to the mentioned DPWM decimation phenomenon, seen in Fig. 3. As observed, for $N > 2$, the noise power remains nearly constant, with small

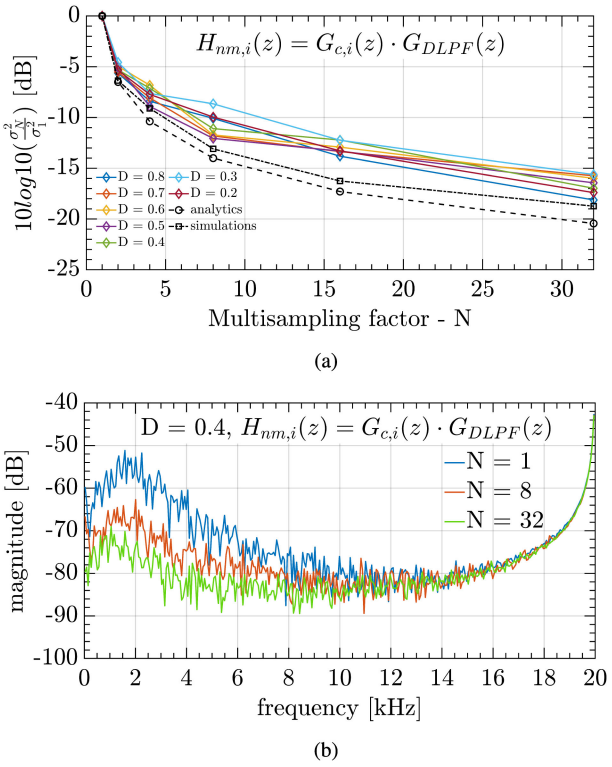

Fig. 8. Comparison between experiments, simulations and analytics for the current loop with $G_{\text{DLPF}}(z)$: (a) variance results and (b) spectral results.

variations caused by the impact of the magnitude response of $H_n(z)$. Note that this result is completely coherent with the reasoning made in Section IV-B. Namely, if no digital filtering is used to attenuate components in zone B in Fig. 4, DPWM "resampling" action causes aliasing, and no benefit in terms of noise attenuation is obtained compared to double-update. The spectral plots in Fig. 7(b) show negligible difference in noise floor between cases with $N = 2$ and $N = 32$. All spectral results are averaged over 60 Hz window for clarity and the dc component is removed. For this control loop realization, phase margins are equal to $\{25.75, 53.3, 66.98, 73.77, 77.15, 78.84\}$ [deg] for $N = \{1, 2, 4, 8, 16, 32\}$, respectively. The experimentally obtained variances, relative to $N = 1$ and averaged over the tested values of D, are equal to $\{-5.2, -6.45, -6.75, -6.76, -7.12\}$ [dB], for N starting from 2. It can be seen that strong noise attenuation is obtained when increasing N from 1 to 2, due to the much higher phase margin that results in a higher filtering action by $H_n(z)$.

In Fig. 8(a), variance results are shown for the case when the DLPF is introduced in the feedback, i.e., $H_{nm,i}(z) = G_{c,i}(z) \cdot G_{\text{DLPF}}(z)$. It can be seen that the addition of $G_{\text{DLPF}}(z)$ results in a good match with analytical predictions of both simulations and experimental results. The results are consistent for all operating points. For this control loop realization, phase margins are equal to $\{25.75, 53.3, 61.2, 68, 71.38, 73.1\}$ [deg] for $N = \{1, 2, 4, 8, 16, 32\}$, respectively. The experimentally obtained variances, relative to $N = 1$ and averaged over the tested values of D, are equal to $\{-5.2, -7.81, -10.77, -13.3, -16.6\}$ [dB], for N starting from 2. It can be seen that for higher values

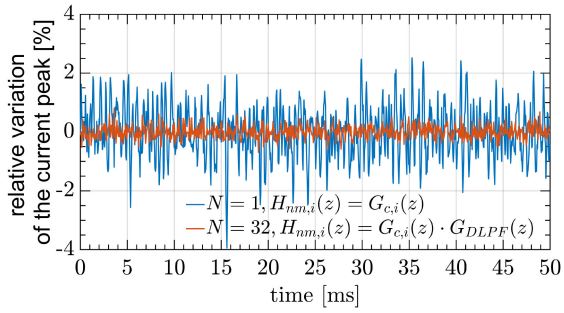

Fig. 9. Experimental results for time-domain noise impact illustration in current loops. The case featuring $N = 1$ is compared with the case featuring $N = 32$ and $G_{\text{DLPF}}(z)$. The results show relative variation of detected current peak values.

of N, where the phase margin is nearly constant, noise power attenuation is close to -3 dB when the value of N is doubled. This is consistent with (4), where for a constant value of $|H_n(z)|$, change of the oversampling factor from N_1 to N_2 scales the variance as $\frac{N_2}{N_1}$. It can be seen that a multisampled control loop with the $G_{\text{DLPF}}(z)$ significantly suppresses the noise content, while retaining high dynamic performance. In Fig. 8(b), spectral results show significant difference in noise floor when multisampling factor is increased. It should be noted again that the $G_{\text{DLPF}}(z)$ does not directly impact noise attenuation in frequency window for variance calculation by modifying $|H_n(z)|$, but by reducing the DPWM aliasing. The results for $N = 1$ and $N = 2$ are performed without $G_{\text{DLPF}}(z)$ as the DPWM decimation does not occur for those cases.

For time domain illustration, peaks of i_L are detected and plotted in Fig. 9 for $N = 1$ and $N = 32$ with DLPF, as extreme cases. The plot features relative values, obtained by subtracting the mean value of current peaks, and dividing by the dc value of i_L, for $D = 0.4$.

From these results, it is concluded that MS-MU-PWM control loops with a PI controller can offer high noise attenuation, without a significant impact on the dynamic response.

C. *Results for the PID Voltage Loop*

In Fig. 10, variance results are shown for the voltage loop, without and with $G_{\text{DLPF}}(z)$ added in the feedback. The noise power is shown relative to $N = 2$. It is interesting to note that here, unlike for the current loop, using MS-MU-PWM control without any digital filters [see Fig. 10(a)] results in the noise amplification rather than attenuation, for reasons described in Section IV-C. For this control loop realization, phase margins are equal to $\{20.1, 35.5, 43.1, 46.8, 48.7\}$ [deg] for $N = \{2, 4, 8, 16, 32\}$, respectively. The experimentally obtained variances, relative to $N = 2$ and averaged over the tested values of D, are equal to $\{6.36, 6.16, 6.64, 7.3\}$ [dB], for N starting from 4. With the increase of N, even though the filtering action of $H_n(z)$ is increased, the noise power is amplified due to the high-frequency behavior of the derivative action. This suggests that using PID controllers can strongly limit the benefits of multisampling.

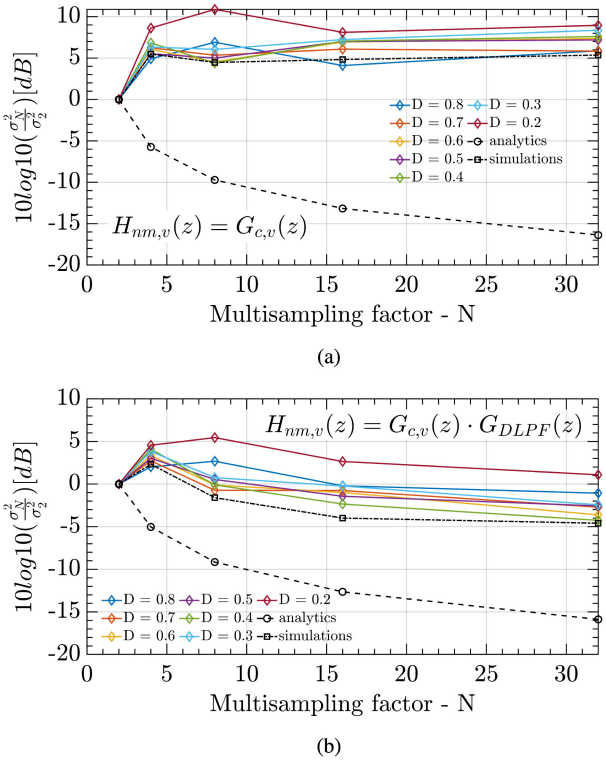

Fig. 10. Comparison between variances obtained through experiments, simulations, and analytics for the voltage loop, (a) without feedback filter and (b) with $G_{\mathrm{DLPF}}(z)$.

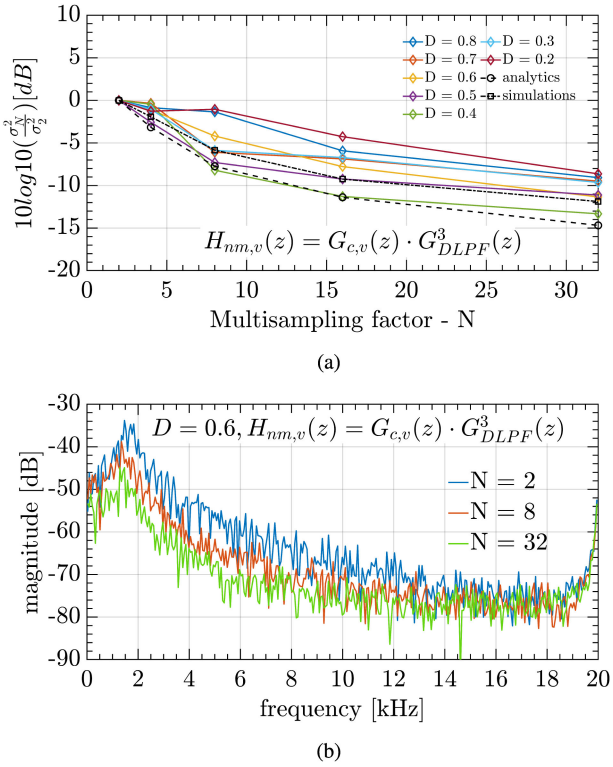

Fig. 11. Comparison between experiments, simulations, and analytics for the voltage loop with $G^3_{\mathrm{DLPF}}(z)$: (a) variance results and (b) spectral results.

When the $G_{\mathrm{DLPF}}(z)$ is introduced [see Fig. 10(b)], the noise power is improved, however, not significantly. The phase margins are equal to $\{20.1, 30.2, 37.8, 41.6, 43.4\}$ [deg] for $N = \{2, 4, 8, 16, 32\}$, respectively. The experimentally obtained variances, relative to $N = 2$ and averaged over the tested values of D, are equal to $\{3.37, 1.21, -0.482, -2.23\}$ [dB], for N starting from 4.

The experimental results show a good match with simulations, and are consistent with the change of operating point. A slightly higher mismatch in Fig. 10(a) can be seen for $D = 0.2$ and $N = 8$, and in Fig. 10(b) for $D = 0.2$ and $N > 4$ and $D = 0.8$ and $N = 8$. This is most likely due to the switching noise, which is unavoidably being sampled at those values of D and N [3].

In order to further test the suppression of the DPWM nonlinearity, a third-order $G^3_{\mathrm{DLPF}}(z)$ is added to the feedback. These results are shown in Fig. 11. The variance results in Fig. 11(a) show that the DPWM decimation is indeed suppressed by using filters with higher attenuation at $f > f_{\mathrm{pwm}}$, and the noise power keeps decreasing with the increase of N. The simulation results show a good match with the analytical prediction. For this control loop realization, phase margins are equal to $\{20.1, 19.7, 27.3, 31.1, 33\}$ [deg] for $N = \{2, 4, 8, 16, 32\}$, respectively. The experimentally obtained variances, relative to $N = 2$ and averaged over the tested values of D, are equal to $\{-0.97, -4.87, -7.44, -10.38\}$ [dB], for N starting from 4. Again, for higher values of N, the noise power is reduced by approximately -3 dB for each doubling of the N. A similar operating point dependency is seen as the one in cases without a DLPF and with the $G_{\mathrm{DLPF}}(z)$, supposedly due to the switching noise impact. The sensitivity to switching noise propagation depends on the values of N and D, and the impulse response of $H_{nm}(z)$. The switching noise is correlated to the feedback, and is, hence, out of the scope of this article. However, it should be noted that the voltage loop shows higher sensitivity to switching noise than the current loop. This sensitivity certainly rises due to the derivative action, as well as the higher relative magnitude of the switching noise, visible in Fig. 6. In Fig. 11(b), spectral plots are given to show the impact of MS-MU-PWM control on reducing the noise floor.

It is concluded that the MS-MU-PWM voltage control loops with PID controllers can offer high noise attenuation, however, not without a significant impact on the dynamic response. The filter $G^3_{\mathrm{DLPF}}(z)$ introduces nearly 16° of phase lag at $f_{c,v}$, which is close to using an MAF, where N latest feedback samples are averaged ($G_{\mathrm{MAF}}(z)$). Hence, feedback configuration with $G_{\mathrm{MAF}}(z)$ is tested as well, and the variance results are shown in Fig. 12. These experimental results show an excellent match with simulations and analytics, while being very consistent at all operating points. For this scenario, the phase margins are equal to $\{20.1, 23.1, 28.6, 31.4, 32.7\}$ [deg] for $N = \{2, 4, 8, 16, 32\}$, respectively. The experimentally obtained variances, relative to $N = 2$ and averaged over the tested values of D, are equal to $\{-3.9, -7.4, -10.5, -13.5\}$ [dB], for N starting from 4. Fig. 13 is given to compare the voltage spectra for all tested feedback configurations. For time-domain illustration, peaks of v_c are detected and plotted in Fig. 14 for $N = 2$ and $N = 32$ with the MAF, as extreme cases. The plot features relative values,

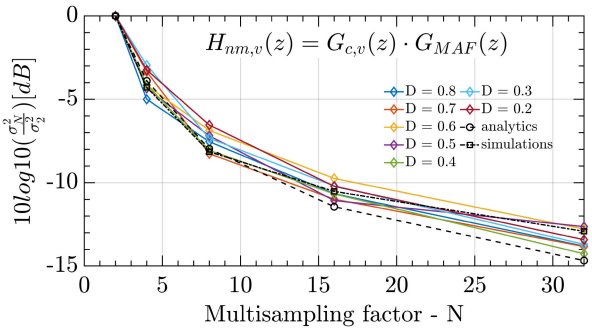

Fig. 12. Comparison between variances obtained through experiments, simulations, and analytics for the voltage loop with $G_{\text{MAF}}(z)$.

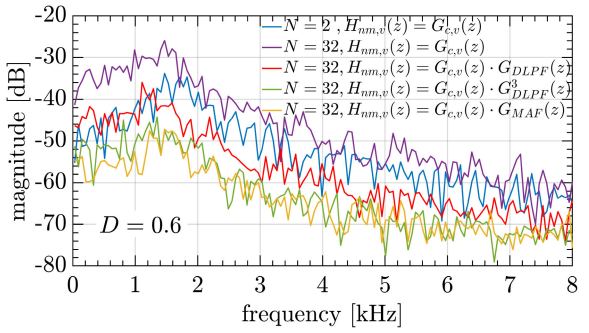

Fig. 13. Spectral results in frequency window for variance calculations for all tested feedback configurations of the voltage loop.

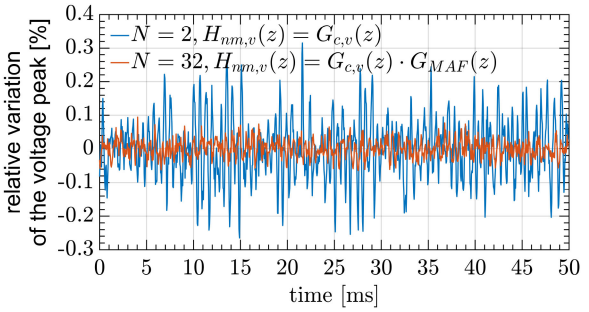

Fig. 14. Experimental results for time-domain noise impact illustration in voltage loops. The case featuring $N = 2$ is compared with the case featuring $N = 32$ and $G_{\text{MAF}}(z)$. The results show relative variation of detected voltage peak values.

obtained by subtracting the mean value of voltage peaks, and dividing by the dc value of v_c, for $D = 0.6$.

It is concluded that MS-MU-PWM voltage loops with PID controllers show higher sensitivity to variation of operating points, compared to the current loops with a PI controller, and high noise attenuation can only be achieved with a significant impact on the system dynamics [see Figs. 11 and 12]. For strong noise attenuation, it is highly recommended to use $G_{\text{MAF}}(z)$ instead of $G^3_{\text{DLPF}}(z)$ due to the higher noise attenuation, higher consistency across operating points, and a similar impact on the dynamic response. Furthermore, the MAF completely filters out the switching ripple, which removes the problems related to the modulating waveform discontinuity [3], [17]. If a strong noise attenuation is not required, it is still recommended to use antialiasing DLPFs, such as the $G_{\text{DLPF}}(z)$, in PID loops, as the dynamic improvements obtained by MS-MU-PWM are not notably deteriorated and the noise properties are significantly improved.

It should be noted that, as N is increased, even with the use of filters with high attenuation (such as MAFs), the dynamic properties are improved compared to the double-update without any filtering. The MS-MU-PWM impact on the dynamics and comparison with DS-DU-PWM and MS-DU-PWM methods is further analyzed in the following section.

VI. Comparison With DS-DU-PWM and MS-DU-PWM Methods

As FPGA platforms are not always available for digital control, noise attenuation is also analyzed for cases that can be implemented in DSPs. These methods belong to MS-SU-PWM or MS-DU-PWM groups, where the feedback is acquired with high sampling rate, and then averaged over T_{pwm} in a control routine that runs at single- or double-update rate [2], [24]. The analysis is performed for current loops. For all oversampled strategies, N is equal to 16.

In the following, five cases are compared in terms of dynamics and noise attenuation. Case A represents standard DS-DU-PWM control, which is used as a benchmark. The equivalent time delay introduced by digital controller and DPWM is equal to $T_{d,A} = \frac{3}{2}T_{s,A} = \frac{3}{4}T_{\text{pwm}}$. Case A is expected to have worst performance regarding noise propagation. Case B represents MS-DU-PWM control, as implemented in [2]. This kind of controller uses DMA module of the DSP in order to highly oversample the feedback signal and then average obtained samples over the switching period. Given that the phase response of an MAF over T_{pwm} is very close to pure delay of $\frac{1}{2}T_{\text{pwm}}$, the total time delay of case B is $T_{d,B} \approx \frac{3}{2}T_{s,B} + \frac{1}{2}T_{\text{pwm}} = \frac{5}{4}T_{\text{pwm}}$. Case B is expected to provide strong noise attenuation, with significantly reduced phase margin. Case C is the same as case B, without the calculational delay [24]. This is achieved in DSPs by averaging the feedback, and rescheduling the controller interrupt just before the instants where DPWM is equal to zero or to its maximum value. The equivalent time delay of case C is $T_{d,C} \approx \frac{1}{2}T_{s,C} + \frac{1}{2}T_{\text{pwm}} = \frac{3}{4}T_{\text{pwm}}$. Case C is expected to provide strong noise attenuation with similar dynamics as case A. Case D is MS-MU-DPWM control with the MAF in the feedback. The equivalent time delay of case D is $T_{d,D} = \frac{3}{2}T_{s,D} + \frac{1}{2}T_{\text{pwm}} = \frac{\frac{3}{N}+1}{2}T_{\text{pwm}}$. As noted, the results are always given for $N = 16$, however, it is interesting to point out that starting from $N = 6$ MS-MU-DPWM control with an MAF features less delay than double-update without the MAF. Case D is expected to provide strong noise attenuation with better phase margin compared to the cases mentioned above. Finally, case E represents the MS-MU-DPWM control with the $G_{\text{DLPF}}(z)$ in the feedback. This case is expected to provide strong noise attenuation and best dynamic performance.

For all strategies, the current controller features the same structure as in (7), but with gains changed compared to Section V-B. The remaining parameters of experimental setup are the same as in Section V. The summary of compared strategies and their parameters are shown in Table III.

TABLE III
CONTROL STRATEGIES TESTED IN SECTION VI

Description	label	value	unit
Controller configuration	$G_{c,i}$	PI	/
Relative proportional gain	$\frac{V_{in}}{R} k_{p,i}$	0.3064	/
Relative integral gain	$\frac{V_{in}}{R} k_{i,i}$	366	$\frac{1}{s}$
Crossover frequency	$f_{c,i}$	1900	Hz
DS-DU-PWM group			
case A	label	value	unit
Filter configuration	/	/	/
Phase margin	PM	58.2	deg
MS-DU-PWM group - $N = 16$			
case B	label	value	unit
Filter configuration	$G_{MAF}(z)$	/	/
Phase margin	PM	41.4	deg
case C	label	value	unit
Filter configuration	$G_{MAF}(z)$	/	/
Phase margin	PM	58.6	deg
MS-MU-PWM group - $N = 16$			
case D	label	value	unit
Filter configuration	$G_{MAF}(z)$	/	/
Phase margin	PM	65.1	deg
case E	label	value	unit
Filter configuration	$G_{DLPF}(z)$	/	/
Phase margin	PM	75.6	deg

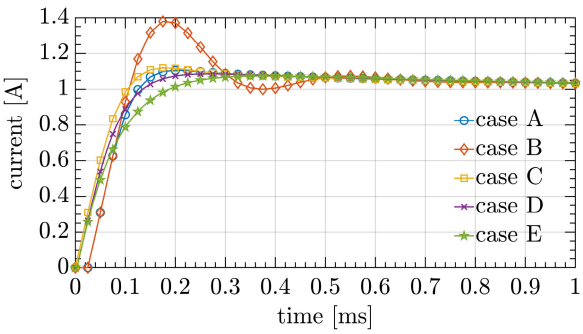

Fig. 15. Step responses of discrete closed-loop transfer functions corresponding to strategies tested in Section IV.

For illustration of dynamic properties, step responses obtained using closed-loop discrete-time transfer functions, are given in Fig. 15.

The noise power attenuation, relative to case A, is shown in Fig. 16. As consistency of the results for different operating points is demonstrated in Section V-B, noise attenuation is shown just for one duty cycle, $D = 0.45$.

From Fig. 16, it can be seen that all examined strategies that use multisampling and digital filtering result in a strong noise

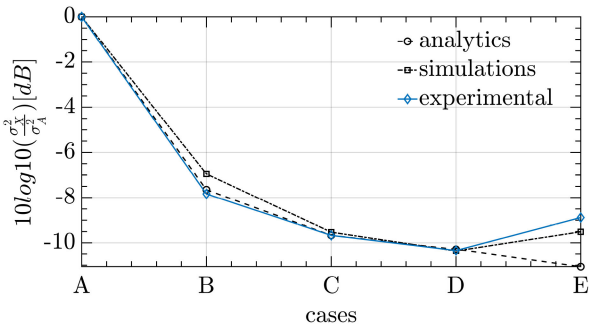

Fig. 16. Comparison of noise attenuation (variances) for strategies tested in Section IV. The results are given for $D = 0.45$.

attenuation, compared to DS-DU-PWM. The attenuation values are consistent with results in Fig. 8(a) ($N = 16$ compared to $N = 2$). The difference between cases B and C is due to a higher phase margin in case C, which results in a higher attenuation provided by $H_n(z)$ in (4). As expected, results between cases C and D are very similar as the same digital MAF is used and the only difference is the update frequency of $m_s[k]$. Finally, case E shows nearly the same noise attenuation as cases C and D, while the dynamic properties are significantly improved. This is a confirmation that, in order to have a high noise attenuation in current loops, MS-MU-PWM control with the antialiasing $G_{\text{DLPF}}(z)$ is a good choice.

VII. CONCLUSION

This article has shown that MS-MU-PWM control loops can offer high noise attenuation in the control bandwidth, with improved dynamic properties compared to DS-DU-PWM and MS-DU-PWM. In order to do so, some digital filtration above f_{pwm} is required to suppress the decimation effect caused by the DPWM. After suppressing the DPWM decimation, experimental and simulation results show a good match with the analytical modeling. For control loops that use PI controllers, high noise attenuation is achieved with antialiasing digital filters that do not significantly impair the dynamic properties. Without any digital filters, noise attenuation remains nearly constant as N is increased above 2. For control loops with PID controllers, strong noise reduction is achieved with the use of digital filters that provide a greater high-frequency attenuation. Without any digital filters, the noise power is increased when N is raised above 2.

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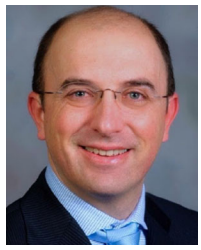

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