Letters

Fault Current Bypass-Based LVDC Solid-State Circuit Breakers

Reza Kheirollahi, *Student Member, IEEE*, Shuyan Zhao, *Student Member, IEEE*, and Fei Lu, *Member, IEEE*

***Abstract*—This letter presents a new low-voltage direct-current fault current bypass-based solid-state circuit breaker (SSCB) using silicon-carbide MOSFETs. The proposed SSCB provides the possibility to select the clamping voltage of metal–oxide varistors (MOVs) close to the nominal voltage of the dc system. This reduces voltage overshoots across the main switch and snubber components and extends the maximum allowable dc bus voltage on the SSCB. The MOVs are removed from the power line, and their leakage currents are completely eliminated. The clamping voltage of the MOV and its surge energy rating is considered to optimize the MOV. The *dv/dt* across the main switch is controlled by an auxiliary capacitor, where a design procedure is presented to optimize its value. Also, the stored inductive energy of the line inductor in dc systems is bypassed using an auxiliary branch and prevented from flowing through the faulty section to enhance the safety. LTspice simulations are presented to show the significance of the proposed SSCB. The experiments of 375 V/170 A/2.4 μs and 600 V/163 A/2.4 μs verify the effectiveness of the proposed design in practice.**

***Index Terms*—DC circuit breaker, fault current bypass, low-voltage direct-current (LVDC), solid-state circuit breaker (SSCB).**

I. Introduction

SOLID-STATE circuit breakers (SSCBs) have been witnessing impressive progress with the aid of wide bandgap devices, such as silicon-carbide (SiC) MOSFETs [1], [2]. Along with obtaining high efficiency as the result of low ON-state resistance, the response time has been gaining remarkable achievements in the microseconds range [3], [4]. Not only that, but the reported successes in control and gate drivers design [5] and incorporating fault detection/location techniques in SSCBs are highly promising as well [6], [7]. SSCBs have been reviewed in depth during recent years [8].

Energy absorbing elements, such as metal–oxide varistors (MOVs), are mostly used in combination with the solid-state switches in dc SSCBs [9], [10]. First, the lack of a zero-crossing point in dc systems leads to high-voltage oscillations and overshoot during the dc current interruption [8]. Second, the capacity of the semiconductor devices in dissipating the inductive energy of the line inductance is limited [11]. Therefore, MOVs are used to absorb the energy and clamp the voltage across the SSCBs during the dc current breaking.

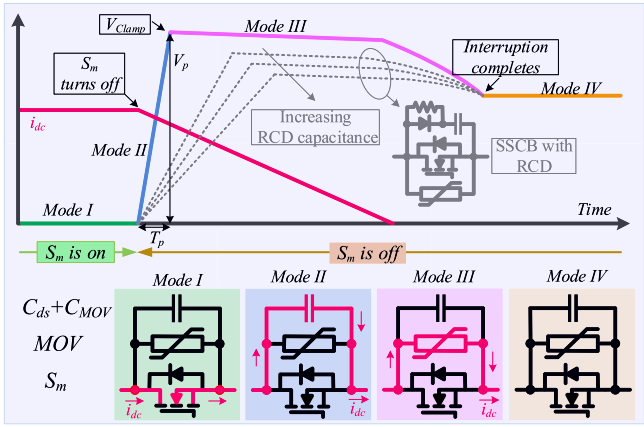

Fig. 1. SSCBs with MOV, and voltage and current waveforms in the top and operating modes in the bottom. SSCB, including RCD, is shown in gray color.

Fig. 1 indicates the conventional SSCB with MOV [2]. Four modes of operation during turn-OFF are represented along with the current and voltage waveforms. $C_{\rm ds}$+$C_{\rm MOV}$ stands for the drain–source and MOV parasitic capacitances, and S_m shows the main switch. As illustrated, the current quickly commutates to the parasitic capacitances at the end of mode *I*, and the voltage across the SSCB rises to V_p in T_p interval depending on $C_{\rm ds}$+$C_{\rm MOV}$ and the dc current values. The V_p is limited to the maximum clamping voltage of the MOV ($V_{\rm Clamp}$). High V_p/T_p induces voltage oscillations on the gate of the switch and leads to a spurious turn-ON. During mode III, the current commutates to the MOV, and the interruption completes at the end of this mode.

Capacitor-diode [12], resistor-capacitor (*RC*) [13], and resistor-capacitor-diode (RCD) [14] snubbers are also used in combination with MOVs to reduce V_p/T_p in SSCBs. RCD snubbers benefit from low oscillations, low clamping voltages, and small V_p/T_p [8], and their capabilities in interrupting kiloampere dc currents have been proved [15]. The circuit diagram and the resulted voltage waveforms for different capacitance values are indicated in gray color in Fig. 1. Although the RCD network includes more components, it helps to increase the turn-OFF capability of voltage and current for SSCBs.

Manuscript received April 8, 2021; revised May 7, 2021 and June 8, 2021; accepted June 21, 2021. Date of publication June 25, 2021; date of current version September 16, 2021. This work was supported by the Advanced Research Projects Agency-Energy, U.S. Department of Energy, under Award No. DE-AR0001114 in the BREAKERS Program monitored by Dr. Isik Kizilyalli *(Corresponding author: Fei Lu.)*

The authors are with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA 19104 USA (e-mail: reza.kheirollahi@drexel.edu; shuyan.zhao@drexel.edu; fei.lu@drexel.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3092695.

Digital Object Identifier 10.1109/TPEL.2021.3092695

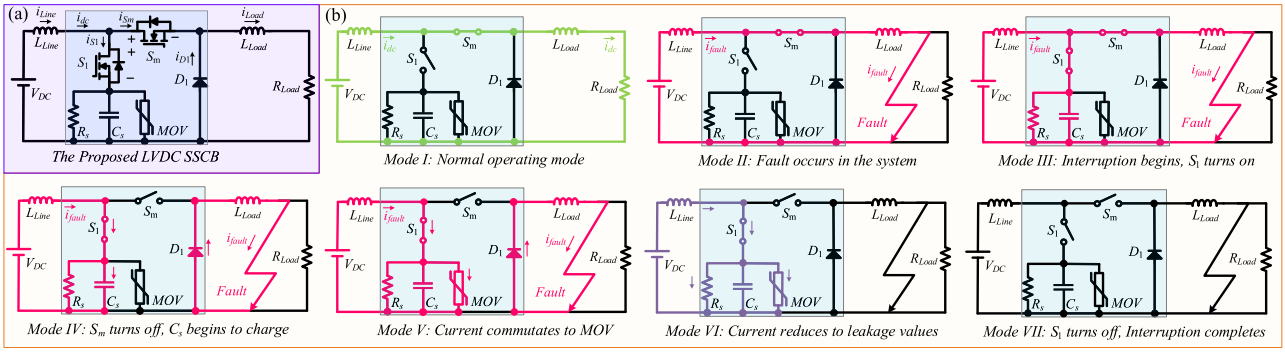

Fig. 2. Proposed LVdc fault current bypass-based SSCB. (a) Proposed SSCB in a typical dc system, including the line inductor L_{Line} and load-side components (L_{Load} and R_{Load}). (b) Proposed SSCB operating modes during the dc current interruption.

Applying MOV-RCD snubbers to SSCBs is practical; however, there are two main issues. First, to minimize the MOVs leakage current during the OFF-state, and the clamping voltage of the MOV places between 1.5 and 2.5 times of the nominal voltage [8]. This imposes higher operating voltage obligations on the solid-state switch and the RCD capacitor. Using residual current mechanical disconnectors [16] is useful to optimize the MOV and avoid leakage currents; however, it affects the SSCB operating speed during the reclosing process. Second, the stored inductive energy of the line inductor in dc systems needs to flow through the faulty section. That is, regarding Fig. 1, although the switch is OFF in mode III, the MOV conducts the fault current until it decays to zero.

Fig. 2(a) shows the proposed SSCB in a typical dc system where connections to both lines are required [17], [18]. The presented SSCB is supposed to be placed at the load side, where current limiting line inductors are employed to reduce the rate of rise of the fault current. In this letter, 63 μH line inductor is used, which is enough to limit the rate of rise of fault current to 10 A/μs under the dc bus voltage up to 600 V.

II. Proposed Low-Voltage Direct-Current (LVDC) SSCB

Regarding Fig. 2(a), there are five contributions.

1) The MOV is removed from the power line and the main switch; the MOVs leakage current is eliminated.
2) V_p/T_p is controlled by optimizing the value of C_s (100 s of nanofarad); there is no oscillation voltage across or on the gate of the main switch S_m.
3) S_1 turns OFF at almost zero current; no oscillations appear on S_1 during the current interruption.
4) During the current interruption, the stored inductive energy of the line inductor is bypassed using an auxiliary branch, and it is not allowed to flow through the faulty section that increases the safety.
5) The maximum allowable dc bus voltage on the SSCB is extended.

Although the focus of this letter is proposing a new LVdc topology, the fault detection mechanism is of great importance in the breaker operation, and the fault current detection time interval must be included in calculating the total response time of interrupting the fault current.

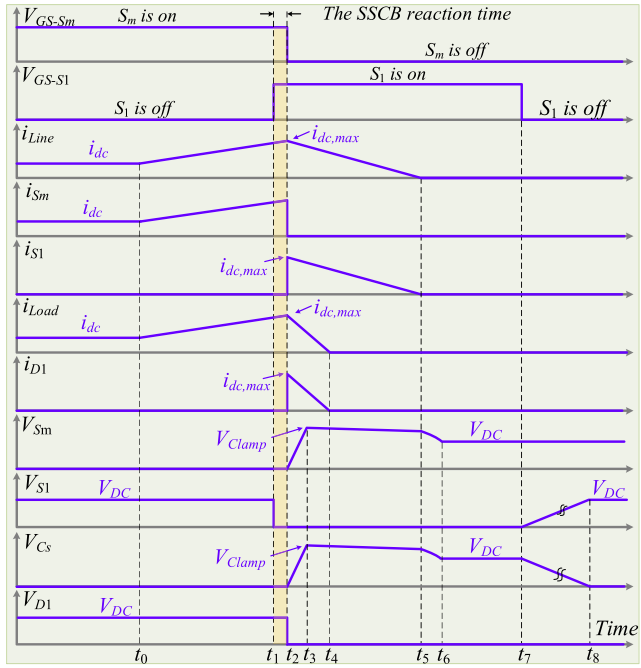

Fig. 3. Proposed SSCBs electrical waveforms during dc current breaking.

A. Working Principle and Operating Modes

Figs. 2(b) and 3 represent the operating modes and the electrical waveforms of the proposed SSCB in interrupting dc current, respectively. Also, Fig. 4 shows the flowchart of the proposed current interruption process.

Mode I (*Before* t_0): SSCB operates at normal condition. The main switch S_m conducts the current, meaning $i_{\mathrm{Line}} = i_{\mathrm{Load}} = i_{\mathrm{dc}}$. S_1 and D_1 are OFF, so $i_{S1} = i_{D1} = 0$ and $V_{S1} = V_{D1} = V_{\mathrm{DC}}$.

Mode II ($t_0 \leq t < t_1$): Fault occurs in the system at $t = t_0$.

Mode III ($t_1 \leq t < t_2$): The fault is detected at $t = t_1$. S_1 turns ON, but the fault current cannot commutate to S_1. That is, after turning S_1 ON (while S_m is still ON), the fault current (i_{fault}) does not reduce to zero in S_m in this mode.

Mode IV ($t_2 \leq t < t_3$): S_m turns OFF ($i_{Sm} = 0$) at $t = t_2$; the fault current commutates to S_1 ($i_{\mathrm{Line}} = i_{S1}$), and V_{Cs} begins to

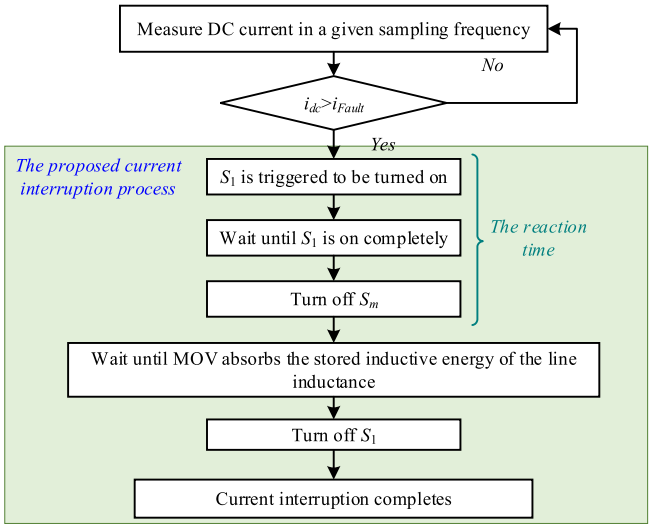

Fig. 4. Proposed current interruption process.

increase; D_1 turns ON to conduct the load current ($i_{\text{Load}} = i_{D1}$). In this case, $V_{Sm} = V_{Cs}$ till S_1 is ON.

Mode V ($t_3 \le t \le t_6$): V_{Cs} is clamped by the MOV at $t = t_3$ ($V_{Cs} = V_{\text{Clamp}}$), and the fault current commutates to the MOV ($i_{\text{Line}} = i_{S1} = i_{\text{MOV}}$); the load current decays to zero at $t = t_4$ ($i_{D1} = i_{\text{Load}} = 0$); at $t = t_5$, the line current reduces to the MOV leakage current ($i_{S1} = i_{\text{Line}} = i_{\text{MOV-Leakage}}$), and the voltage across the MOV starts to return to the nominal voltage; finally, $V_{Cs} = V_{Sm} = V_{\text{DC}}$ at $t = t_6$.

Mode VI ($t_6 < t < t_7$): There is a leakage current in the system due to the MOV operation ($i_{S1} = i_{\text{Line}} = i_{\text{MOV-Leakage}}$).

Mode VII ($t_7 \le t \le t_8$): S_1 turns OFF to eliminate the MOVs leakage current ($i_{S1} = i_{\text{Line}} = 0$) at $t = t_7$. As the resistance value across S_1 at the OFF-state (MΩ range) is much higher than the resistance value of R_s (kΩ range), V_{DC} places across S_1 gradually. At $t = t_8$, $V_{S1} = V_{\text{DC}}$ and $V_{CS} = 0$; then, the interruption completes.

The reaction time interval of the SSCB is defined as t_2-t_1; however, it also includes the transients of gate signals in practice. It should be noted that the reaction time interval is calculated from the detection of the fault ($t = t_1$) to the instant the fault current begins to reduce at the load side ($t = t_2$). This definition excludes the conduction time interval of the MOV that follows the same definition in [19].

B. C_s Design Procedure

With respect to Fig. 1, C_s design objective is minimizing V_p/T_p. According to Section II-A, V_p is determined based on V_{Clamp}. So, C_s is selected optimally to optimize T_p. Based on Fig. 3, $T_p = t_3 - t_2$. At $t = t_2$, the following equation can be developed in the loop of V_{DC}-L_{Line}-S_1-V_{Cs}:

$$R_e i_{Cs}(t) + L_{\text{Line}} \frac{di_{Cs}(t)}{dt} + V_{Cs}(t) = V_{\text{DC}} \tag{1}$$

where R_e is the parasitic resistance of the V_{DC}-L_{Line}-S_1-V_{Cs} loop. Considering (1), $V_{Cs}(t)$ can be described by the following differential equation:

$$\frac{d^2V_{Cs}(t)}{dt^2} + \frac{R_e}{L_{\text{Line}}}\frac{dV_{Cs}(t)}{dt} + \frac{1}{L_{\text{Line}}C_s}V_{Cs}(t) = \frac{V_{\text{DC}}}{L_{\text{Line}}C_s} \tag{2}$$

where the initial conditions for $V_{Cs}(t)$ are defined as follows:

$$V_{Cs}(0^+) = 0, \quad i_{Cs}(0^+) = i_{\text{dc,max}} \rightarrow \frac{dV_{Cs}(0^+)}{dt} = \frac{i_{\text{dc,max}}}{C_s}. \tag{3}$$

In (3), $i_{\text{dc,max}}$ is the maximum dc current value aimed to be interrupted. Regarding (2) and (3)

$$V_{Cs}(t) = V_{\text{DC}} + e^{-\alpha t}\left(\left(\frac{i_{\text{dc,max}}}{C_s} + \alpha V_{\text{DC}}\right)\frac{\sin(\omega_d t)}{\omega_d} - V_{\text{DC}}\cos(\omega_d t)\right) \tag{4}$$

where ω_d and α are defined as follows:

$$\alpha = R_e/2L_{\text{Line}}, \quad \omega_0 = 1/\sqrt{L_{\text{Line}}C_s}, \quad \omega_d = \sqrt{|\alpha^2 - \omega_0{}^2|}. \tag{5}$$

For a given value of C_s, T_p is the time instant in which $V_{Cs}(T_p) = V_{\text{Clamp}}$; that is

$$V_{\text{Clamp}} = V_{\text{DC}} + e^{-\alpha T_p}\left(\left(\frac{i_{\text{dc,max}}}{C_s} + \alpha V_{\text{DC}}\right)\frac{\sin(\omega_d T_p)}{\omega_d} - V_{\text{DC}}\cos(\omega_d T_p)\right). \tag{6}$$

Solving (6) leads to a complex statement. To simply find T_p, the following approximations can be made as T_p places in microseconds range:

$$e^{-\alpha T_p} \approx 1, \quad \sin(\omega_d T_p) \approx \omega_d T_p, \quad \cos(\omega_d T_p) \approx 1, \quad \frac{i_{\text{dc,max}}}{C_s} \gg \alpha V_{\text{DC}}. \tag{7}$$

In this case, (6) can be simplified and rewritten as the following to find the optimized value of C_s based on a desired T_p:

$$C_s \approx T_p i_{\text{dc,max}}/V_{\text{Clamp}}. \tag{8}$$

C. MOV Design Procedure

There are four parameters that are of importance in selecting the MOV. They are as follows:

1) V_{Clamp};
2) the allowable continuous dc voltage on the MOV ($V_{\text{DC,MOV}}$);
3) the surge energy rating of the MOV (E_r);
4) the surge current capability (i_{Peak}).

Since reducing V_{Clamp} helps to decrease the voltage overshoots across the SSCBs and enhance the compactness, minimizing V_{Clamp} is the design objective. However, according to the working principle of the proposed SSCB, as explained in Section II-A, two design criteria are considered in selecting the optimal MOV.

1) According to Fig. 3, the time interval of $t_3 \le t < t_5$ is regarded as the fault current extinguishing time ($T_{\text{ET}} = t_5 - t_3$) in which the MOV conducts the current and clamps

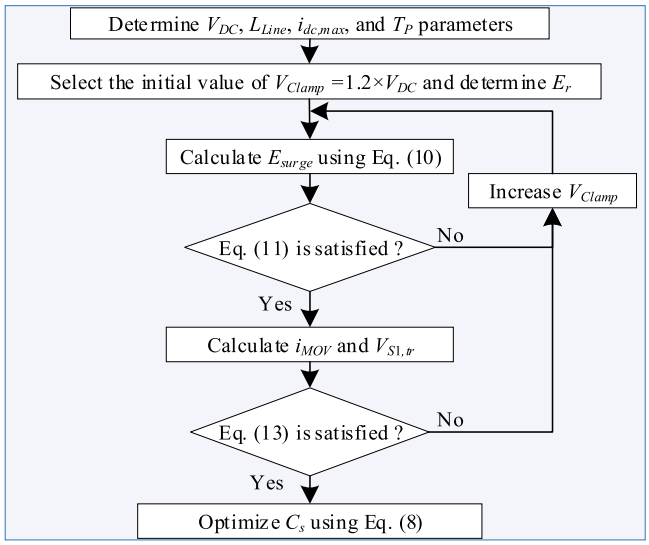

Fig. 5. Design procedure to select the optimized values of Cs and V_{Clamp}.

the voltage on S_m and C_s. The following equation approximates the MOV current in this interval:

$$i_{\mathrm{dc}}(t) = i_{\mathrm{dc,max}} - \frac{V_{\mathrm{MOV}} - V_{\mathrm{DC}}}{L_{\mathrm{Line}}}(t - t_3) \tag{9}$$

where V_{MOV} is the transient voltage across the MOV that limits to V_{Clamp}. With respect to (9), T_{ET} depends on four factors, including $i_{\mathrm{dc,max}}$, L_{Line}, V_{DC}, and V_{Clamp}. The surge energy on the MOV during T_{ET} can be calculated as follows:

$$E_{\mathrm{surge}} = \int_{t_3}^{t_5} V_{\mathrm{MOV}} i_{\mathrm{dc}} dt. \tag{10}$$

This surge energy should not exceed the E_r in the MOV; therefore, the selected MOV needs to satisfy the following:

$$E_{\mathrm{surge}} < E_r. \tag{11}$$

2) With respect to the working principle in Section II-A and Fig. 3, at $t = t_7$, the auxiliary switch S_1 turns OFF to remove the MOV leakage current (i_{MOV}) in the system. Regarding the value of L_{Line}, the di/dt voltage across S_1 in interrupting i_{MOV} is

$$V_{S1,tr} = L_{\mathrm{Line}}(di_{\mathrm{MOV}}/dt). \tag{12}$$

In (12), C_s discharge current on the auxiliary resistor R_s has been neglected. Regarding (12), V_{Clamp} should be selected in a way that

$$V_{S1,tr} \leq V_{\mathrm{Clamp}} - V_{\mathrm{DC}}. \tag{13}$$

Therefore, (11) and (13) are used to optimize the MOV in the proposed SSCB. Fig. 5 summarizes the presented design procedures of C_s and the MOV.

III. Simulation Results

To show the significance of the MOV optimization, simulations are conducted in LTspice. Table I includes the optimized components of the MOV-RCD-based SSCB and the proposed SSCB with two sets of different parameters.

TABLE I
Simulation Parameters of MOV-RCD-Based SSCB and the Proposed SSCB Design #1 and Design #2

Parameter	MOV-RCD based SSCB	Proposed SSCB design #1	Proposed SSCB design #2
V_{DC}	375V	375V	800V
L_{Line}	40μH	40μH	80μH
R_{Load}	2.34Ω	2.34Ω	5Ω
MOV	V321DB40	V251DB40	V421DA40
$V_{DC,MOV}$	420V	330V	560V
V_{Clamp}	830V	650V	1130V
C_s	500nF	600nF	550nF
R_s	200Ω	6.8kΩ	10k
S_m	C3M0016120D 1200V/115A $i_{Ss,pulse}$(1)=250A	C3M0015065D 650V/120A $i_{Ss,pulse}$=418A	C3M0016120D 1200V/115A $i_{Ss,pulse}$=250A

(1) $i_{Ss,\mathrm{pulse}}$ refers to the pulse current capability in the SiC MOSFETs.

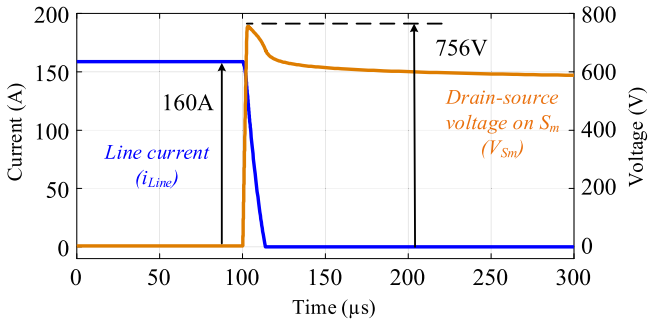

Fig. 6. LTspice simulation results of the MOV-RCD-based SSCB.

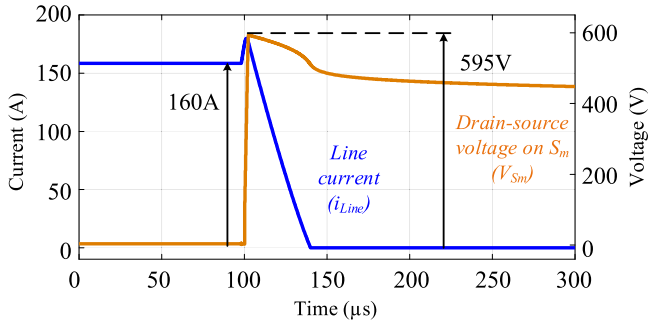

Fig. 7. LTspice simulation results of the proposed SSCB design #1.

Considering the simulation results, as shown in Figs. 6–8.

1) Regarding Figs. 6 and 7: For the same dc bus voltage of 375 V, the voltage overshoot is 756 V for the MOV-RCD-based SSCB, while this value is 595 V for the proposed SSCB. The voltage peak reduction provides the possibility to use SiC MOSFETs with lower voltage rating in the main switch and reduce the design cost when SiC MOSFETs are connected in parallel to achieve high efficiency.
2) Regarding Figs. 6 and 8: For the same 1.2 kV SiC MOSFETs, the proposed SSCB can operate well under the dc bus voltage up to 800 V, which is attractive for industrial applications.

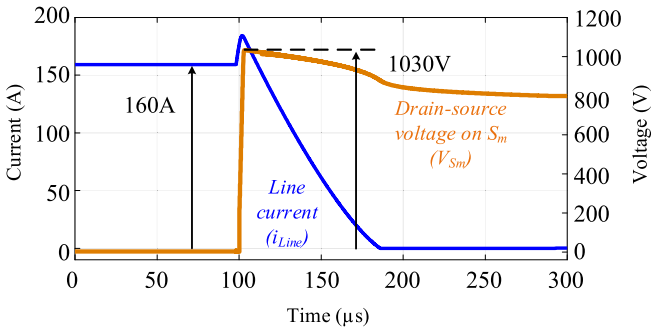

Fig. 8. LTspice simulation results of the proposed SSCB design #2.

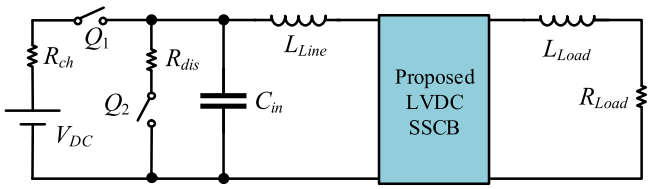

Fig. 9. DC test circuit.

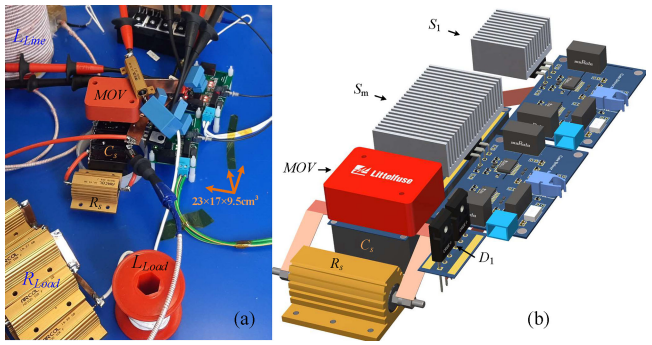

Fig. 10. Proposed SSCB. (a) Implemented design. (b) Three-dimensional design view.

IV. Experimental Validation

In this section, the experimental results of 375 V/170 A/2.4 μs and 600 V/163 A/2.4 μs are presented to validate three significant points.

1) The working principle and operating modes of Section II.
2) The proposed SSCB can work correctly in different voltage levels (below the clamping voltage of the MOV with a safe margin) with the same components.
3) Selecting MOVs with the voltage ratings below the nominal voltage of the dc system does not lead to leakage currents while reducing the voltage overshoots during the dc current interruption.

Fig. 9 indicates the dc test circuit. Switch Q_1 and resistor $R_{\rm ch}$ are the charge circuits, and switch Q_2 and resistor $R_{\rm dis}$ are the discharge circuits. SSCB turns ON for a given interval, and when the dc current in the system reaches a test value, SSCB is triggered to be turned OFF.

Fig. 10 displays the implemented SSCB and the three-dimensional design view. Table I presents the selected semiconductor devices and the components' values. The MOV voltage rating ($V_{\rm DC,MOV}$) is 420 V with the maximum clamping voltage ($V_{\rm Clamp}$) of 830 V. The power density of the hardware setup is 70.6 kW/dm^3 with the continuous load current of 30 A in S_m under the dc bus voltage of 600 V.

In designing the gate driver circuits, external gate–source capacitors, gate resistors, and ferrite beads have been included, as their values are listed in Table II. Although the added gate components slow down the falling and rising of the gate signals, they are effective to eliminate the voltage oscillations on the gate of the SiC MOSFETs and prevent the spurious turn-ON during the dc current interruption.

TABLE II
DC System and SSCB Parameters Values

Parameter	Design Value	Parameter	Design Value
V_{DC}	375V(600V)	L_{Line}	63μH
L_{Load} (R_{Load})	14μH (1.5Ω)	S_m *and* S_1	C3M0016120D
D_1	C4D20120D	C_S	500nF
MOV	V321DB40	R_s	6.8kΩ
$C_{GS}^{(1)}$ *on* S_m	10nF	C_{GS} *on* S_1	15.3nF
Gate resistance	7.5Ω	*Gate FB*$^{(2)}$	30Ω

(1) Gate–source capacitor, (2) Gate ferrite bead (impedance in 100 MHz).

A. Experiments of 375 V/170 A/2.4 μs

Fig. 11 shows the experimental results of 375 V/170 A with the S_m drain–source voltage (V_{Sm}) and the line inductor $L_{\rm Line}$ current ($i_{\rm Line}$) waveforms in the top and the gate–source voltages and load current ($i_{\rm Load}$) waveforms in the bottom. To compensate the leakage inductance in the main switch S_m, an *RC* snubber ($R = 1\,\Omega$ and $C = 100$ nF) has been connected to the drain–source terminals of S_m.

As illustrated in Fig. 11, the main switch S_m turns ON for 65 μs, and when the dc current reaches about 160 A, the current interruption begins by turning S_1 ON. After a safe delay ($\approx$2 μs), S_m is triggered to be turned OFF. S_m turns OFF completely after 400 ns, and the dc current is interrupted in the main switch after 2.4 μs. Next, the current commutates to S_1 and charges C_s. The V_{Cs} ($= V_{Sm}$) rises to 799 V in 2.7 μs, which is close to the expected value of (8) (2.5 μs considering $C_s = 500$ nF, $V_{\rm clamp} = 799$ V, and $i_{\rm dc,max} = 160$ A). The peak of the current in the S_1 reaches 170 A, and it reduces to leakage values in 37 μs.

S_1 turns OFF after 250 μs. This interval is determined considering the fault current extinguishing time interval ($T_{\rm ET}$) that depends on $i_{\rm dc,max}$, $L_{\rm Line}$, $V_{\rm DC}$, and $V_{\rm Clamp}$ factors. As S_1 turns OFF, it holds the $V_{\rm DC}$ in the auxiliary branch. Also, the current in the load side begins to decrease after S_m turns OFF, reducing to zero in 55 μs.

According to the gate–source voltage waveforms in Fig. 11, it is concluded that no voltage oscillations appear on the gate terminals during the dc current breaking, which facilitates the full utilization of the electrical ratings of SiC MOSFETs in practice. The *dv/dt* across S_m is controlled using the correct selection of C_s. Also, the stored inductive energy of $L_{\rm Line}$ is prevented to flow through the faulty section after S_m turns OFF.

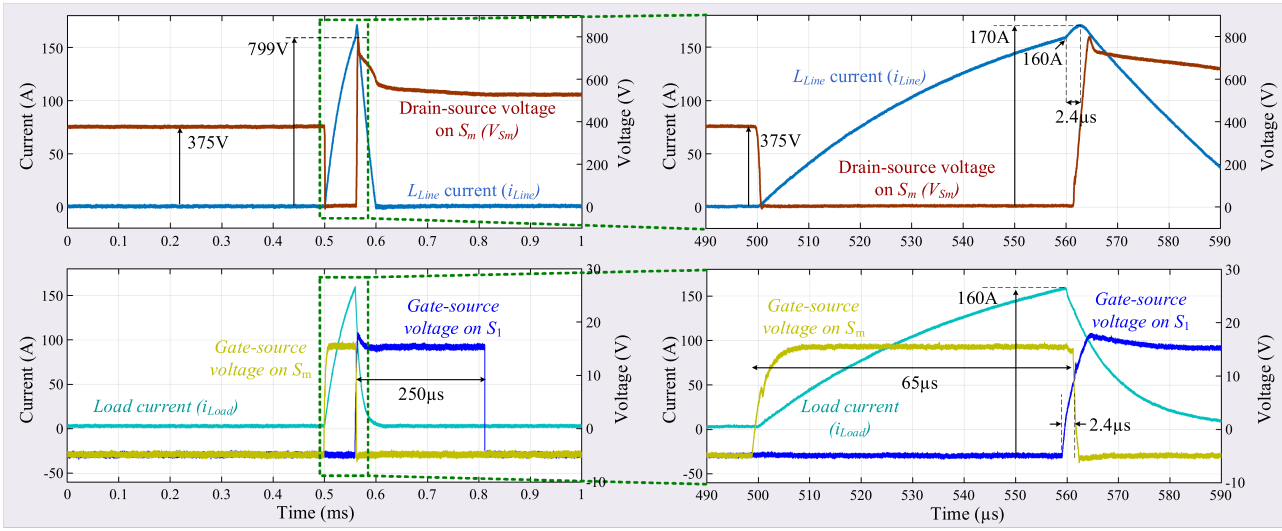

Fig. 11. Experimental results: 375 V/170 A/2.4 μs dc current interruption test. The top figure includes the drain–source voltage across the main switch (V_{Sm}) and line inductor L_{Line} current (i_{Line}). The bottom figure involves the gate–source voltage on S_m and S_1 and also the load current (i_{Load}).

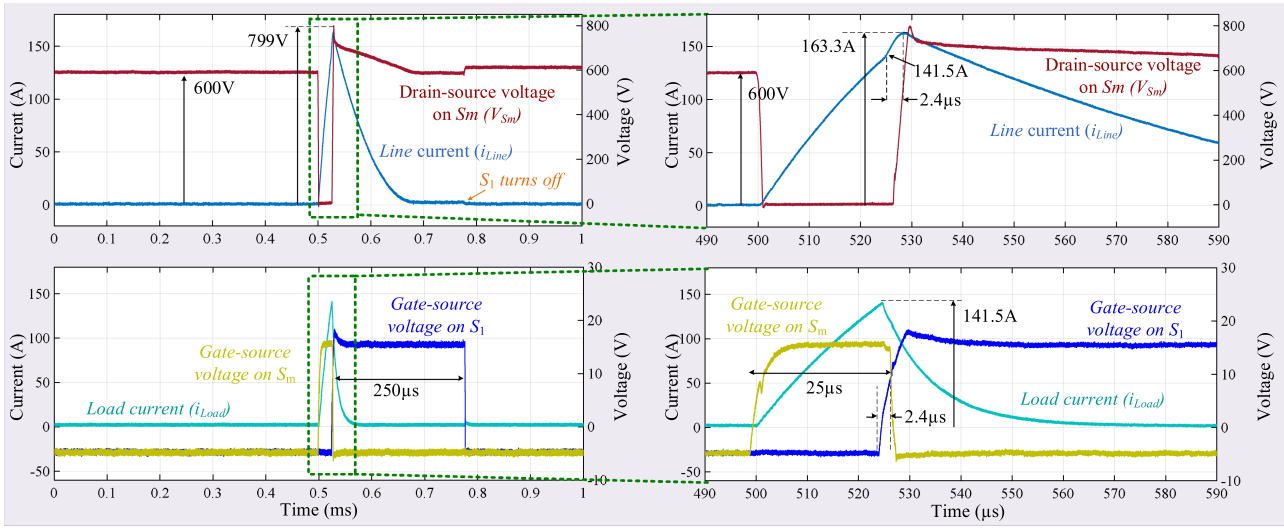

Fig. 12. Experimental results: 600 V/163 A/2.4 μs dc current interruption test. The top figure includes the drain–source voltage across the main switch (V_{Sm}) and line inductor L_{Line} current (i_{Line}). The bottom figure involves the gate–source voltage on S_m and S_1 and also the load current (i_{Load}).

B. Experiments of 600 V/163 A/2.4 μs

The designed SSCB of Fig. 10 is tested in a 600 V dc system with the same components. The resulted waveforms are represented in Fig. 12. S_m turns ON for 25 μs, and when the value of the dc current reaches around 141.5 A, S_1 turns ON. With the time sequence, as presented in Section II-A and the flowchart of Fig. 4, S_m turns OFF completely after 2.4 μs, showing the same reaction time.

The current in S_1 gets the peak value of 163.3 A, and it reduces to 2.3 A ($= i_{S1}$) in 177 μs where the current share of resistor R_s ($= 6.8$ kΩ) is 88 mA, and the remaining 2.212 A flows through the MOV as the leakage current. Also, the current at the load side decays to zero in 55 μs after S_m turns OFF. The maximum voltage across C_s ($V_{Cs} = V_{Sm}$) reaches 799 V (V_{Clamp}) in 3 μs (T_p). As indicated in Fig. 12, S_1 turns OFF after 250 μs, and the leakage current in the auxiliary branch ($= i_{S1}$) reduces to zero.

In addition to the advantages of the proposed SSCB, as explained in Section III-A, the experimental results in the 600 V dc system show that MOVs with the dc ratings below the nominal voltage of the dc system can be used to achieve lower clamping voltage. In this case, the voltage overshoot across the main switch is decreased, and the V_p/T_p is reduced. Besides, the designed SSCB has the capability to be adjusted for different voltage and current ratings, which is highly beneficial in industrial applications.

C. Significance of the Proposed SSCB

The proposed topology can bypass the stored inductive energy of the line inductor during the dc current interruption, and it will not flow through the main switch and the faulty sections. This

TABLE III
COMPARATIVE STUDY

SSCBs	MOV-RCD [14]	MOV-RCD [14] with the residual current disconnector [16]	Proposed SSCB
# Solid-state switch	1	1	2
# Mechanical switch	0	1	0
# Diode	1	1	1
# Resistor	1	1	1
# Capacitor	1	1	1
# MOV	1	1	1
MOV leakage issue	Yes	No	No
Reclosing speed	Fast	Slow	Fast
Fault current bypass	No	No	Yes

achievement enhances the safety in the dc system. Also, MOV optimization brings three important advantages:

1) reducing the voltage overshoots;
2) extending the allowable dc bus voltage on the MOV;
3) addressing the MOV failure during the degradation stage.

The practicality of the proposed SSCB has been verified by experiments in two different dc bus voltages.

Table III presents a comparative study. Compared with the MOV-RCD-based SSCBs [14], the proposed SSCB includes one more solid-state switch; however, it offers the following:

1) addressing the MOV leakage current;
2) obtaining the chance to extend the maximum allowable dc bus voltage on the breaker;
3) bypassing the fault current.

Compared with the MOV-RCD-based SSCB [14] with the residual current disconnector [16], the number of the switches is the same; on the other hand, the proposed SSCB presents the fast reclosing process and bypassing the fault current.

V. CONCLUSION

A new SSCB was developed in this letter for LVdc applications. The advantages of the presented SSCB are as follows

1) The oscillation voltages on the solid-state switches are removed.
2) The MOVs leakage currents are eliminated.
3) The voltage overshoot across the SSCB is reduced.
4) The auxiliary switch turns OFF at currents close to zero.
5) The tail of the fault current is bypassed and prevented to flow through faulty sections to enhance the safety.
6) The SSCB can operate correctly in dc systems with different voltage levels.

The correctness of the proposed SSCB has been verified with the experiments of 375 V/170 A/2.4 μs and 600 V/163 A/2.4 μs.

ACKNOWLEDGMENT

The views and opinions of the authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

REFERENCES

[1] X. Song, C. Peng, and A. Q. Huang, "A medium-voltage hybrid dc circuit breaker—Part I: Solid-state main breaker based on 15 kV SiC emitter turn-off thyristor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 278–288, Mar. 2017.

[2] D. Marroquí, J. M. Blanes, A. Garrigós, and R. Gutiérrez, "Self-powered 380 V DC SiC solid-state circuit breaker and fault current limiter," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9600–9608, Oct. 2019.

[3] Z. J. Shen, "Ultrafast solid-state circuit breakers: Protecting converter-based ac and dc microgrids against short circuit faults," *IEEE Electrific. Mag.*, vol. 4, no. 2, pp. 72–80, Jun. 2016.

[4] U. Mehrotra, B. Ballard, T.-H. Cheng, B. J. Baliga, S. Bhattacharya, and D. C. Hopkins, "Optimized highly efficient SSCB using organic substrate packaging for electric vehicle applications," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, Chicago, IL, USA, 2020, pp. 128–133.

[5] Y. Ren, X. Yang, F. Zhang, F. Wang, L. M. Tolbert, and Y. Pei, "A single gate driver based solid-state circuit breaker using series connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2002–2006, Mar. 2019.

[6] D. He, Z. Shuai, Z. Lei, W. Wang, X. Yang, and Z. J. Shen, "A SiC JFET-based solid state circuit breaker with digitally controlled current-time profiles," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1556–1565, Sep. 2019.

[7] W. Liu, F. Liu, X. Zha, M. Huang, C. Chen, and Y. Zhuang, "An improved SSCB combining fault interruption and fault location functions for DC line short-circuit fault protection," *IEEE Trans. Power Del.*, vol. 34, no. 3, pp. 858–868, Jun. 2019.

[8] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021.

[9] X. Zhang, Z. Yu, Z. Chen, Y. Huang, B. Zhao, and R. Zeng, "Modular design methodology of dc breaker based on discrete metal oxide varistors with series power electronic devices for HVDC application," *IEEE Trans. Ind. Electron.*, vol. 66, no. 10, pp. 7653–7662, Oct. 2019.

[10] M. R. Kaisar Rachi, M. Akhter Khan, and I. Husain, "Current derivative assisted protection coordination system for faster fault isolation in a radial dc microgrid," in *Proc. IEEE Energy Convers. Congr. Expo.*, Detroit, MI, USA, 2020, pp. 1292–1298.

[11] Z. J. Shen, Z. Miao, and A. M. Roshandeh, "Solid state circuit breakers for DC microgrids: Current status and future trends," in *Proc. IEEE 1st Int. Conf. DC Microgrids*, Atlanta, GA, USA, 2015, pp. 228–233.

[12] Z. Wang and E. M. S. Narayanan, "Design of a snubber circuit for low voltage DC solid-state circuit breakers," *IET Power Electron.*, vol. 14, pp. 1111–1120, 2021.

[13] U. Mehrotra, B. Ballard, and D. C. Hopkins, "High current medium voltage bidirectional solid state circuit breaker using SiC JFET super cascode," in *Proc. IEEE Energy Convers. Congr. Expo.*, Detroit, MI, USA, 2020, pp. 6049–6056.

[14] S. J. K. Berg, A. Giannakis, and D. Peftitsis, "Analytical design considerations for MVDC solid-state circuit breakers," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, 2019, pp. 1–10.

[15] Y. Wu, Q. Yi, Y. Wu, F. Yang, Z. Zhang, and J. Wen, "Research on snubber circuits for power electronic switch in DC current breaking," in *Proc. 14th IEEE Conf. Ind. Electron. Appl.*, 2019, pp. 2082–2086.

[16] B. Li, J. He, Y. Li, and W. Wen, "A novel DCCB reclosing strategy for the flexible HVDC grid," *IEEE Trans. Power Del.*, vol. 35, no. 1, pp. 244–257, Feb. 2020.

[17] J. Xu, D. Wu, J. Li, X. Zhao, and X. Jia, "The voltage clamping based DC circuit breaker with decoupled fault isolation and energy dissipation processes," *IEEE Trans. Power Del.*, vol. 36, no. 1, pp. 64–73, Feb. 2021.

[18] Q. Kong, S. Wu, F. Zhang, P. Yang, Y. Zhou, and J. Wei, "DC solid state circuit breaker based on GaN," in *Proc. 15th IEEE Conf. Ind. Electron. Appl.*, Kristiansand, Norway, 2020, pp. 675–680.

[19] Y. Zhou, Y. Feng, N. Shatalov, R. Na, and Z. J. Shen, "An ultraefficient DC hybrid circuit breaker architecture based on transient commutation current injection," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 2500–2509, Jun. 2021.