Diode Open-Circuit Fault Research on the Parallel-Connected 24-Pulse Rectifier With DC-Side Passive Harmonic Reduction Circuit

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***Abstract*—Multipulse rectifiers (MPRs) with dc side passive harmonic reduction circuits often have lower input current total harmonic distortion (THD) values and power losses, that fulfill power requirements for many industrial occasions. In addition to normal operation properties, fault tolerance is another aspect closely related to overall performance of MPRs. This article takes a common parallel-connected 24-pulse rectifier as an example, researches its operation characteristics and fault tolerance under diode open-circuit fault conditions. Operation modes under single or double diodes open-circuit fault in the main circuit, as well as diode open-circuit fault in the dc side harmonic reduction circuit are discussed in details. It can be determined that load voltage is the characteristic parameter that directly reflects the fault information. Related simulation and experimental verifications are performed, all results are consistence with theoretical waveforms. This article provides useful guidance for fault handling and clarifies factors related to the reliability of MPRs, which are helpful for novel MPRs design.**

***Index Terms*—24-pulse rectifier, dc side harmonic reduction circuit, diode open-circuit fault research, fault tolerance.**

I. Introduction

THE MULTIPULSE rectification technology is a useful method to eliminate harmonics existing in input currents. Due to that pulse number is associated with power quality of the multipulse rectifier (MPR), so that increasing pulse number is one of the main design goals of the MPRs. At the first stage of the development of this technology, researches use two or more three-phase bridge rectifiers connected in series or parallel form to increase pulse number, although this design method is easy to realize, complexity and equivalent capacity of magnetic devices increase accordingly [1]–[3]. To achieve a balance between harmonic elimination performance and the use of magnetic devices, the dc side harmonic reduction methods have been proposed in recent decades [4]–[18]. Generally, the dc side harmonic reduction circuits are cooperated with the 12-pulse rectifier, which can provide higher quality power but without using complicated phase-shifting transformer. Compared to active harmonic reduction methods, the passive methods have advantages of easy realization, higher reliability, lower costs and power losses, and they can meet most power quality requirements for ordinary industrial occasions [19]. Therefore, MPRs with dc side passive harmonic reduction methods have been used in aeronautical power system, power supply system for rocket launchers and other low-capacity power systems.

There are two kinds of methods to construct the 24-pulse rectifier based on a 12-pulse rectifier, one is using double-taps interphase reactor (IPR) [7], the other is using IPR and single-phase rectifier connected to the secondary side winding of the IPR [8], [9]. The first method causes more power losses due to that diodes connected with two taps of IPR flow through all load currents, while the second method can effectively avoid part of power losses by using parallel-connected structure between the main circuit and the dc side single-phase rectifier. From previous research, it can be found that the key point of this method is to properly design turns ratio of the IPR, however, the previous calculate processes are more complicated. In [8] and [10], the turns ratio is determined from the viewpoint of minimizing the input current total harmonic distortion (THD) value, and the current is associated with the actual phase-shifting transformer design. This article gives another way to determine the optimum turns ratio of IPR, which only uses voltage relations and successfully breaks the configuration restriction of phase-shifting transformer.

In addition to the normal operation performance, the fault tolerance ability is another essential aspect to do comprehensive evaluations on MPRs. In most cases, when a serious short-circuit fault occurs, the protection system will start immediately. However, the open-circuit fault may not result in over-current or over-voltage, so that the rectifier can still operate for a certain period of time. During this fault operation stage, the power quality on both ac and dc sides of the MPR will inevitably decrease, which can even cause damage to electrical devices connected to MPR. Among all kinds of open-circuit faults in an MPR, diode open-circuit fault is one of the most common faults. Previous fault tolerance researches are mainly concentrated on conventional rectifiers [20]–[22]. After using the dc side harmonic reduction circuit, both normal and fault operation modes of the MPR are quite different from that of the

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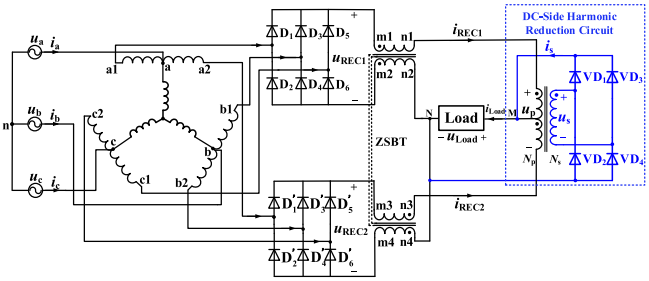

Fig. 1. Parallel-connected 24-pulse rectifier.

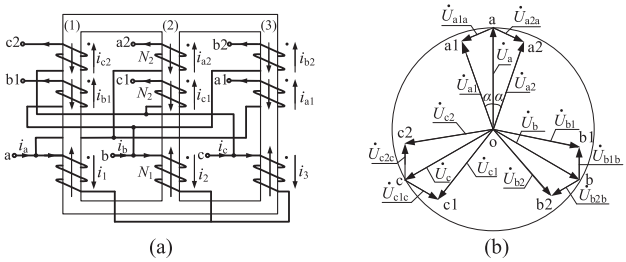

Fig. 2. Winding configuration and phasor diagram of the phase-shifting transformer ($\alpha = 30^{\circ}$). (a) Winding configuration. (b) Phasor diagram.

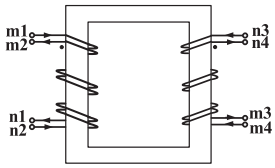

Fig. 3. Winding configuration of the ZSBT.

conventional MPR. It is necessary to do research on operation modes variations of the novel MPR under fault conditions, and find the fault characteristics to identify the fault type, but this work has not been done in previous study.

This article discusses the operation modes of the 24-pulse rectifier under single or double diodes open-circuit fault conditions in the main circuit for the first time, the diode open-circuit faults in dc side harmonic reduction circuit are also considered. Based on theoretical and experimental verifications, fault characteristics for each fault type and the characteristic parameter that can accurately reflect the fault information are finally determined. Besides, the key factors affecting the fault tolerance ability of rectifier are analyzed. All above works are helpful for improving the reliability of the MPRs and providing useful guides for novel MPR design.

II. Normal Operation Mode Analysis on the Parallel-Connected 24-Pulse Rectifier

Fig. 1 is a 24-pulse rectifier with dc side single passive harmonic reduction circuit. The configuration and phasor diagram of the Y-connected autotransformer is shown in Fig. 2. Figs. 3 and 4 are winding configurations of the other two magnetic devices, which are the zero-sequence blocking transformer (ZSBT) and the IPR. The function of ZSBT is to suppress the

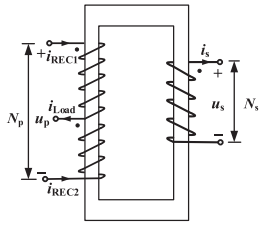

Fig. 4. Winding configuration of the IPR.

zero-sequence current formed by the triple frequency current and make sure that the two bridge rectifiers can work properly. The IPR ensures that the two three-phase bridge rectifiers in the main circuit can operate in parallel, consequently, this rectifier is named as parallel-connected rectifier in related research.

The turns ratio (m) of the IPR is defined as

$$m = \frac{u_{\rm s}}{u_{\rm p}} = \frac{N_{\rm s}}{N_{\rm p}} \tag{1}$$

where $u_{\rm p}$ and $u_{\rm s}$ are the primary and secondary side voltage of IPR, $N_{\rm p}$ and $N_{\rm s}$ are the turns number of both sides of IPR.

It is known that the turns ratio of the IPR takes the optimum value when the THD value of the input currents is the minimum [8]. This article gives an easier method to calculate the turns ratio m from the perspective of minimizing the load voltage ripple factor. It can be proved that the optimum turns ratio value is the same one by using these two methods.

Assuming that the three-phase input voltages of the system are

$$\begin{cases} u_a = \sqrt{2}E\sin\omega t \\ u_b = \sqrt{2}E\sin(\omega t - 2\pi/3) \\ u_c = \sqrt{2}E\sin(\omega t + 2\pi/3) \end{cases} \tag{2}$$

where E is the RMS value of the input voltage.

The two sets of output voltages are

$$\begin{cases} u_{a1} = \sqrt{2}KE\sin(\omega t + \pi/12) \\ u_{b1} = \sqrt{2}KE\sin(\omega t - 7\pi/12) \\ u_{c1} = \sqrt{2}KE\sin(\omega t + 3\pi/4) \\ u_{a2} = \sqrt{2}KE\sin(\omega t - \pi/12) \\ u_{b2} = \sqrt{2}KE\sin(\omega t - 3\pi/4) \\ u_{c2} = \sqrt{2}KE\sin(\omega t + 7\pi/12) \end{cases} \tag{3}$$

where K is the ratio of the RMS values of the output voltage to the input voltage.

The formation of the 24-pulse rectifier is essentially the superimposed effect of the dc side harmonic reduction circuit and the 12-pulse rectifier. Fig. 5 shows the formation process of the 24-pulse load voltage $u_{\rm Load\_24}$, in which the first intersection point of the load voltage $u_{\rm Load\_12}$ and $|u_{s\cdot 12}|$ is marked as ωt_1.

Based on the relations between secondary side voltage of IPR $|u_{\rm s}|$ and the load voltage $u_{\rm Load}$, there are three operation modes of the dc side single-phase bridge rectifier. The following voltages $u_{\rm s}$ and $u_{\rm Load}$ refer to the transient state from the 12-pulse to 24-pulse rectification state. The variables containing subscript "12"

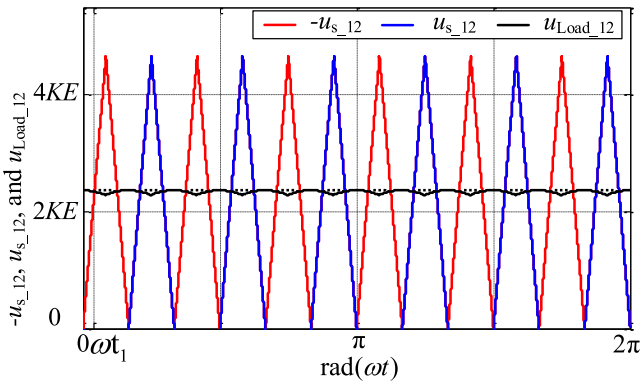

Fig. 5. Formation process of the 24-pulse load voltage $u_{\mathrm{Load\_24}}$.

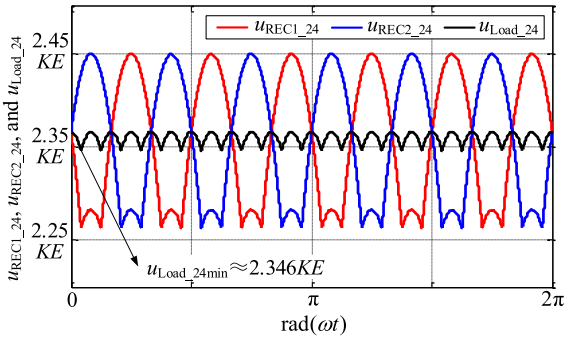

Fig. 6. Waveforms of voltages $u_{\mathrm{REC1\_24}}$, $u_{\mathrm{REC2\_24}}$ and $u_{\mathrm{Load\_24}}$.

and "24" correspond to the 12-pulse and 24-pulse rectification states, respectively.

1) *Case 1:* $|u_s| < u_{\mathrm{Load}}$, under this case, the single-phase bridge rectifier cannot work. The three-phase diode bridge rectifiers REC1 and REC2 are under 6-pulse operation modes respectively, the output voltages $u_{\mathrm{REC1\_12}}$ and $u_{\mathrm{REC2\_12}}$ are totally determined by the input voltage relations of the rectifiers

$$\begin{cases} u_{\mathrm{REC1\_24}}{=}u_{\mathrm{REC1\_12}} = S_{a1}u_{a1} + S_{b1}u_{b1} + S_{c1}u_{c1} \\ u_{\mathrm{REC1\_24}}{=}u_{\mathrm{REC2\_12}} = S_{a2}u_{a2} + S_{b2}u_{b2} + S_{c2}u_{c2} \end{cases} \tag{4}$$

and the switching function *S* of each phase can be presented as

$$\begin{cases} S_{a1} = \frac{1}{2}\left\{\mathrm{sgn}\left[u_{a1} - u_{c1}\right] - \mathrm{sgn}\left[u_{b1} - u_{a1}\right]\right\} \\ S_{b1} = S_{a1}\angle - 2\pi/3 \\ S_{c1} = S_{a1}\angle + 2\pi/3 \\ S_{a2} = S_{a1}\angle - \pi/6 \\ S_{b2} = S_{a1}\angle - 5\pi/6 \\ S_{c2} = S_{a1}\angle + \pi/2 \end{cases}. \tag{5}$$

The load voltage is the same as that in the 12-pulse rectifier

$$u_{\mathrm{Load\_24}}{=}u_{\mathrm{Load\_12}}{=}\frac{1}{2}(u_{\mathrm{REC1\_12}} + u_{\mathrm{REC2\_12}}). \tag{6}$$

2) *Case 2:* $u_s > u_{\mathrm{Load}}$, under this case, the diodes VD_1 and VD_4 are turned ON, the other two diodes VD_2 and VD_3 are turned OFF, which results in the increase in the voltage u_{Rec2}. So that rectifier REC2 is turned off, and rectifier REC1 is under six-pulse rectification mode. In combination with the KVL, the voltage $u_{\mathrm{REC2\_24}}$ and $u_{\mathrm{Load\_24}}$ can be presented by u_{REC1}

$$\begin{cases} u_{\mathrm{REC2\_24}} = \frac{2m-1}{2m+1}u_{\mathrm{REC1\_12}} \\ u_{\mathrm{Load\_24}} = \frac{2m}{2m+1}u_{\mathrm{REC1\_12}} \end{cases}. \tag{7}$$

3) *Case 3:* $-u_s > u_{\mathrm{Load}}$, under this case, the operation modes of diodes in single-phase rectifier are inverse to that in case 2, which results in the increase in the voltage u_{REC1}. So that rectifier REC1 is turned OFF, and REC2 is under six-pulse rectification mode. Similarly, voltages $u_{\mathrm{REC1\_24}}$ and $u_{\mathrm{Load\_24}}$ are

$$\begin{cases} u_{\mathrm{REC1\_24}} = \frac{2m-1}{2m+1}u_{\mathrm{REC2\_12}} \\ u_{\mathrm{Load\_24}} = \frac{2m}{2m+1}u_{\mathrm{REC2\_12}} \end{cases}. \tag{8}$$

Based on the above analysis, the output voltages of the three-phase diode bridge rectifiers are

$$u_{\mathrm{REC1\_24}} = \begin{cases} \sqrt{6}KE\sin(\omega t + \frac{7\pi}{12} - \frac{k\pi}{3})\omega t \in \left[\frac{k\pi}{3}, \omega t_1 + \frac{k\pi}{3}\right) \\ \sqrt{6}KE\frac{2m-1}{2m+1}\sin(\omega t + \frac{5\pi}{12} - \frac{k\pi}{3})\omega t \\ \in \left[\omega t_1 + \frac{k\pi}{3}, \frac{\pi}{6} - \omega t_1 + \frac{k\pi}{3}\right) \\ \sqrt{6}KE\sin(\omega t + \frac{\pi}{4} - \frac{k\pi}{3})\omega t \in \left[\frac{\pi}{6} - \omega t_1 + \frac{k\pi}{3}, \frac{(k+1)\pi}{3}\right) \end{cases}$$

$$u_{\mathrm{REC2\_24}} = \begin{cases} \sqrt{6}KE\sin(\omega t + \frac{5\pi}{12} - \frac{k\pi}{3})\omega t \in \left[\frac{k\pi}{3}, \frac{\pi}{6} + \omega t_1 + \frac{k\pi}{3}\right) \\ \sqrt{6}KE\frac{2m-1}{2m+1}\sin(\omega t + \frac{\pi}{4} - \frac{k\pi}{3})\omega t \\ \in \left[\frac{\pi}{6} + \omega t_1 + \frac{k\pi}{3}, \frac{\pi}{3} - \omega t_1 + \frac{k\pi}{3}\right) \\ \sqrt{6}KE\sin(\omega t + \frac{\pi}{12} - \frac{k\pi}{3})\omega t \in \left[\frac{\pi}{3} - \omega t_1 + \frac{k\pi}{3}, \frac{(k+1)\pi}{3}\right) \end{cases} \tag{9}$$

where *k* is a natural number.

The load voltage $u_{\mathrm{Load\_24}}$ is

$$u_{\mathrm{Load\_24}} = \begin{cases} \frac{3+\sqrt{3}}{2}KE\sin(\omega t + \frac{\pi}{2} - \frac{k\pi}{6})\omega t \in \left[\frac{k\pi}{6}, \omega t_1 + \frac{k\pi}{6}\right) \\ \sqrt{6}KE\frac{2m}{2m+1}\sin(\omega t + \frac{5\pi}{12} - \frac{k\pi}{6})\omega t \\ \in \left[\omega t_1 + \frac{k\pi}{6}, -\omega t_1 + \frac{(k+1)\pi}{6}\right) \\ \frac{3+\sqrt{3}}{2}KE\sin(\omega t + \frac{\pi}{3} - \frac{k\pi}{6})\omega t \in \left[-\omega t_1 + \frac{(k+1)\pi}{6}, \frac{(k+1)\pi}{6}\right) \end{cases}. \tag{10}$$

From (10), it can be observed that when the ripple factor of the load voltage takes the minimum value, the amplitudes of the piecewise function should be the same, and the minimum value of each continuous curve should also be equal, that is

$$\begin{cases} \omega t_1 = \frac{\pi}{24} \\ m = \frac{3+\sqrt{3}}{4\sqrt{6}-2\sqrt{3}-6} \end{cases}. \tag{11}$$

The optimum turns ratio presented in (11) is equal to that given in [8], so that the optimum THD and harmonic content of the input currents is match with the optimum dc voltage ripple.

Substitute (11) into (9) and (10), the waveforms of voltages $u_{\mathrm{REC1\_24}}$, $u_{\mathrm{REC2\_24}}$ and $u_{\mathrm{Load\_24}}$ can be plotted as shown in Fig. 6, and the minimum value of the voltage $u_{\mathrm{Load\_24}}$ is

$$u_{\mathrm{Load\_24min}} \approx 2.346KE\omega t = \frac{\pi}{24} + \frac{k\pi}{12}. \tag{12}$$

Based on Fig. 6, the conduction sequences of the diodes in the 24-pulse rectifier under normal operation are given in Table III (APPENDIX).

III. DIODE OPEN-CIRCUIT FAULT ANALYSIS ON THE PARALLEL-CONNECTED 24-PULSE RECTIFIER

Assuming that the three-phase input voltages are standard sine waves, the rectifier is working in continuous conduction mode, and the impact of flux imbalance on IPR is ignored.

A. Single Diode Open-Circuit Fault in the Main Circuit

The probability of the single diode open-circuit fault is the highest, diode D_1 (see Fig. 1) is taken as an example to study the operation modes and derive the voltage variations under this kind of fault condition. This article is helpful for timely detecting the fault type and fault position, thus improving the reliability of the system.

Based on theoretical analysis in part I, it can be known that the conduction interval of the diode D_1 under normal operation should be $\omega t \in [\frac{\pi}{8}, \frac{3\pi}{8}] \cup [\frac{11\pi}{24}, \frac{17\pi}{24}]$. While open-circuit fault occurs on diode D_1, the maximum voltage provided by the rectifier itself is lower than its dc side voltage, so that the three-phase bridge rectifier REC1 is turned OFF under the back pressure, only rectifier REC2 is continuously working in six-pulse rectification state. Compared to normal operation state, the affected intervals of rectifiers REC1 and REC2 are, respectively,

$$\begin{cases} \text{REC1}: \omega t \in \left[\frac{\pi}{8}, \frac{3\pi}{8}\right] \cup \left[\frac{11\pi}{24}, \frac{17\pi}{24}\right] \\ \text{REC2}: \omega t \in \left[\frac{9\pi}{24}, \frac{7\pi}{24}\right] \cup \left[\frac{13\pi}{24}, \frac{5\pi}{8}\right] \end{cases}.$$

Therefore, in combination with (8), the output voltages $u_{\text{REC1\_24}}$ and $u_{\text{REC2\_24}}$ are changed into

$$u_{\text{REC2\_24}(D1\text{fault})} = \begin{cases} \sqrt{6}KE\sin(\omega t + \frac{5\pi}{12}) \omega t \in \left[\frac{5\pi}{24}, \frac{\pi}{4}\right) \\ \sqrt{6}KE\sin(\omega t + \frac{\pi}{12}) \omega t \in \left[\frac{\pi}{4}, \frac{7\pi}{24}\right] \cup \left[\frac{13\pi}{24}, \frac{7\pi}{12}\right) \\ \sqrt{6}KE\sin(\omega t - \frac{\pi}{4}) \omega t \in \left[\frac{7\pi}{12}, \frac{5\pi}{8}\right] \end{cases}$$

$$u_{\text{REC1\_24}(D1\text{fault})} = \begin{cases} \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t + \frac{5\pi}{12}) \omega t \in \left[\frac{\pi}{8}, \frac{\pi}{4}\right) \\ \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t + \frac{\pi}{12}) \omega t \in \left[\frac{\pi}{4}, \frac{3\pi}{8}\right] \cup \left[\frac{11\pi}{24}, \frac{7\pi}{12}\right) \\ \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t - \frac{\pi}{4}) \omega t \in \left[\frac{7\pi}{12}, \frac{17\pi}{24}\right] \end{cases}. \quad (13)$$

From (13) and KVL, the load voltage in this fault operation interval is

$$u_{\text{Load\_24}(D1\text{fault})} = \begin{cases} \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t + \frac{5\pi}{12}) \omega t \in \left[\frac{\pi}{8}, \frac{\pi}{4}\right) \\ \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t + \frac{\pi}{12}) \omega t \in \left[\frac{\pi}{4}, \frac{3\pi}{8}\right] \cup \left[\frac{11\pi}{24}, \frac{7\pi}{12}\right) \\ \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t - \frac{\pi}{4}) \omega t \in \left[\frac{7\pi}{12}, \frac{17\pi}{24}\right] \end{cases}. \quad (14)$$

Substitute (11) into (13) and (14), the waveforms of voltages $u_{\text{REC1\_24(D1fault)}}$, $u_{\text{REC2\_24(D1fault)}}$ and $u_{\text{Load\_24(D1fault)}}$ can be plotted as shown in Fig. 7, and the minimum value of the voltage $u_{\text{Load\_24(D1fault)}}$ is

$$u_{\text{Load\_24}(D1\text{fault})\min} \approx 2.049KE\omega t = \frac{\pi}{4} \text{ and } \frac{7\pi}{12}. \quad (15)$$

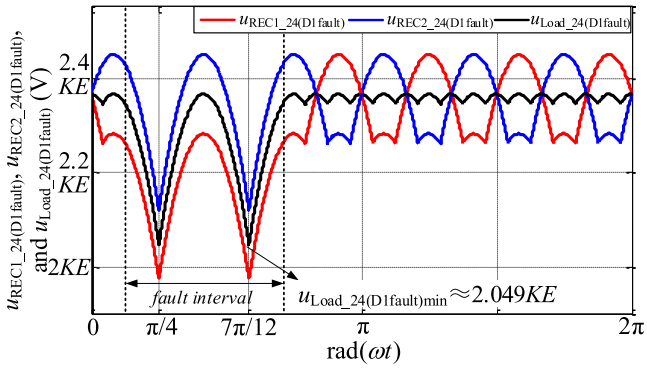

Fig. 7. Waveforms of voltages $u_{\text{REC1\_24(D1fault)}}$, $u_{\text{REC2\_24(D1fault)}}$, and $u_{\text{Load\_24(D1fault)}}$.

TABLE I
MINIMUM POINTS OF THE LOAD VOLTAGE UNDER EACH DIODE OPEN-CIRCUIT FAULT

Diode	D_1	D_2	D_3	D_4	D_5	D_6
Phase	$\frac{5\pi}{12}\pm\frac{\pi}{6}$	$\frac{17\pi}{12}\pm\frac{\pi}{6}$	$\frac{13\pi}{12}\pm\frac{\pi}{6}$	$\frac{7\pi}{12}\pm\frac{\pi}{6}$	$\frac{7\pi}{4}\pm\frac{\pi}{6}$	$\frac{3\pi}{4}\pm\frac{\pi}{6}$
Diode	D_1'	D_2'	D_3'	D_4'	D_5'	D_6'
Phase	$\frac{7\pi}{12}\pm\frac{\pi}{6}$	$\frac{19\pi}{12}\pm\frac{\pi}{6}$	$\frac{5\pi}{4}\pm\frac{\pi}{6}$	$\frac{\pi}{4}\pm\frac{\pi}{6}$	$\frac{23\pi}{12}\pm\frac{\pi}{6}$	$\frac{11\pi}{12}\pm\frac{\pi}{6}$

In combination with Fig. 4, the minimum points of load voltage appear twice per power cycle, which are at the midpoints of the two conduction intervals under normal operation modes. The use of dc side harmonic reduction circuit is helpful for reducing voltage drops under the main circuit diode open-circuit fault. Under this fault type, load voltage is the variable that can obviously indicate the fault locations. In this design, the minimum points under each diode open-circuit fault in the main circuit are given as Table I.

B. Two Diodes Open-Circuit Fault in the Main Circuit

Based on the fault characteristic, there are three types of double diodes opencircuit fault.

1) *Case 1:* The two open-circuit fault diodes are located at the same bridge rectifier. This case can be generally divided into three subcases, which are the two fault diodes are in the same phase (e.g., D_1 and D_2), or in the same bridge arm (e.g., D_1 and D_3) or two fault diodes have common conducting interval under normal operation (e.g., D_1 and D_6). Under this case, the fault rectifier is shut OFF, and the other rectifier is operating in the six-pulse rectification state. Their fault characteristics have some similarities with single diode open-circuit fault condition, in all mentioned subcases, the fault load voltage is the union set of the single diode fault, and the minimum values remain constant. Due to that the existing of the common conduction interval, compared to the former two cases, the minimum load

voltage points in the third case reduce from four to three per power cycle.

Similarly, based on Table I, the fault diodes can be determined from the position of the minimum load voltages.

2) *Case 2:* The two open-circuit fault diodes are separately located at two bridge rectifiers but there is no common conduction interval between these two fault diodes under normal operation (e.g., D_1 and D_2').

Under this case, the bridge rectifier corresponds to the fault diode is tuned off in the interval that the fault diode should be conducted, while the other one operates under 6-pulse rectification state. The load voltage also has the same minimum voltage as the single diode open-circuit fault cases, the phases of the minimum points all follow that in Table I.

3) *Case 3:* The two open-circuit fault diodes are separately located at two bridge rectifiers and there are common conducting intervals between these two fault diodes under normal operation.

This case has some differences compared with the former two cases, which is main content for discussion. There are two subcases in case 3, the first one is that the length of the two fault diodes' common conduction interval under normal operation is $\pi/12$ per power cycle (e.g., D_1 and D_5'), the second one has the common conduction interval length of $\pi/4$ (e.g., D_1 and D_1').

a) Diodes D_1 and D_5' are under open-circuit fault: Based on the input voltages relations of rectifiers REC1 and REC2, in a power cycle, the conduction order of the diodes in the upper bridge arm of REC1 is that: $D_5 \rightarrow D_1 \rightarrow D_3 \rightarrow D_5$, and that in the upper bridge arm of REC2 is that: $D_5' \rightarrow D_1' \rightarrow D_3' \rightarrow D_5'$.

If only diode D_1 is open-circuit, based on the operation modes of single diode open-circuit fault, the diodes D_5' and D_1' are continuously conducting in the intervals [π/12, π/4] and [π/4, 3π/4], respectively. Similarly, if only diode D_5' is open-circuit, the diodes D_1 is turned-ON in the interval [π/12, π/4] and D_5 is turned-ON in the intervals [0, π/12] and [19π/12, 2π]. Under this case, the two diodes D_1 and D_5' are simultaneously open-circuit, the diode D_5 has to extend the conduction interval to a point $\omega t\_{\text{fault}\,A}$, accordingly, the diode D_1' has to advance the conduction interval to a point $\omega t\_{\text{fault}\,B}$.

In combination with derivations in part B, the output voltages of the rectifiers REC1 and REC2 under didoes D_1 and D_5' fault condition can be obtained

$$u_{\text{REC1\_24}(D1\text{and}D5'\text{fault})} = \begin{cases} \sqrt{6}KE\sin(\omega t+\frac{7\pi}{12})\omega t \in [0, \omega t\_{\text{fault}\,A}) \\ \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t+\frac{\pi}{12})\omega t \in \left[\omega t\_{\text{fault}\,A}, \frac{7\pi}{12}\right) \\ \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t-\frac{\pi}{4})\omega t \in \left[\frac{7\pi}{12}, \frac{3\pi}{4}\right] \\ \sqrt{6}KE\sin(\omega t-\frac{13\pi}{12})\omega t \in \left[\frac{19\pi}{12}, \frac{7\pi}{4}\right) \\ \sqrt{6}KE\sin(\omega t-\frac{17\pi}{12})\omega t \in \left[\frac{7\pi}{4}, 2\pi\right] \end{cases}$$

$$u_{\text{REC2\_24}(D1\text{and}D5'\text{fault})} = \begin{cases} \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t+\frac{7\pi}{12})\omega t \in [0, \omega t\_{\text{fault}\,B}) \\ \sqrt{6}KE\sin(\omega t+\frac{\pi}{12})\omega t \in \left[\omega t\_{\text{fault}\,B}, \frac{7\pi}{12}\right) \\ \sqrt{6}KE\sin(\omega t-\frac{\pi}{4})\omega t \in \left[\frac{7\pi}{12}, \frac{3\pi}{4}\right] \\ \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t-\frac{13\pi}{12})\omega t \in \left[\frac{19\pi}{12}, \frac{7\pi}{4}\right) \\ \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t-\frac{17\pi}{12})\omega t \in \left[\frac{7\pi}{4}, 2\pi\right] \end{cases} . \quad (16)$$

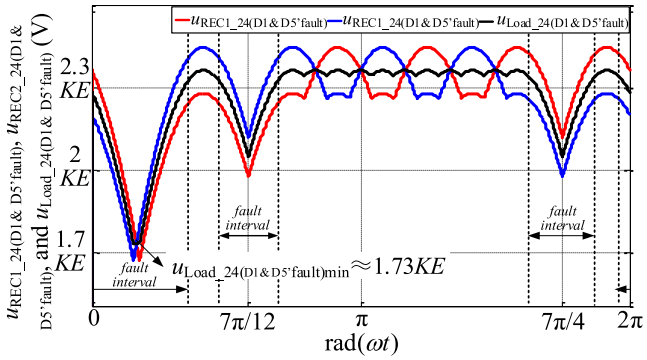

Fig. 8. Waveforms of voltages $u_{\text{REC1\_24}\,(D1\text{and}\quad D5'\text{fault})}$, $u_{\text{REC2\_24}\,(D1\text{ and }D5'\text{fault})}$, and $u_{\text{Load\_24}\,(D1\text{ and }D5'\text{fault})}$.

From (16), the phase information of $\omega t\_{\text{fault}\,A}$ and $\omega t\_{\text{fault}\,B}$ can be determined

$$\begin{cases} \omega t\_{\text{fault}\,A} = \arctan\left(\frac{2m+1}{2m-1}\right) - \frac{\pi}{12} \\ \omega t\_{\text{fault}\,B} = \arctan\left(\frac{2m-1}{2m+1}\right) - \frac{\pi}{12} \end{cases} . \quad (17)$$

From (16), the load voltage $u_{\text{Load\_24}(D1\text{ and }D5'\text{fault})}$ is

$$u_{\text{Load\_24}(D1\text{ and }D5'\text{fault})} = \begin{cases} \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t+\frac{7\pi}{12})\omega t \in [0, \omega t\_{\text{fault}\,B}) \\ \sqrt{3}KE\sin(\omega t+\frac{\pi}{3})\omega t \in [\omega t\_{\text{fault}\,B}, \omega t\_{\text{fault}\,A}) \\ \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t+\frac{\pi}{12})\omega t \in \left[\omega t\_{\text{fault}\,A}, \frac{7\pi}{12}\right) \\ \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t-\frac{\pi}{4})\omega t \in \left[\frac{7\pi}{12}, \frac{3\pi}{4}\right] \\ \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t-\frac{13\pi}{12})\omega t \in \left[\frac{19\pi}{12}, \frac{7\pi}{4}\right) \\ \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t-\frac{17\pi}{12})\omega t \in \left[\frac{7\pi}{4}, 2\pi\right] \end{cases} . \quad (18)$$

From (18), the local and global minimum values of the load voltage $u_{\text{Load\_24}(D1\text{ and }D5'\text{fault})}$ is

$$u_{\text{Load\_24}(D1\text{ and }D5'\text{fault})\text{mins}} \approx \begin{cases} 2.049KE\omega t = \frac{7\pi}{12}\text{ and }\frac{7\pi}{4} \\ 1.73KE\omega t \in [\omega t\_{\text{fault}\,B}, \omega t\_{\text{fault}\,A}] \end{cases} . \quad (19)$$

It can be concluded from (19) that the midpoint of the common conduction interval of the two fault diodes takes the global minimum load voltage, and the noncommon conduction intervals keep consistent with the single diode fault characteristics, therefore the local minimum value is same with that shown in (15). Fig. 8 is the theoretical waveforms of voltages $u_{\text{REC1\_24}(D1\text{ and }D5'\text{fault})}$, $u_{\text{REC2\_24}(D1\text{ and }D5'\text{fault})}$, and $u_{\text{Load\_24}(D1\text{ and }D5'\text{fault})}$.

b) Diodes D_1 and D_1' are under open-circuit fault: After changing fault diode D_5' to diode D_1', the major analysis method is the same, only the difference part is clarified here. If only diode D_1' is open-circuit, the diodes D_1 and D_3 are continuously conducting in the intervals [π/12, 3π/4] and [3π/4, 17π/12] respectively. Similarly, if the two diodes D_1 and D_1' are open-circuit at the same time, the diode D_5' has to extend the conduction interval to a point $\omega t\_{\text{fault}\,C}$, and the D_3 has to advance the conduction interval to a point $\omega t\_{\text{fault}\,D}$.

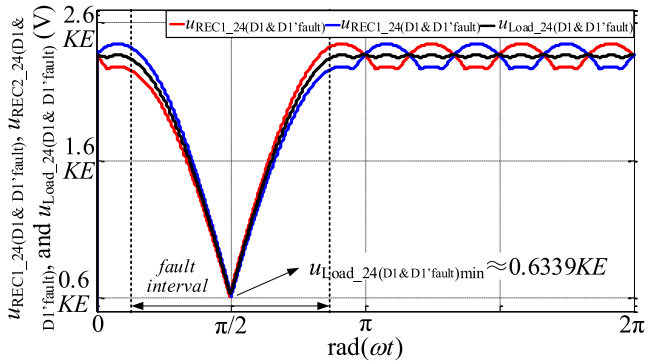

Fig. 9. Waveforms of voltages $u_{\mathrm{REC1\_24}(D1\mathrm{and}\ D1'\mathrm{fault})}$, $u_{\mathrm{REC2\_24}(D1\mathrm{and}\ D1'\mathrm{fault})}$ and $u_{\mathrm{Load\_24}(D1\mathrm{and}\ D1'\mathrm{fault})}$.

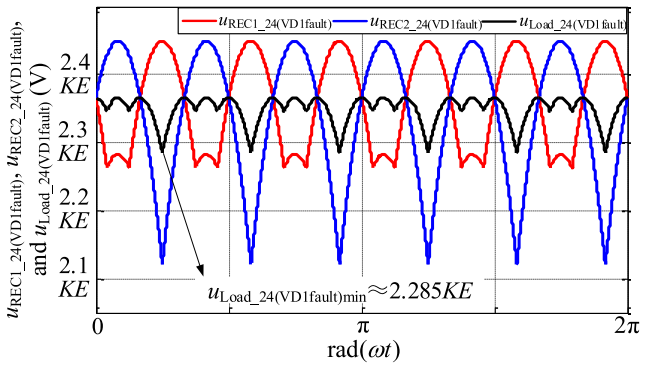

Fig. 10. Waveforms of voltages $_{\mathrm{REC1\_24(VD1fault)}}$, $u_{\mathrm{REC2\_24(VD1fault)}}$ and $u_{\mathrm{Load\_24(VD1fault)}}$.

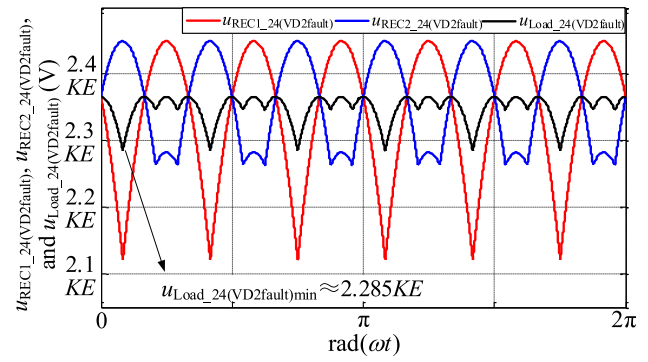

Fig. 11. Waveforms of voltages $_{\mathrm{REC1\_24(VD2fault)}}$, $u_{\mathrm{REC2\_24(VD2fault)}}$, and $u_{\mathrm{Load\_24(VD2fault)}}$.

Under this case, the output voltages of REC1 and REC2 are

$$u_{\mathrm{REC1\_24}(D1\ \mathrm{and}\ D1'\mathrm{fault})} = \begin{cases} \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t+\frac{5\pi}{12}) & \omega t\in\left[\frac{\pi}{12},\omega t_{\_\mathrm{fault}C}\right) \\ \sqrt{6}KE\sin(\omega t-\frac{5\pi}{12}) & \omega t\in\left[\omega t_{\_\mathrm{fault}C},\frac{11\pi}{12}\right] \end{cases}$$

$$u_{\mathrm{REC2\_24}(D1\ \mathrm{and}\ D1'\mathrm{fault})} = \begin{cases} \sqrt{6}KE\sin(\omega t+\frac{5\pi}{12}) & \omega t\in\left[\frac{\pi}{12},\omega t_{\_\mathrm{fault}D}\right) \\ \frac{2m-1}{2m+1}\sqrt{6}KE\sin(\omega t-\frac{5\pi}{12}) & \omega t\in\left[\omega t_{\_\mathrm{fault}D},\frac{11\pi}{12}\right] \end{cases}. \quad (20)$$

TABLE II
THE SIMULATION AND EXPERIMENTAL CONDITIONS

The step-up ratio K of the Y-connected autotransformer	$(3-\sqrt{3})/\sqrt{2}$
The turns ratio m of the IPR	14.17
The RMS value E of the input voltages	50V
The load resistance	30Ω

Due to that the angles $\omega t_{\cdot\mathrm{fault}\,C}$ and $\omega t_{\cdot\mathrm{fault}\,D}$ are in the range of $\omega t\in[\pi/4+\omega t_1, 3\pi/4-\omega t_1]$, in combination with (20), $\omega t_{\cdot\mathrm{fault}\,C}$ and $\omega t_{\cdot\mathrm{fault}\,D}$ can be determined

$$\begin{cases} \omega t_{\_\mathrm{fault}C} = \arctan\left(2m\tan\frac{5\pi}{12}\right)\approx 89.4582^{\mathrm{o}} \\ \omega t_{\_\mathrm{fault}D} = \arctan\left(-2m\tan\frac{5\pi}{12}\right)\approx 90.5417^{\mathrm{o}} \end{cases}. \quad (21)$$

From (21), the load voltage is

$$u_{\mathrm{Load\_24}(D1\mathrm{and}D1'\mathrm{fault})} = \begin{cases} \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t+\frac{5\pi}{12}) & \omega t\in\left[\frac{\pi}{12},\omega t_{\_\mathrm{fault}C}\right) \\ \frac{3-\sqrt{3}}{2}KE\sin(\omega t) & \omega t\in\left[\omega t_{\_\mathrm{fault}C},\omega t_{\_\mathrm{fault}D}\right) \\ \frac{2m}{2m+1}\sqrt{6}KE\sin(\omega t-\frac{5\pi}{12}) & \omega t\in\left[\omega t_{\_\mathrm{fault}D},\frac{11\pi}{12}\right] \end{cases}. \quad (22)$$

From (22), the minimum value of the load voltage can be calculated

$$u_{\mathrm{Load\_24}(D1\ \mathrm{and}D1'\mathrm{fault})\,\min}\approx 0.6339KE\omega t \in\left[\omega t_{\_\mathrm{fault}C},\omega t_{\_\mathrm{fault}D}\right]. \quad (23)$$

Compared with the former case, the load voltage drop further increases in the fault interval with the increasing of the common conduction interval between two fault diodes. Fig. 9 is the theoretical waveforms of voltages $u_{\mathrm{REC1\_24}(D1\ \mathrm{and}\ D1'\mathrm{fault})}$, $u_{\mathrm{REC2\_24}(D1\ \mathrm{and}\ D\ 1'\mathrm{fault})}$, and $u_{\mathrm{Load\_24}(D1\ \mathrm{and}\ D1'\mathrm{fault})}$.

C. Diode Open-Circuit Fault in the DC-Side Harmonic Reduction Circuit

In addition to the diode fault in the main circuit, the diode open-circuit fault also occurs in the dc side harmonic reduction circuit. In Fig. 1, the dc side auxiliary circuit is the single-phase diode bridge rectifier, which has two kinds of operation modes. As mentioned in part A, compared to the operation modes in the 12-pulse rectifier, the existence of the two operation modes has functions to change the operation modes of the three-phase rectifiers REC1 and REC2. If diodes VD_1 and VD_4 are turned-ON, rectifier REC2 is turned-OFF, on the contrary, the turned-OFF of rectifier REC1 is caused by the conduction of diodes VD_2 and VD_3. The output voltage in the nonconduction interval is determined by the output voltage of the other conduction rectifier.

1) *Case 1:* One or both of diodes VD_1 and VD_4 are under open-circuit fault.

Under this case, the operation mode of rectifier REC1 is not changed compared with the normal mode. While due to the

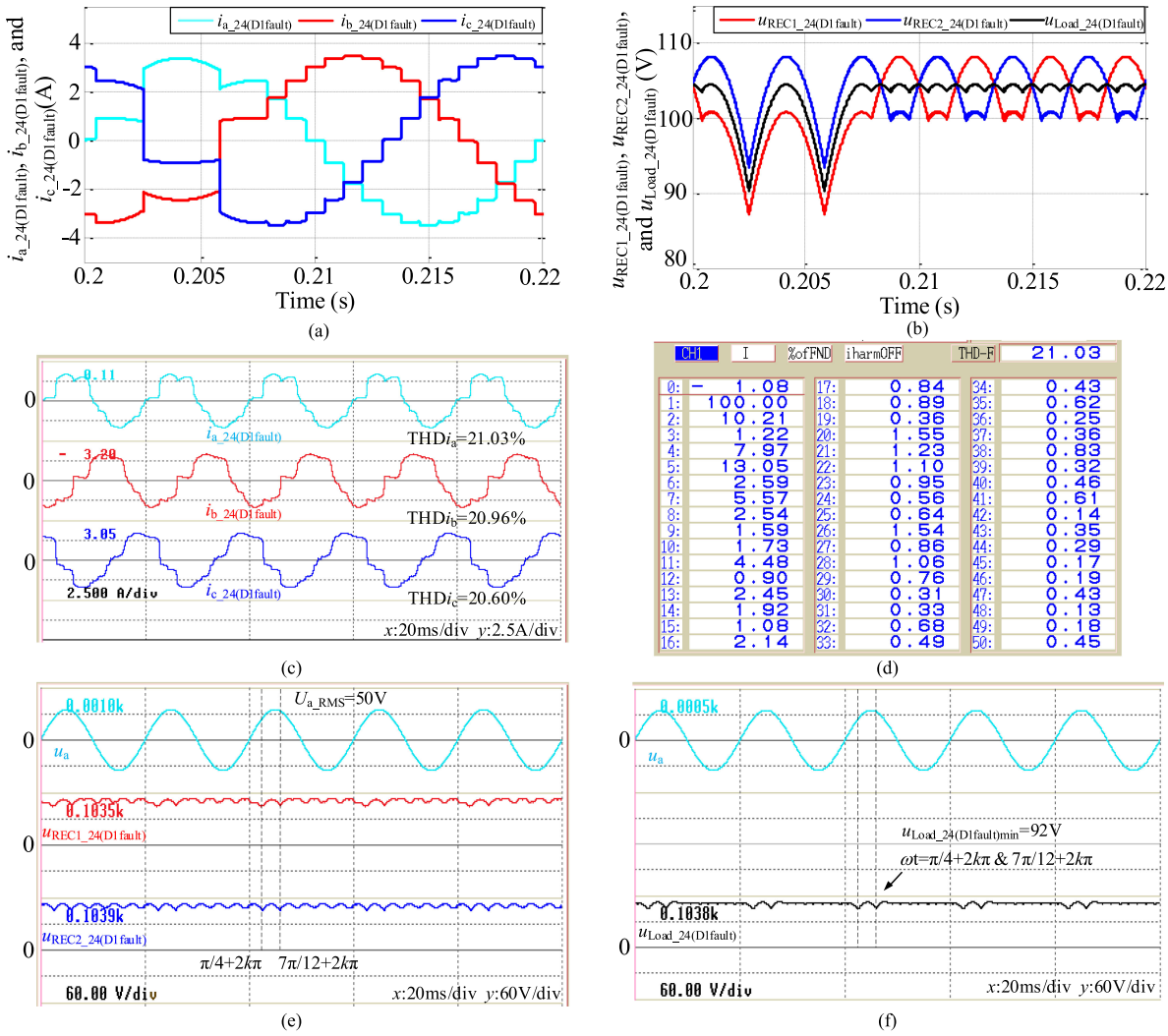

Fig. 12. Verification results of the power quality under diode D_1 open-circuit fault. (a) Simulation results of input currents $i_{a\_24(D1fault)}$, $i_{b\_24(D1fault)}$ and $i_{c\_24(D1fault)}$. (b) Simulation results of voltages $u_{REC1\_24(D1fault)}$, $u_{REC2\_24(D1fault)}$, and $u_{Load\_24(D1fault)}$. (c) Experiment results of input currents $i_{a\_24(D1fault)}$, $i_{b\_24(D1fault)}$, and $i_{c\_24(D1fault)}$. (d) THD value and spectrum of input current $i_{a\_24(D1fault)}$. (e) Experiment results of voltages $u_{REC1\_24(D1fault)}$ and $u_{REC2\_24(D1fault)}$. (f) Experiment result of voltage $u_{Load\_24(D1fault)}$.

shut-OFF of diodes VD_1 and VD_4, the rectifier REC2 keeps working in the six-pulse rectification state, which is same as the rectifier in the 12-pulse rectification system. In combination with (4) and (9), the output voltages $u_{REC1\_24(VD1fault)}$ and $u_{REC2\_24(VD1fault)}$ are

$$u_{REC1\_24(VD1fault)} = \begin{cases} \sqrt{6}KE\sin(\omega t+\frac{7\pi}{12}-\frac{k\pi}{3})\omega t\in\left[\frac{k\pi}{3},\frac{\pi}{24}+\frac{k\pi}{3}\right) \\ \sqrt{6}KE\frac{2m-1}{2m+1}\sin(\omega t+\frac{5\pi}{12}-\frac{k\pi}{3})\omega t\in\left[\frac{\pi}{24}+\frac{k\pi}{3},\frac{\pi}{8}+\frac{k\pi}{3}\right) \\ \sqrt{6}KE\sin(\omega t+\frac{\pi}{4}-\frac{k\pi}{3})\omega t\in\left[\frac{\pi}{8}+\frac{k\pi}{3},\frac{(k+1)\pi}{3}\right) \end{cases}$$

$$u_{REC2\_24(VD1fault)} = \begin{cases} \sqrt{6}KE\sin(\omega t+\frac{5\pi}{12}-\frac{k\pi}{3})\omega t\in\left[\frac{k\pi}{3},\frac{\pi}{4}+\frac{k\pi}{3}\right) \\ \sqrt{6}KE\sin(\omega t+\frac{\pi}{12}-\frac{k\pi}{3})\omega t\in\left[\frac{\pi}{4}+\frac{k\pi}{3},\frac{(k+1)\pi}{3}\right) \end{cases}. \quad (24)$$

Therefore, the load voltage can be obtained

$$u_{Load\_24(VD1fault)} = \begin{cases} \sqrt{6}KE\cos(\frac{\pi}{12})\sin(\omega t+\frac{\pi}{2}-\frac{k\pi}{3})\omega t\in\left[\frac{k\pi}{3},\frac{\pi}{24}+\frac{k\pi}{3}\right) \\ \sqrt{6}KE\frac{2m}{2m+1}\sin(\omega t+\frac{5\pi}{12}-\frac{k\pi}{3})\omega t\in\left[\frac{\pi}{24}+\frac{k\pi}{3},\frac{\pi}{8}+\frac{k\pi}{3}\right) \\ \sqrt{6}KE\cos(\frac{\pi}{12})\sin(\omega t+\frac{\pi}{3}-\frac{k\pi}{3})\omega t\in\left[\frac{\pi}{8}+\frac{k\pi}{3},\frac{\pi}{4}+\frac{k\pi}{3}\right) \\ \sqrt{6}KE\cos(\frac{\pi}{12})\sin(\omega t+\frac{\pi}{6}-\frac{k\pi}{3})\omega t\in\left[\frac{\pi}{4}+\frac{k\pi}{3},\frac{(k+1)\pi}{3}\right) \end{cases}. \quad (25)$$

From (25), the minimum value of the load voltage under this fault case is

$$u_{Load\_24(VD1fault)min}=\frac{2\sqrt{6}+3\sqrt{2}}{4}KE\approx 2.2854KE\omega t = \frac{\pi}{4}+\frac{k\pi}{3}. \quad (26)$$

From (26), the minimum value of the load voltage under diodes open-circuit fault in the dc side harmonic reduction

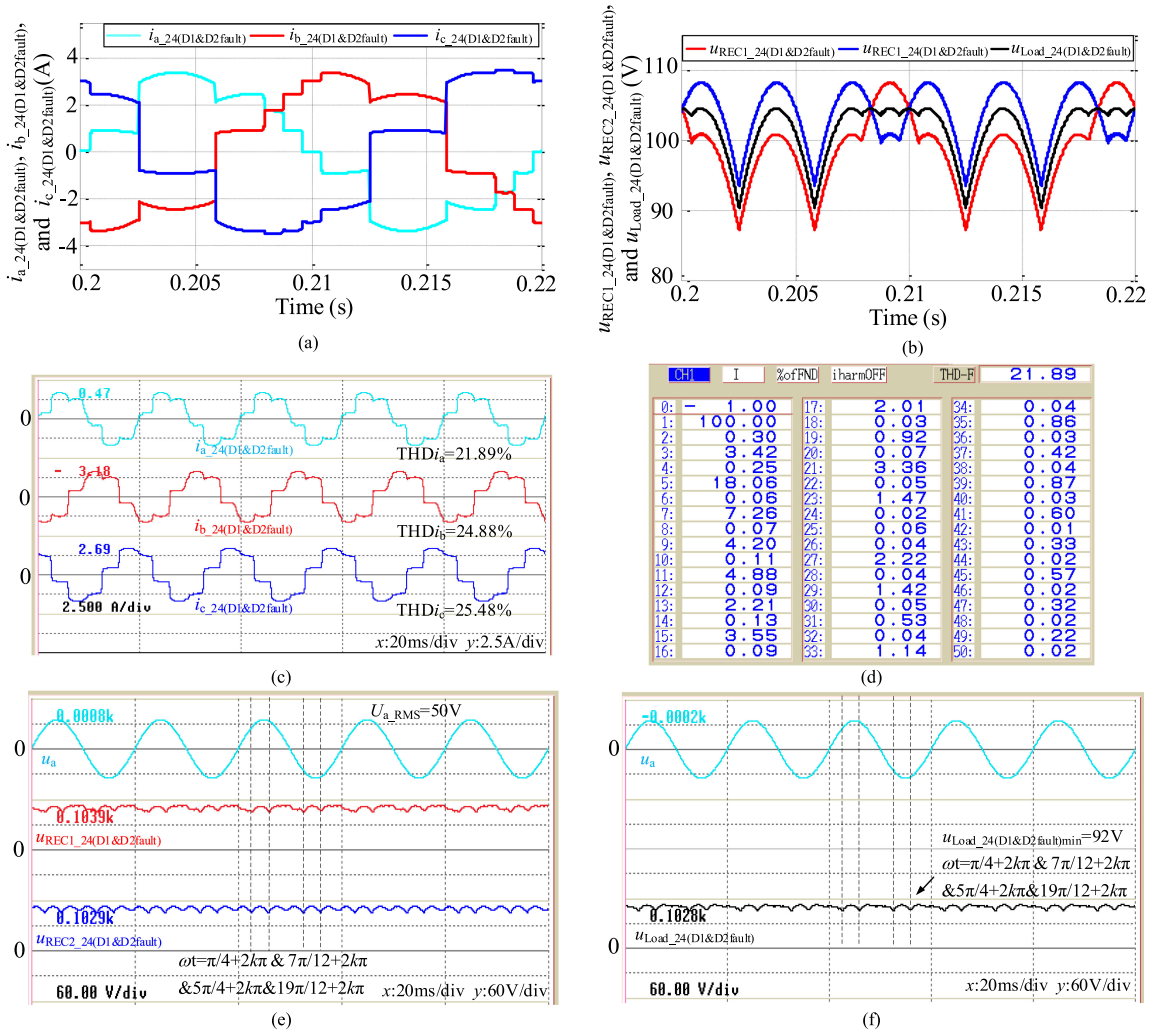

Fig. 13. Verification results of the power quality under diode D_1 and D_2 open-circuit fault. (a) Simulation results of input currents $i_{a\cdot 24(D1 \text{ and } D2\text{fault})}$, $i_{b\cdot 24(D1 \text{ and } D2 \text{ fault})}$, and $i_{c\cdot 24(D1 \text{ and } D2\text{fault})}$. (b) Simulation results of voltages $u_{\text{REC1\_24}(D1 \text{ and } D2 \text{ fault})}$, $u_{\text{REC2\_24}(D1 \text{ and } D2\text{fault})}$, and $u_{\text{Load\_24}(D1 \text{ and } D2\text{fault})}$. (c) Experiment results of input currents $i_{a\cdot 24(D1 \text{ and } D2\text{fault})}$, $i_{b\cdot 24(D1 \text{ and } D2\text{fault})}$, and $i_{c\cdot 24(D1 \text{ and } D2\text{fault})}$. (d) THD value and spectrum of input current $i_{a\cdot 24(D1 \text{ and } D2 \text{ fault})}$. (e) Experiment results of voltages $u_{\text{REC1\_24}(D1 \text{ and } D2\text{fault})}$ and $u_{\text{REC2\_24}(D1 \text{ and } D2\text{fault})}$. (f) Experiment result of voltage $u_{\text{Load\_24}(D1 \text{ and } D2\text{fault})}$.

circuit is same as that value of the minimum value of the normal operation load voltage of the 12-pulse rectifier. Fig. 10 is the theoretical waveforms of voltages $u_{\text{REC1\_24(VD1fault)}}$, $u_{\text{REC2\_24(VD1fault)}}$ and $u_{\text{Load\_24(VD1fault)}}$.

2) *Case 2:* One or both of diodes VD_2 and VD_3 are under open-circuit fault.

This case is the mirror case of Case 1 in this section, so that the detailed explanations and calculations are omitted here.

By using the same way, the minimum value of the load voltage under this fault case can be determined:

$$u_{\text{Load\_24(VD2fault)min}}=\frac{2\sqrt{6}+3\sqrt{2}}{4}KE\approx 2.2854KE$$

$$omegat=\frac{\pi}{12}+\frac{k\pi}{3}. \tag{27}$$

Compared with (26) and (27), the minimum value of the two fault cases is the same, the only difference is the phase of the minimums.

The waveforms of voltages $u_{\text{REC1\_24(VD2fault)}}$, $u_{\text{REC2\_24(VD2fault)}}$ and $u_{\text{Load\_24(VD2fault)}}$ are plotted as shown in Fig. 11.

In this circuit, fault location only can be limited between the two diodes that should simultaneously operate under normal operation. When using a single-phase full-wave diode bridge rectifier to replace the single-phase diode bridge rectifier, the operation modes and the fault diode in the dc side harmonic reduction circuit can be exactly identified by using the same way.

IV. Simulation and Experimental Verifications

To verify the theoretical analysis, the simulation model and experimental platform are constructed based on Fig. 1, the simulation and experimental conditions are given in Table II.

Fig. 12 shows the verification results under diode D_1 open-circuit fault, Fig. 12(a) and (b) are simulation results of the input

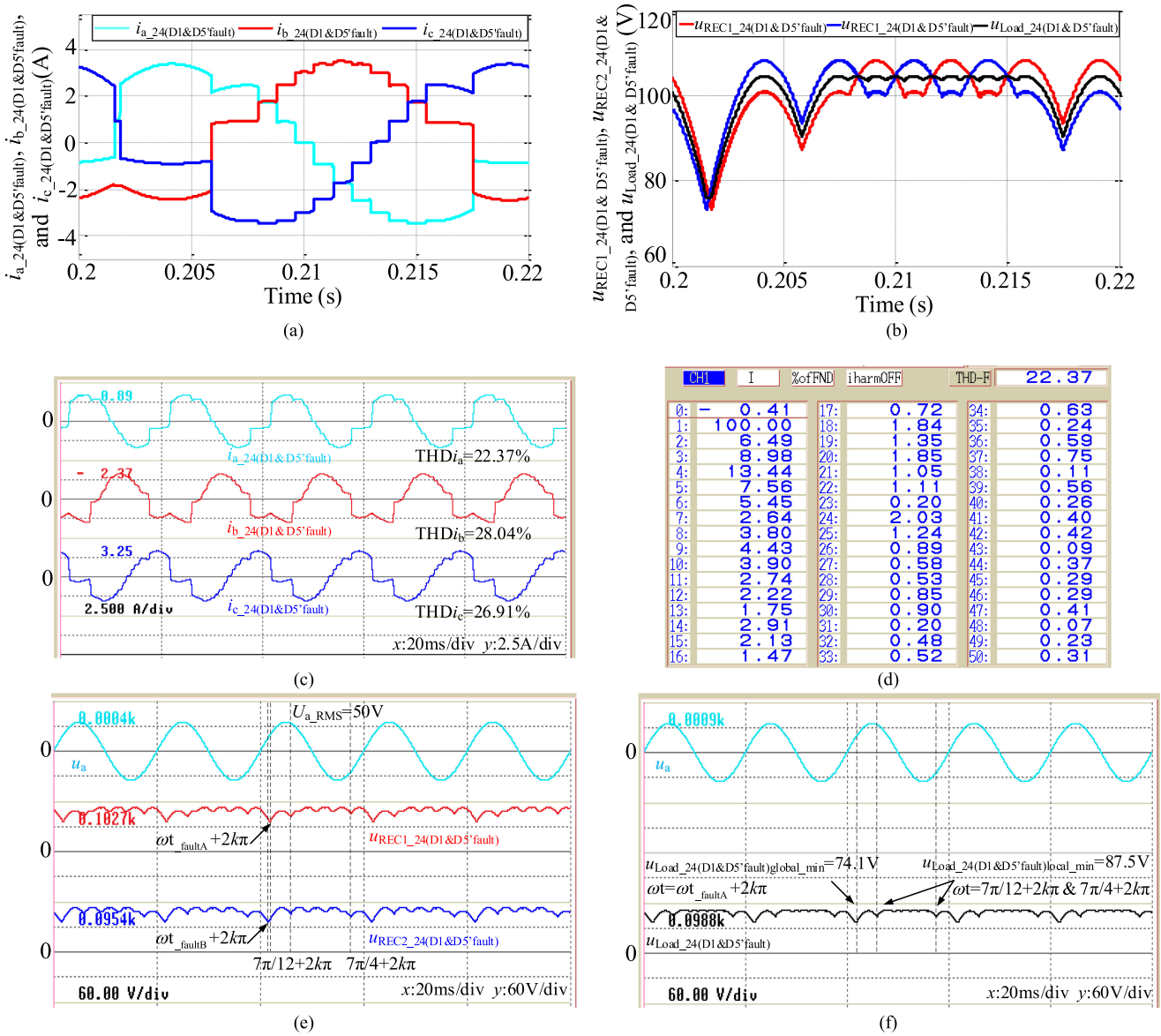

Fig. 14. Verification results of the power quality under diodes D_1 and D_5' open-circuit fault. (a) Simulation results of input currents $i_{a\cdot 24(D1 \text{ and } D5'\text{fault})}$, $i_{b\cdot 24(D1 \text{ and } D5'\text{fault})}$, and $i_{c\cdot 24(D1 \text{ and } D5'\text{fault})}$. (b) Simulation results of voltages $u_{\text{REC1\_24}(D1 \text{ and } D5'\text{fault})}$, $u_{\text{REC2\_24}(D1 \text{ and } D5'\text{fault})}$, and $u_{\text{Load\_24}(D1 \text{ and } D5'\text{fault})}$. (c) Experiment results of input currents $i_{a\cdot 24(D1 \text{ and } D5'\text{fault})}$, $i_{b\cdot 24(D1 \text{ and } D5'\text{fault})}$, and $i_{c\cdot 24(D1 \text{ and } D5'\text{fault})}$. (d) THD value and spectrum of input current $i_{a\cdot 24(D1 \text{ and } D5'\text{fault})}$. (e) Experiment results of voltages $u_{\text{REC1\_24}(D1 \text{ and } D5'\text{fault})}$ and $u_{\text{REC2\_24}(D1 \text{ and } D5'\text{fault})}$. (f) Experiment result of voltage $u_{\text{Load\_24}(D1 \text{ and } D5'\text{fault})}$.

currents and output voltages, Fig. 12(c) and (d) are experiment results of input currents and the spectrum, and the last two waveforms are experiment results of output voltages of the two three-phase rectifiers [see Fig. 12(e)] and the load voltage [see Fig. 12(f)]. Similarly, the verification results under diodes D_1 and D_2, D_1 and D_5', D_1 and D_1', and VD_1 open-circuit fault are respectively presented in Figs. 13–16.

First of all, the results of input currents are analyzed as follows.

1) Compare Figs. 12 and 13, when two didoes open-circuit fault occurs in the same phase, the distortion degree is higher than only one diode fault, and the content of each harmonic changes accordingly.
2) From Figs. 14 and 15, it can be obviously observed that the current distortion occurs in the failure intervals, but the rest parts operate normally that can present obvious steps.
3) When diode open-circuit fault occurs in the dc side harmonic reduction circuit (see Fig. 16), the impact under this case causes less damage on the power quality compared with single diode open-circuit fault in the main circuit, the input currents are more symmetrical and the THD value reduces from around 20 to 7.9%.

Then, the results related to the voltages are analyzed as follows.

1) From Figs. 12 and 13, the minimum points of the load voltage correspond to that given in Table I. The effect of

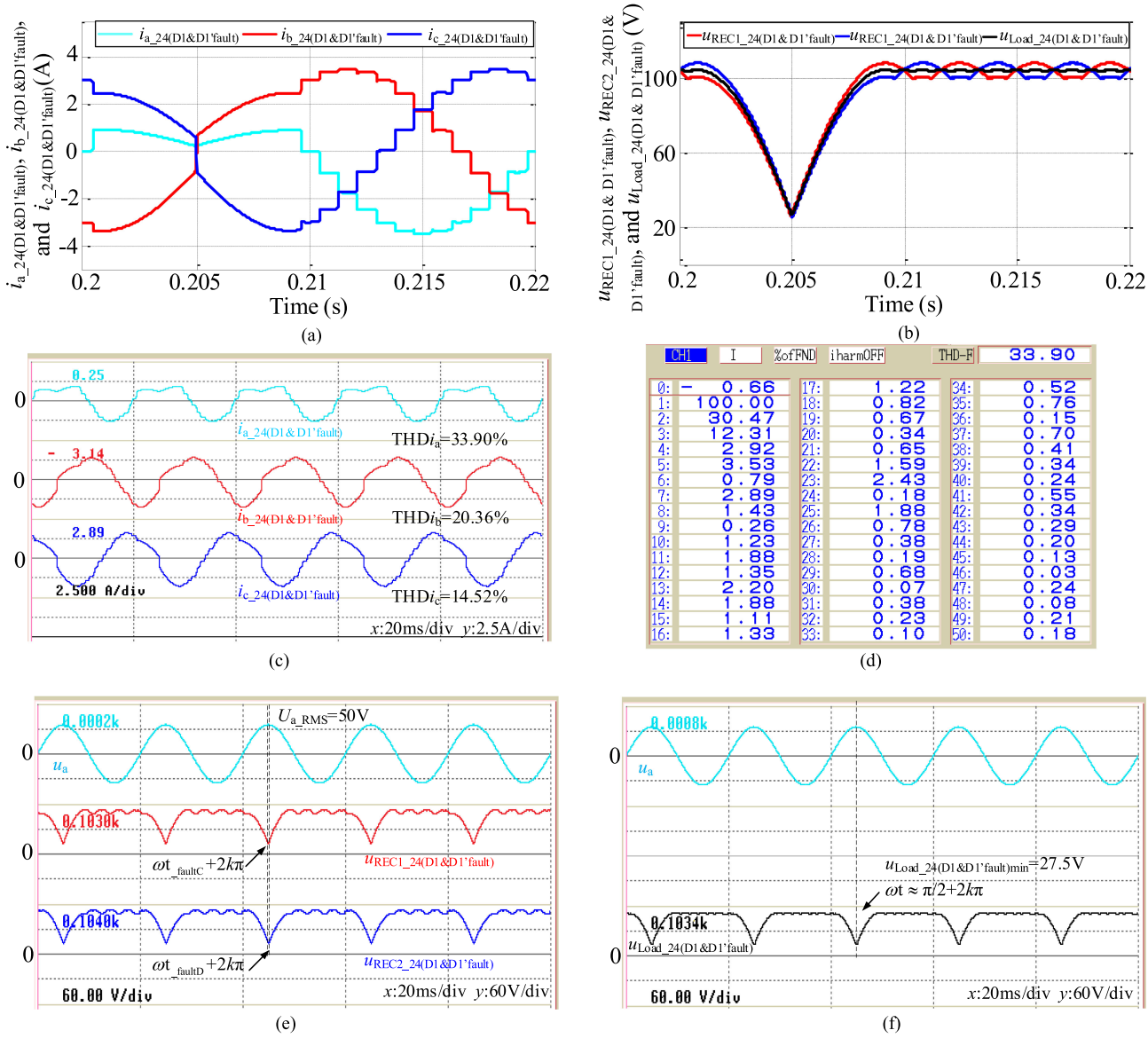

Fig. 15. Verification results of the power quality under diodes D_1 and D_1' open-circuit fault. (a) Simulation results of input currents $i_{a\_24(D1 \text{ and } D1'\text{fault})}$, $i_{b\_24(D1 \text{ and } D1'\text{fault})}$ and $i_{c\_24(D1 \text{ and } D1'\text{fault})}$. (b) Simulation results of voltages $u_{REC1\_24(D1 \text{ and } D1'\text{fault})}$, $u_{REC2\_24(D1 \text{ and } D1'\text{fault})}$, and $u_{Load\_24(D1 \text{ and } D1'\text{fault})}$. (c) Experiment results of input currents $i_{a\_24(D1 \text{ and } D1'\text{fault})}$, $i_{b\_24(D1 \text{ and } D1'\text{fault})}$, and $i_{c\_24(D1 \text{ and } D1'\text{fault})}$. (d) THD value and spectrum of input current $i_{a\_24(D1 \text{ and } D1'\text{fault})}$. (e) Experiment results of voltages $u_{REC1\_24(D1 \text{ and } D1'\text{fault})}$ and $u_{REC2\_24(D1 \text{ and } D1'\text{fault})}$. (f) Experiment result of voltage $u_{Load\_24(D1 \text{ and } D1'\text{fault})}$.

two didoes D_1 and D_2 open-circuit fault is the superposition of the single diode fault. In combination with load voltage waveforms, the fault type and locations of fault diodes can be determined.

2) From Figs. 14 and 15, the phase of the global minimum voltage is nearby the min-point of the common conduction interval of the two open-circuit diodes, the other fault intervals are kept consistent with the rule of single diode open-circuit fault. In experiment, the minimum values are close to the theoretical values and the phases exactly correspond to the theoretical analysis. When the length of the common conduction interval increases from $\pi/12$ to $\pi/4$, the voltage drop increases as follows.

3) Fig. 16 gives the experimental results under the diode VD_1 open-circuit fault. Compared with single diode fault in the main circuit, although affected interval of this kind fault increases, the voltage drop decreases and the minimum value of the load voltage is about 99.8 V in experiment.

In summary, all diode open-circuit fault types can be exactly distinguished based on the information reflected by the load voltage waveforms, but fault characteristics of input current waveforms and harmonic contents are less obvious and regular, so that it is more suitable to select the load voltage as a variable for fault detection. The load voltage drop under diode open-circuit fault is associated with the conduction angle of the diode under normal operation mode, reducing the conduction angle of

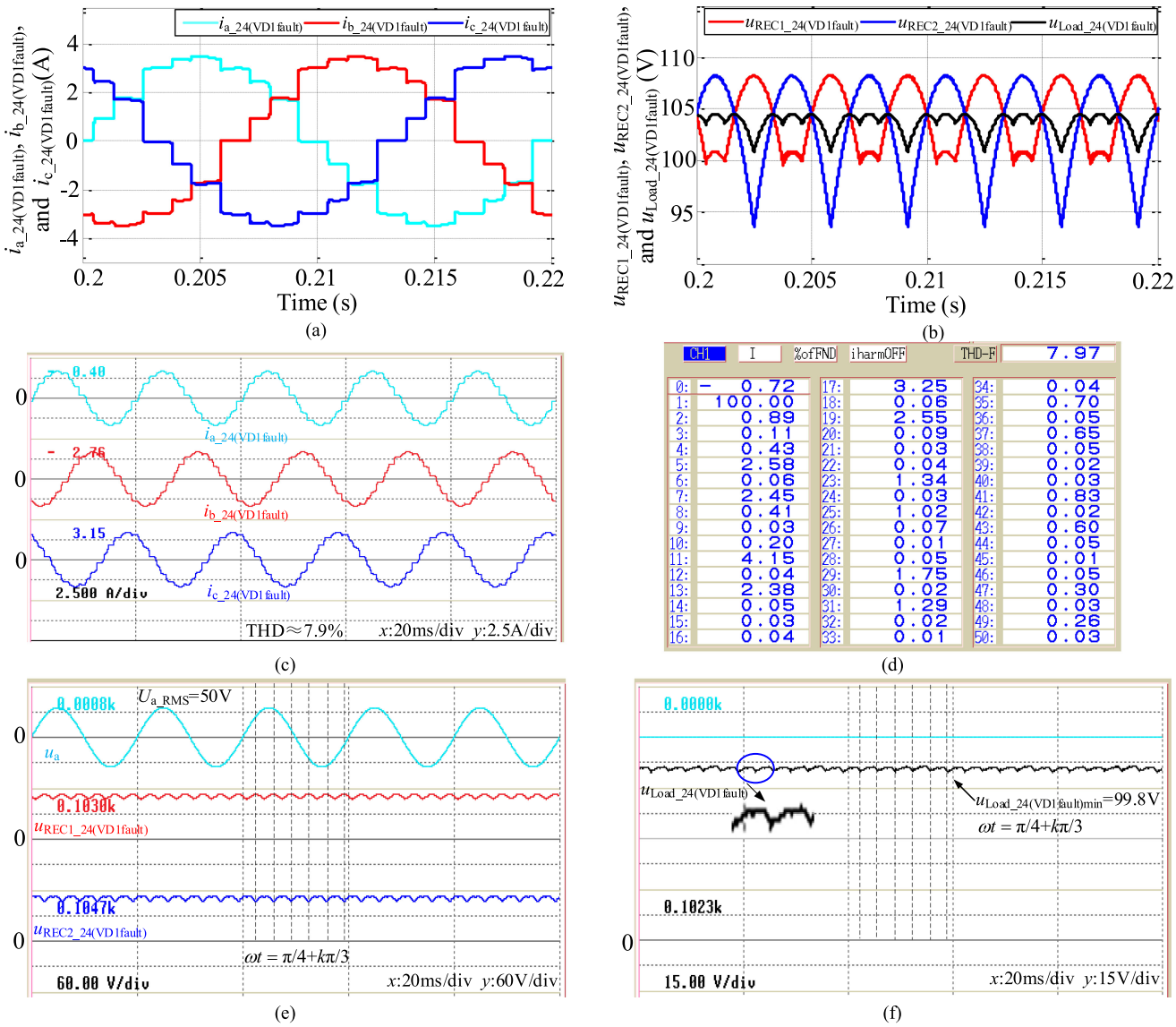

Fig. 16. Verification results of the power quality under diode VD_1 open-circuit fault. (a) Simulation results of input currents $i_{a\_24(VD1fault)}$, $i_{b\_24(VD1fault)}$, and $i_{c\_24(VD1fault)}$. (b) Simulation results of voltages $u_{REC1\_24(VD1fault)}$, $u_{REC2\_24(VD1fault)}$, and $u_{Load\_24(VD1fault)}$. (c) Experiment results of input currents $i_{a\_24(VD1fault)}$, $i_{b\_24(VD1fault)}$, and $i_{c\_24(VD1fault)}$. (d) THD value and spectrum of input current $i_{a\_24(VD1fault)}$. (e) Experiment results of voltages $u_{REC1\_24(VD1fault)}$ and $u_{REC2\_24(VD1fault)}$. (f) The experiment result of voltage $u_{Load\_24(VD1fault)}$.

each diode in the main circuit is a useful way to mitigate the fault voltage drop. The location of the fault diode is also related to the formation of the fault characteristic, generally, the fault occurs in the harmonic reduction circuit cause less damage to the power quality than that in the main circuit.

V. Conclusion

This article provides another method to determine the optimum turns ratio of the IPR from the perspective of minimizing the load ripple factor, this method can avoid some difficulties caused by complexity current relations of the phase-shifting transformer. Then, the operation modes of the MPR under some possible diode open-circuit fault cases are analyzed in detail, their corresponding voltage expressions are derived. The correctness of the theoretical analysis is verified by simulations and experiments. It is indicated that the load voltage can be seen as a typical parameter to accurately identify the fault type and location. Under all above mentioned diode open-circuit fault cases, the fault diode located in the main circuit often causes more obvious load voltage drop, the fault diode located in the harmonic reduction circuit shows less impact on the power quality. The impact range of the diode open-circuit fault increases as the increasing of the conduction angle during normal operation. When properly increasing the phase number of the diode bridge rectifiers in the main circuit, the conduction angle of each diode reduces, so that it should be an effective way to improve the fault tolerance ability of the rectifier.

APPENDIX

TABLE III
CONDUCTION SEQUENCE OF THE DIODES IN THE RECTIFIER UNDER NORMAL OPERATION.

Interval	Conduction Diodes	Interval	Conduction Diodes
$[0, \pi/24) \cup [47\pi/24, 2\pi]$	D_4, D_5, D_4', D_5'	$[23\pi/24, 25\pi/24)$	D_3, D_6, D_3', D_6'
$[\pi/24, \pi/8)$	D_4', D_5', VD_2, VD_3	$[25\pi/24, 9\pi/8)$	D_3', D_6', VD_2, VD_3
$[\pi/8, 5\pi/24)$	D_1, D_4, D_4', D_5'	$[9\pi/8, 29\pi/24)$	D_2, D_3, D_3', D_6'
$[5\pi/24, 7\pi/24)$	D_1, D_4, VD_1, VD_4	$[29\pi/24, 31\pi/24)$	D_2, D_3, VD_1, VD_4
$[7\pi/24, 3\pi/8)$	D_1, D_4, D_1', D_4'	$[31\pi/24, 11\pi/8)$	D_2, D_3, D_2', D_3'
$[3\pi/8, 11\pi/24)$	D_1', D_4', VD_2, VD_3	$[11\pi/8, 35\pi/24)$	D_2', D_3', VD_2, VD_3
$[11\pi/24, 13\pi/24)$	D_1, D_6, D_1', D_4'	$[35\pi/24, 37\pi/24)$	D_2, D_5, D_2', D_3'
$[13\pi/24, 5\pi/8)$	D_1, D_6, VD_1, VD_4	$[37\pi/24, 13\pi/8)$	D_2, D_5, VD_1, VD_4
$[5\pi/8, 17\pi/24)$	D_1, D_6, D_1', D_6'	$[13\pi/8, 41\pi/24)$	D_2, D_5, D_2', D_5'
$[17\pi/24, 19\pi/24)$	D_1', D_6', VD_2, VD_3	$[41\pi/24, 43\pi/24)$	D_2', D_5', VD_2, VD_3
$[19\pi/24, 7\pi/8)$	D_3, D_6, D_1', D_6'	$[43\pi/24, 15\pi/8)$	D_4, D_5, D_2', D_5'
$[7\pi/8, 23\pi/24)$	D_3, D_6, VD_1, VD_4	$[15\pi/8, 47\pi/24)$	D_4, D_5, VD_1, VD_4

REFERENCES

[1] B. Singh, G. Bhuvaneswari, V. Garg, and A. Chandra, "Star connected autotransformer based 30-pulse AC-DC converter for power quality improvement in vector controlled induction motor drives," in *Proc. IEEE Power India Conf.*, 2006, pp. 1–6.

[2] B. Singh, G. Bhuvaneswari, and V. Garg, "A tapped delta autotransformer based 24-pulse rectifier for variable frequency induction motor drives," in *Proc. IEEE Symp. Ind. Electron.*, 2006, pp. 2046–2051.

[3] A. N. Arvindan and A. Guha, "Novel topologies of 24-pulse rectifier with conventional transformers for phaseshifting," in *Proc. 1st Int. Conf. Elect. Energy Syst.*, 2011, pp. 108–114.

[4] J. Arrillaga and M. Villablanca, "A modified parallel HVDC convertor for 24 pulse operation," *IEEE Trans. Power Del.*, vol. 6, no. 1, pp. 231–237, Jan. 1991.

[5] S. Choi, B. S. Lee, and P. N. Enjeti, "New 24-pulse diode rectifier systems for utility interface of high-power AC motor drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 2, pp. 531–541, Mar./Apr. 1997.

[6] D. A. Paice, *Power Electronics Converter Harmonics: Multipulse Methods for Clean Power*. Hoboken, NJ, USA: Wiley, Sep. 1999.

[7] S. Yang, F. Meng, and W. Yang, "Optimum design of interphase reactor with double-tap changer applied to multipulse diode rectifier," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3022–3029, Sep. 2010.

[8] F. Meng, X. Xu, and L. Gao, "A simple harmonic reduction method in multipulse rectifier using passive devices," *IEEE Trans. Ind. Informat.*, vol. 13, no. 5, pp. 2680–2692, Oct. 2017.

[9] Y. Lian, S. Yang, K. Xu, Y. Li, and W. Yang, "Harmonic reduction mechanism at DC link of two different 24-pulse rectifiers," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2017, pp. 1–6.

[10] Y. Li, K. Xu, Y. Lian, W. Yang, and S. Yang, "A novel 36-pulse rectifier with a low loss interphase converter at DC side," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2017, pp. 2–7.

[11] L. Gao, X. Xu, Z. Man, and J. Lee, "A 36-Pulse diode-bridge rectifier using dual passive harmonic reduction methods at DC link," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1216–1226, Feb. 2019.

[12] S. Choi, "A three-phase unity-power-factor diode rectifier," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1711–1714, Dec. 2005.

[13] M. E. Villablanca, J. I. Nadal, and M. A. Bravo, "A 12-pulse AC–DC rectifier with high-quality input/output waveforms," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1875–1881, Sep. 2007.

[14] F. Meng, W. Yang, S. Yang, and L. Gao, "Active harmonic reduction for 12-pulse diode bridge rectifier at DC side with two-stage auxiliary circuit," *IEEE Trans. Ind. Informat.*, vol. 11, no. 1, pp. 64–73, Feb. 2015.

[15] Z. Liu, F. Meng, and W. Yang, "Harmonic reduction technology at DC link in star-connected-autotransformer-based multi-pulse rectifier," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2017, pp. 1–6.

[16] X. Lian, S. Yang, and W. Yang, "Optimum design of 48-pulse rectifier using unconventional interphase reactor," *IEEE Access*, vol. 7, pp. 61240–61250, 2019.

[17] F. J. Chivite-Zabalza, A. J. Forsyth, and D. R. Trainer, "A simple, passive 24-pulse AC–DC converter with inherent load balancing," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 430–439, Mar. 2006.

[18] F. J. Chivite-Zabalza and A. J. Forsyth, "A passive 36-pulse AC–DC converter with inherent load balancing using combined harmonic voltage and current injection," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1027–1035, May 2007.

[19] Q. Du, L. Gao, Q. Li, T. Li, and F. Meng, "Harmonic reduction methods at DC side of parallel-connected multipulse rectifiers: A review," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2768–2782, Mar. 2021.

[20] C. Shu, L. Wei, D. Rong-Jun, and C. Te-Fang, "Fault diagnosis and fault-tolerant control scheme for open-circuit faults in three-stepped bridge converters," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2203–2214, Mar. 2017.

[21] R. Kalpana, P. S. Prakash, V. S. Vidyasagar, and B. Singh, "Investigations on single-phasing effect of zigzag autoconfigured transformer based 12-pulse rectifier," in *Proc. IEEE Int. Conf. Power Electron. Drives Energy Syst.*, 2018, pp. 1–6.

[22] J. S. Perisé, M. Bakkar, and S. B. Rodríguez, "Open-circuit fault diagnosis and maintenance in multi-pulse parallel and series TRU topologies," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10906–10916, Oct. 2020.

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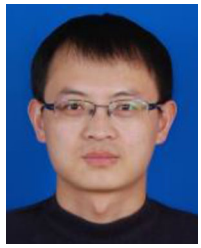

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