An Isolated High Step-Up Converter Based on the Active Secondary-Side Quasi-Resonant Loops

Pengyu Jia, *Member, IEEE*, Zhe Su, Tiancong Shao, *Member, IEEE*, and Yang Mei, *Member, IEEE*

***Abstract*—Resonant converter is a good solution as the isolated high step-up converter due to its soft-switching features and less component count. However, since the resonant tank is placed on the primary side (low-voltage side) in most traditional resonant converters, large input current still leads to a big proportion of power loss. Besides, synchronous rectification (SR) is also a big issue. The diode conducting time in a resonant converter is hard to be predicted so a current transformer or an analog SR chip is usually employed to detect the current zero-crossing point when the higher efficiency is required. In this article, an isolated high step-up converter with active secondary-side quasi-resonant tank is proposed. Since the whole resonant tank is placed on the high-voltage side, the current stress of the resonant capacitors and their power loss can be greatly alleviated. Besides, the analytical solution of the diode conducting time is derived and two SR control schemes are proposed, without the need to detect the current zero-crossing point. All the switches and diodes achieve the soft-switching so this leads to a good efficiency performance. The validity is confirmed by the experimental results of a 500 W prototype with 36–48 V input and 380 V output.**

***Index Terms*—DC–DC converter, high step-up converter, secondary-side resonant loop, soft switching, synchronous rectification (SR).**

I. Introduction

THE high gain converters attract more and more attentions in recent years with the development of renewable energy industry such as the fuel cell and photovoltaic (PV). For example, the two-stage configuration constructed by a front-end dc–dc converter and a grid-connected inverter is widely applied in the field of PV micro-inverter system, where a high-frequency (HF) transformer is usually employed within the dc/dc conversion stage [1]. Due to the low-voltage (LV) solar panel connected to the input, high step-up function must be achieved by the dc/dc converter, as shown in Fig. 1.

Manuscript received March 5, 2021; revised May 26, 2021; accepted July 16, 2021. Date of publication July 26, 2021; date of current version September 16, 2021. This work was supported in part by the National Natural Science Foundation of China under Grant 51907002 and in part by the Beijing Natural Science Foundation under Grant 3192012. Recommended for publication by Associate Editor D. Dujic. *(Corresponding author: Pengyu Jia.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3098852.

Digital Object Identifier 10.1109/TPEL.2021.3098852

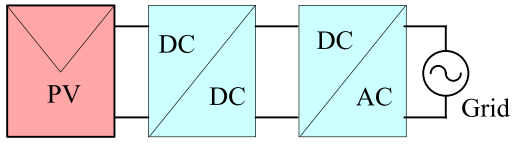

Fig. 1. Typical two-stage configuration diagram of the microinverter.

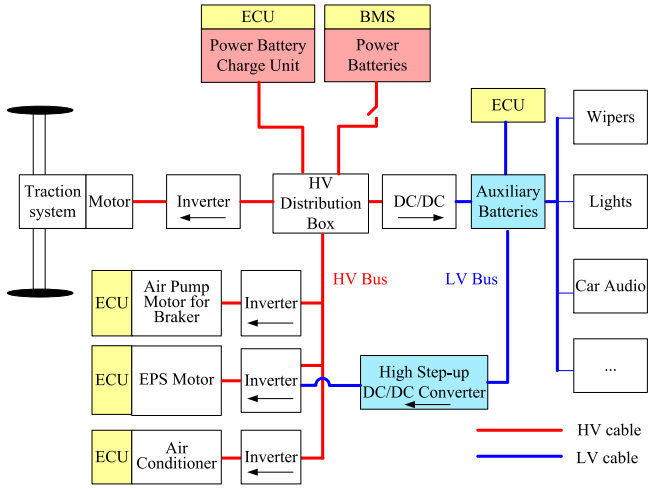

Fig. 2. Typical power distribution system diagram of the electric coach.

Besides, in the field of electrical vehicles (EVs), especially in electric coaches, high step-up converters are also employed and developed. There are two independent power systems in the EVs as shown in Fig. 2, i.e., high-voltage (HV) and LV power systems, respectively. The voltage rating of HV bus is 380–400 V dc, which is composed of lithium-ion batteries. The HV bus mainly supplies the inverters of motor drive and electrical power-steering (EPS) motor, etc. The LV bus is usually composed of lead-acid batteries and mainly supplies the computer system, lights, wipers, etc. If the HV bus is fault and breakdown while the EV is driving, the EPS and drive motor will be out of control. In case of that accident, a high step-up dc/dc converter is employed to supply the EPS motor by using LV batteries as the input, boosting its output up to 380–400 V dc range in an emergency [2]. Hence, the EPS can keep working to ensure EV leave the fast lane and stop at the emergency lane.

The isolated high step-up function can be easily achieved by a two-stage configuration of converters [3]–[6]. However, the low power density is the main defect. A hard-switching converter

employing a high-ratio step-up transformer, such as a flyback, can also obtain a high voltage gain but it usually shows a low efficiency due to the huge switching loss. Besides, high-ratio transformer always induces undesirable voltage spikes during the switching process due to the leakage inductance. These spikes increase the voltage stresses of switches. Moreover, the reverse-recovery loss of the rectifier diode is also a big issue and this will further degrade the efficiency. To alleviate these problems, nondissipative snubbers are introduced into flyback type converters to recycle the energy stored in the leakage inductance [7]–[9]. However, the core of the coupled-inductor (or transformer) in a flyback converter is magnetized only in the first quadrant and not fully utilized, so it is mainly applied in low power applications. In order to achieve a high voltage gain, a inductor structure named "Winding-Cross-Coupled Inductors" (WCCI) is proposed in [10]–[13]. Correspondingly, lots of topologies have been derived. These converters can achieve a high voltage gain with a relatively low component stress. However, the design process of the WCCI is complicated. Moreover, the leakage inductance of the WCCI can also lead to the voltage spikes. Therefore, active clamp circuit must be introduced, which increases the complexity of the circuit.

Impedance source converter is another effective solution to achieve high voltage gain. A shoot-through switching duration, which is the simultaneous conducting time of both switches in the same inverter's phase leg, is introduced into the impedance source converter. Hence, the energy can be accumulated in the inductors of the impedance networks. After that duration, the energy is released and boosts the output voltage [14]–[17]. However, the large primary-side current brings non-negligible power loss due to the complicated impedance networks placed at the input port, especially under high power condition. Furthermore, there exist other magnetic devices except the transformer so the power density is decreased.

The resonant converter, such as the *SRC*, *PRC,* and *LLC*, can be also applied to achieve the high voltage conversion ratio [18]–[26]. Since the stray parameters of the transformer can be utilized to make up the resonant tank, the device count and the cost can be very low. Moreover, their natural soft-switching features make the converters show a good efficiency performance. However, most traditional resonant converters are with a primary-side resonant tank, so the large input current still leads to a big proportion of power loss on the ESR of the resonant capacitors. Some literature have tried to move the passive components, i.e., capacitors and inductors, to the secondary side in order to decrease the power loss caused by the large primary-side current, such as [21]–[26]. In [21], an improved *LLC* converter with a notch filter is proposed in order to decrease the current stress in the resonant tank. By moving the notch filter from the primary side to the secondary side, the converter shows a better efficiency. However, the main resonant inductor cannot be moved to the high voltage side and it still takes a big proportion of power loss. In [22]–[24], the reverse structure of the traditional *LLC* converter is employed to realize the high voltage conversion ratio. By this means, the whole resonant tank is located at the high voltage side. However, since the voltage across the magnetizing inductance is always clamped by the input, the resonant tank only consists of one inductor and one capacitor. Therefore, the gain feature is similar to a traditional *SRC*, which results in a very wide frequency range especially in the light load condition. As a result, it is normally applied to provide the fixed voltage gain but not suitable for the variable voltage condition. In order to solve this problem, an additional inductor can be inserted into the ac port of the rectifier stage, so to make an equivalent *LLC* resonant tank on the high voltage side [25], [26]. By this means, the gain feature is the same as a traditional *LLC* converter. However, the high voltage gain normally requires a high transformer turns ratio [27]. Besides, the additional inductor also decreases the power density.

It also needs to be pointed out that an important issue of the resonant converter is the synchronous rectification (SR) realization. To achieve high efficiency, the rectifier diode can be replaced by active switches with proper driving pulses. Take an *LLC* converter for example, since it is difficult to accurately predict the conducting time of the rectifier switch, an SR chip or a current transformer (CT) is usually employed to detect the current zero-crossing point [28]–[30]. However, these additional circuits also increase the cost and the complexity of the converter.

In this article, a quasi-resonant high step-up converter is proposed. The converter is with the following features.

1) There are no other power devices on the primary side except the active switches, so the primary-side loss is in a very minor range.
2) The conducting time for all the switches and the rectifier diodes can be predicted so SR can be easily realized without detecting the current zero-crossing point.
3) The current stresses of the resonant capacitors are significantly decreased. Hence, the power loss caused by the capacitor ESR is reduced to a great extent.
4) Soft-switching can be naturally realized by all the switches and diodes.

The rest of this article is organized as follows: The operation principle of the proposed converter is presented in Section II. The steady-state operation process is analyzed in detail in Section III. Design considerations are given in Section IV. Two SR control schemes are presented in Section V and a prototype is performed in Section VI. Moreover, a comparison between the proposed converter and a traditional *LLC* converter is made in Section VII. Finally, the conclusion is summarized in Section VIII.

II. Operation Principle of the Proposed Converter

The proposed quasi-resonant converter is shown in Fig. 3. The primary-side circuit is realized by a full-bridge structure in order to generate the HF voltage square waveforms. Certainly, a half-bridge or a push-pull structure can be also employed instead. L_r and L_m, respectively, denote the resonant and magnetizing inductors. To simplify the analysis, L_m is assumed large enough so the transformer magnetizing current i_{Lm} can be neglected. Capacitors C_1 and C_2 are employed as the split resonant capacitors with the same value, where D_1 and D_2 are in parallel with them as the clamp diodes. Capacitors C_3 and C_4

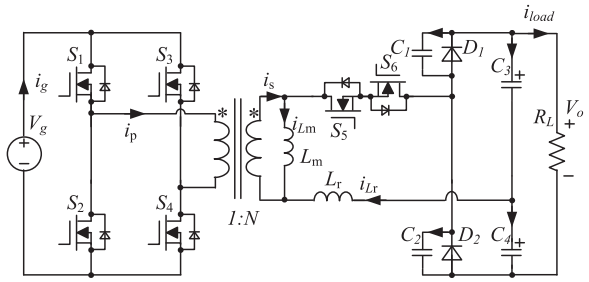

Fig. 3. Schematic of the proposed converter.

are the output filters. Their voltages can be considered constant and equal to half of the output. As a result, C_1, C_2, and L_r make up the resonant tank.

The converter operating modes are illustrated in Fig. 4. The actual current directions in different stages are marked by red arrows. The corresponding key waveforms during steady-state operation are shown in Fig. 5 and the reference positive directions are defined in Fig. 3. The duty ratios for all the switches are equal to 0.5 theoretically but a switching dead-time t_d must be introduced into the switches S_1–S_4 in order to avoid the shoot-through situation in the bridge leg.

There are eight operating modes in one switching period. For simplicity, only the first four modes are discussed in detail because the operation process is symmetrical.

Mode I ($t_0 < t < t_1$): When S_2, S_3, and S_6 are switched OFF at t_0, the turn-ON signals of S_1, S_4, and S_5 are not applied until the switching dead time t_d exhausts, which ranges from t_0 to t_1. Under the assumption that L_m is sufficiently large, the primary-side and secondary-side winding currents keep zero during t_d, which provides the sufficient conditions for ZCS turn-ON of the switches. The corresponding stages of Mode I is illustrated in Fig. 4(a).

Mode II ($t_1 < t < t_2$): The turn-ON driving signals are applied on S_1, S_4, and S_5 at t_1. The secondary-side winding voltage, v_{ab}, can be calculated as NV_g. Therefore, the resonant current i_{Lr} increases from zero and it flows though S_5 and the body diode of S_6, so S_5 realizes a ZCS turn-ON. The current flows through two resonant paths: One path consists of L_r, C_1, and C_3. The other path consists of L_r, C_2, and C_4. Because C_3 and C_4 provide large capacitance to filter the ripple, the resonant process is determined by L_r, C_1, and C_2. Since the primary-side winding current i_p is with the same shape of i_{Lr}, S_1 and S_4 also realize a ZCS turn-ON at t_1. The corresponding stages of Mode II is illustrated in Fig. 4(b).

Mode III ($t_2 < t < t_3$): At t_2, v_{C2} equals V_o and v_{C1} decreases to zero, so D_1 conducts while D_2 is still OFF. The resonant process is suspended at instant t_2. The inductor current i_L decreases linearly under the effect of v_{ab} and v_{C3}, where v_{ab} equals NV_g and v_{C3} equals V_o/2. Correspondingly, i_{D1} is with the same current decline rates as i_{Lr}. So does the current in the body-diode of S_6. Therefore, a ZCS turn-OFF can be guaranteed by both D_1 and the body-diode of S_6. So the diode reverse-recovery problem is alleviated. The corresponding stage of Mode III is illustrated in Fig. 4(c).

Mode IV ($t_3 < t < t_4$): At t_3, inductor current i_{Lr} decreases to zero. S_5 is still ON but there is no current through it. So the output stage is decoupled from the input stage. The load is supplied only by the output filter capacitors, C_3 and C_4. The switches S_1, S_4, and S_5 are switched OFF simultaneously at t_4 so the ZCS turn-OFF can be obtained. The corresponding stage of Mode IV is illustrated in Fig. 4(d).

The corresponding stages of Modes V–VIII are illustrated from Fig. 4(e)–(h). They are symmetrical to Mode I–IV as mentioned above, respectively.

III. Steady-State Analysis of the Proposed Converter

As discussed before, the converter operating process consists of two symmetrical parts in one switching period, so only the first four modes are necessary to calculate its steady-state input-output relationship.

From t_1 to t_2 (Mode II), the converter operates in resonant modes. The equivalent circuit can be described as Fig. 6. Due to the large capacitance of C_3 and C_4, the voltages v_{C3} and v_{C4} can be considered as constant voltage and equal to V_o/2. The resonant angular frequency ω_r is expressed as (1), where C_r is defined as the capacitance value of C_1 and C_2, besides, t_d denotes the dead time. The characteristic impedance R_0 is defined in (2). During this stage, the expressions of v_{C1}, v_{C2}, and i_{Lr} can be derived as (3)–(5), where M denotes the voltage gain

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{2C_rL_r}} \tag{1}$$

$$R_0 = \sqrt{\frac{L_r}{2C_r}} \tag{2}$$

$$\begin{cases} v_{C1} = V_g(\frac{M}{2}+N)\cos(\omega_r t - \omega_r t_d) + V_g(\frac{M}{2}-N) & (3) \\ v_{C2} = V_g(N+\frac{M}{2}) - V_g(N+\frac{M}{2})\cos(\omega_r t - \omega_r t_d) & (4) \\ i_{Lr} = \frac{V_g(M+2N)}{2R_0}\sin(\omega_r t - \omega_r t_d). & (5) \end{cases}$$

At t_2, voltage v_{C1} equals zero. Therefore, t_2 can be expressed as (6) according to (3)–(5)

$$\begin{aligned} t_2 &= \frac{1}{\omega_r}\arccos(\frac{2N-M}{2N+M}) + t_1 \\ &= \frac{1}{\omega_r}\arccos(\frac{2N-M}{2N+M}) + t_d. \end{aligned} \tag{6}$$

From t_2 to t_3 (Mode III), the resonant process is suspended and the resonant current i_{Lr} decreases linearly. The equivalent circuit can be described as Fig. 7. Therefore, v_{C1}, v_{C2}, and i_{Lr} can be derived as shown in the following:

$$\begin{cases} i_{Lr} = i_{Lr(t2)} + \frac{1}{L_r}(NV_g - \frac{V_o}{2})(t-t_2) & (7) \\ v_{C2} = V_o & (8) \\ v_{C1} = 0. & (9) \end{cases}$$

At t_3, i_{Lr} decreases to zero. According to (7)–(9), the duration from t_2 to t_3 can be derived as shown in the following

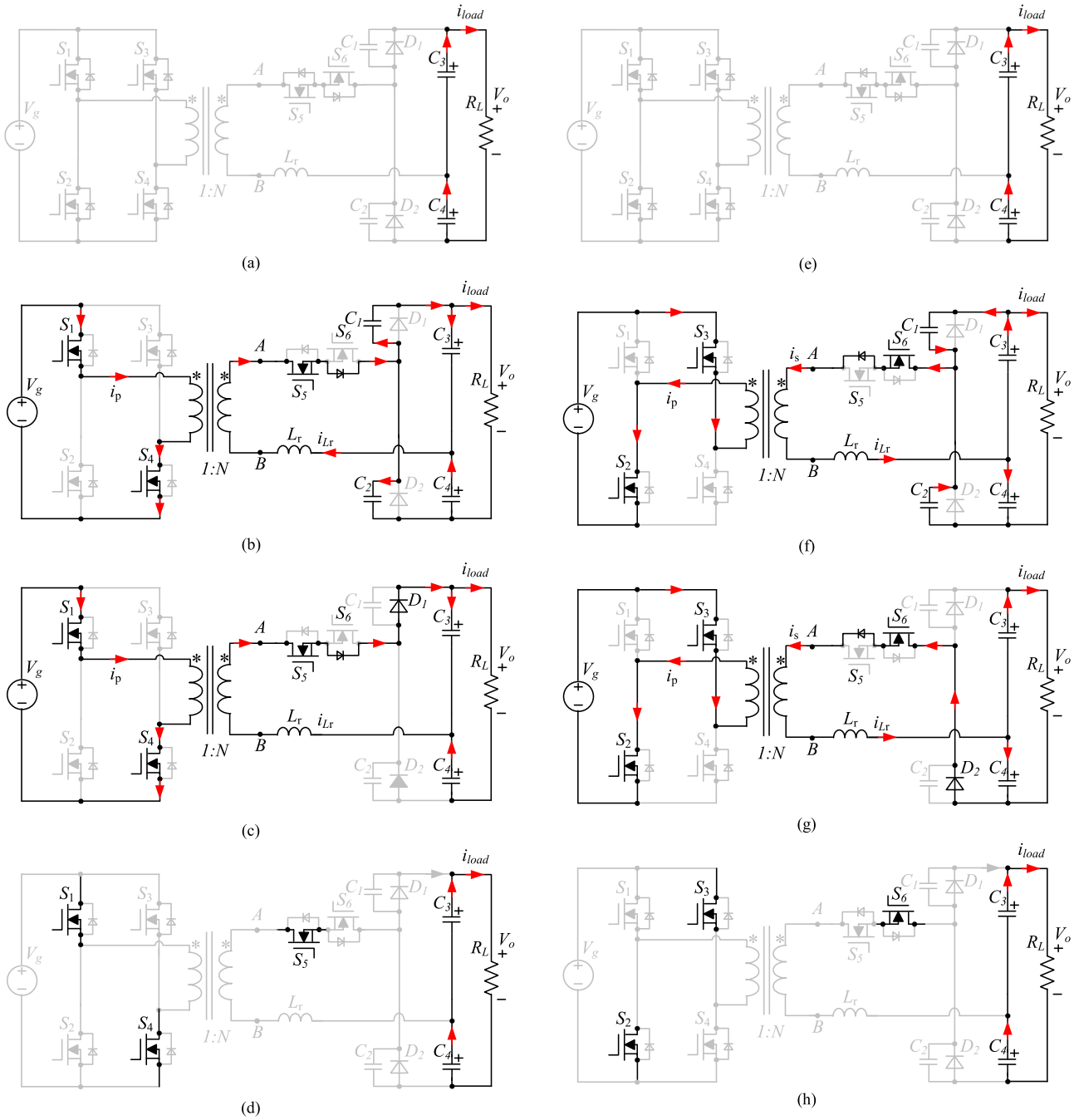

Fig. 4. Equivalent circuits of the proposed converter at different stages. (a) Mode I ($t_0 < t < t_1$). (b) Mode II ($t_1 < t < t_2$). (c) Mode III ($t_2 < t < t_3$). (d) Mode IV ($t_3 < t < t_4$). (e) Mode V ($t_4 < t < t_5$). (f) Mode VI ($t_5 < t < t_6$). (g) Mode VII ($t_6 < t < t_7$). (h) Mode VIII ($t_7 < t < t_8$).

equation:

$$t_3 - t_2 = \frac{2\sqrt{2MN}}{\omega_r(M-2N)}. \tag{10}$$

Because there is no current flowing through L_r from t_3 to t_5 (Modes IV and V), the average value of i_{Lr} in half switching period can be calculated as shown in the following equation:

$$I_{Lr\_avg} = \frac{2}{T_s}\left(\int_{t1}^{t2} i_{Lr}dt + \int_{t2}^{t3} i_{Lr}dt\right)$$

$$= 2f_s V_o\left(2C_r + \frac{4NC_r}{M-2N}\right). \tag{11}$$

Based on the energy conservation law, the following can be derived:

$$\frac{V_o^2}{R_L} = NV_g I_{Lr\_avg}. \tag{12}$$

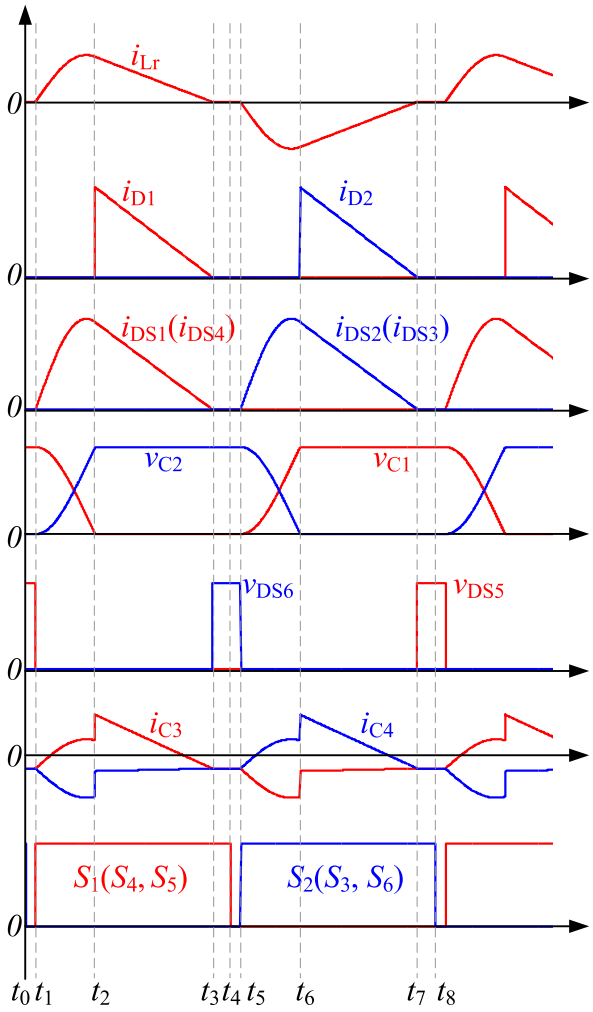

Fig. 5. Waveforms of the proposed converter.

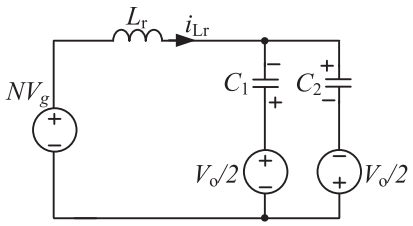

Fig. 6. Equivalent circuit model of proposed converter in Mode II.

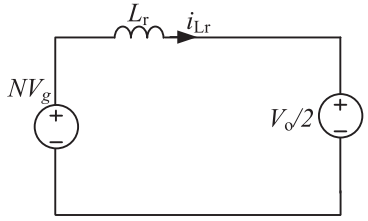

Fig. 7. Equivalent circuit model of the proposed converter in Mode III.

Finally, the voltage conversion ratio M can be given as shown in (13) according to (11) and (12)

$$M = 2N(1 + 2R_L C_r f_s) = \frac{N}{\pi}(2\pi + f_m Q) \tag{13}$$

where f_{m} denotes the normalized frequency and Q denotes the quality factor

$$f_m = \frac{f_s}{f_r} \tag{14}$$

$$Q = \frac{R_L}{R_0}. \tag{15}$$

From above, the voltage conversion ratio M shows a linear relationship with f_{m}. Therefore, the control scheme with pulse frequency modulation can be applied to regulate the output. The detailed derivation for (13) can be found at Appendix I.

IV. Design Consideration of the Proposed Converter

A. Design Considerations for the Quasi-Resonant Operation Modes

As discussed before, the converter operates in the quasi-resonant modes. It can be concluded that the duration from t_0 to t_3 must be less than $T_{\mathrm{s}}/2$, where T_{s} denotes the switching period. Therefore, the maximum switching frequency must be restricted. So the following inequality can be derived

$$t_3 - t_1 < \frac{1}{2f_s} - t_d. \tag{16}$$

According to (6) and (10), (16) can be simplified as the following equation:

$$\frac{f_m}{\pi}\arccos\left(\frac{-f_m Q}{4\pi + f_m Q}\right) + \frac{2}{Q}\sqrt{4 + \frac{2f_m Q}{\pi}} + 2f_s t_d < 1. \tag{17}$$

It is equivalent to another expression as shown in (18). Hence, the maximum resonant inductance $L_{r\_\max}$ can be computed

$$L_r < \left(\frac{1 - 2f_s t_d}{\frac{8f_s\sqrt{MNC_r}}{M-2N} + 2f_s\sqrt{2C_r}\arccos\left(\frac{2N-M}{2N+M}\right)}\right)^2. \tag{18}$$

B. Selection of Resonant Capacitance $\mathrm{C_r}$ and Inductance $\mathrm{L_r}$

For the design process of a converter, the input voltage V_g, voltage gain M and the nominal power P_{nominal} must be given first as the specification. As shown in (13), if M keeps constant during the load variation, f_{s} must change. Therefore, the maximum switching frequency $f_{s\_\max}$ is corresponding to the minimum load resistance $R_{L\_\min}$, which is determined by $(MV_g)^2/P_{\mathrm{nominal}}$. During design process, the switching frequency range should be determined firstly in order to facilitate the transformer design process.

Since there is the N factor in (13) but not in (17), so it can be considered as a design freedom-degree and should be determined at first. Meanwhile, the maximum switching frequency $f_{s\_\max}$ should be also determined as the premise. Then, the required resonant capacitance C_r can be computed according

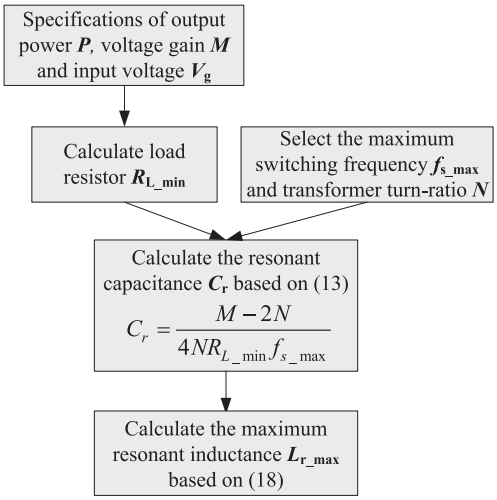

Fig. 8. Flowchart of the determination of C_r and L_r.

to (13) corresponding to $R_{L\_\min}$. After that, the maximum resonant inductance $L_{r\_\max}$ can be computed by (18). This design process can be illustrated by the flowchart in Fig. 8.

C. Design Considerations for the Magnetizing Inductance L_m

In the analysis above, the magnetizing inductance is assumed sufficiently large so a ZCS turn-ON can be realized by all the primary-side switches. However, L_m cannot be infinity in practical. Since the voltage across L_m is always clamped by v_{ab}, the maximum magnetizing current i_{Lm} can be calculated. Correspondingly, we can also set a permissible magnetizing current ripple Δi_{Lm} and so to derive the minimum value for L_m, as shown in (19) and (20). With a small value of Δi_{Lm}, the primary-side switches can be considered with a ZCS turn-ON approximately

$$L_m = \frac{NV_g}{2f_s\Delta i_{Lm}} \tag{19}$$

$$\Delta i_{Lm} = \frac{2\left|i_{DS1}(t_1)\right|}{N} = \frac{2\left|i_{DS2}(t_5)\right|}{N}. \tag{20}$$

D. Selection of Active Switches and Diodes

The current stresses of D_1 and D_2 are equal to $i_{Lr}(t_2)$, so this value can be expressed as (21) according to (5) and (6)

$$i_{D1,D2\_\max} = \frac{V_g(M+2N)}{2R_0}\sin(\omega_r t_2 - \omega_r t_d) = \frac{V_g\sqrt{2MN}}{R_0}. \tag{21}$$

The current stresses of S_3 and S_4 are equal to the maximum value of i_{Lr}. This value can be computed according to the following equation:

$$i_{Lr\_\max}, i_{S3,S4\_\max} = \begin{cases} \frac{V_g(\frac{M}{2}+N)}{R_0}, & \omega_r(t_2-t_d) > \frac{\pi}{2} \\ \frac{V_g\sqrt{2MN}}{R_0}, & 0 < \omega_r(t_2-t_d) < \frac{\pi}{2}. \end{cases} \tag{22}$$

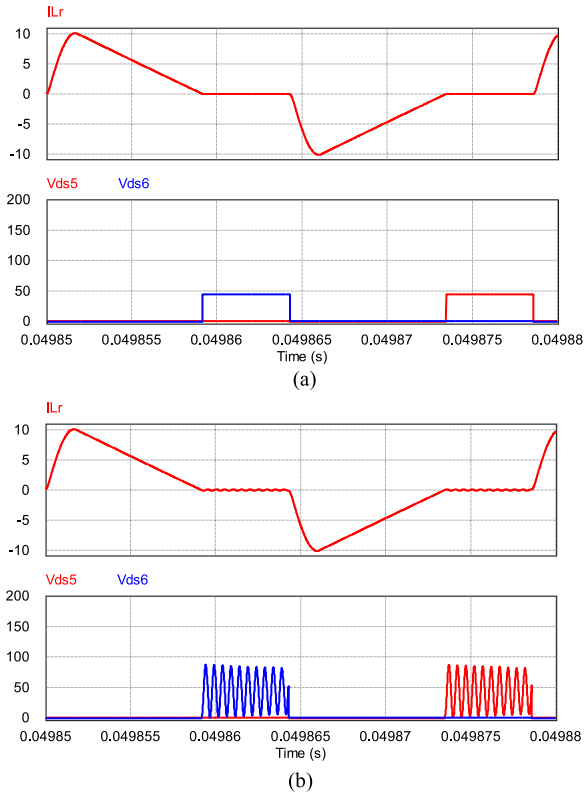

Fig. 9. Simulated waveform results of v_{DS5} and v_{DS6}. (a) Simulated waveforms with ideal active switches as S_5 and S_6. (b) Simulated waveforms with practical switch parameters for S_5 and S_6.

The current stresses of S_1 and S_2 can be derived as (23) approximately according to the following equation:

$$i_{S1,S2\_\max} \approx \begin{cases} \frac{NV_g(\frac{M}{2}+N)}{R_0}, & \omega_r(t_2-t_d) > \frac{\pi}{2} \\ \frac{NV_g\sqrt{2MN}}{R_0}, & 0 < \omega_r(t_2-t_d) < \frac{\pi}{2}. \end{cases} \tag{23}$$

From Fig. 4, the voltage stresses of S_1–S_4 are equal to V_g and those of D_1 and D_2 are equal to V_o. The voltage stresses for S_5 and S_6 can be computed according to Fig. 4, which is equal to $V_o/2 - NV_g$ theoretically. However, it should be pointed out that there is drain-source capacitance in the active switch, which can resonate with L_r after the inductor current decreases to zero. If the drain-source capacitance is constant, its maximum voltage is twice that in Fig. 9(a) because the drain-source voltages only resonate in the positive value range due to the body diode as shown in Fig. 9(b), which means

$$v_{DS5,6\_\max} = V_o - 2NV_g. \tag{24}$$

However, it must be pointed out that the drain-source capacitance C_{ds} can vary with the change of the drain-source voltage v_{ds}. Especially in the low voltage condition, the C_{ds} can show a big capacitance value, which is normally equal to several nanofarads. However, this capacitance can be changed to several picofarads when its voltage increases to a high voltage range. This nonlinear capacitance results in a slow resonant process under a low v_{ds} value but a fast resonant process under a

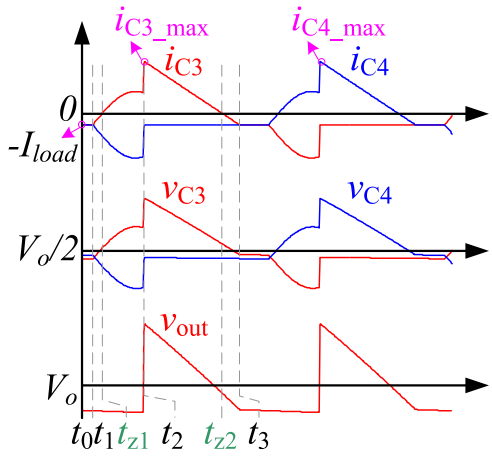

Fig. 10. Key waveforms of output filter stage with consideration of ESR.

high v_{ds} value. Besides, this phenomenon also leads to a higher voltage value in practice than the computed result in (24). To get a more precise value for the voltage stress of S_5 and S_6, we first need to obtain the mathematical function expression between C_{ds} and v_{ds}. By referring to the datasheet of a certain MOSFET, a group of C_{ds} ($C_{ds} = C_{\text{oss}} - C_{\text{rss}}$) versus v_{ds} numbers can be obtained. Since these two variables approximately show an power function relationship, the mathematical expression ($C_{ds} = f(v_{ds}) = a(v_{ds}+b)^{-c}$) can be easily accomplished by adding a trend curve with a simple EXCEL software or other mathematical software. Then, by solving the following nonlinear differential equations, we can finally obtain the maximum value of v_{ds}. An example to predict the maximum voltage values of S_5 and S_6 is given in Section VI

$$\begin{cases} C_{ds}\frac{dv_{ds}}{dt} = i_{Lr} \\ L_r\frac{di_{Lr}}{dt} + v_{ds} = \frac{V_o}{2} - NV_g \\ C_{ds} = a(v_{ds}+b)^{-c}. \end{cases} \tag{25}$$

E. Selection of Output Filter Capacitors C_3 and C_4

The filter capacitors C_3 and C_4 should provide sufficiently low impedance in order to filter output voltage ripple effectively. Usually, a high voltage rated capacitor normally shows a non-negligible ESR value and the output ripple is mainly affected by it. Therefore, the voltages v_{C3} and v_{C4} are with the same waveform shapes of capacitor current i_{C3} and i_{C4}, as shown in Fig. 10. Here capacitors C_3 and C_4 are supposed the same with each other. The instants t_{z1} and t_{z2} respectively denote the time instants when i_{C3} equals zero.

The output voltage v_{out} always equals the sum of v_{C3} and v_{C4}. From t_1 to t_2, v_{C3} and v_{C4} vary in the opposite directions. The sum of these two voltages, i.e., output voltage v_o, still shows a constant voltage value. Hence, the output voltage ripple can be calculated approximately by

$$\Delta v_{out} = R_{esr}(i_{C3,C4\_\max} + I_{load}). \tag{26}$$

The maximum values of i_{C3} and i_{C4} can be given in (27) according to Fig. 4

$$\begin{aligned} i_{C3,C4\_\max} &= i_{Lr}(t_2) - I_{load} \\ &= \frac{(M+2N)V_g}{2R_0}\sin(\omega_r t_2 - \omega_r t_d) - I_{load} \\ &= \frac{V_g\sqrt{2MN}}{R_0} - I_{load}. \end{aligned} \tag{27}$$

By substituting (27) into (26), the output voltage ripple of converter can be estimated by the following equation:

$$\Delta v_{out} = \frac{V_g R_{esr}\sqrt{2MN}}{R_0}. \tag{28}$$

F. Power Loss Estimation

The power loss of each primary-side switch can be computed according to (29). With a large magnetizing inductance, the magnetizing current is omitted here and so the switch can be considered with a ZCS turn-ON. Note that there is also the loss caused by the drain-source capacitance C_{ds} when the switch is turned ON

$$\begin{aligned} P_{primos} &= R_{ds-pri}N^2 f_s \int_{t1}^{t3} i_{Lr}^2 dt + \frac{1}{2}C_{ds}V_g^2 f_s \\ &= R_{ds-pri}N^2 f_s \left[\frac{V_g^2(M+2N)^2 \arccos\left(\frac{2N-M}{2N+M}\right)}{8\omega_r R_0^2}\right. \\ &\quad \left. - \frac{V_g^2(2N-M)\sqrt{2MN})}{4\omega_r R_0^2} + \frac{4V_g^2 MN\sqrt{2MN}}{3\omega_r R_0^2(M-2N)}\right] \\ &\quad + \frac{1}{2}C_{ds}V_g^2 f_s. \end{aligned} \tag{29}$$

The power loss of the secondary-side active switch can be distributed into three parts. When the current flows from drain to source (t_1–t_3), the conduction resistance mainly contributes the power loss and this proportion can be described as the following equation:

$$\begin{aligned} P_{\text{sec}\,mos-pos} &= R_{ds-\text{sec}} f_s \int_{t1}^{t3} i_{Lr}^2 dt \\ &= R_{ds-\text{sec}} f_s \left[\frac{V_g^2(M+2N)^2 \arccos\left(\frac{2N-M}{2N+M}\right)}{8\omega_r R_0^2}\right. \\ &\quad - \frac{V_g^2(2N-M)\sqrt{2MN})}{4\omega_r R_0^2} \\ &\quad \left. + \frac{4V_g^2 MN\sqrt{2MN}}{3\omega_r R_0^2(M-2N)}\right]. \end{aligned} \tag{30}$$

When the current flows from source to drain (t_5–t_7), this proportion of loss can be computed as (31) since the body-diode conducts

$$P_{\sec mos-diode} = V_F f_s \int_{t1}^{t3} i_{Lr} dt = \frac{V_F f_s V_g M^2}{\omega_r R_0 (M-2N)}. \quad (31)$$

Besides, there is also the loss provoked by the drain-source capacitance. Hence, the power loss of the secondary-side active switch can be finally described as the following equation:

$$P_{\sec mos} = P_{\sec mos-pos} + P_{\sec mos-diode} + \frac{1}{2} C_{ds} V_{ds}^2 f_s \quad (32)$$

where V_{ds} can be found in (24).

The clamp-diode loss can be computed as the following equation:

$$\begin{aligned} P_{clamp-diode} &= f_s V_F \int_{t2}^{t3} i_{d1} dt \\ &= \frac{2 f_s V_F \sqrt{2MN}}{\omega_r (M-2N)} \left[\frac{V_g (M+2N)}{2R_0} \sin \omega_r (t_2 - t_1) \right. \\ &\quad \left. + \frac{(2NV_g - V_o)\sqrt{2MN}}{2\omega_r L_r (M-2N)} \right] \\ &= \frac{4MN f_s C_r V_F V_g}{M-2N} \\ &= \frac{M V_g V_F}{R_L}. \end{aligned} \quad (33)$$

The power loss produced by each filter capacitor can be computed as the following equation:

$$\begin{aligned} P_{Co\_esr} &= R_{esr} f_s \int_{t0}^{t8} i_{C3,C4}^2 dt \\ &= R_{esr} f_s \left[\int_{t0}^{t1} (-I_{load})^2 dt + \int_{t1}^{t2} \left(\frac{i_{Lr}}{2} - I_{load} \right)^2 dt \right. \\ &\quad + \int_{t2}^{t3} (i_{Lr} - I_{load})^2 dt + \int_{t3}^{t5} (-I_{load})^2 dt \\ &\quad \left. + \int_{t5}^{t6} \left(-\frac{i_{Lr}}{2} - I_{load} \right)^2 dt + \int_{t6}^{t8} (-I_{load})^2 dt \right] \\ &= P_{part1} + P_{part2} + P_{part3} + P_{part4} \end{aligned} \quad (34)$$

where P_{part1} to P_{part4} is defined and simplified as follows:

$$\begin{aligned} P_{part1} &= R_{esr} f_s I_{load}^2 (t_1 - t_0 + t_5 - t_3 + t_8 - t_6) \\ &= R_{esr} f_s I_{load}^2 \left[T_s - \frac{2}{\omega_r} \arccos \left(\frac{2N-M}{2N+M} \right) \right. \\ &\quad \left. - \frac{2\sqrt{2MN}}{\omega_r (M-2N)} \right] \end{aligned} \quad (35)$$

$$\begin{aligned} P_{part2} &= R_{esr} f_s \int_{t1}^{t2} \left(\frac{i_{Lr}}{2} - I_{load} \right)^2 dt \\ &= R_{esr} f_s \left[\left(\frac{V_g^2 (M+2N)^2}{32\omega_r R_0^2} + \frac{I_{load}^2}{\omega_r} \right) \right. \\ &\quad \times \arccos \left(\frac{2N-M}{2N+M} \right) \\ &\quad \left. - \frac{V_g^2 (2N-M)\sqrt{2MN}}{16\omega_r R_0^2} - \frac{M V_g I_{load}}{\omega_r R_0} \right] \end{aligned} \quad (36)$$

$$\begin{aligned} P_{part3} &= R_{esr} f_s \int_{t2}^{t3} (i_{Lr} - I_{load})^2 dt \\ &= \frac{2R_{esr} f_s \sqrt{2MN}}{\omega_r (M-2N)} \\ &\quad \times \left(I_{load}^2 - \frac{V_g I_{load} \sqrt{2MN}}{R_0} + \frac{2MNV_g^2}{3R_0^2} \right) \end{aligned} \quad (37)$$

$$\begin{aligned} P_{part4} &= R_{esr} f_s \int_{t5}^{t6} \left(-\frac{i_{Lr}}{2} - I_{load} \right)^2 dt \\ &= R_{esr} f_s \left[\left(\frac{V_g^2 (M+2N)^2}{32R_0^2} + I_{load}^2 \right) \right. \\ &\quad \times \frac{1}{\omega_r} \arccos \left(\frac{2N-M}{2N+M} \right) + \frac{V_g I_{load} M}{\omega_r R_0} \\ &\quad \left. - \frac{2V_g^2 (2N-M)\sqrt{2MN}}{32\omega_r R_0^2} \right]. \end{aligned} \quad (38)$$

V. Improved SR Control

According to Section II, the current i_{L} always flows through one reverse-diode of the secondary-side switch. Since the switches S_5 and S_6 are present, an improved SR control scheme can be obtained.

In Fig. 5, if the driving signal falling-edge of S_5 is postponed from t_4 to t_7, the SR can be actively realized by S_5. Similarly, S_6 can operate in the same way. Hence, the delay time for the falling-edge can be calculated as follows:

$$\begin{aligned} t_7 - t_4 &= t_3 - t_0 \\ &= \frac{2\sqrt{2MN}}{\omega_r (M-2N)} + \frac{1}{\omega_r} \arccos \left(\frac{2N-M}{2N+M} \right) + t_d. \end{aligned} \quad (39)$$

This SR scheme is implemented only by changing the pulse modulation but the clamping diodes D_1 and D_2 are still present, so it can be defined as the "partial-SR" for the converter. In order to achieve a "full-SR," the clamp diodes can be replaced by two switches (S_7 and S_8) as shown in Fig. 11. Correspondingly, the control pulses for different switches can be illustrated in Fig. 12. The conducting time of S_7 and S_8 can be calculated according to (10). The delay time for the driving rising edges between S_7 and S_1, that is the duration from t_1 to t_2, can be obtained by (6). With the full-SR control scheme, the power loss of the secondary-side active switches can be revised from (32) to (40), where $P_{\text{secmos-pos}}$ is given in (30). Besides, the power loss of the clamp SR switch can be revised from (33) to (41).

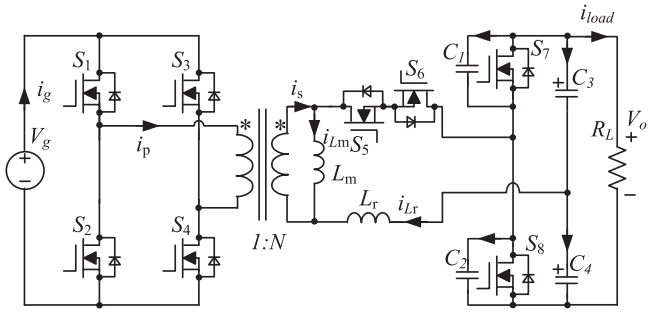

Fig. 11. Proposed converter with active clamp switch.

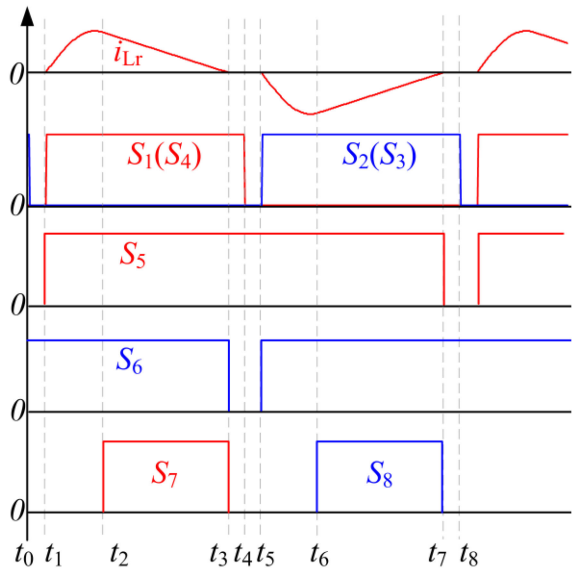

Fig. 12. Driving pulses of full-SR control scheme.

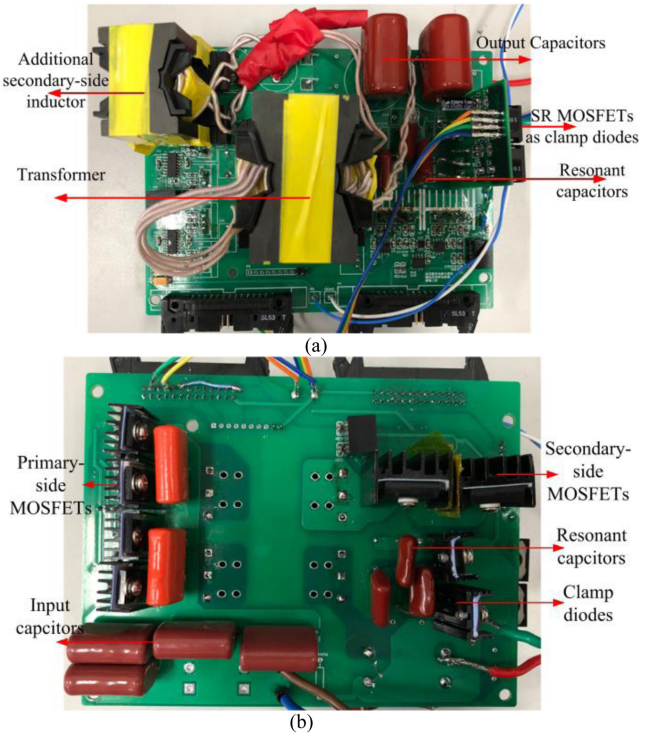

Fig. 13. Photograph of the proposed converter prototype. (a) Top side. (b) Bottom side.

As discussed before, it is clear that the SR realization is based on only three formulas, which are (6), (10), and (39). Since the turns ratio N, the natural resonant angular frequency ω_r and the switching dead time t_d are all determined beforehand, the only variable is the voltage conversion ratio M. That means, the SR scheme is independent of the power level. For a dc/dc converter, the output detection circuit always exists because the output voltage is always required to be regulated at the specified value in most situations. Hence, we only need to add the input voltage detection circuit to compute the time durations of t_1–$t_2(t_5$–$t_6)$, t_2–$t_3(t_6$–$t_7)$, t_0–$t_3(t_4$–$t_7)$. This can be realized by a simple resistor divider when the control system has a common ground with the primary-side circuits. The computation can be accomplished by a digital signal processor, such as a DSP28x series chip. Although there are trigonometrical and square root functions in the formulas, they can be fast solved by including some mathematical library files provided by the supplier, such as the "C28x Floating Point Unit fastRTS Library" provided by Texas Instruments

$$P_{\sec mos} = 2P_{\sec mos-pos} + \frac{1}{2}C_{ds}V_{ds}^2 f_s \qquad (40)$$

$$P_{clamp-diode\_SR} = f_s R_{ds\_on}\int_{t2}^{t3} i_{D1}^2 dt = \frac{2R_{ds\_on}V_g^2\sqrt{2M^3N}}{3R_L R_0}. \qquad (41)$$

VI. Experimental Verification

A 500-W prototype of the proposed converter is built to verify the theoretical conclusions. The photograph of the prototype is shown in Fig. 13. The nominal input voltage is 42 V that can vary from 36 to 48 V and the output voltage is regulated at 380 V. The proposed partial-SR and full-SR schemes are both applied to the prototype.

As shown in Fig. 8, the resonant parameters are selected with the considerations of the maximum switching frequency $f_{s\_\max}$ and the transformer turns ratio N. Meanwhile, the maximum value of resonant inductance, i.e., $L_{r\_\max}$, must be restricted by (18) in order to guarantee the quasi-resonant operation mode. That means, when the resonant inductance is selected equal to $L_{r\_\max}$, the durations t_3–t_4 and t_7–t_8 are eliminated. Obviously, the current stresses can be decreased with the increase of L_r according to (21)–(23) but note that L_r cannot exceed $L_{r\_\max}$. Hence, L_r is usually selected slightly less than its theoretical maximum value from (18).

From (13) it can be concluded that $f_{s\_\max}$ depends on the lowest input voltage and the nominal power point. That means the maximum switching frequency appears when V_g is 36 V, V_{out} is 380 V and R_{L} is 289 Ω. In the prototype, $f_{s\_\max}$ is designed

TABLE I
DIFFERENT RESONANT PARAMETERS AND CURRENT STRESSES CORRESPONDING TO DIFFERENT TURNS RATIO ($V_g = 36$ V, $P = 500$ W, $f_{s\_max} = 80$ kHz)

N	C_r (nF)	L_{r_max} (μH)	R_0 (Ω)	f_m	Q	Primary-side Peak current (A)	Secondary-side Peak current (A)
1	92.6	18.3	9.94	0.93	29.07	22.75	22.75
2	35.5	34	21.88	0.78	13.21	23.96	11.98
3	16.4	41.7	35.64	0.59	8.11	25.08	8.36
4	6.91	35.7	50.82	0.35	5.69	26.29	6.57
5	1.2	10.9	67.42	0.08	4.29	27.44	5.49

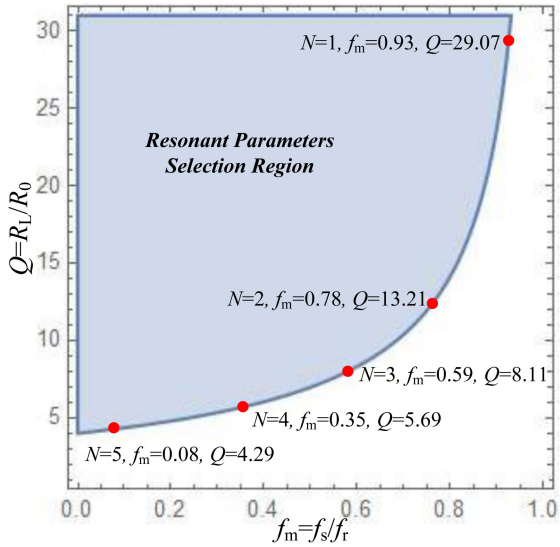

Fig. 14. Resonant parameters selection region with different turn-ratios.

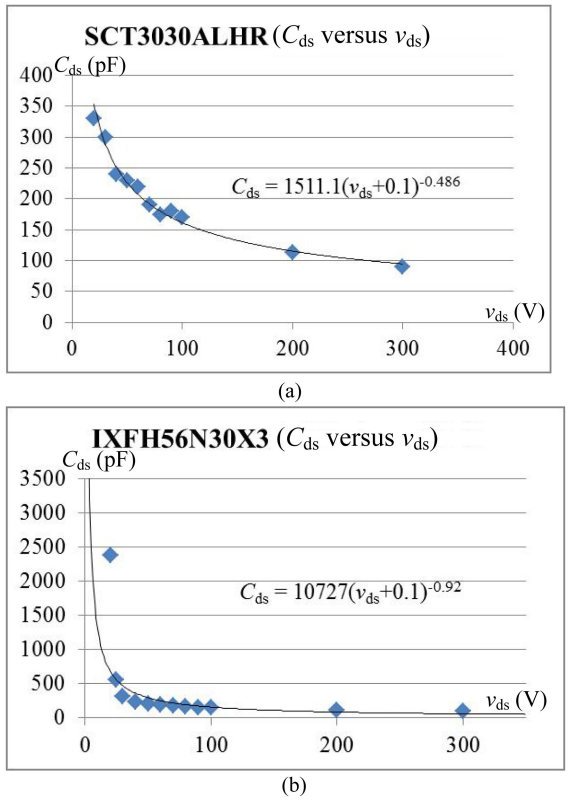

Fig. 15. Curve fitting for the C_{ds} of a MOSFET. (a) SCT3030ALHR (silicon carbide MOSFET). (b) IXFH56N30X3 (silicon MOSFET).

around 80 kHz. Hence, different values of C_r can be obtained with different selection for N values. The current stresses of both the primary-side and the secondary-side windings are calculated with different N values, which are listed in Table I, where the resonant inductance is selected equal to L_{r_max} from (18). The current stresses of the secondary-side winding can be alleviated by increasing N.

The selection region for the resonant parameters, which is shaded with blue, is illustrated in Fig. 14 based on (17). The different rows of Table I are marked by red points and they are on the border line of the selection region. If the resonant inductance is selected less than L_{r_max}, these points move towards the inside of the blue shaded area.

With the increase of N, f_m will decrease gradually. This will lead to a short-time resonant stage and a long-time diode-clamping stage. That means the duration of t_1–t_2 (t_5–t_6) is decreased while the duration of t_2–t_3 (t_6–t_7) is increased. It needs to be pointed out that the leakage inductance of a transformer with high turns ratio is hard to be controlled in a minor range and, sometimes, this value may exceed L_{r_max}. Therefore, the turns ratio of the prototype is finally selected equal to 3, considering the tradeoff between the current stresses and the design feasibility of the transformer leakage inductance.

The switch device for S_5 and S_6 needs to be carefully selected based on the predicted voltage stress value. As discussed in Section IV-D, the drain-source capacitance value can lead to higher peak voltage than the theoretical result in (24) because the capacitance varies dramatically with the drain-source voltage. Strictly speaking, the resonant process in Fig. 9(b) is a nonlinear process. This can be predicted by solving the nonlinear differential (25). The analytical solution of v_{ds_max} normally shows a big value when considering the characteristics of a silicon MOSFET. The value of C_{ds} can reach more than several tens of nanofarads but decrease to several tens of picofarads as the voltage increases. Fortunately, this phenomenon can be alleviated by using a silicon carbide MOSFET since the difference between its maximum and minimum capacitances is much smaller than that of a silicon MOSFET. Here, we take a silicon MOSFET (IXFH56N30X3) and a silicon carbide device (SCT3030ALHR) to make a comparison for example. Fig. 15 shows their drain-source capacitance trend curves and the corresponding function expressions. Fig. 16 illustrates their predicted waveforms when S_5 or S_6 resonate with the inductor by the Mathematica software based on (25). Obviously, the maximum drain-source voltage exceeds the silicon MOSFET'S rated voltage (300 V). Besides, the phenomenon of a fast resonance with high v_{ds} and a slow resonance with low v_{ds} is also observed.

However, the peak voltage is less than 240 V in the whole operating range with the use of the silicon carbide MOSFET. Moreover, the peak voltage will be less than this predicted value in a practical circuit due to the existence of the stay resistance so the resonant process shows a damped oscillation.

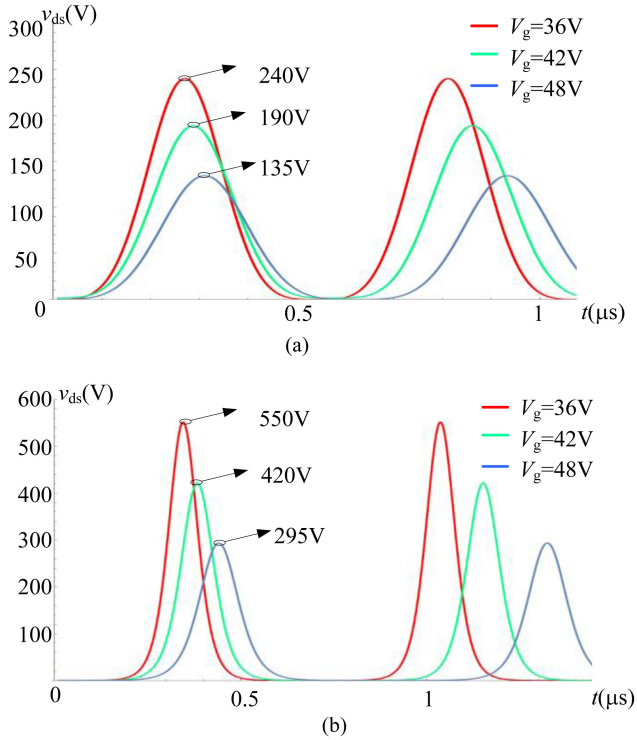

Fig. 16. Predicted resonant waveforms for the C_{ds} of a MOSFET. (a) SCT3030ALHR (silicon carbide MOSFET). (b) IXFH56N30X3 (silicon MOSFET).

Nevertheless, the minimum voltage rating for a silicon carbide MOSFET is 650 V. Hence, the 650 V silicon carbide MOSFET is selected as the switch device for S_5 and S_6 of the prototype.

Finally, the main circuit parameters of the prototype are determined as shown in Table II. In order to achieve both the ZCS turn-ON and turn-OFF for the primary-side and secondary-side switches, a large L_m value is obtained by tightly combine the transformer core without additional air gap.

The experimental waveforms of the prototype under nominal power condition are given in Fig. 17. The decline rate of the secondary-side winding current, i_{Lr}, is restricted by the resonant inductor L_r. Therefore, the reverse-recovery problems of D_1 and D_2 are significantly alleviated. According to (7), the current decline rate ranges from only 1.46 to 2.6 A/μs corresponding to the whole input voltage range.

The measured efficiency curves are plotted in Fig. 18. The power loss under nominal power and the corresponding breakdown illustrations are shown in Fig. 19. The efficiency with full-SR control scheme is increased up to about 0.2% higher than that with partial-SR scheme. Moreover, the loss of the resonant capacitors only contributes less than 1% over the total loss due to the small secondary-side current.

VII. Performance Comparison With an *LLC* Converter

The *LLC* resonant converter shows a good efficiency performance and it is widely applied in variety kinds of applications. Hence, it is selected as a comparison with the proposed one. Table III shows a brief summary of the comparison results

TABLE II
Main Circuit Parameters of the Proposed Converter

Input voltage	V_g	42V (36V~48V)
Output voltage	V_o	380V
Leakage inductance reflected onto the secondary side	L_k	2.96μH
Additional resonant inductance	L_a	28.5μH
Secondary-side resonant inductance	L_r=L_k+L_a	31.46μH
Secondary-side magnetizing inductance	L_m	6.95mH
Additional inductor winding turns	N_a	9 turns
Transformer turns ratio	N_p:N_s	10 turns : 30 turns
Primary-side winding resistance	R_{pw}	6mΩ
Secondary-side winding resistance	R_{sw}	31mΩ
Winding resistance of the additional resonant inductor	R_{aw}	4.6mΩ
Resonant capacitance	C_1, C_2	15.8nF (6.8nF/1.6kV CBB x2 2.2nF/1.6kV CBB x1)
Filter capacitance	C_3, C_4	10μF (10μF/250V CBB x1)
Nominal Power	P	500W
Primary-side MOSFETs	S_1-S_4	FDPF045N10A
Secondary-side MOSFETs	S_5, S_6	SCT3030ALHR
Clamp diodes / SR MOSFETs	D_1, D_2/ S_7, S_8	RFN20TF6SFH / IPW60R040CFD7

between the two converters and the detailed comparison is given as follows.

The rectifier stage of the *LLC* usually employed a full-bridge (with four diodes) or a full-wave (with two diodes) rectifier configuration. The voltage stress of the diode in a center-tapped rectifier structure is much larger than twice the value of the output voltage [32]. Therefore, the full-bridge *LLC* converter is normally employed under the high step-up application [21]–[26]. The primary-side switch in either the *LLC* converter or the proposed one is with the same voltage stress. In the *LLC* converter, the voltage stress of the secondary-side diode is equal to the output voltage, which is the same as the clamp diode in the proposed converter. The voltage stress of S_5 and S_6 in the proposed converter depends on the drain-source capacitance characteristics of a MOSFET as discussed in Sections IV and VI.

Considering the design process of an *LLC* converter, since the input voltage varies in a range but the output is regulated at a constant value, the minimum gain should be set around the gain at the resonant frequency in order to achieve good efficiency [27]. For the specification mentioned in Section VI, the transformer turns ratio can be selected equal to 380 V/48 V = 8. This is much higher than that in the proposed converter, which only needs 3. Moreover, the magnetizing inductance value should be designed around 3–7 times the value of resonant inductance so to make a tradeoff between the peak voltage gain and the current stress [27]. This usually results in a small magnetizing inductance and a large air gap in the core, which complicates the transformer manufacturing process. Moreover, sometimes the designers have to make a segmented air gap in a core so to improve efficiency. In the proposed converter, the selection for magnetizing inductance value is relatively free. No air gap is

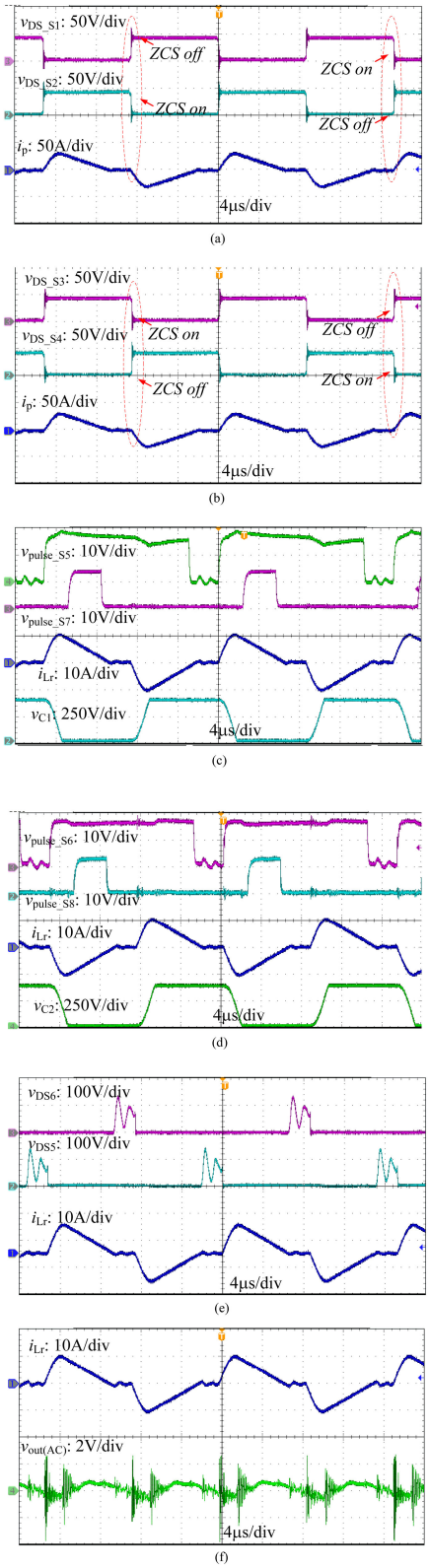

Fig. 17. Experimental waveforms when the converter is operated with full-SR control scheme ($V_g = 42$ V, $V_o = 380$ V, $P = 500$ W). (a) Drain-source voltages of S_1 and S_2, primary-side winding current $i_{\rm p}$. (b) Drain-source voltages of S_3 and S_4, primary-side winding current $i_{\rm p}$. (c) Driving pulses of S_5 and S_7, resonant current i_{Lr} and voltage of capacitors C_1. (d) Driving pulses of S_6 and S_8, resonant current i_{Lr}, and voltage of capacitors C_2. (e) Drain-source voltages of S_5 and S_6, resonant current i_{Lr}. (f) Output voltage ripple $v_{\rm out(AC)}$ without snubber, resonant current $i_{\rm Lr}$.

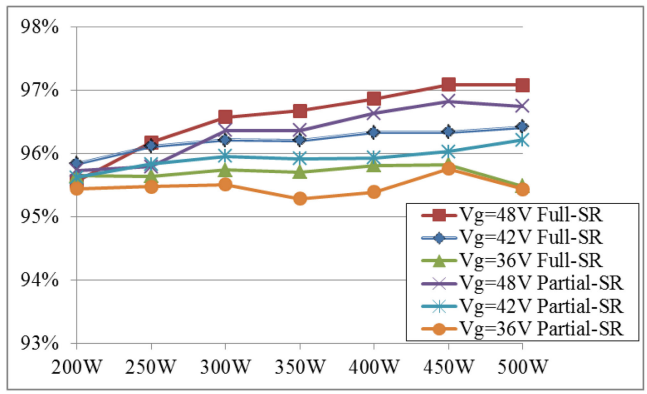

Fig. 18. Measured efficiency curves.

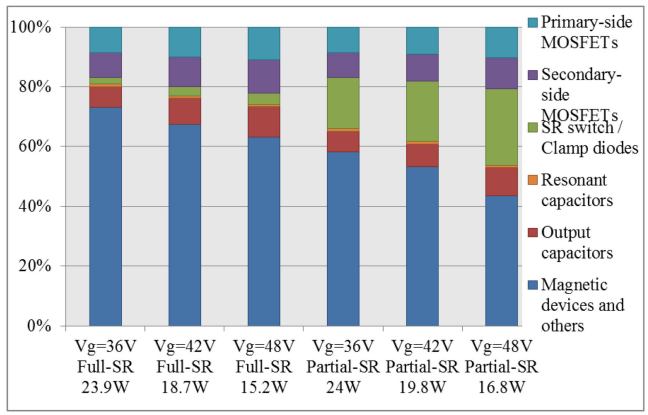

Fig. 19. Power loss and the breakdown illustration.

TABLE III
PERFORMANCE COMPARISON

	Proposed converter	*LLC* converter
switch/diode voltage stress	-	-
switch/diode current stress	×	√
complexity of SR realization	√	×
complexity of transformer manufacturing process	√	×
transformer turns ratio	√	×
switching frequency range	×	√

required so that the transformer manufacturing process is simple. However, it should be pointed out that the switching frequency in the *LLC* converter can be narrowed by a proper inductance ratio L_n ($L_n = L_m/L_r$), but the voltage gain of the proposed one shows a linear relationship with the switching frequency, which is much wider. Hence, this is its drawback.

If the inductance ratio L_n of an optimized *LLC* converter is selected around 5 as usual, the corresponding quality factors can be obtained equal to 0.4. Considering its resonant frequency is set around our prototype's maximum switching frequency, an *LLC* converter with $L_r = 3$ μH, $L_m = 15$ μH, and $C_r = 1.33$ μF can be obtained. In this condition, the current stresses of

TABLE IV
DETAILED LOSS ITEMS IN A DESIGN EXAMPLE FOR THE *LLC* AND THE PROTOTYPE WITH FULL-SR CONTROL SCHEME

	V_g=36V		V_g=42V		V_g=48V	
	LLC	proposed converter	*LLC*	proposed converter	*LLC*	proposed converter
Primary-side switches	2.46	2.08	2.08	1.82	1.78	1.65
Secondary-side switches	-	2.48	-	2.32	-	2.24
Secondary-side diodes	4.08	-	4.08	-	4.08	-
transformer primary-side windings	1.08	1.74	0.85	1.55	0.71	1.4
transformer secondary-side windings	0.46	1	0.38	0.89	0.31	0.81
Resonant capacitors	3.69	0.21	2.92	0.16	2.45	0.1
Resonant inductor windings	0.14	0.15	0.11	0.13	0.1	0.12
filter capacitors	0.12	1.64	0.08	1.56	0.04	1.52
total (W)	**12.04**	**9.31**	**10.51**	**8.43**	**9.47**	**7.83**

the primary-side and secondary-side windings are respectively equal to 26 and 3 A. They are less than the current stresses in the proposed converter, which are, respectively, 30 and 10 A according to the experiment waveforms. Hence, the *LLC* converter shows advantages in this aspect.

Table IV shows the loss breakdown items in a design example for the *LLC* converter and our proposed prototype with full-SR control scheme. To keep the same flux density with nearly the same switching frequency at the nominal operating condition, the count of the primary and secondary-side transformer turns in the *LLC* converter can be designed respectively equal to 8 and 64. Meanwhile, the count of the *LLC*'s resonant inductor winding turns is equal to 3. In this condition, the ferrite loss can be considered nearly the same as the proposed prototype. Considering the same window utilization factor (fill factor) of the transformer's and inductor's cores as the prototype, the winding resistances of the *LLC*'s transformer are equal to 3.84 mΩ (6 m$\Omega$$*8*$8/10/10) and 141 m$\Omega$ (31 m$\Omega$$*64*$64/30/30) respectively. The resonant inductor's winding resistance is 0.51 mΩ (4.6 m$\Omega$$*3*$3/9/9). Due to the less Peak/RMS value of the resonant current in the *LLC* converter, both the transformer and the inductor copper losses are less than our proposed converter but the difference is not obvious. The significant loss difference appears at the resonant capacitors and the rectifier stages as shown in Table IV. Since the resonant capacitance of the two converters differ greatly (1.33 μF for the *LLC* versus 15.8 nF for our prototype), the selection for the capacitors can vary greatly. For the *LLC* converter, here we can use one 1 μF/100 V (ESR$\approx$20 mΩ) and one 330 nF/100 V (ESR$\approx$30 mΩ) capacitor to achieve the desirable value. Even if the ESR values are only several tens of milliohms, the ESR loss of the resonant capacitors in the *LLC* converter still ranges from 2.45 to 3.69 W. This is because the loss is proportional to the square value of the large primary-side current. However, thanks to the secondary-side resonant tank, the ESR loss of the resonant capacitors in our proposed converter is no more than 0.21 W.

Another high loss position in the *LLC* converter is the rectifier diode. Without SR, the decrease of the diode loss only relies on the device development technology. Although the SR realization can decrease the diode loss, however, this is a big issue for the *LLC* converter under high output voltage condition [28]–[30]. The SR control relies on the accurate detection of zero-crossing point of the resonant current, which dramatically increases the converter control complexity because the duty ratios of the SR driving pulses are not the same as the input-side switches. For the secondary-side switches, the system controller needs to accurately determine the time instant of turn-ON and turn-OFF edges of driving pulses. As a usual method to reduce the control complexity, it is selecting a self-driven SR chip, and distinguishing the current zero-crossing point by sensing the drain-source voltage of the SR MOSFET. However, the maximum drain-source detection voltage rating is only about 230 V by the technology at the present stage, which limits its application to higher output voltage [31]. In Section V, the SR control for our proposed converter is given in detail. Because the time durations for each operating stage can be exactly calculated by (6), (10), and (39), detecting the current zero-crossing point is not necessary.

VIII. CONCLUSION

A secondary-side quasi-resonant converter is proposed in this article. There are only active switches without any passive components on the primary side, so the power loss caused by the large input current can be minimized. With the secondary-side resonant tank, the current stresses and the loss of the resonant capacitors are greatly reduced. Moreover, the resonant inductor can be realized by only the leakage transformer inductor, or by the sum of the leakage and an additional inductor. Furthermore, the complexity of the transformer manufacture process is decreased since there is no additional air gap in the transformer core. So the transformer design process is much easier than that in an *LLC* converter.

In the proposed converter, all the active switches and diodes can realize the soft switching naturally. Besides, the SR technology can be applied without the current zero-crossing point detection because each period for a different operating phase can be exactly predicted. A 500-W prototype with 36–48 V input and 380 V output is built. The experimental results have shown good agreement with theoretical analysis.

APPENDIX

The inductor current i_{Lr} is re-illustrated in Fig. 20 in order to clearly show the analysis process.

If the integration of i_{Lr} from t_1 to t_2 is denoted by A_1, it can be expressed as shown in the following equation:

$$A_1 = \int_{t1}^{t2} i_{Lr} dt. \tag{A1}$$

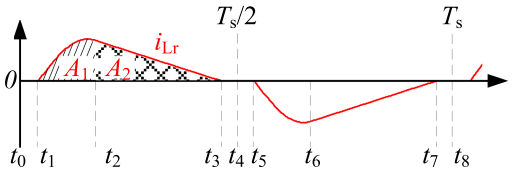

Fig. 20. Waveforms of i_{Lr}

According to (5), A_1 can be simplified as follows:

$$\begin{aligned} A_1 &= \int_{t1}^{t2} \frac{V_g(M+2N)}{2R_0} \sin(\omega_r t - \omega_r t_d) dt \\ &= \frac{V_g(M+2N)}{2\omega_r R_0} * (1 - \cos(\omega_r t_2 - \omega_r t_d)) \\ &= \frac{V_g(M+2N)}{2\omega_r R_0} * \left(1 - \frac{2N-M}{2N+M}\right) \\ &= \frac{V_o}{\omega_r R_0} = 2C_r V_o \end{aligned} \tag{A2}$$

where t_d is the duration from t_0 to t_1.

From t_2 to t_3, i_{Lr} decreases linearly until it equals zero at t_3. Obviously, the shape of area A_2 is a triangle. Hence, A_2 can be calculated according to the following equation:

$$A_2 = \int_{t2}^{t3} i_{Lr} dt = \frac{i_{Lr(t2)}(t_3 - t_2)}{2}. \tag{A3}$$

According to (5), $i_{\mathrm{Lr}(t_2)}$ can be calculated as follows:

$$i_{Lr(t2)} = \frac{V_g(M+2N)}{2R_0} \sin(\omega_r t_2 - \omega_r t_d) \tag{A4}$$

where t_2 can be found from (6).

Because i_{Lr} decreases to zero at t_3, the duration from t_2 to t_3 can be derived as follows according to the following equation:

$$\begin{aligned} t_3 - t_2 &= \frac{L_r i_{Lr(t2)}}{\frac{V_o}{2} - NV_g} \\ &= \frac{L_r}{\frac{V_o}{2} - NV_g} * \frac{V_g(M+2N)}{2R_0} \sin(\omega_r t_2 - \omega_r t_d) \\ &= \frac{M+2N}{(M-2N)\omega_r} \sin(\omega_r t_2 - \omega_r t_d) \\ &= \frac{M+2N}{(M-2N)\omega_r} \sqrt{1 - \left(\frac{M-2N}{M+2N}\right)^2} \\ &= \frac{2\sqrt{2MN}}{\omega_r (M-2N)}. \end{aligned} \tag{A5}$$

By substituting (E4), (E5), and (6) into (E3), A_2 can be simplified as the following equation:

$$A_2 = \frac{4NV_oC_r}{M-2N}. \tag{A6}$$

Finally, the average current value during half switching period can be obtained as shown in (11).

REFERENCES

[1] D. Cao, S. Jiang, F. Z. Peng, and Y. Li, "Low cost transformer isolated boost half-bridge micro-inverter for single-phase grid-connected photovoltaic system," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 71–78.

[2] "National safety standard for electric buses and coaches," Ministry of Industry and Information Technology of the People's Republic of China. [Online] Available: http://www.miit.gov.cn/n1146285/n1146352/n3054355/n3057585/n3057590/c5361197/content.html

[3] G. Cao, Z. Guo, Y. Wang, and K. Sun, "A high step-up modular DC/DC converter for photovoltaic generation integrated into DC grids," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 4421–4426.

[4] J. Lee, Y. Jeong, and B. Han, "An isolated DC/DC converter using high-frequency unregulated LLC resonant converter for fuel cell applications," *IEEE Trans Ind. Electron.*, vol. 58, no. 7, pp. 2926–2934, Jul. 2011.

[5] T. Qian and B. Lehman, "Buck/half-bridge input-series two stage converter," *IET Power Electron.*, vol. 3, no. 6, pp. 965–976, Nov. 2010.

[6] Z. Yao and L. Xiao, "Family of zero-voltage-switching unregulated isolated step-up DC-DC converters," *IET Power Electron.*, vol. 6, no. 5, pp. 862–868, May 2013.

[7] E. O. Lindstrom, L. A. Garcia-Rodriguez, A. R. Oliva, and J. C. Balda, "Designing an optimum non-dissipative LC snubber for step-up flyback converters in DCM," in *Proc. IEEE 8th Latin Amer. Symp. Circuits Syst.*, Jun. 2017, pp. 1–4.

[8] J. H. Lee, T. J. Liang, and J. F. Chen, "Isolated coupled-inductor-integrated DC–DC converter with nondissipative snubber for solar energy applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3337–3348, Jul. 2014.

[9] B. Wu, S. Li, and K. M. Smedley, "A new single-switch isolated high-gain hybrid boosting converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4978–4988, Aug. 2016.

[10] W. Li, J. Liu, J. Wu, and X. He, "Design and analysis of isolated ZVT boost converters for high-efficiency and high-step-up applications," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2363–2374, Nov. 2007.

[11] W. Li and X. He, "A family of isolated interleaved boost and buck converters with winding-cross-coupled inductors," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 3164–3173, Nov. 2008.

[12] Y. Zhao, W. Li, Y. Deng, and X. He, "Analysis, design, and experimentation of an isolated ZVT boost converter with coupled inductors," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 541–550, Feb. 2011.

[13] W. Li, D. Xu, B. Wu, Y. Zhao, H. Yang, and X. He, "Zero-voltage-switching dual-boost converter with multi-functional inductors and improved symmetrical rectifier for distributed generation systems," *IET Power Electron.*, vol. 5, no. 7, pp. 969–977, Aug. 2012.

[14] D. Vinnikov, I. Roasto, R. Strzelecki, and M. Adamowicz, "Step-up DC/DC converters with cascaded quasi-Z-source network," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3727–3736, Oct. 2012.

[15] D. Vinnikov and I. Roasto, "Quasi-Z-source-based isolated DC/DC converters for distributed power generation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 192–201, Jan. 2011.

[16] Y. P. Siwakoti, F. Blaabjerg, P. C. Loh, and G. E. Town, "High-voltage boost quasi-Z-source isolated DC/DC converter," *IET Power Electron.*, vol. 7, no. 9, pp. 2387–2395, Sep. 2014.

[17] M. Forouzesh and A. Baghramian, "Galvanically isolated high gain Y-source DC–DC converters for dispersed power generation," *IET Power Electron.*, vol. 9, no. 6, pp. 1192–1203, 2016.

[18] J. Sun, X. Ding, M. Nakaoka, and H. Takano, "Series resonant ZCS-PFM DC-DC converter with multistage rectified voltage multiplier and dual-mode PFM control scheme for medical-use high-voltage X-ray power generator," *IEE Proc., Electric Power Appl.*, vol. 147, no. 6, pp. 527–534, Nov. 2000.

[19] J. Diaz, P. J. Villegas Saiz, J. A. Martin-Ramos, A. Martin-Pernia, and J. A. Martinez, "A high-voltage AC/DC resonant converter based on PRC with single capacitor as an output filter," *IEEE Trans. Ind. Appl.*, vol. 46, no. 6, pp. 2134–2142, Nov./Dec. 2010.

[20] A. Pokryvailo, C. Carp, and C. Scapellati, "A 100 kW high voltage power supply for dual energy computer tomography applications," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 22, no. 4, pp. 1945–1953, Aug. 2015.

[21] H. Wu, X. Jin, H. Hu, and Y. Xing, "Multielement resonant converters with a notch filter on secondary side," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 3999–4004, Jun. 2016.

[22] J. Yan, X. Zhao, C. Chen, and J. Lai, "Comparison of secondary topology of the LLC converter for photovoltaic application," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 4750–4755.

[23] X. Chen *et al.*, "A natural bidirectional input-series–output-parallel LLC-DCX converter with automatic power sharing and power limitation capability for li-ion battery formation and grading system," *IEEE J. Emerg. Sel. Top. Power Electron* ., vol. 8, no. 4, pp. 3618–3632, Dec. 2020.
[24] J. Xu *et al.*, "PWM modulation and control strategy for LLC-DCX converter to achieve bidirectional power flow in facing with resonant parameters variation," *IEEE Access*, vol. 7, pp. 54693–54704, 2019.
[25] A. N. Rahman, H. Chiu, and Y. Hsieh, "Design of wide input voltage range high step-up DC-DC converter based on secondary-side resonant tank full bridge LLC," in *Proc. 3rd Int. Conf. Intell. Green Building Smart Grid*, 2018, pp. 1–6.
[26] T. Jiang, J. Zhang, X. Wu, K. Sheng, and Y. Wang, "A bidirectional LLC resonant converter with automatic forward and backward mode transition," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 757–770, Feb. 2015.
[27] H. Huang, "Designing an LLC resonant half-bridge power converter," Texas Instruments (TI) Power Supply Design Seminar, SEM1900, 2010, TI Literature No. SLUP263. [Online] Available: https://www.ti.com/seclit/ml/slup263/slup263.pdf
[28] J. Zhang, J. Liao, J. Wang, and Z. Qian, "A current-driving synchronous rectifier for an LLC resonant converter with voltage-doubler rectifier structure," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1894–1904, Apr. 2012.
[29] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.
[30] B.-C. Kim, H.-S. Park, S. C. Moon, Y.-D. Kim, D.-Y. Kim, and G. Moon, "The novel synchronous rectifier driving method for LLC series resonant converter," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc.*, 2012, pp. 810–813.
[31] P. Jia, Z. Su, T. Guo, H. Zhu, H. Guo, and Y. Hao, "High Efficiency Isolated Quasi-Resonant Converter for High Step-Up Applications," *2021 IEEE 12th Energy Conversion Congress Exposition - Asia (ECCE-Asia)*, 2021, pp. 1952–1957.
[32] C. Zhao, M. Chen, G. Zhang, X. Wu, and Z. Qian, "A novel symmetrical rectifier configuration with low voltage stress and ultralow output-current ripple," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1820–1831, Jul. 2010.

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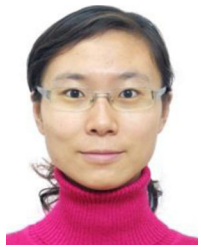

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