A Switched-Capacitors-Based 13-Level Inverter

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***Abstract*—The merit of switched-capacitors-based multilevel inverters (SCMLIs) is generally quantified in terms of a "cost function" (CF) that incorporates parameters such as voltage gain, component count, total standing voltage (TSV), and number of levels. In this article, a 13-level inverter is proposed with the aim of achieving a low value of CF. The proposed single-stage SCMLI uses one input source and three capacitors to attain a voltage gain of 3. It requires 13 power switches, of which the peak inverse voltage (PIV) of nine switches is restricted to the source voltage. The remaining four switches have PIV equal to twice the source voltage and they operate at low frequency. Thus, for all switches, the PIV is less than the amplitude of the output voltage. Moreover, the capacitors are self-balanced at all regions of modulation index values. The proposed inverter is validated through simulation and experimental results. A comparison of the proposed topology with other contemporary SCMLIs shows that it is highly competent in terms of CF, PIV and TSV requirements, waveform resolution, and capability to achieve voltage balancing of capacitors at low values of modulation index.**

***Index Terms*—Multilevel inverter (MLI), peak inverse voltage (PIV), single stage, switched capacitors, topology.**

I. Introduction

A. Emergence of Switched-Capacitors-Based Multilevel Inverters (SCMLIs)

MULTILEVEL inverters (MLIs) are being increasingly employed in numerous applications including motor drives, renewable power generation, battery energy storage systems, electric vehicles (EVs), contactless power transfer, and high power density apparatus, etc. [1]–[5]. MLIs offer many advantages over a conventional two-level inverter, such as power switches with much less peak inverse voltage (PIV) as compared to the "operating voltage (i.e., amplitude of the output multilevel waveform)," better harmonic profile, much reduced *dv*/*dt* stress on the ac load and power switches, etc. In the past few decades, the so-called conventional topologies, viz. diode-clamped (DC), flying capacitors (FC), and cascaded H-bridge (CHB) have been intensely studied and are commercialized [3], [5]. Apart from the issues that specifically pertain to DC, FC, and CHB, these conventional topologies have the following two general limitations [3]–[12]:

1) For a high-resolution waveform (i.e., large number of levels), they require an increased number of power switches. This increases the system complexity, costs, and volume.
2) They operate with a unity voltage gain (i.e., ratio of the operating voltage to the input dc voltage) and thus do not offer any inherent voltage boosting. Such a feature is desirable especially for applications that involve a low input dc voltage (such as photovoltaic (PV) systems and EVs). Otherwise, a boost dc–dc converter or a transformer is employed, which increases system volume and power losses [12]. Moreover, balancing of capacitors in DC and FC topologies poses a significant challenge, especially for an increased number of levels [3].

Thus, research efforts are being made to reduce the component count and innovate new MLIs with an inherent voltage boosting [6]–[22] and simplified voltage balancing. Of these, SCMLIs have emerged as a special class. In SCMLIs, a capacitor is brought in parallel with the dc source for charging and then it is brought in series when connected to the load. Thus, SCs not only add levels but they also enable the voltage gain to be >1. In order to maximize the voltage gain with less number of capacitors, some SCMLIs, e.g., those proposed in [11], [19]–[21], use the input dc source and one (or more) charged capacitors together to charge the other capacitor(s). This approach, however, leads to the following disadvantages: 1) requirement of large capacitors for high power factor loads; and 2) severely restricted charging of capacitors at low values of modulation index.

B. Factors on Which SCMLIs Are Evaluated and Compared

Based on a survey of papers [6]–[22], it has been determined by the authors that the numerous SCMLIs are generally evaluated and compared with one another in terms of the following six features.

1) *Voltage gain (β)*: A higher voltage gain reduces (or eliminates) the boosting requirement prior to the input dc link [7], [12], [20]. Higher gain, however, may lead to an increased component count and higher PIVs of power switches.

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2) *Resolution of the output waveform (i.e., number of levels, N_L)*: A higher resolution multilevel waveform reduces output filter requirement, enhances the lifetime of the load due to much less *dv/dt* stress, and improves efficiency by improving the harmonic profile of the load current [11], [20]. A higher resolution output, however, may increase the component count.
3) *Total component count:* Attempts to increase waveform resolution and voltage gain may lead to an increased component count, which in turn, increases volume, complexity, and losses in the system [6]–[10]. The component count includes the number of input dc sources (N_{IS}), number of transistor switches (N_S), number of main and auxiliary diodes (N_D and N_{AD}), number of gate drivers (N_{GD}), and number of capacitors (N_C).
4) *Total standing voltage (TSV)*: Overall semiconductor requirement and its cost is reflected in the TSV of the topology, obtained by adding the PIVs of all power switches and auxiliary diodes [6], [17]–[21].
5) *PIVs of power switches with respect to the operating voltage*: A topology with even a single switch with a large PIV requirement limits its applicability to a high-voltage high-power application [12], [14], [16]. It is desirable to keep PIVs of all switches as less as possible as compared to the operating voltage.
6) *Effective balancing of capacitors at various modulation indices*: Ease of voltage balancing of capacitors is an essential feature of SCMLIs and should be retained at all values of modulation index [7].

Now, of these features, those discussed in 1)–4) above are quantified in terms of a so-called "cost function (CF)," which is defined as follows [6], [9]–[12], [18]–[21]:

$$\mathrm{CF}=\left(\frac{N_{IS}}{N_L}\right)*\left\{N_S+N_D+N_{AD}+N_{GD}+N_C+\left(\frac{\alpha*\mathrm{TSV}}{\beta}\right)\right\} \tag{1}$$

where α is the "weighing factor" to assign weightage to TSV in comparison to the component count. As can be seen, a lesser value of CF indicates better structural features of the topology and many authors have used this CF to evaluate the SCMLIs.

C. Classification of SCMLIs and State of the Art

A survey of topologies [6]–[22] also indicates that the SCMLIs can be broadly categorized as "two-stage" and "single-stage" topologies. These are discussed as follows.

1) *Two-stage topologies*: In a two-stage SCMLI, a unipolar multilevel waveform is first synthesized and thereafter, an H-bridge (or equivalent) unfolds it to a bipolar waveform. These H-bridge switches experience a high voltage stress equal to the amplitude of the output. Structures proposed in [6]–[11] are examples of two-stage topologies. SCMLI proposed in [6] is an easily extendable structure, but the component count is very high, whereas the basic unit offers a low voltage gain of 2. The topology presented in [7] is highly modular, but requires switches with high PIVs. Similarly, the modular SCMLI described in [8] offers low voltage gain and exhibits high CF. Another modular SCMLI is presented in [9], which uses low PIV switches and has low TSV, but each module requires two capacitors to synthesize only five levels. It has numerous redundant states and offers low-resolution waveform and low gain, leading to high CF. In [10], the SCMLI has less component count, but with a significantly large TSV and high CF. A high voltage gain SCMLI is proposed in [11] with low component count and low CF, but PIV and TSV requirements are extremely high, whereas the topology is incapable of voltage balancing of capacitors at low values of modulation index. Thus, as far as two-stage SCMLIs are concerned, the requirement of switches with high PIV is a serious limitation, especially for high voltage applications.
2) *Single-stage topologies* (e.g., [12]–[22]): A single-stage SCMLI synthesizes a bipolar waveform and hence presents the possibility of incorporating power switches with less PIVs, though the number of power switches per level is significantly large. As an example, the SCMLI proposed in [12] uses switches with PIV restricted to the input voltage, but offers a low-resolution waveform and low voltage gain. In [13], an innovative structure is presented with the integration of conventional H-bridges and switched capacitors using additional power switches. However, a complex methodology is required for capacitor voltage balancing, whereas the topology exhibits a high value of CF. The modular SCMLI presented [14] has a high component count per level, though it uses power switches with less PIV. In [15], FCs are used for clamping and a large voltage gain equal to 4 is attained, but the topology has a high component count per level, whereas it synthesizes a low-resolution waveform. The topology proposed in [16] requires a large number of power switches with high PIVs, though the structure is highly modular. In [17], the SCMLI utilizes low PIV switches to synthesize nine-level waveform, but the component count is high and voltage gain is low. Similarly, the topologies proposed in [18] and [22] use low PIV switches but at the cost of large semiconductor requirement and low voltage gain. The high voltage gain topology proposed in [19] requires less number of components per level, but the TSV is high and large capacitors are required, especially for high power factor loads. A high voltage gain of six is offered by the SCMLI proposed in [20], but the component count is high and capacitors have restricted charging at low values of modulation index. SCMLI proposed in [21] too offers a high voltage gain of six, but the PIV requirement is very high with a restricted charging of capacitors at low values of modulation index.

D. Research Gaps Related to SCMLI Topologies and Contribution of This Article

On the basis of the previous analysis, major research gaps related to SCMLIs are summarized in Table I. It can be seen that there is an immense scope of conceptualizing a single-stage SCMLI with a high-resolution output, power switches with low

TABLE I
RESEARCH GAPS PERTAINING TO SCMLIS AND THE SOLUTION PROPOSED IN THIS ARTICLE

Major research gaps related to SCMLI topologies	Solution offered by the topology proposed in this paper
High value of Cost Function (CF) as defined in (1): in topologies [7-10, 12-16]	Low value of CF due to reduced component count per level and high resolution waveform
Low resolution waveform: in topologies [8-10,12, 14-16]	High resolution 13-level waveform is synthesized by the topology
Low voltage gain, in topologies [6, 8-10, 12, 14, 16-18, 22]	Offers a voltage gain of 3
High peak-inverse-voltage (PIV), equal to the operating voltage: in topologies [6-8, 10,11,16, 21]	Single-stage topology, PIV of all switches restricted to values much less than the operating voltage
Restricted voltage balancing of capacitors at low values of modulation index: in topologies [11, 19-21]	All capacitors come in parallel with the dc source during the synthesis of zero-level and hence they are balanced at all values of modulation index

PIVs, large voltage gain, low semiconductor requirement, an overall low CF, and effective voltage balancing of capacitors at low modulation indices. In this article, a single-stage structure is conceptualized and it offers the following advantages:

1) a voltage gain of three is achieved by it;
2) a high-resolution 13-level waveform is synthesized;
3) all capacitors are self-balanced even at low modulation indices;
4) PIVs of all power switches are significantly less than the operating voltage;
5) low value of CF.

Each research gap is addressed by the proposed solution, as summarized in Table I.

E. Organization of This Article

The proposed inverter is described in Section II. A switching methodology for the proposed SCMLI is also described. In Section III, voltage and current ratings of power switches, calculation of capacitances, and loss analysis are discussed, along with the design procedure. A detailed comparison with other SCMLI topologies is presented in Section IV. Simulation and experimental results are presented in Section V, along with a detailed note on possible applications and extension of the topology to its three-phase version with a single dc input. Finally, Section VI concludes this article.

II. PROPOSED 13-LEVEL INVERTER

A. Circuit Topology

The structure of the proposed 13-level inverter is shown in Fig. 1 and it consists of 13 power switches S_j $\{j = 1$ to $13\}$, one diode D, three capacitors (C_1, C_2, and C_3), and one dc source ($V_{\rm dc}$). The output ac voltage is marked as "$v_{\rm ac}$." Voltage v_{C1} of capacitor C_1 is to be maintained at $V_{\rm dc}$, whereas respective voltages v_{C2} and v_{C3} of capacitors C_2 and C_3 are to be maintained at $0.5V_{\rm dc}$ each.

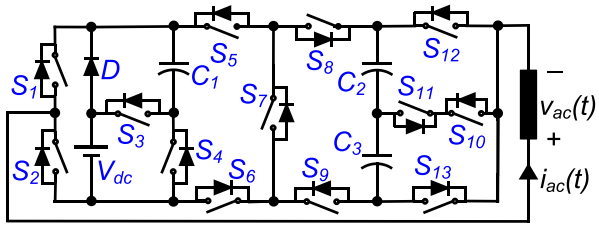

Fig. 1. Power circuit of the switched-capacitors-based 13-level inverter proposed in this article.

B. Description of the Working States and Voltage Balancing

All the valid operating states σ_j $\{j = 1$ to $14\}$ for the proposed inverter are summarized in Fig. 2. In each state, wherever valid, two paths are shown: 1) the path following which the voltage level is synthesized is shown in light blue; and 2) the path following which a capacitor is charged is shown in light pink. The states are described as follows.

1) *State* σ_1: In this state, the output voltage $v_{\rm ac} = 0$ with the simultaneous conduction of S_1, S_5, S_8, and S_{12}. Also, conduction of D and S_4 brings C_1 in parallel with the dc source and it gets charged approximately to $V_{\rm dc}$. Similarly, a series connection of C_2 and C_3 is brought in parallel with the dc source by the simultaneous conduction of D, S_5, S_6, S_8, and S_9 and they get charged approximately to a voltage $0.5V_{\rm dc}$ each.
2) *State* σ_2: In this state, the load terminals are connected to C_2 with the simultaneous conduction of S_1, S_5, S_8, S_{10}, and S_{11}. Thus, output voltage $v_{ab} = v_{C2} \approx 0.5V_{\rm dc}$. Also, conduction of D and S_4 brings C_1 in parallel with the dc source, charging it approximately to $V_{\rm dc}$. Similarly, a series connection of C_2 and C_3 is brought in parallel with the dc source by the simultaneous conduction of D, S_5, S_6, S_8, and S_9 and they get charged approximately to a voltage $0.5V_{\rm dc}$ each.
3) *State* σ_3: In this state, the load terminals are connected to $V_{\rm dc}$ with the simultaneous conduction of S_1, D, S_6, S_9, and S_{13}. Thus, output voltage $v_{\rm ac} = V_{\rm dc}$. Also, conduction of D and S_4 brings C_1 in parallel with the dc source, charging it approximately to $V_{\rm dc}$. Similarly, a series connection of C_2 and C_3 is brought in parallel with the dc source by the simultaneous conduction of D, S_5, S_6, S_8, and S_9 and they get charged approximately to a voltage $0.5V_{\rm dc}$ each.
4) *State* σ_4: In this state, the load terminals are connected to $V_{\rm dc}$ and C_2 with the simultaneous conduction of S_1, S_4, S_6, S_7, S_8, S_{10}, and S_{11}. Thus, output voltage $v_{\rm ac} = V_{\rm dc} + v_{C2} \approx 1.5V_{\rm dc}$. Also, conduction of D and S_4 brings C_1 in parallel with the dc source, charging it approximately to $V_{\rm dc}$.
5) *State* σ_5: In this state, the load terminals are connected to a series configuration of $V_{\rm dc}$ and C_1 with the simultaneous conduction of S_1, S_3, S_6, S_9, and S_{13}. Thus, output voltage $v_{\rm ac} = V_{\rm dc} + v_{C1} \approx 2V_{\rm dc}$.
6) *State* σ_6: In this state, the load terminals are connected to a series configuration of C_1, C_2, and $V_{\rm dc}$ with the

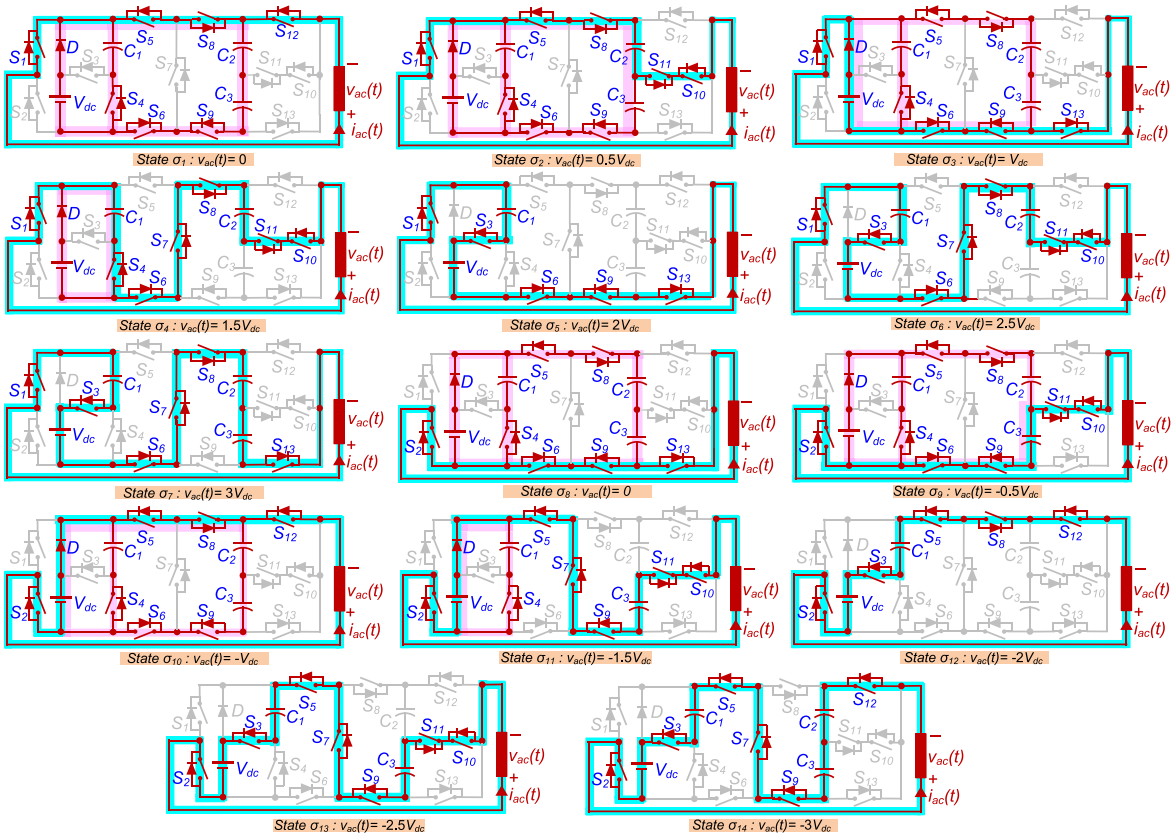

Fig. 2. Switching states for the proposed 13-level inverter.

simultaneous conduction of S_1, S_3, S_6, S_7, S_8, S_{10}, and S_{11}.Thus, output voltage $v_{\rm ac} = v_{C1} + v_{C2} + V_{\rm dc} \approx 2.5V_{\rm dc}$.

7) *State* σ_7 : In this state, the load terminals are connected to a series configuration of C_1, C_2, C_3, and $V_{\rm dc}$ with the simultaneous conduction of S_1, S_3, S_6, S_7, S_8, and S_{13}. Thus, output voltage $v_{\rm ac} = v_{C1} + v_{C2} + v_{C3} + V_{\rm dc} \approx 3V_{\rm dc}$.
8) *State* σ_8: In this zero state, the output voltage $v_{\rm ac} = 0$ with the simultaneous conduction of S_2, S_6, S_9, and S_{13}. Also, conduction of D and S_4 brings C_1 in parallel with the dc source, charging it approximately to $V_{\rm dc}$. Similarly, a series connection of C_2 and C_3 is brought in parallel with the dc source by the simultaneous conduction of D, S_5, S_6, S_8, and S_9 and they get charged approximately to a voltage $0.5V_{\rm dc}$ each.
9) *State* σ_9: In this state, the load terminals are connected to C_3 with the simultaneous conduction of S_2, S_6, S_9, S_{10}, and S_{11}. Thus, output voltage $v_{\rm ac} = -v_{C3} \approx -0.5V_{\rm dc}$. Also, conduction of D and S_4 brings C_1 in parallel with the dc source, charging it approximately to $V_{\rm dc}$. Similarly, a series connection of C_2 and C_3 is brought in parallel with the dc source by the simultaneous conduction of D, S_5, S_6, S_8, and S_9 and they get charged approximately to a voltage $0.5V_{\rm dc}$ each.
10) *State* σ_{10}: In this state, the load terminals are connected to $V_{\rm dc}$ with the simultaneous conduction of S_2, D, S_5, S_8, and S_{12}, such that output voltage $v_{ab} = -v_{C1} \approx -V_{\rm dc}$. Also, conduction of D and S_4 brings C_1 in parallel with the dc source, charging it approximately to $V_{\rm dc}$. Similarly, a series connection of C_2 and C_3 is brought in parallel with the dc source by the simultaneous conduction of D, S_5, S_6, S_8, and S_9 and they get charged approximately to a voltage $0.5V_{\rm dc}$ each.
11) *State* σ_{11}: In this state, the load terminals are connected to $V_{\rm dc}$ and C_3 with the simultaneous conduction of S_2, D, S_5, S_7, S_9, S_{10}, and S_{11}. Thus, output voltage $v_{\rm ac} = -(v_{C1} + v_{C3}) \approx -1.5V_{\rm dc}$. Also, conduction of D and S_4 brings C_1 in parallel with the dc source, charging it approximately to $V_{\rm dc}$.
12) *State* σ_{12}: In this state, the load terminals are connected to a series configuration of $V_{\rm dc}$ and C_1 with the simultaneous conduction of S_2, S_3, S_5, S_8, and S_{12}, such that the output voltage $v_{\rm ac} = -(v_{C1} + V_{\rm dc}) \approx -2V_{\rm dc}$.
13) *State* σ_{13}: In this state, the load terminals are connected to a series configuration of C_1, C_3, and $V_{\rm dc}$ with the simultaneous conduction of S_2, S_3, S_5, S_7, S_9, S_{10}, and S_{11}, such that the output voltage $v_{\rm ac} = -(v_{C1} + v_{C3} + V_{\rm dc}) \approx -2.5V_{\rm dc}$.
14) *State* σ_{14}: In this state, the load terminals are connected to a series configuration of C_1, C_2, C_3, and $V_{\rm dc}$ with the simultaneous conduction of S_2, S_3, S_5, S_7, S_9, and S_{12}, such that the output voltage $v_{\rm ac} = -(v_{C1} + v_{C2} + v_{C3} + V_{\rm dc}) \approx -3V_{\rm dc}$.

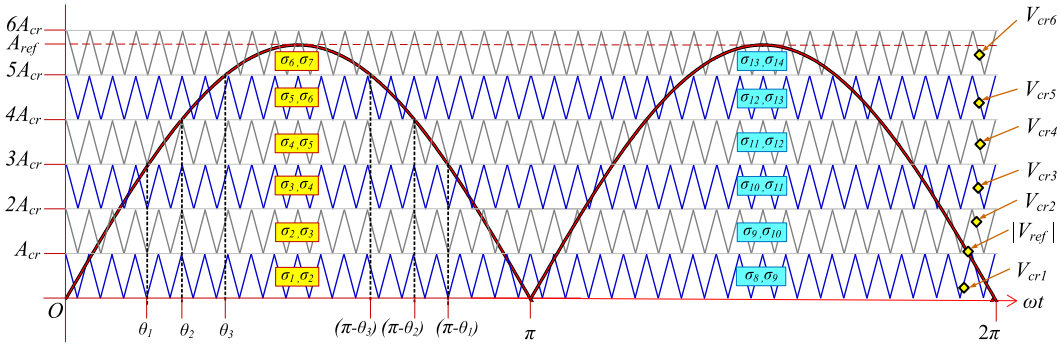

Fig. 3. Reference and carrier waveforms to modulate the proposed inverter.

Thus, in states σ_1, σ_2, σ_3, σ_4, σ_8, σ_9, σ_{10}, and σ_{11}, C_1 comes in parallel with $V_{\rm dc}$, thereby achieving self-balance. Similarly, C_2 and C_3 combined come in parallel with $V_{\rm dc}$ during the states σ_1, σ_2, σ_3, σ_8, σ_9, and σ_{10}. It can be also seen that both the states σ_1 and σ_8 synthesize zero voltage at the output terminals. Optimal use of states can help in operating the switches S_1 and S_2 at a frequency equal to the line frequency. For this, zero voltage levels in the positive and negative halves should be obtained by using states σ_1 and σ_8, respectively. A procedure to attain the same is described in the following section.

C. Modulation Strategy

For the modulation of MLIs, various methods have been used, including high-switching-frequency methods (such as multicarrier pulsewidth modulation (PWM) and space vector PWM) [1]–[3] and low-switching-frequency methods (such as active harmonic elimination, selective harmonic elimination, and nearest level control) [23]–[25]. The proposed SCMLI can be modulated with any one of these methods with suitable adaptation. In the present work, a level-shifted multicarrier PWM (LSPWM) scheme is used. In a multicarrier PWM scheme, triangular carrier signals are compared with the sinusoidal reference signal. The pulses so obtained are used for switching of devices corresponding to respective voltage levels. In this section, an LSPWM methodology is formulated in a manner that it facilitates the utilization of both the zero states, viz. σ_1 and σ_8. As shown in Fig. 3, six carrier waveforms V_{crj} $\{j = 1 \text{ to } 6\}$ of same frequency (f_{cr}), phase, and peak-to-peak value (A_{cr}) are used as carriers. A sinusoidal waveform $V_{\rm ref}$ of amplitude $A_{\rm ref}$ and frequency $f_{\rm ref}$ is taken as reference and its absolute value $|V_{\rm ref}|$ is compared with the carriers. Thus, modulation index (M) can be defined as

$$M = \frac{A_{\rm ref}}{6A_{cr}}. \tag{2}$$

For one complete power cycle, e.g., during $(0 \le \omega t \le 2\pi)$, the requirement of various operating states is also shown in Fig. 3. It is shown that during $(0 \le \omega t \le \pi)$, when V_{cr1} is compared with $|V_{\rm ref}|$, the expected voltage levels are $(0, 0.5V_{\rm dc})$, which are to be, respectively, obtained by commanding gate signals for states (σ_1, σ_2). Similarly, when V_{cr2}, V_{cr3}, V_{cr4}, V_{cr5}, and V_{cr6} are compared with $|V_{\rm ref}|$, the expected levels during $(0 \le \omega t \le \pi)$ are $(0.5V_{\rm dc}, V_{\rm dc})$, $(V_{\rm dc}, 1.5V_{\rm dc})$, $(1.5V_{\rm dc}, 2V_{\rm dc})$, $(2V_{\rm dc}, 2.5V_{\rm dc})$, and $(2.5V_{\rm dc}, 3V_{\rm dc})$, which are to be, respectively, obtained by commanding gate signals for states (σ_2, σ_3), (σ_3, σ_4), (σ_4, σ_5), (σ_5, σ_6), and (σ_6, σ_7).

TABLE II
EFFECT OF MODULATION INDEX (M) ON THE PROPOSED INVERTER

Modulation Index (M) Region	Number of output levels	Missing voltage levels	Capacitor charging			Switches utilized
			C_1	C_2	C_3	
$> \frac{5}{6}$	13	None	Yes	Yes	Yes	All
$\frac{2}{3}$ to $\frac{5}{6}$	11	$\pm 3V_{dc}$	Yes	Yes	Yes	All
$\frac{1}{2}$ to $\frac{2}{3}$	9	$\pm 3V_{dc}$, $\pm 2.5V_{dc}$	Yes	Yes	Yes	All
$\frac{1}{3}$ to $\frac{1}{2}$	7	$\pm 3V_{dc}$,$\pm 2.5V_{dc}$, $\pm 2V_{dc}$	Yes	Yes	Yes	All except S_3
$\frac{1}{6}$ to $\frac{1}{3}$	5	$\pm 3V_{dc}$,$\pm 2.5V_{dc}$, $\pm 2V_{dc}$, $\pm 1.5V_{dc}$	Yes	Yes	Yes	All except S_3, S_7
0 to $\frac{1}{6}$	3	$\pm 3V_{dc}$,$\pm 2.5V_{dc}$, $\pm 2V_{dc}$, $\pm 1.5V_{dc}$, $\pm V_{dc}$	Yes	Yes	Yes	All except S_3, S_7

For the remaining half cycle, the states for the negative half cycle are to be enacted and the zero level is to be obtained by the state σ_8. Thus, for $(\pi \le \omega t \le 2\pi)$, when V_{cr1}, V_{cr2}, V_{cr3}, V_{cr4}, V_{cr5}, and V_{cr6} are compared with $|V_{\rm ref}|$, the expected levels are $(0, -0.5V_{\rm dc})$, $(-0.5V_{\rm dc}, -V_{\rm dc})$, $(-V_{\rm dc}, -1.5V_{\rm dc})$, $(-1.5V_{\rm dc}, -2V_{\rm dc})$, $(-2V_{\rm dc}, -2.5V_{\rm dc})$, and $(-2.5V_{\rm dc}, -3V_{\rm dc})$, which are to be, respectively, obtained by commanding gate signals for states (σ_8, σ_9), (σ_9, σ_{10}), $(\sigma_{10}, \sigma_{11})$, $(\sigma_{11}, \sigma_{12})$, $(\sigma_{12}, \sigma_{13})$, and $(\sigma_{13}, \sigma_{14})$. Based on the aforementioned requirement, the implementation of the state-selection logic is given in Fig. 4, where the gate signals for specific states are first obtained and are eventually fed to OR gates so as to obtain consolidated firing pulses for each power switch.

It can be noted that the switches S_1 and S_2 are switched at the fundamental frequency to lower the overall switching losses. Other switches, with lesser PIVs, operate at higher frequencies. With reference to Table II, it can be seen that the proposed

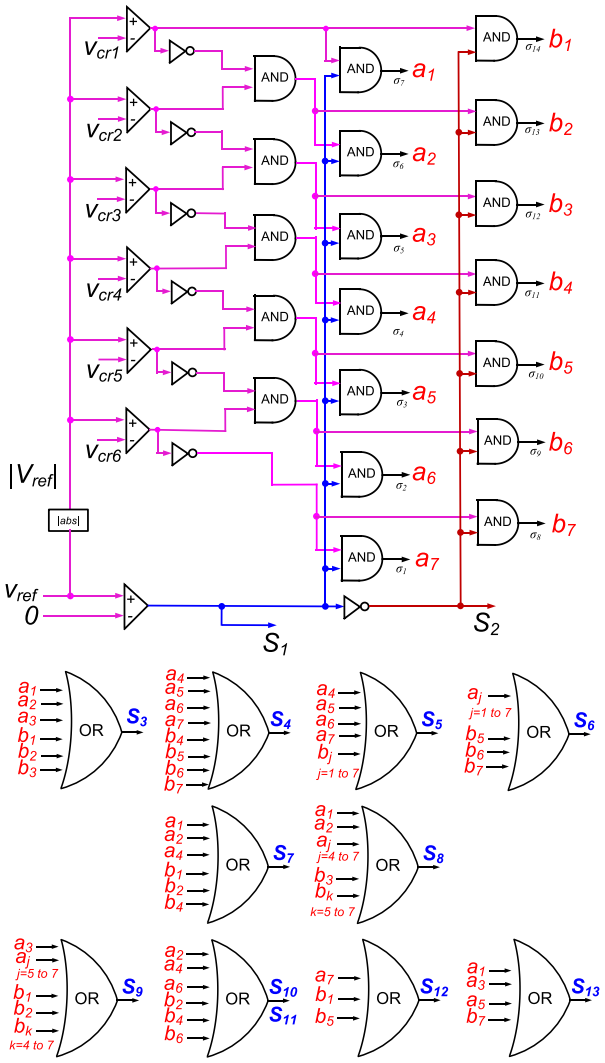

Fig. 4. Logic gates based implementation of modulation scheme.

structure offers voltage balancing of capacitors even at low modulation indices because the charging paths are provided at lower levels of voltages, viz. 0 (for C_1, C_2, and C_3), $\pm 0.5V_{\rm dc}$ (for C_1, C_2, and C_3), $\pm V_{\rm dc}$ (for C_1, C_2, and C_3), and $\pm 1.5V_{\rm dc}$ (for C_1). Also, as far as utilization of power switches is concerned, all switches are fully utilized when the modulation index is in the range of 0.5 to 1. When M is in the range of 0.3 to 0.5, switch S_3 is not utilized. Similarly, both S_3 and S_7 are not utilized when M is in the range of 0 to 0.3. Thus, 11 of the 13 power switches are utilized at all the regions of the modulation index.

III. Components' Ratings, Capacitances, Loss Analysis, and Design

A. Voltage and Current Ratings of Power Switches

For the proposed inverter, the PIV requirements for the power switches are presented in Table III. It can be seen that the PIV rating of two switches is ≈17% of the operating voltage. For seven switches, the PIV rating is ≈34% of the operating voltage.

TABLE III
PIVs of Power Switches in the Proposed Inverter With $V_{\rm DC}$ as Input Voltage and $3V_{\rm DC}$ as Peak Output

PIV	Power Switches
$0.5\ V_{dc}$	S_{10}, S_{11}
V_{dc}	D, S_3, S_4, S_7, S_8, S_9, S_{12}, S_{13}
$2V_{dc}$	S_1, S_2, S_5, S_6

TABLE IV
Maximum Currents Through Power Switches in the Proposed Inverter

Current stress	Power Switches
I_{ac}	S_1, S_2, S_3, S_7,S_{10},S_{11},S_{12},S_{13}
I_{C1}	S_4
I_{ac}+I_{C2C3}	S_5, S_6, S_8, S_9
I_{ac}+I_{C1}+I_{C2C3}	D

$I_{\rm ac}$, I_{C1}, and $I_{C2\,C3}$ are the maximum values of currents $i_{\rm ac}$, i_{C1}, and $i_{C2\,C3}$, respectively.

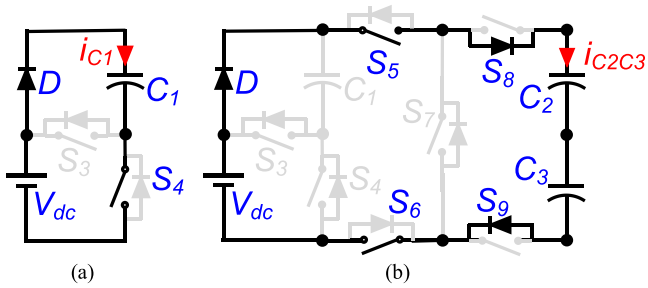

Fig. 5. Charging path for: (a) capacitor C_1 and (b) capacitors C_2 and C_3.

And, only for four switches, the PIV rating is ≈67% of the operating voltage.

Moreover, the minimum current ratings of power switches are presented in Table IV. Eight power switches (S_1, S_2, S_3, S_7, S_{10}, S_{11}, S_{12}, and S_{13}) need to carry only the load current ($i_{\rm ac}$) and hence they should be minimally rated at the value equal to the amplitude of the load current ($I_{\rm ac}$). For a power rating equal to P_o, and considering the case of unity power factor load (i.e., the worst case scenario for determining the values of capacitances, as discussed in the following section), this value can be calculated as

$$I_{\rm ac} = \frac{\sqrt{2} * P_o}{3 * M * V_{\rm dc}}. \tag{3}$$

Switch S_4 needs to carry the charging current for the capacitor C_1 and hence it should be rated at least at the value equal to peak value (I_{C1}) of the charging current i_{C1} of the capacitor C_1. The path for i_{C1} is shown in Fig. 5(a), and it can be calculated as [26]

$$i_{C_1} = \left(\frac{V_{\rm dc} - V_D - v_{C1}}{r_D + r_{S4} + R_{{\rm ESR},C1}}\right) * \exp\left(-\frac{t}{(r_D + r_{S4} + R_{{\rm ESR},C1}) * C_1}\right) \tag{4}$$

where V_D is the ON-state voltage drop across the diode D, v_{C1} is the voltage across capacitor C_1, r_D and r_{S4} are the ON-state resistances of D and transistor part of S_4, and $R_{\mathrm{ESR},C1}$ is the equivalent series resistance (ESR) of C_1.

Switches S_5, S_6, S_8, and S_9 need to carry two currents: the load current (i_{ac}) and the charging current for the capacitors C_2 and C_3 ($i_{C2\,C3}$) and hence it should be rated at least at the value equal to sum of their peak values. The path for $i_{C2\,C3}$ is shown in Fig. 5(b), and it can be calculated as

$$i_{C_2C_3} = \left(\frac{V_2}{R_2}\right) * \exp\left\{-\frac{t}{(R_2) * \left(\frac{C_2C_3}{C_2+C_3}\right)}\right\} \tag{5}$$

where

$$V_2 = V_{\mathrm{dc}} - V_D - V_{D8} - V_{D9} - v_{C2} - v_{C3} \tag{6}$$

$$R_2 = r_D + r_{D8} + r_{D9} + r_{S5} + r_{S6} + R_{\mathrm{ESR},C2C3}. \tag{7}$$

Here, V_D, V_{D8}, and V_{D9} are the ON-state voltage drops across D, the diodes of switches S_8 and S_9, respectively, v_{C2} and v_{C3} are the voltages across capacitors C_2 and C_3, respectively, r_D, r_{D8}, r_{D9}, r_{S5}, and r_{S6} are the respective ON-state resistances of D, diode of S_8, diode of S_9, transistor part of S_5 and transistor part of S_6, and $R_{\mathrm{ESR},C2\,C3}$ is the ESR of the series combination of C_2 and C_3.

B. Capacitance Calculations

The three capacitors C_1, C_2, and C_3 in the proposed inverter are maintained at V_{dc}, $0.5V_{\mathrm{dc}}$, and $0.5V_{\mathrm{dc}}$, respectively, by employing the switched-capacitors principle as described previously. Now, when these capacitors discharge to supply the load, voltage ripples will appear on them, which should not be more than 10% of the capacitors' desired voltages [27].

The voltage ripple that a capacitor experiences is determined by its capacitance, discharging time, and the load current. As far as load current is concerned, the worst case scenario is when the load is purely resistive [6], [7]. It can be inferred from Figs. 2 and 3 that during the transitions $(+1.5V_{\mathrm{dc}}) \leftrightarrow (+2V_{\mathrm{dc}})$ and $(+2.5V_{\mathrm{dc}}) \leftrightarrow (+3V_{\mathrm{dc}})$, C_1 undergoes discharging without any in-between state that offers opportunity for charging. Thus, for a resistive load R_L and angular frequency $\omega_o = 2\pi f_{\mathrm{ref}}$, the maximum discharge can be expressed as

$$\Delta Q_{C_1} = C_1 * \Delta V_{C_1} = \tag{8}$$

$$\int_{\theta_2/\omega_o}^{\theta_3/\omega_o} \frac{2.5V_{\mathrm{dc}}}{R_L}dt + \int_{\theta_3/\omega_o}^{(\pi-\theta_3)/\omega_o} \frac{3V_{\mathrm{dc}}}{R_L}dt + \int_{(\pi-\theta_3)/\omega_o}^{(\pi-\theta_2)/\omega_o} \frac{2.5V_{\mathrm{dc}}}{R_L}dt$$

$$\Delta Q_{C_1} = \frac{V_{\mathrm{dc}}}{\omega_o * R_L} * (3\pi - 5\theta_2 - \theta_3). \tag{9}$$

And, it can be observed from Fig. 3 that

$$\theta_2 = \sin^{-1}\left(\frac{2}{3M}\right) \tag{10}$$

$$\theta_3 = \sin^{-1}\left(\frac{5}{6M}\right). \tag{11}$$

With a maximum allowed voltage ripple of 10%, we have

$$\frac{100\Delta V_{C_1}}{V_{\mathrm{dc}}} \leq 10. \tag{12}$$

Using these equations, we have

$$C_1 \geq \frac{10}{2\pi * f_o * R_L} * \left\{3\pi - 5\sin^{-1}\left(\frac{2}{3M}\right) - \sin^{-1}\left(\frac{5}{6M}\right)\right\}. \tag{13}$$

Similarly, for capacitor C_2, we have

$$\Delta Q_{C_2} = C_2 * \Delta V_{C_2} = \int_{\theta_1/\omega_o}^{\theta_2/\omega_o} \frac{1.5V_{\mathrm{dc}}}{R_L}dt + \int_{\theta_2/\omega_o}^{\theta_3/\omega_o} \frac{2.5V_{\mathrm{dc}}}{R_L}dt + \int_{\theta_3/\omega_o}^{(\pi-\theta_3)/\omega_o} \frac{3V_{\mathrm{dc}}}{R_L}dt + \int_{(\pi-\theta_3)/\omega_o}^{(\pi-\theta_2)/\omega_o} \frac{2.5V_{\mathrm{dc}}}{R_L}dt + \int_{(\pi-\theta_2)/\omega_o}^{(\pi-\theta_1)/\omega_o} \frac{1.5V_{\mathrm{dc}}}{R_L}dt \tag{14}$$

$$\Delta Q_{C_2} = \frac{V_{\mathrm{dc}}}{\omega_o * R_L} * (3\pi - 3\theta_1 - 2\theta_2 - \theta_3) \tag{15}$$

where

$$\theta_1 = \sin^{-1}\left(\frac{1}{2M}\right). \tag{16}$$

With a maximum allowed voltage ripple of 10%, we have

$$\frac{100\Delta V_{C_2}}{0.5V_{\mathrm{dc}}} \leq 10. \tag{17}$$

Using these equations, we have

$$C_2 \geq \frac{20}{2\pi f_o R_L} \left\{3\pi - 3\sin^{-1}\left(\frac{1}{2M}\right) - 2\sin^{-1}\left(\frac{2}{3M}\right) - \sin^{-1}\left(\frac{5}{6M}\right)\right\}. \tag{18}$$

A similar analysis for C_3 would show that it is equal to C_2, i.e.,

$$C_3 = C_2. \tag{19}$$

C. Loss Analysis

The efficiency of the inverter can be expressed as

$$\eta = \frac{P_{\mathrm{output}}}{P_{\mathrm{input}}} = \frac{P_{\mathrm{output}}}{P_{\mathrm{output}} + P_{\mathrm{loss}}} \tag{20}$$

where P_{output}, P_{input}, and P_{loss} are the output power, input power, and total power losses, respectively.

Power losses in SCMLIs are categorized into [20], [21]: 1) capacitor power losses; 2) switching power losses; and 3) conduction power losses. These are discussed in brief herewith.

1) Capacitor Power Losses: In any given working states of the inverter, voltage ripple in a switched capacitor with current i_C is obtained as [20]

$$\Delta V_C = \frac{1}{C}\int_{t_a}^{t_b} i_C dt \tag{21}$$

where (t_b–t_a) is the time span of discharging during the state being considered. If $f_{\rm ref}$ is the power frequency, then the power losses caused due to voltage ripple during a state are given by

$$P_{\rm loss,ripple} = \frac{f_{\rm ref}}{2} C(\Delta V_C)^2. \tag{22}$$

Power losses also take place in a capacitor due to its ESR ($R_{\rm ESR}$), given by

$$P_{\rm loss,cc} = \frac{R_{\rm ESR} f_{\rm ref}}{2}\int_{t_a}^{t_b} i_C^2 dt. \tag{23}$$

Hence, total losses in a capacitor during a working state can be obtained by adding (22) and (23).

2) Switching Power Losses: Switching losses take place in power switches during transitions. For a switch, considering the overlap between current and voltage waveforms during transitions, these losses are obtained as [27]:

$$P_{\rm loss,sw} \approx \frac{1}{2} V_o\, I_o\, (t_{\rm on} + t_{\rm off}) f_{\rm sw} \tag{24}$$

where $t_{\rm on}$ and $t_{\rm off}$ are turn-ON and turn-OFF times of the switch, $f_{\rm sw}$ is the switching frequency, I_o is the current during conduction, and V_o is the blocking voltage.

Switching losses in a power switch can be also calculated by considering the parasitic capacitance C_{oss} between the power terminals of the power switch, the voltage stress $V_{\rm o}$ across it, and the switching frequency $f_{\rm sw}$ as [23]

$$P_{\rm loss,sw} = C_{oss} V_o^2 f_{\rm sw}. \tag{25}$$

Equations (24) and (25) lead to similar results.

3) Conduction Power Losses: Power losses due to conduction in a switch ($P_{\rm loss,con,sw}$) and a power diode ($P_{\rm loss,con,d}$) are obtained as [27]

$$P_{\rm loss,con,sw} \approx V_{\rm on,sw} I_{\rm sw,avg} + R_{\rm on,sw} I_{\rm sw,rms}^2 \tag{26}$$

$$P_{\rm loss,con,d} \approx V_{\rm on,d} I_{\rm d,avg} + R_{\rm on,d} I_{\rm d,rms}^2 \tag{27}$$

where $V_{\rm on,sw}$ and $V_{\rm on,d}$ are the ON-state voltage drops across the transistor part and diode of a switch, respectively, $R_{\rm on,sw}$ and $R_{\rm on,d}$ are the ON-state resistances of the transistor part and diode of the switch, respectively, $I_{\rm sw,avg}$ and $I_{\rm sw,rms}$ are the average and rms currents through the transistor part, respectively, and $I_{\rm d,avg}$ and $I_{\rm d,rms}$ are the average and rms currents through the diode of the power switch, respectively.

Hence, the overall power losses can be calculated by the aggregation of these losses.

D. Design Procedure

In order to design the proposed inverter for a given application, the primary calculations relate to the voltage and current ratings of power switches and values of capacitors, once the output specifications are known. A procedure for design is depicted in Fig. 6.

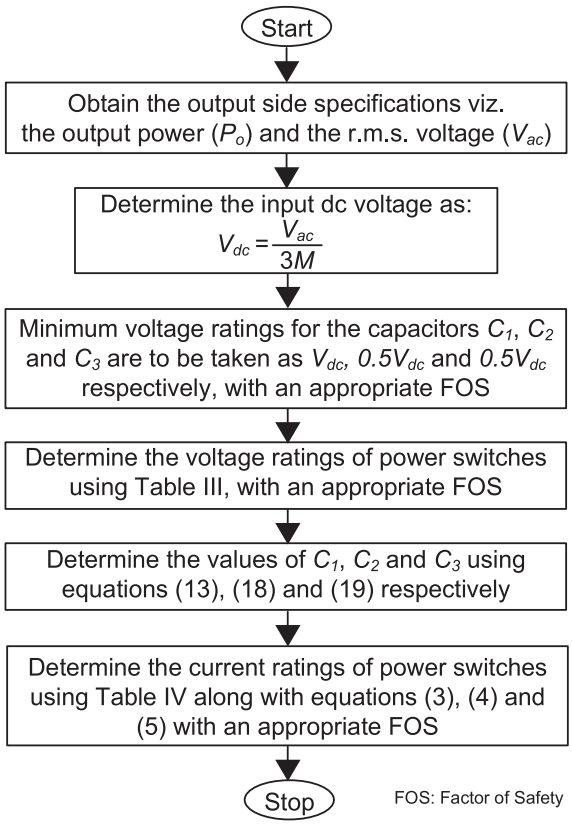

Fig. 6. Design procedure for determination of component ratings in the proposed inverter.

IV. Comparison With Other SCMLI Topologies

As far as the classical multilevel topologies (viz. DC, FC, and CHB) are concerned, the voltage gain is unity, whereas SCMLI structures offer a voltage gain greater than unity. Hence, an appropriate comparison of the proposed topology would be with other switched capacitors based structures. In this section, the proposed inverter is compared with the topologies proposed in [6]–[22].

In Table V, a comparison of the proposed inverter with other SCMLIs is presented in terms of components, PIV and TSV, voltage gain, number of components per level, CF as defined in (1), and possibility of voltage balancing of capacitor(s) at all values of modulation index. It can be observed that the per level component count is lowest as compared to all structures except the one proposed in [11]. But the TSV and PIV are very high in [11] and it does not offer voltage balancing of capacitors at all values of modulation index. The CF is also least in the proposed topology as compared to the other except [11], but once again at the cost of other disadvantages.

The topologies presented in [9], [12], [14], [15], [17], [18], and [22] require power switches with lesser PIVs, but the values of component count per level and CF are higher. The proposed topology has partial structural similarity with the SCMLI

TABLE V
COMPARISON OF THE PROPOSED TOPOLOGY WITH SCMLI TOPOLOGIES PRESENTED IN [6]–[22]*

Reference	N_L	N_{IS}	N_S	N_D	N_{AD}	N_{GD}	N_C	$TSV_{p.u}$	$PIV_{p.u}$	β	N_{Comp}/N_L	*CF*		Possibility of capacitors' voltage balancing at all modulation indices
												(α=1)	(α=1.5)	
[6]	9	1	10	10	1	8	2	11	2	2	3.444	4.056	4.361	Yes
[7]	7	1	10	10	0	10	2	18	3	3	4.571	5.429	5.857	Yes
[8]	5	1	6	6	2	6	1	12	2	2	4.200	5.400	6.000	Yes
[9]	5	1	6	6	2	6	2	8	1	2	4.400	5.200	5.600	Yes
[10]	5	1	6	6	1	6	1	11	2	2	4.000	5.100	5.650	Yes
[11]	13	1	10	10	4	10	4	36	6	6	2.923	3.385	3.615	No
[12]	5	1	9	9	0	9	1	9	1	2	5.600	6.500	6.950	Yes
[13]	7	1	16	16	0	14	2	16	2	3	6.857	7.619	8.000	Yes
[14]	5	1	9	9	1	8	1	9	1	2	5.600	6.500	6.950	Yes
[15]	5	1	12	12	0	12	4	20	1	4	8.000	9.000	9.500	Yes
[16]	5	1	7	7	3	7	2	9	2	2	5.200	6.100	6.550	Yes
[17]	9	1	12	12	0	11	2	11	1	2	4.111	4.722	5.028	Yes
[18]	9	1	11	11	0	10	2	10	1	2	3.778	4.333	4.611	Yes
[19]	9	1	12	12	0	12	2	22	2	4	4.222	4.833	5.139	No
[20]	13	1	14	14	1	14	3	28	3	6	3.538	3.897	4.077	No
[21]	13	1	13	13	2	13	3	39	6	6	3.385	3.884	4.135	No
[22]	9	1	11	11	0	10	2	10	1	2	3.778	4.333	4.611	Yes
Proposed	13	1	13	13	1	12	3	17	2	3	3.231	3.667	3.885	Yes

*$TSV_{p.u.}$ and $PIV_{p.u.}$ are w.r.t. input voltage V_{dc}.

presented in [17] as both include two capacitors split with a bidirectional-blocking switch. The component count per level is significantly high in SCMLI presented in [17], even though it is marginally superior in terms of TSV and PIV. However, the proposed topology offers better waveform resolution and larger voltage gain.

The proposed inverter also has similarity to SCMLI presented in [18] and [22] in terms of two capacitors split with a bidirectional-blocking switch and the way a set of five switches (S_5–S_9) are configured. Once again, as observed from Table V, though the structures presented in [18] and [22] are marginally better than the proposed inverter in terms of TSV and PIV, but they require more components per level. Also, the proposed inverter offers more number of levels and a higher voltage gain.

Additionally, as far as the structural comparison with the topology presented in [19] is concerned, the only major change in the proposed inverter is that the single capacitor is split into two (and a bidirectional-blocking switch is inserted), thereby yielding 13 levels instead of nine. With this modification, the gain is reduced to three from four, but simultaneously, the per level values of component count, TSV, and PIV are also significantly reduced. Moreover, the topology proposed in [19] uses the dc source (of voltage V_{dc}) and one capacitor (charged to V_{dc}) together to charge the second capacitor to voltage $2V_{dc}$, so as to obtain a voltage gain of 4. This, however, affects the charging of capacitors at low values of modulation index.

It can be thus said that the proposed inverter has better structural characteristics (in terms of component count, PIV, TSV, and waveform resolution, and hence much lower value of CF) and performance characteristics (in terms of functioning at low modulation indices and capacitors voltage balancing) compared to the topology presented in [19], though the voltage gain is less as compared to that of [19]. The topologies presented in [11], [20], and [21] offer a very high voltage gain of 6, but at the cost of large PIV ratings and subdued performance at lower modulation indices.

TABLE VI
SIMULATION PARAMETERS FOR VERIFICATION OF THE PROPOSED INVERTER

Parameter	Unit	Value
V_{dc}	[V]	130
C_1	[μF]	3000
C_2, C_3	[μF]	4500
f_{ref}	[Hz]	50
f_{cr}	[Hz]	2100
M	-	0.85, 0.9, 0.45, 0.14
Load resistance	[Ω]	100,50
Load inductance	[mH]	160,80

Hence, it can be safely concluded that the topology proposed in this work is highly competent in terms of an overall CF, PIV and TSV requirements, and operation at low modulation indices. One limitation of the proposed structure is that it may not readily eliminate leakage currents (especially in PV application), as the dc input is not directly connected to one of the load terminals. Also, the switched-capacitor operation in the proposed inverter leads to large inrush currents, and hence, the topology will be limited to relatively low current applications.

V. SIMULATION AND EXPERIMENTAL VERIFICATION, POSSIBLE APPLICATIONS, AND EXTENSION OF TOPOLOGY

A. Simulation Results

To examine the performance of the proposed topology and the control scheme, a simulation model is developed using piecewise linear electrical circuit simulation (PLECS) software tool, developed by Plexim. Values of various components and parameters are listed in Table VI. The model is developed using the design procedure mentioned in Fig. 6, for 1 kW output power and 230 V rms voltage at a power frequency of 50 Hz.

Simulation results for $M = 0.85$ and load comprising resistance of 50 Ω and inductance of 80 mH are shown in Fig. 7. It can be seen in Fig. 7(a) that the load voltage has 13 levels in steps of 65 V and the peak value ≈390 V as expected. The load

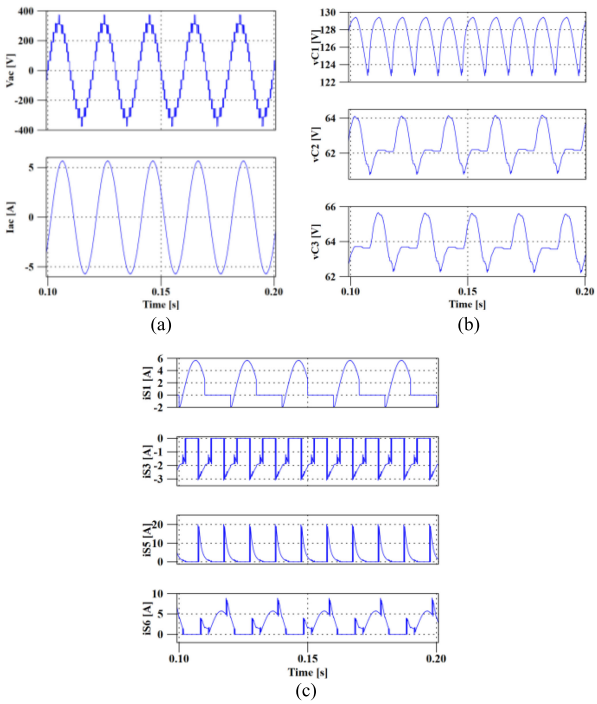

Fig. 7. For $M = 0.85$ and load with (50 Ω, 80 mH), simulation results showing (a) load voltage and load current; (b) voltages of capacitors C_1, C_2, and C_3; and (c) currents through devices S_1, D, S_4, and S_5.

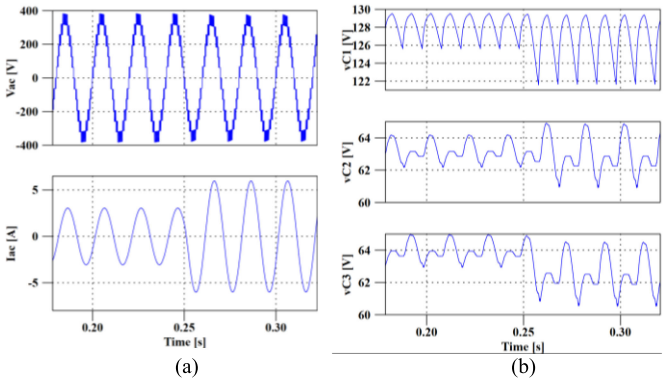

Fig. 8. For $M = 0.90$ and transition in load from (100 Ω, 160 mH) to (50 Ω, 80 mH), simulation results showing (a) load voltage and load current; and (b) voltages of capacitors C_1, C_2, and C_3.

current waveform indicates the inductive nature of the load, the output power being approximately 1 kW. The voltages of the three capacitors are shown in Fig. 7(b) and it can be seen that C_1, C_2, and C_3 get charged approximately to 130, 65, and 65 V, with 5% voltage ripples. From Table IV, it can be observed that there are four variations of switch current and accordingly, the currents through power switches S_1, D, S_4, and S_5 are shown in Fig. 7(c). It can be seen that the steady-state peak currents are within 20 A in the switches.

In Fig. 8, simulation results for a sudden change in load are shown. For t <0.25 s, the load comprises resistance of 100 Ω and inductance of 160 mH and at $t = 0.25$ s, it is changed to 50 Ω, 80 mH. It can be seen from Fig. 8(a) that as the load current

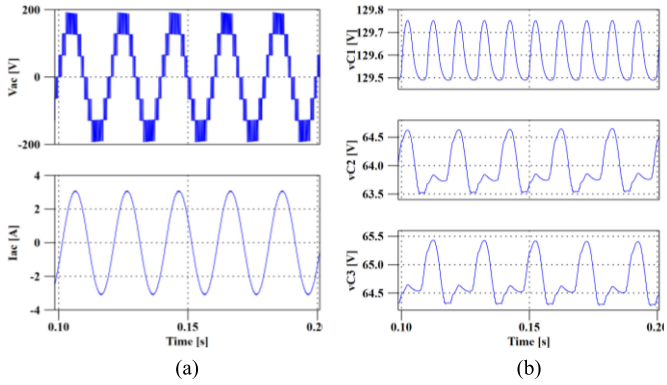

Fig. 9. For $M = 0.45$ and load (50 Ω, 80 mH), simulation results showing (a) load voltage and load current; and (b) voltages of capacitors C_1, C_2, and C_3.

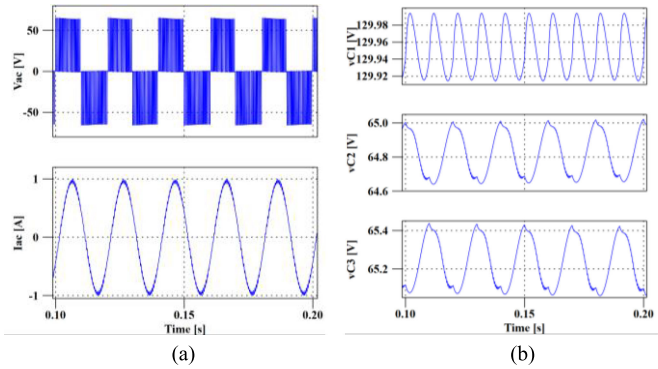

Fig. 10. For $M = 0.14$ and load (50 Ω, 80 mH), simulation results showing (a) load voltage and load current; and (b) voltages of capacitors C_1, C_2, and C_3.

is changed significantly, the load voltage is maintained satisfactorily. The voltages of the capacitors are shown in Fig. 8(b) and they are within the limit of 10% voltage ripples.

For a lower modulation index of 0.45, the waveforms are shown in Fig. 9. As expected, the load voltage has seven levels with a reduced peak value, as can be seen in Fig. 9(a). Moreover, the capacitors remain balanced at their respective desired voltages of 130, 65, and 65 V, as can be seen in Fig. 9(b).

Finally, the modulation index is further reduced to a very low value of 0.14 and the results are shown in Fig. 10. It can be seen in Fig. 10(a) that the output voltage has three levels as expected with reference to Table II. More importantly, even at a very low modulation index, the capacitors remain balanced, as can be seen in Fig. 10(b).

In the PLECS-based simulation model, IRFP460 MOSFETs were used as power switches and the datasheet of IRFP460 was imported for the analysis of power losses. The distribution of power losses is presented in Fig. 11 under full load conditions. The total loss incurred in power switches is 34.59 W, whereas the overall efficiency achieved is 96.53%.

B. Experimental Results

To validate the proposed inverter, a laboratory setup was made using power switch modules (with MOSFETs IRFP460 with

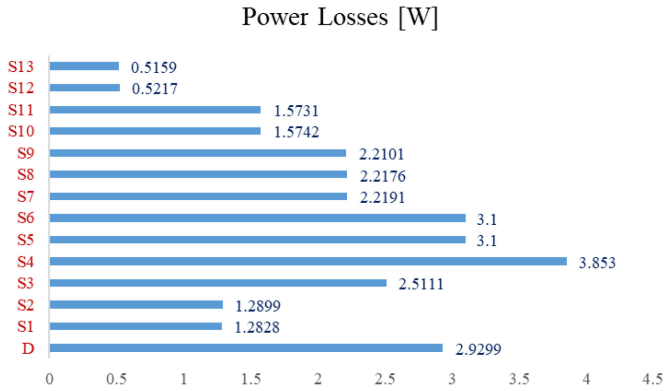

Fig. 11. Power losses obtained using the simulation model of the proposed inverter in PLECS software (output power is 1 kW with $M = 0.85$ and inductive load of 50 Ω, 80 mH).

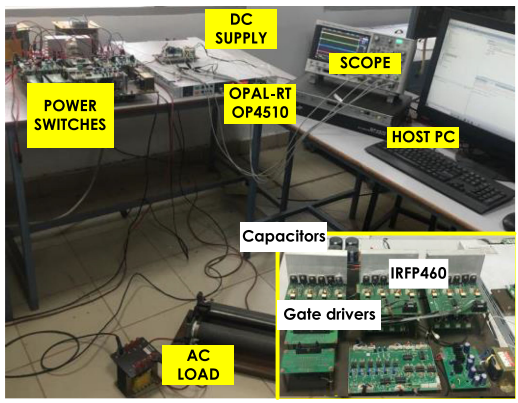

Fig. 12. Main parts of the experimental setup and power switches with drivers.

TABLE VII
PARAMETERS FOR EXPERIMENTAL VERIFICATION OF THE PROPOSED INVERTER

Parameter	Unit	Value
V_{dc}	[V]	130
C_1	[μF]	3000
C_2, C_3	[μF]	4500
f_{ref}	[Hz]	50
f_{cr}	[Hz]	2100
M	-	0.95, 0.14
Load resistance	[Ω]	100,50
Load inductance	[mH]	160,80

Si827-5 gate driver ICs, with electrically isolated power supplies). A photograph of the setup is shown in Fig. 12. Values of various components and parameters are listed in Table VII. Regulated dc power supply Keysight N8952A (0-200V/0-210A) was used as input dc source. OPAL-RT OP4510 real-time controller was used in conjunction with MATLAB/Simulink to generate the gate signals. These signals are shown for a modulation index of 0.95 and $f_{cr} = 2100$ Hz in Fig. 13. Accordingly, the switching frequencies of the power switches are presented in Table VIII. It can be seen that the switches with higher PIVs operate with low switching frequency.

The waveforms for load voltage and load current, capacitors' voltages and currents of power switches S_1, D, S_4, and S_5 are,

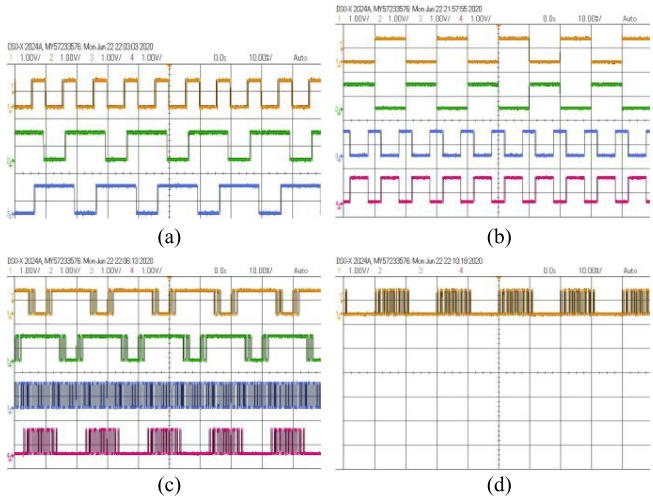

Fig. 13. Switching signals for power switches: (a) S_1, S_2, and S_3; (b) S_4, S_5, S_6, and S_7; (c) S_8, S_9, S_{10} (same as S_{11}), and S_{12}; and (d) S_{13}.

TABLE VIII
SWITCHING FREQUENCIES FOR $M = 0.95$, $FCR = 2100$ Hz

Power switch(es)	Switching Frequency [Hz]
S_1 , S_2	50
S_6	300
S_5	450
S_3, S_4	600
S_8, S_9	1100
S_7	2200
S_{12}, S_{13}	2500
S_{10}, S_{11}	4800

respectively, shown in Fig. 14(a)–(c). It can be seen that C_1 gets approximately charged to 130 V, whereas C_2 and C_3 attain 65 V each and a 13-level waveform is synthesized in steps of 65 V, with a peak value of almost 390 V as expected. Power measurements indicate an efficiency of 94.7% at full load with 0.85 pf, which is less than that obtained with PLECS-based simulation model. This may be attributed to the additional losses caused in the driving units of the power switches, which include a multiwinding transformer used to obtain isolated dc supplies. In Fig. 15(a), results for sudden change in load are shown, when the load is changed from (100 Ω, 160 mH) to (50 Ω, 80 mH). It can be seen that as the load current is changed significantly, the load voltage is maintained satisfactorily. The voltages of the capacitors too are within the limit of 10% ripples. Also, the harmonic profiles of the voltage and current waveforms are shown in Fig. 15(b) and (c). The respective THDs of the voltage are current waveforms are 7.2% and 0.6%. When the modulation index is reduced to a very low value of 0.14, the output voltage is three-level, as shown in Fig. 16. It can also be seen that the capacitors remain balanced even at this low value of modulation index.

C. Discussions on Results and Possible Applications

As the simulation and experimental results for the 1-kW inverter based on the proposed topology show, a high-resolution

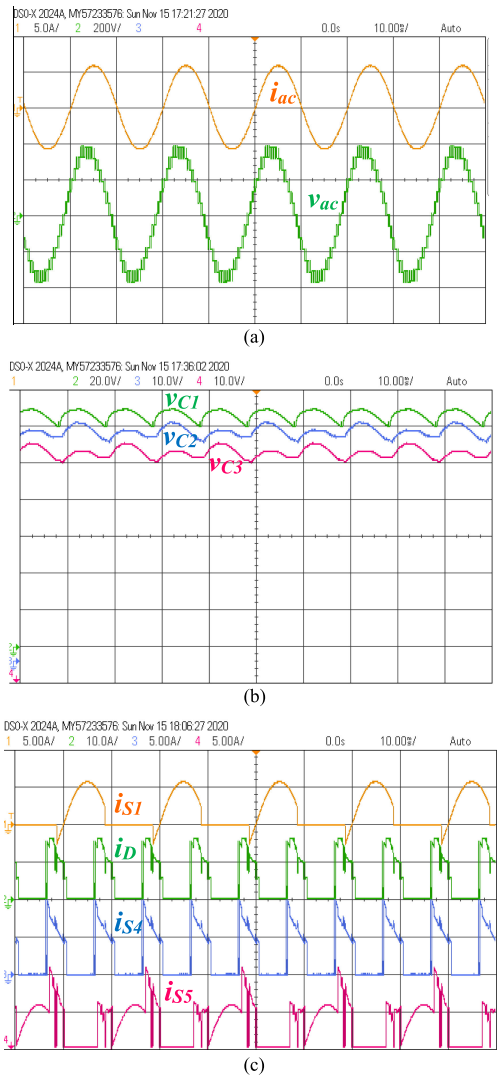

Fig. 14. Experimental results with $f_{cr} = 2100$ Hz and $M = 0.95$ showing: (a) load voltage and load current; (b) voltages of capacitors C_1, C_2, and C_3; and (c) currents through switches S_1, D, S_4, and S_5.

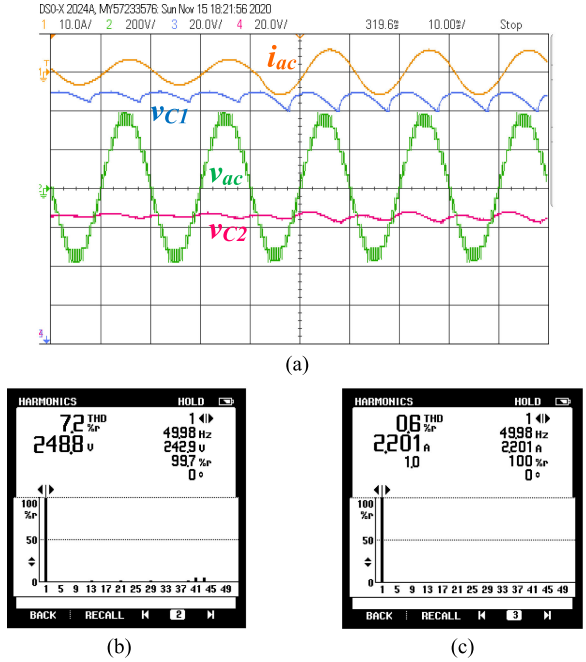

Fig. 15. (a) Experimental results with $f_{cr} = 2100$ Hz and $M = 0.95$, with transition in load from (100 Ω, 160 mH) to (50 Ω, 80 mH) showing: load voltage, load current, and voltages of capacitors C_1 and C_2. (b) Harmonic profile of the output voltage. (c) Harmonic profile of the load current (100 Ω, 160 mH).

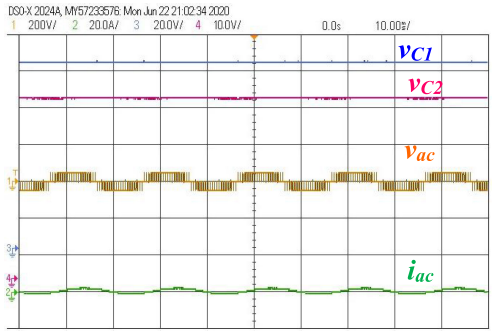

Fig. 16. Experimental results with $f_{cr} = 2100$ Hz and $M = 0.14$, with load (50 Ω, 80 mH), showing: load voltage, load current, and voltages of capacitors C_1 and C_2.

13-level waveform is obtained with triple voltage gain. The designed values enable a satisfactory performance of capacitors in terms of voltage ripples at full load. In addition, operation at low values of modulation index does not affect the balancing of the voltages of capacitors. The distribution of power losses in the switches indicates that the fundamental frequency operation of S_1 and S_2 helps in limiting their losses, though they have higher PIVs as compared to other power switches. Similarly, the low-frequency operation of S_5 and S_6 helps in limiting their losses. These results also validate the efficacy of the proposed modulation scheme.

As far as the possible applications of the proposed topology are concerned, based on the survey of literature on SCMLIs, the following possibilities have been identified.

1) High-Frequency AC (HFAC) Distribution: Power distribution system (PDS) based on HFAC technology has been increasingly used in high power density applications such as telecommunication [28], [29], spacecraft [28], and computer systems [28], [30] because HFAC-PDS greatly reduces the number of power conversion stages [28], transformer size, and filter size [31]. Other emerging applications of HFAC PDS are in small-scale networks such as microgrids [32], buildings [32], and EVs [33]. In these applications, conventional multilevel topologies with a number of levels more than five have less feasibility due to the capacitor voltage imbalance issues [34]. As a result, SCMLIs have become a popular solution for HFAC applications, as the high fundamental frequency increases the practicality of SCMLIs [35]. For such applications, SCMLI topologies eliminate the requirement of bulky step-up transformers or boost dc–dc converters in systems where only a low-voltage dc bus is available.

2) PV-Based Power Generation Systems: Since the output voltage of most PV arrays is relatively low, some sort of voltage

boosting for the grid connection becomes necessary. Boosting can be achieved by the following.

1) Cascading numerous PV modules as a high-voltage string [36]. Such arrangement, however, presents challenge in terms of many mismatch issues.
2) By adding a dc–dc boost converter at the front end. Such a two-stage approach adds to the component count, costs, volume, and power losses [37].
3) By using a step-up transformer at the ac side. This, however, increases the volume, costs, and power losses of the system.

When employed in PV systems, SCMLIs present benefits in terms of inherent voltage boost, self-balancing of capacitors, high-resolution waveform for grid compatibility, and reduced filtering requirements [38].

3) EV Traction System: For the EV traction system, the following two configurations are generally used.

1) A battery is directly connected to a two-level inverter: This configuration necessitates an expensive battery with a large number of series-connected cells to achieve a high dc-link voltage [39]. Major limitations with this approach are: charge equalization among cells is slow [40], isolating one faulty cell causes reduction in the dc-link voltage, and the corresponding row of batteries needs to be disconnected from the dc link. This configuration is used only in extended-range EVs with large batteries.
2) A battery is connected to the inverter via dc–dc boost stage [41]: This configuration is used in medium-range EVs, where the energy rating of battery lies within 5–50 kWh. The presence of dc–dc boost converter extends the constant torque region but a large inductor is required at the dc–dc conversion stage, leading to increased weight and costs.

To overcome these limitations of the traditional EV drives, SCMLIs are emerging as a viable interface to convert low voltage dc to high voltage ac [42]. Additionally, as SCMLIs allow usage of low-voltage devices (MOSFETs), high switching frequency operation is facilitated, which is mainly required during increased speeds, when the frequency of the reference waveform gets close to carrier waveforms [7].

D. Extension of the Proposed Topology

The multiphase version of the proposed topology can be realized with single dc source. One leg of the three-phase structure is shown in Fig. 17(a), where v_{ao} is the pole voltage. This leg is intended to be unipolar (i.e., it generates only positive levels) and hence it is obtained by removing the switches S_1 and S_2 from the power circuit shown in Fig. 1. Various switching combinations can impart seven levels to the pole voltage (as summarized in Table IX) and hence the line voltage will have 13 levels, when a three-phase structure is realized as shown in Fig. 17(b).

Also, a single-phase extension of the proposed topology with 17-level output is shown in Fig. 18(a), in which it can be seen that the part shown in a shaded box is added to the original structure. Further extension can be carried out by adding the part shown in the shaded box, and such a generalized structure is shown in Fig. 18(b).

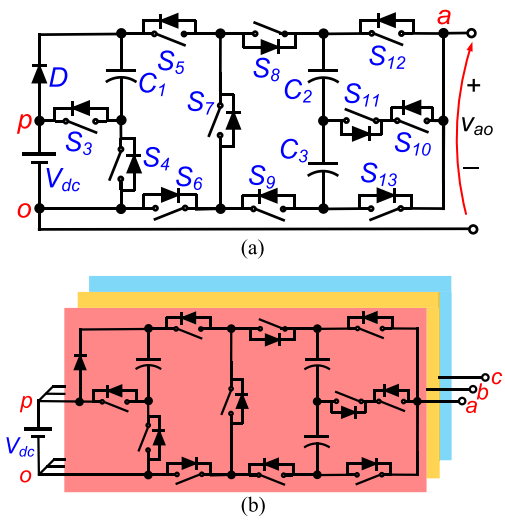

Fig. 17. (a) One leg for the multiphase version of the proposed topology. (b) Three-phase structure of the proposed topology.

TABLE IX
SWITCHING STATES FOR ONE LEG SHOWN IN FIG. 17(A)

Switches in ON state	v_{ao}
$S_4, S_5, S_8, S_6, S_9, S_{13}$	0
$S_4, S_5, S_8, S_6, S_9, S_{10}, S_{11}$	$0.5V_{dc}$
$S_4, S_5, S_8, S_6, S_9, S_{12}$	V_{dc}
$S_4, S_5, S_7, S_9, S_{10}, S_{11}$	$1.5V_{dc}$
S_3, S_5, S_8, S_{12}	$2V_{dc}$
$S_3, S_5, S_7, S_9, S_{10}, S_{11}$	$2.5V_{dc}$
$S_3, S_5, S_7, S_9, S_{12}$	$3V_{dc}$

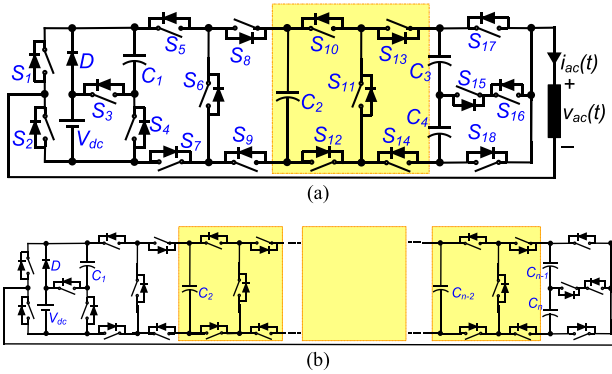

Fig. 18. (a) 17-level single-phase version of the proposed topology. (b) Generalized single-phase version of the proposed topology.

VI. CONCLUSION

A 13-level inverter with three-time voltage boosting capability is presented in this article. The switched capacitors used in the topology are self-balanced at all ranges of modulation index and the PIVs of all the power switches are significantly less as compared to the operating voltage. A comparative study of the proposed topology with the contemporary topologies

indicates its merit in terms of an overall CF based on number of components, waveform resolution, and TSV requirements. Simulation and experimental results validate the proposed structure. Generalized single-phase version and single-source three-phase version of the topology are also discussed briefly.

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