A Soft-Switching Interleaved Buck–Boost LED Driver With Coupled Inductor

Yao-Ching Hsieh, *Member, IEEE*, Hung-Liang Cheng, *Member, IEEE*, En-Chih Chang, and Wei-Di Huang

***Abstract*—In this article, a novel dc–dc light-emitting diode driver employing an interleaved converter is proposed and analyzed. The circuit topology mainly consists of two parallel buck–boost converters. A coupled inductor, which is composed of a magnetic core and two windings, is used to replace the energy storage inductors of the two buck–boost converters. This not only does not add any components, but also saves a magnetic core. The buck–boost converters are designed to operate near boundary conduction mode. Due to the characteristics of magnetic flux balance, the magnetic-excited current can be converted between the windings of the coupled inductor. By using the magnetic-excited current to release the charge stored in the parasitic capacitors of the active switches, these switches can fulfill zero-voltage switching ON (ZVS) without the use of any auxiliary switches, active clamping circuits, or snubber circuits. Moreover, the freewheel diodes of both buck–boost converters can achieve zero-current switching OFF (ZCS). The steady-state analyses for different operation modes are provided, and the mathematical equations for designing circuit components are conducted. Finally, a 200-W prototype circuit was built and tested to verify the analytical predictions. According to the experimental results, all the semiconductor devices are operated at either ZVS or ZCS, and the circuit efficiency as high as 95.0% is measured. Satisfactory performance has verified the feasibility of the proposed converter.**

***Index Terms*—Buck-boost converter, interleaved operation, light-emitting diode, zero current switching, zero voltage switching.**

I. Introduction

NOWADAYS, owing to the advantages of small size, extreme energy efficiency, long lifetime, fast response, high color rendering index, and environmental friendly, light-emitting diodes (LEDs) have been popularly used in various lighting applications to gradually replace fluorescent lamps and high-intensity discharge lamps [1]–[5]. In recent years, global warming caused by the exhaustion of fossil fuels has received widespread attention. In modern industrialized countries, the proportion of electricity consumed by lighting apparatuses to overall electricity consumption is high. In addition, the loss of the LED driver will cause the temperature to rise and shorten its lifetime. Therefore, improving the circuit efficiency of the LED lighting appliances not only saves energy, but is also essential for extending their lifetime [6], [7]. Many papers have focused on improving the efficiency of the LED driver by reducing power transfer process and/or enabling the semiconductor device to achieve soft switching [3]–[10].

Generally, LEDs are driven by dc voltage. A variety of dc–dc circuit topologies have been proposed to serve as LED drivers. The circuit efficiency is one of the main concerns. In order to improve circuit efficiency, it is important to operate the active switches at zero-voltage switching ON (ZVS) and the diodes at zero-current switching OFF (ZCS) to reduce the switching losses [11], [12]. For resonant converters, the active switches can operate at ZVS by appropriately designing the resonant circuits to present inductive, i.e., the switching frequency is above the resonant frequency [13]–[17]. In addition, the rectifier diodes can operate at ZCS. However, compared with pulsewidth modulation (PWM) converters, resonant converters require additional transformers and rectifier diodes in addition to resonant components. This not only increases the number of components, but also increases the conduction loss of circuit components.

Owing to the benefits of simple circuit topology and easy control, PWM-type converters, such as buck, buck–boost, boost, and flyback converters, and so on, are widely used to drive LEDs. However, when compared to the resonant-type converters, the PWM converters have a serious disadvantage, a hard-switching problem of the semiconductor devices. Hard-switching problems usually cause high voltage spikes or current spikes, which can lead to high switching losses and reduce component reliability. In order to solve this problem, some technologies that use active clamping circuits and passive or lossless snubber circuits are applied in the PWM converters to enable the semiconductor devices to achieve ZVS or ZCS [11], [18]–[21]. In addition to requiring more complex control, these approaches also require the use of auxiliary switches, diodes, and passive components, resulting in higher product cost. Moreover, the current loops in the active clamping circuit or the snubber circuit would produce conduction losses and even more switching losses in the auxiliary switches. The synchronous rectification (SR) technique is widely used, especially in low-voltage high-current applications. A MOSFET is served as the synchronous switch to replace the

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Yao-Ching Hsieh is with the Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung 80424, Taiwan (e-mail: ychsieh@mail.ee.nsysu.edu.tw).

Hung-Liang Cheng and En-Chih Chang are with the Department of Electrical Engineering, I-Shou University, Kaohsiung 84001, Taiwan (e-mail: hlcheng@isu.edu.tw; enchihchang@isu.edu.tw).

Wei-Di Huang is with the Department of Research and Development, Zippy Technology Corporation, New Taipei City 23142, Taiwan (e-mail: relax592@gmail.com).

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freewheel diode. The synchronous switch will be turned ON after a short deadtime when the main switch is turned OFF. Owing to smaller conducting voltage than that of a diode, there is smaller conduction losses in the synchronous switch. If the synchronous switch remains ON until the inductor current decreases from positive to a small negative value, the inductor will be operated close to boundary conduction mode (BCM). The active switch can fulfill ZVS operation by flowing the negative inductor current to release to charge stored in its parasitic capacitor [22]–[24]. However, the SR technique requires an additional current sensor and complicates control to precisely turn OFF the synchronous switch.

On the other hand, interleaved technology is useful for increasing power capacity and reducing the size of filter components. An interleaved dc–dc converter is equivalent to a parallel combination of two sets of active switches, diodes, and inductors connected to a shared filter capacitor and load. The active switches are operated 180° out of phase, producing inductor currents that are also 180° out of phase. The inductor currents flow into the shared capacitor, resulting in a smaller current ripple and voltage ripple in the capacitor than that would be achieved with a single converter. In addition, some interleaved dc–dc converters also have the advantages of ZVS operation with the aid of soft-switching technologies [25]–[31]. In the literature [25]–[27], the principle of ZVS operation is similar to that of SR technology. However, an additional inductor is required in these interleaved converters to fulfill soft switching. The additional inductor is designed to operate at the continuous-conduction mode (CCM). Before turning ON one active switch, its parasitic capacitor will be completely discharged by the current in the additional inductor. By this way, the active switch can operate at ZVS. The disadvantage is that the added inductor should operate at the CCM and is usually larger than that of the energy storage inductor in a single converter. Among the PWM-type converters, the buck–boost converter and the flyback converter can provide output voltage either higher or lower than the input voltage. With the help of the winding turn ratio of the coupled inductor, the flyback converter can provide a wider range of output voltage. However, in addition to hard switching at turning ON, high voltage spikes usually occur when the active switch is turned OFF due to the leakage inductance of the coupled inductor. In the literature [28]–[31], the interleaved flyback converters with an active clamping circuit or lossless passive snubbers have been proposed to achieve ZVS and recycle the leakage inductance energy. However, these approaches still require the use of additional auxiliary switches, diodes, and passive components to absorb or recycle the leakage inductance energy and clamp the switch voltage to a very small value.

In this article, a novel LED driver with soft-switching characteristic is proposed. The circuit topology is an interleaved converter consisting of two parallel-connected buck–boost converters using a coupled inductor.

The rest of this article is organized as follows. Section II shows the proposed circuit topology and describes the detailed operation modes at the steady state. Section III derives the mathematical equations for designing the component parameters. In Section IV, a 200-W prototype LED driver is built and tested to verify the feasibility of the proposed circuit. Finally, Section V concludes this article.

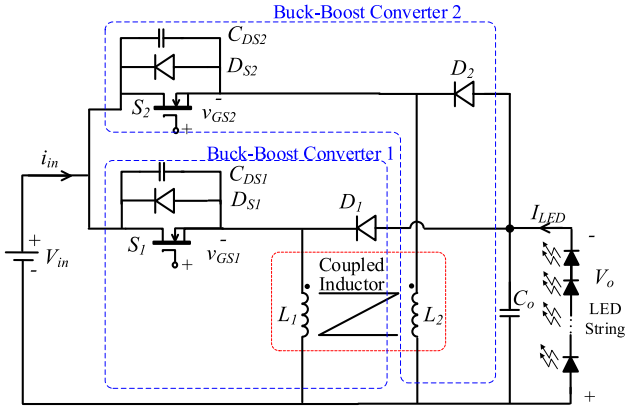

Fig. 1. Proposed LED driver with interleaved buck–boost converters.

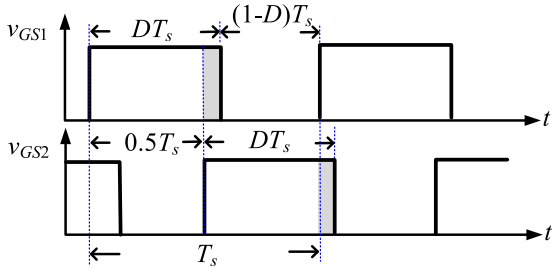

Fig. 2. Gate voltages v_{GS1} and v_{GS2}.

II. Proposed LED Driver and Operation Analysis

A. Proposed LED Driver

Fig. 1 shows the proposed dc–dc LED driver that mainly consists of two buck–boost converters. Buck–Boost Converter 1 is composed of an inductor L_1, an active switch S_1, and a freewheel diode D_1, while Buck–Boost Converter 2 is composed of L_2, S_2, and D_2. The two converters are connected in parallel to drive two strings of LEDs. L_1 and L_2 are made of a magnetic core with two windings, namely, a coupled inductor. The two windings have the same number of turns. S_1 and S_2 are two MOSFETs with inherent body diodes D_{S1} and D_{S2}, and parasitic capacitances C_{DS1} and C_{DS2}, respectively. S_1 and S_2 are alternatively turned ON and OFF by two gate voltages (v_{GS1} and v_{GS2}) at a high-switching frequency f_s.

The waveforms of v_{GS1} and v_{GS2} are shown in Fig. 2. They are complementary rectangular waveforms with a short overlap time, during which both active switches are turned ON. In the proposed LED driver, the active switches and freewheel diodes are designed to fulfill ZVS and ZCS operations, respectively, to improve the circuit efficiency. In order to achieve this design goal, the current flowing in each freewheeling diode must decrease to zero in each switching cycle.

B. Steady-State Operation

To simplify circuit analysis, the following assumptions are made.

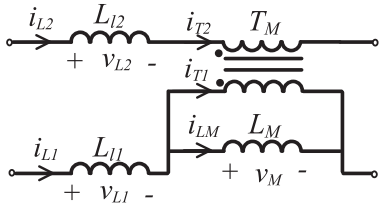

Fig. 3. Equivalent simplified model of the coupled inductor.

1) All the semiconductor devices are ideal except that the inherent body diode and parasitic capacitance of the MOSFETs are considered.
2) The output capacitor C_o is large enough to ensure constant output voltage V_o.
3) The winding resistance and the core losses of the coupled inductor are ignored. L_1 and L_2 have the same number of turns, and their leakage inductances are equal ($L_{l1} = L_{l2} = L_l$). In addition, the magnetizing inductance L_M is large enough, and the magnetic exciting current is regarded as constant I_{LM}.

Fig. 3 shows the equivalent simplified model of the coupled inductor, where T_M is an ideal transformer with a turn ratio equal to 1, and L_M is its magnetizing inductance. L_{l1} and L_{l2} represent the leakage inductances in the primary winding and the secondary winding, respectively. The voltages across L_{l1}, L_{l2}, and L_M are denoted by v_{L1}, v_{L2}, and v_M, respectively. Based on the equivalent circuit, the currents flowing in the leakages inductances, denoted by i_{L1} and i_{L2}, can be expressed as

$$i_{L1} = i_{LM} + i_{T1} \tag{1}$$

$$i_{L2} = i_{T2} = -i_{T1} \tag{2}$$

where i_{T1}, i_{T2}, and i_{LM} are the primary current, the secondary current, and the magnetic exciting current of the transformer, respectively. Combining (1) and (2), one gets

$$i_{L1} + i_{L2} = i_{LM}. \tag{3}$$

Because it is assumed that L_M is large enough and i_{LM} is almost constant, (3) demonstrates that the magnetic exciting current is converted between the primary winding and the secondary winding. Based on the Faraday's law of induction, the voltages across the magnetizing inductance is expressed as

$$v_M = \frac{L_M di_{LM}}{dt}. \tag{4}$$

Accorrding to the conducting status of the semiconductor devices, the steady-state operation can be divided into eight modes in one high-frequency cycle. The current loops in each mode are shown in Fig. 4, where the equivalent simplified model of the coupled inductor is used and $R_{\rm LED}$ represents the equivalent resistance of the LED strings. Fig. 5 illustrates the conceptual voltage and current waveforms of the main components. The detailed description of each operation mode is as follows.

1) Mode I ($t_0 < t < t_1$): Before the start of Mode I, the gated voltages v_{GS1} and v_{GS2} are at a high level, and the active switches S_1 and S_2 are both in the conducting state. The input current is divided into two parts, as shown in Fig. 4(h). One part is i_{L1} flowing through S_1 and the first winding of the coupled inductor, and the other is i_{L2} flowing through S_2 and the secondary winding. It is noted that since S_2 conducts earlier than S_1, i_{L2} is much higher than i_{L1}. In other words, from (3), it can be seen that most of the magnetic exciting current, i_{LM}, flows in the secondary winding.

Mode I starts when the gated voltage v_{GS2} becomes a low level. The current loops are shown in Fig. 4(a). S_2 is turned OFF, while S_1 remains ON. At the beginning of Mode I, i_{L2} diverts from S_2 to charge its parasitic capacitance C_{DS2}. Since the parasitic capacitance is generally very small, it only takes a very short time to charge C_{DS2} to a voltage equal to $V_{\rm in} + V_o$. As soon as v_{DS2} equals $V_{\rm in} + V_o$, i_{L2} diverts from C_{DS2} and flows through D_2 to charge the output capacitance C_o. The input and output voltages can be expressed as

$$V_{in} = v_{L1} + v_M \tag{5}$$

$$V_o = -(v_{L2} + v_M) \tag{6}$$

where v_{L1}, v_{L2}, and v_M are defined, as shown in Fig. 3. Combining (5) and (6) leads to

$$V_{\rm in} = (v_{L1} + v_{L2}) + 2v_M + V_o. \tag{7}$$

Applying the Faraday's law of induction to (3) yields

$$v_{L1} + v_{L2} = \frac{L_{l1} di_{L1}}{dt} + \frac{L_{l2} di_{L2}}{dt} = \frac{L_l di_{LM}}{dt} \tag{8}$$

where L_l is the leakage inductance. The voltage across the magnetizing inductance can be obtained by substituting (4) and (8) into (7) as

$$v_M = \frac{L_M}{L_l + 2L_M}(V_{\rm in} - V_o). \tag{9}$$

According to (9), v_M would be negative by designing V_o higher than $V_{\rm in}$. Since L_M is large enough, i_{LM} decreases linearly and slowly. Substituting (9) into (5) and (6) results in

$$v_{L1} = \frac{(L_l + L_M) V_{\rm in}}{L_l + 2L_M} + \frac{L_M V_o}{L_l + 2L_M} \tag{10}$$

$$v_{L2} = \frac{-L_M V_{\rm in}}{L_l + 2L_M} - \frac{(L_l + L_M) V_o}{L_l + 2L_M}. \tag{11}$$

From (10) and (11), v_{L1} is positive and v_{L2} is negative. Hence, i_{L1} rises and i_{L2} decreases linearly. As shown in (3), the sum of i_{L1} and i_{L2} is equal to i_{LM}. It means that the magnetic exciting current diverts from the secondary winding to the primary winding. Mode I ends as soon as i_{L2} decreases to zero.

2) Mode II ($t_1 < t < t_2$): Before this mode, C_{DS2} is clamped at a voltage equal to $V_{\rm in} + V_o$. At the beginning of Mode II, i_{L2} changes its polarity and C_{DS2} starts to release its stored energy to the input source. The equivalent circuit is shown in Fig. 4(b). Applying the Kirchhoff's voltage law (KVL) to the current loop of i_{L2} gives

$$V_{\rm in} - v_{DS2} = v_{L2} + v_M. \tag{12}$$

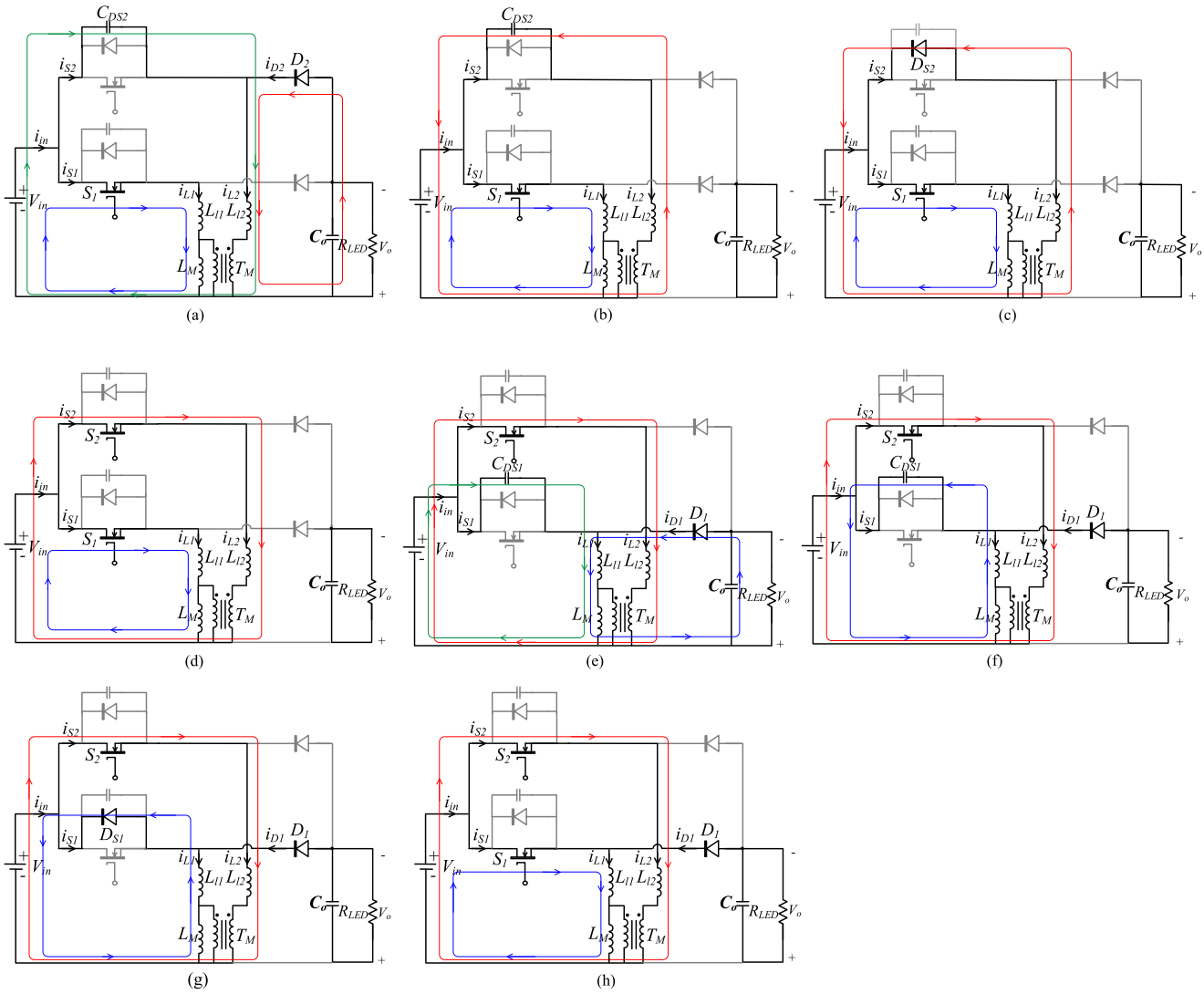

Fig. 4. Operation modes in one high-frequency cycle. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII. (h) Mode VIII.

The voltages equations v_{L1}, v_{L2}, and v_M can be obtained by using (4), (5), (8), and (12) as

$$v_{L1} = \frac{L_l V_{\text{in}}}{L_l + 2L_M} + \frac{L_M v_{DS2}}{L_l + 2L_M} \tag{13}$$

$$v_{L2} = \frac{L_l V_{\text{in}}}{L_l + 2L_M} - \frac{(L_l + L_M)\, v_{DS2}}{L_l + 2L_M} \tag{14}$$

$$v_M = \frac{L_M}{L_l + 2L_M} (2V_{\text{in}} - v_{DS2}). \tag{15}$$

During this mode, C_{DS2} is discharged and v_{DS2} keeps decreasing. As shown in (13)–(15), v_{L1} decreases; on the contrary, v_{L2} and v_M both increase. As shown in Fig. 4(b), i_{L2} is equal to the charging current of C_{DS2}

$$i_{L2}(t - t_1) = C_{DS2} \frac{dv_{DS2}(t - t_1)}{dt}. \tag{16}$$

Applying Faraday's law to the leakage inductance of the secondary winding, we obtain

$$v_{L2}(t - t_1) = L_l \frac{di_{L2}(t - t_1)}{dt} = L_l C_{DS2} \frac{d^2 v_{DS2}(t - t_1)}{dt^2}. \tag{17}$$

Combining (14) and (17) leads to

$$L_l C_{DS2} \frac{d^2 v_{DS2}(t - t_1)}{dt^2} + \frac{(L_l + L_M)}{L_l + 2L_M} v_{DS2}(t - t_1) = \frac{L_l V_{\text{in}}}{L_l + 2L_M}. \tag{18}$$

Solving (16) and (18) with the initial conditions of $i_{L2}(t_1) = 0$ and $v_{DS2}(t_1) = V_{\text{in}} + V_o$ gives

$$v_{DS2}(t - t_1) = \left(\frac{L_M V_{\text{in}}}{L_l + L_M} + V_o \right) \times \cos\left(\sqrt{\frac{(L_l + L_M)}{L_l C_{DS2}(L_l + 2L_M)}} (t - t_1) \right) + \frac{L_l V_{\text{in}}}{(L_l + L_M)} \tag{19}$$

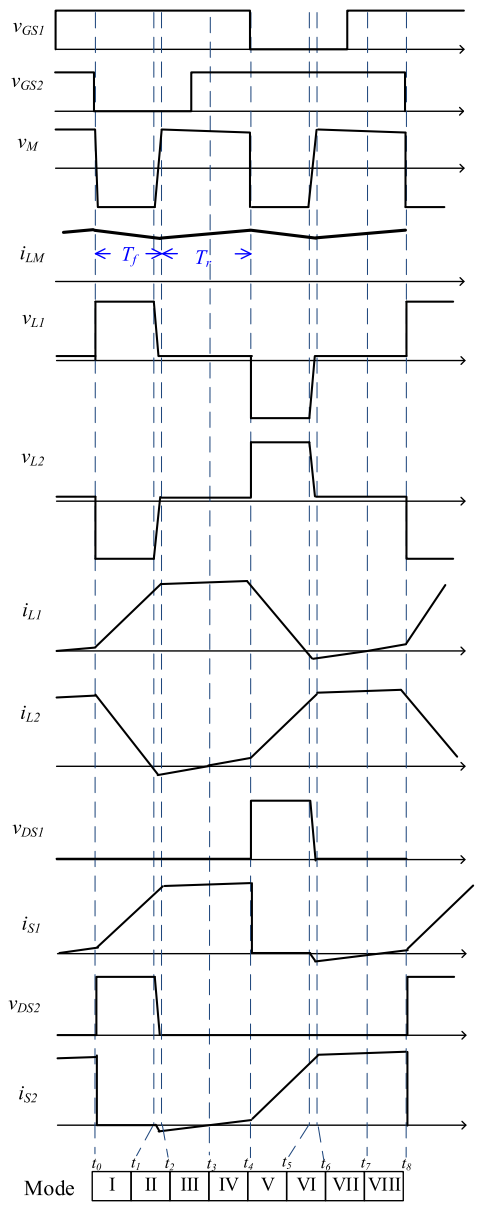

Fig. 5. Conceptual voltage and current waveforms of the main components.

$$i_{L2}(t-t_1) = -C_{DS2}\sqrt{\frac{(L_l+L_M)}{L_l C_{DS2}(L_l+2L_M)}} \times \left(\frac{L_M V_{\text{in}}}{L_l+L_M}+V_o\right)\sin\left(\sqrt{\frac{(L_l+L_M)}{L_l C_{DS2}(L_l+2L_M)}}(t-t_1)\right). \quad (20)$$

In practical, C_{DS2} is very small and would be quickly discharged to 0 V at $t = t_2$, and Mode II ends. From (19), the duration of Mode II is solved

$$t_2 - t_1 = \sqrt{\frac{L_l C_{DS2}(L_l+2L_M)}{L_l+L_M}}\cos^{-1} \times \left(\frac{-L_l V_{\text{in}}}{L_M V_{\text{in}} + V_o(L_l+L_M)}\right). \quad (21)$$

At $t = t_2$, the value of i_{L2} denoted as $I_{L2,\text{negative}}$ is negative and can be calculated by substituting (21) into (20)

$$I_{L2,\text{negative}} = -C_{DS2}\sqrt{\frac{(L_l+L_M)}{L_l C_{DS2}(L_l+2L_M)}} \times \left(\frac{L_M V_{\text{in}}}{L_l+L_M}+V_o\right)\sin\left(\sqrt{\frac{(L_l+L_M)}{L_l C_{DS2}(L_l+2L_M)}}(t_2-t_1)\right). \quad (22)$$

3) Mode III ($t_2 < t < t_3$)*:* Diode D_{S2} starts to conduct i_{L2} as soon as v_{DS2} decreases to 0 V. The current loops for Mode III are shown in Fig. 4(c). Ignoring the conducting voltage of the diode and applying KVL to the current loops, we obtain

$$V_{\text{in}} = v_{L1} + v_M = v_{L2} + v_M. \quad (23)$$

Substituting (4) and (8) into (23) leads to

$$v_M = \frac{2L_M V_{\text{in}}}{L_l+2L_M}. \quad (24)$$

Equation (24) shows that v_M is approximately equal to two times of the input voltage, and i_{LM} slowly increases. Substituting (24) into (23) results in

$$v_{L1} = v_{L2} = \frac{L_l V_{\text{in}}}{L_l+2L_M}. \quad (25)$$

Equation (25) shows that v_{L1} and v_{L2} are equal and have small values. With small v_{L1} and v_{L2}, i_{L1} and i_{L2} rise slowly.

It should be noted that D_{S2} is ON and the drain-to-source voltage of S_2 is clamped at nearly 0 V in this mode. The gated voltage v_{GS2} is designed to become high level before i_{L2} rises to zero. It ensures to turn ON S_2 at zero voltage. When i_{L2} rises to zero and starts to change polarity, S_2 is turned ON at ZVS, and the circuit operation enters the next mode.

4) Mode IV ($t_3 < t < t_4$)*:* As long as either S_2 or D_{S2} is ON, (23) holds. Therefore, the voltage equations of v_M, v_{L1}, and v_{L2} are the same as in Mode III. The voltages v_M, v_{L1}, and v_{L2} are all positive. Therefore, the currents i_{LM}, i_{L1}, and i_{L2} keep rising. When the gated voltage v_{GS1} becomes low level to turn OFF S_1, this circuit operation enters Mode V.

5) Mode V ($t_4 < t < t_5$)*–Mode VIII* ($t_7 < t < t_8$)*:* The current loops of Modes V–VIII are shown in Fig. 4(e)–(h). Due to the symmetrical operation of the two buck–boost converters, the operation analysis of Modes V–VIII is similar to the operation analysis of Modes I–IV. The description for Modes V–VIII is omitted. The circuit operation will go back to Mode I of the next high-frequency cycle when v_{GS2} becomes low level to turn OFF S_2.

III. Mathematical Equations

Based on the analysis of different operating modes, it can be known that once the active switch of one buck–boost converter is turned OFF, the current flowing in one winding of the coupled inductor will be converted to flow in the other winding. During the current conversion period, the leakage current would decrease to a small negative value, which will be used to first discharge the energy stored in the parasitic capacitance of the active switch

and then turn ON the parallel body diode. In this way, the active switch is clamped at a voltage close to 0 V before being turned ON. It ensures to achieve ZVS operation of the active switches.

A. Magnetic Exciting Current, Active Switch Current, and Output Power

Because the mutual inductance L_M is usually much higher than the leakage inductance L_l, the leakage voltages in Mode I, as shown in (10) and (11), are approximately equal to

$$v_{L1} \cong \frac{1}{2}\left(V_{\text{in}} + V_o\right) \tag{26}$$

$$v_{L2} \cong \frac{-1}{2}\left(V_{\text{in}} + V_o\right). \tag{27}$$

It should be pointed out that the parasitic capacitance of the MOSFET is very small, and it only takes a very short time to fully discharge it to 0 V. This means that in Mode II, i_{L2} is only reduced by a small value. Therefore, at the end of Mode II, i_{L2} would be approximately equal to 0 A, i.e.,

$$i_{L2}\left(t_2\right) \cong 0. \tag{28}$$

Combining (3) and (28) leads to

$$i_{L1}\left(t_2\right) \cong I_{LM}. \tag{29}$$

Equations (28) and (29) indicate that the minimum and maximum winding currents are approximately equal to zero and I_{LM}, respectively.

Referring to Fig. 5, the times to reduce and to increase the magnetic exciting current are denoted as T_f and T_r, respectively. At steady-state operation, the average voltage of the magnetizing inductance voltage in a switching cycle should be zero. Using (9) and (24) results in

$$\overline{v_M} = \frac{L_M}{L_l + 2L_M}\left(V_{\text{in}} - V_o\right) \cdot T_f + \frac{2L_M V_{\text{in}}}{L_l + 2L_M} \cdot T_r = 0. \tag{30}$$

The addition of the fall time T_f and the rise time T_r is equal to half of the switching period

$$T_f + T_r = 0.5\text{T}_s \tag{31}$$

where T_s represents the switching period. Combining (30) and (31), T_f and T_r can be expressed as

$$T_f = \frac{V_{\text{in}}}{V_{\text{in}} + V_o} T_s \tag{32}$$

$$T_r = \frac{-V_{\text{in}} + V_o}{2\left(V_{\text{in}} + V_o\right)} T_s. \tag{33}$$

From (33), it can be seen that the design constraint for properly operating the proposed circuit is that the output voltage V_o should be higher than the input voltage V_{in} since T_r must be positive. Referring to Fig. 5, I_{LM} is approximately equal to the product of the decreasing slope of i_{L1} and the fall time. Using (27) and (32), we obtain

$$I_{LM} \cong \frac{V_{\text{in}} + V_o}{2L_l} \cdot \frac{V_{\text{in}}}{\left(V_{\text{in}} + V_o\right)} T_s = \frac{V_{\text{in}} T_s}{2L_l}. \tag{34}$$

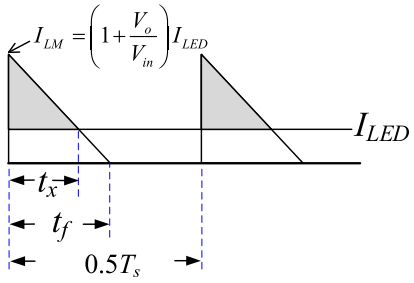

Fig. 6. Current flowing into the output terminal and the LED current.

The average value of the active switch current can be calculated by the following equation:

$$I_{S,\text{avg}} = \frac{1}{T_s}\left(\frac{I_{LM} T_f}{2} + I_{LM} T_r\right). \tag{35}$$

Substituting (32)–(34) into (35) results in

$$I_{S,\text{avg}} = \frac{V_{\text{in}} V_o T_s}{4\left(V_{\text{in}} + V_o\right) L_l}. \tag{36}$$

Each buck–boost converter supplies half of the output power. Based on the principle of energy conservation, the output power can be expressed as

$$P_o = \eta\left(2V_{\text{in}} I_{S,\text{avg}}\right) \tag{37}$$

where η represents the circuit conversion efficiency. Substituting (36) into (37), we obtain

$$P_o = \frac{\eta V_{\text{in}}^2 V_o T_s}{2\left(V_{\text{in}} + V_o\right) L_l} = \frac{\eta V_{\text{in}}^2 V_o}{2\left(V_{\text{in}} + V_o\right) L_l f_s} \tag{38}$$

where f_s represents the switching frequency. Equation (38) indicates that the output power is inversely proportional to leakage inductance and switching frequency.

B. Output Voltage Ripple

The winding currents flow to charge the output capacitor in Modes I and V. Each buck–boost converter supplies half of the output power. Fig. 6 shows the current flowing into the output terminal and the LED current. The relationship between the magnetic exciting current and the LED current is as follows:

$$\frac{t_f I_{LM}}{2} = \frac{T_s}{2} I_{\text{LED}}. \tag{39}$$

Substituting (32) into (39), we obtain

$$I_{LM} = \left(1 + \frac{V_o}{V_{\text{in}}}\right) I_{\text{LED}}. \tag{40}$$

In Mode I, the leakage voltage is expressed as (27), and the time required for the winding current to decrease from I_{LM} to I_{LED} is equal to

$$t_x = \frac{2L_l V_o}{\left(V_{\text{in}} + V_o\right) V_{\text{in}}} I_{\text{LED}}. \tag{41}$$

The light black area represents the amount of charge flowing into the output capacitor, which is expressed as

$$\Delta Q = \frac{V_o I_{\text{LED}}}{2V_{\text{in}}} \cdot t_x = \frac{L_l V_o^2 I_{\text{LED}}^2}{\left(V_{\text{in}} + V_o\right) V_{\text{in}}^2}. \tag{42}$$

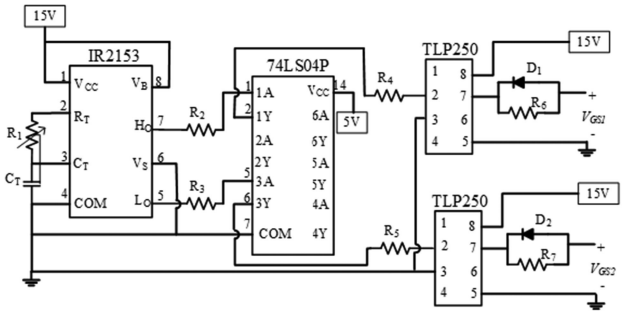

Fig. 7. Control circuit.

From (42), the output voltage ripple factor can be obtained as

$$r_v = \frac{\Delta Q_o / C_o}{V_o} = \frac{L_l V_o I_{\rm LED}^2}{C_o \left(V_{\rm in} + V_o\right) V_{\rm in}^2}. \tag{43}$$

C. Boundary Conditions of Duty Cycle of the Gate Voltages (v_{GS1} and v_{GS2})

In order to ensure ZVS, the MOSFETs must be gated before i_{L1} and i_{L2} will cross zero. As shown in Fig. 2, there is an overlap time in which both the gated voltages v_{GS1} and v_{GS2} are high level. The longer the overlap time, the earlier the gated voltages will become high level. In other words, the control circuit must be designed so that the overlap time is long enough. The minimum overlap time is denoted as $T_{\rm overlap,\ (min)}$. From Fig. 2, the duty cycle must satisfy the following inequality:

$$D \geq 0.5 \left(1 + \frac{T_{\rm overlap,(min)}}{T_s}\right). \tag{44}$$

The winding current starts to decrease at the beginning of Mode I and reaches zero at its end. The duration of Mode I is expressed in (32). The other condition to ensure ZVS operation is that there should be enough time for the winding current decreasing from the peak value to zero. It means

$$(1 - D)\, T_s \geq T_f. \tag{45}$$

Combining (32), (44), and (45), the boundary conditions for the duty cycle are expressed as

$$0.5 \left(1 + \frac{T_{\rm overlap,(min)}}{T_s}\right) < D < \frac{V_o}{V_{\rm in} + V_o}. \tag{46}$$

IV. Illustrative Example and Experimental Results

Fig. 7 shows the open-loop control circuit of the proposed LED driver. It mainly consists of a half-bridge gate driver (IR2153), two inverters (74LS04P), and two power MOSFET gate drivers (TLP250). The IR2153 outputs two complementary square waves, whose frequency is determined by the values of R_1 and C_T. There is a time interval called deadtime (1.2 μs typical value), within which both square waves are 0 V. The outputs of IR2153 are sent to 74LS04P to output two square waves with an overlap time. During this overlap time, the voltages of the two square waves are both at a high level. Finally, both square waves are sent to two TLP250 to produce the gate voltages, v_{GS1} and v_{GS2}.

TABLE I
Circuit Specifications

Input voltage, V_{in}	48 V_{dc}
Output voltage, V_o	124.4 V (=3.77 V × 33)
Output current, I_{LED}	1.6 A
Output power, P_o	200 W
LED Equivalent Resistance, R_{LED}	77.8 Ω
Switching frequency, f_s	50 kHz
Output voltage ripple factor	< 1%

It should be noted that all the equations regarding to ensure ZVS operation are based on the assumption that the mutual inductance of the coupled inductor is high enough to have constant winding current when the active switch is ON. Actually, the mutual inductance is finite, and the winding current will increase slightly during the ON-time of the active switch. The time duration for the winding current to drop from peak to zero will be different at different mutual inductances. When the mutual inductance is not large enough, in order to ensure ZVS operation, the overlap time of the simultaneous conduction of two active switches must be increased. In other words, the duty ratio D must be increased to ensure that the inequality (46) exists.

An illustrative example of a 200-W LED driver is designed. The circuit specification is listed in Table I. The input voltage is 48 $V_{\rm dc}$. The load is two LED strings connected in parallel. Each string consists of thirty-three 3W high-brightness LEDs. The rated voltage and current of each LED are 3.77 V and 0.8 A, respectively. Hence, the output voltage at rated power operation is 124.4 V. The LED equivalent resistance $R_{\rm LED}$ is calculated to be 77.8 Ω. In this illustrative example, the output voltage ripple is designed to be less than 1%.

Assuming a circuit efficiency of 95%, the leakage inductance for rated power operation can be calculated by using (38)

$$L_l = \frac{\eta V_{\rm in}^2 V_o}{2\left(V_{\rm in} + V_o\right) P_o f_s} = \frac{0.95 \times 48^2 \times 124.4}{2 \times (48 + 124.4) \times 200 \times 50 \times 10^3} = 79\,\mu{\rm H}.$$

The coupled inductor is made of E-type ferrite core E55/28/21 with the following parameters: effective magnetic cross-sectional area $A_e = 353$ mm^2 and saturation magnetic flux density $B_{\rm sat} = 0.47$ T. The main goal is to design a coupled inductor with 79-μH leakage inductance, which would not saturate at the maximum winding current. In order to determine the number of turns of the windings, the following two equations are used.

The inductance coefficient (A_L value) is used widely when designing inductors made of ferrite cores. The A_L value is defined as the ratio of inductance to the square of the number of turns, which can be expressed as

$$A_L = \frac{L_s}{N^2} = \frac{\mu_o A_e}{\frac{l_c}{\mu_r} + g} \tag{47}$$

where μ_0, μ_r, l_c, and g represent the magnetic field constant, relative permeability, magnetic path length, and width of air

gap, respectively. The magnetic flux density is expressed as

$$B = \frac{NIA_L}{A_e}. \tag{48}$$

The following steps are used to determine the number of turns of the winding (N)

Step 1: Determined the maximum winding current $I_{\max}$.

Using (40), the average mutual current is calculated as

$$I_{LM} = \left(1 + \frac{V_o}{V_{\text{in}}}\right) I_{\text{LED}} = \left(1 + \frac{124.4}{48}\right) \times 1.6 = 5.75\text{A}.$$

Considering the ripple current, the maximum winding current $I_{\max}$ is set to 6 A.

Step 2: Calculate the self-inductance of each winding (including the leakage inductance and the mutual inductance).

Two windings with the same number of turns were, respectively, wound on the upper and lower half of bobbin. Assuming that the inductive coupling coefficient k is 0.85, the self-inductance is calculated as

$$L_s = L_l/1 - k = 0.079/1 - 0.85 = 0.527\text{mH}.$$

Step 3: Determine the number of turns by the trial and error method.

Step 3a: Calculate the number of turns.

At first, the A_L value of 4000 nH is selected. Using (47), the number of turns is calculated as

$$N = \sqrt{\frac{L}{A_L}} = \sqrt{\frac{0.527 \times 10^{-3}}{4000 \times 10^{-9}}} \approx 12.$$

Step 3b: Calculate the maximum magnetic flux density and compare with the saturation flux density.

Using (48), the maximum magnetic flux density $B_{\max}$ happening at the maximum winding current is calculated as

$$B_{\max} = \frac{12 \times 6 \times 4000 \times 10^{-9}}{353 \times 10^{-6}} = 0.82\text{T}.$$

The calculated $B_{\max}$ is higher than B_{sat}. To prevent saturation of the magnetic core, the air gap should be increased. This means that the A_L value must be reduced.

Step 3c: Reduce the A_L value and repeat Steps 3a and 3b until $B_{\max} < 0.8B_{\text{sat}}$.

By repeating Steps 3a and 3b, when the A_L value is 850 nH, the number of turns is calculated to be

$$N = \sqrt{\frac{0.527 \times 10^{-3}}{850 \times 10^{-9}}} \approx 25.$$

The magnetic flux density at the maximum winding current is calculated to be

$$B_{\max} = \frac{25 \times 6 \times 850 \times 10^{-9}}{353 \times 10^{-6}} = 0.36\text{T}.$$

Step 4: Adjust the air gap to obtain the required leakage inductance.

TABLE II
CIRCUIT PARAMETERS

Leakage inductance L_l	79.2 μH
Magnetizing inductance L_M	0.47 mH
Output capacitance C_o	10 μF + 220 nF
Diodes D_1, D_2	C3D10060A
Active switches S_1, S_2	SPW47N60C3

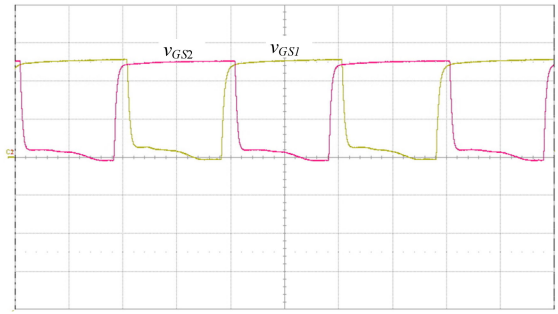

Fig. 8. Waveforms of the gated voltage. (v_{GS1},v_{GS2}: 5 V/div and time: 5 μs/div.)

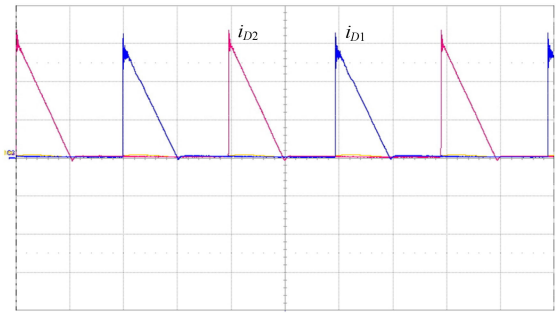

Fig. 9. Current waveforms of the freewheel diodes. (i_{D1}, i_{D2}: 2 A/div and time: 5 μs/div.)

In step 2, assume that the inductive coupling coefficient k is 0.85 based on the rule of thumb. In fact, since the cross-sectional area through which the leakage flux flows and the average length of the field lines of the leakage flux cannot be accurately determined, the coupling coefficient cannot be accurately calculated. Therefore, in this step, the leakage inductance is measured, and the air gap is slightly adjusted to obtain a value of 79.2 μH.

From (43), the output capacitance for achieving voltage ripple factor less than 1% can be calculated as

$$C_o = \frac{L_l V_o I_{\text{LED}}^2}{r_v\,(V_{\text{in}} + V_o)\,V_{\text{in}}^2} = \frac{79 \times 10^{-6} \times 124.4 \times 1.6^2}{0.01 \times (48 + 124.4) \times 48^2} = 6.3\,\mu\text{F}.$$

A prototype LED driver was built and tested using the circuit parameters listed in Table II. Fig. 8 shows the waveforms of the gate voltages, v_{GS1} and v_{GS2}. As shown, there is a short period of time (called overlap time) during which both v_{GS1} and v_{GS2} are at high level. Fig. 9 shows the current waveforms of the freewheel diodes. As expected, both currents decrease to zero. The voltage and current waveforms of the active switches are shown in Fig. 10. These waveforms conform to the conceptual waveforms shown in Fig. 5. It can be seen that there are negative currents flowing in the intrinsic diodes of the active switches.

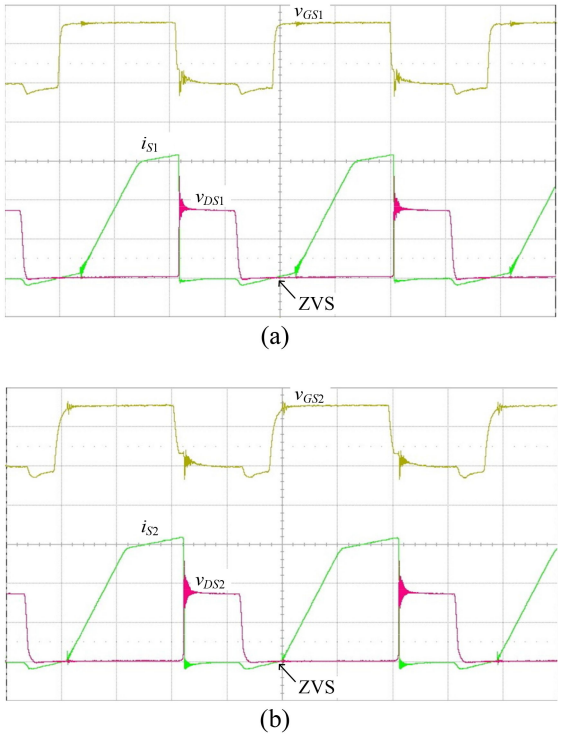

Fig. 10. Voltage and current waveforms of the active switches. (a) v_{GS1}, v_{DS1}, and i_{S1}. (b) v_{GS2}, v_{DS2}, and i_{S2}. (v_{GS1}, v_{GS2}: 10 V/div, v_{DS1}, v_{DS2}: 100 V/div, i_{S1}, i_{S2}: 2 A/div, and time: 5 μs/div.)

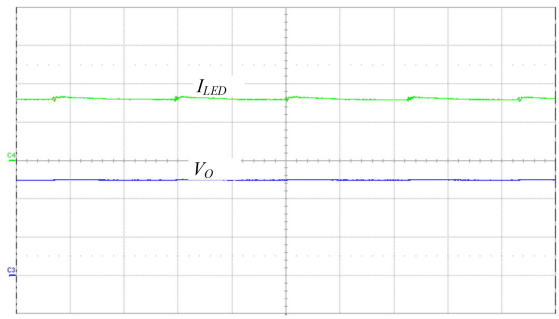

Fig. 11. Waveforms of output voltage and LED current. (V_O: 100 V/div, $I_{\rm LED}$: 1 A/div, and time: 5 μs/div.)

During the negative current period, the voltage across the active switch is clamped to near 0 V. In addition, the gate voltages are applied to the MOSFETs before the currents cross zero. In this way, both active switches can operate at ZVS. Due to the ZVS operation of the active switches and ZCS operation of the freewheel diodes, the switching losses are effectively reduced. The waveforms of the output voltage and LED current are shown in Fig. 11. The measured results are well consistent with the theoretical values. The measured output power and total losses are 202.5 and 10.6 W, respectively. The circuit efficiency is calculated to be 95.0%.

The power losses in the components were measured and shown in Table III. The losses in the couple inductor, including the eddy current loss and hysteresis loss in the magnetic core and copper loss in the windings, are 3.2 W. The active switches are two cool MOSFETs (SPW47N60C3). The ON-resistance is very low, typically 60 mΩ, resulting in low conduction loss. Due to ZVS operation, the turn-ON switching loss is almost zero. The measured losses of S_1 and S_2 are 2.5 and 2.3 W, respectively. The freewheeling diodes D_1 and D_2 can be turned OFF at zero current, which neither generates reverse recovery current nor causes turn-OFF switching losses. The measured loss of each diode is 0.75 W. The measured loss of the output capacitors composed of a 10-μF electrolytic capacitor and a 220-nF ceramic capacitor is 1.1 W. Fig. 12 shows the prototype LED driver.

TABLE III
MEASURED LOSSES IN THE COMPONENTS

Coupler Inductor	3.2 W
Active Switches S_1, S_2	2.5 W, 2.3 W
Diodes D_1, D_2	0.75 W, 0.75W
Output Capacitor C_o	1.1 W

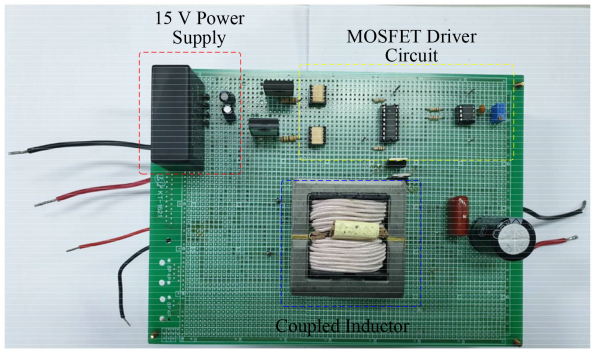

Fig. 12. Prototype LED driver.

The proposed interleaved converter and a traditional boos converter are compared to demonstrate the advantage of the proposed circuit. Both converters have the same specifications, as shown in Table I, and use the same types of MOSFETs (SPW47N60C3), diodes (C3D10060A), and output capacitors. The traditional boost converter using only one active switch has simple circuit configuration and easy control. In contrary, the proposed circuit must add an active switch and a diode. Therefore, the traditional boost converter has the advantages of fewer components, less cost, and smaller size. In addition, the control circuit used to drive two active switches will be slightly more complicated than the control circuit of the boost converter.

Due to interleaved operation, the output voltage ripple of the proposed circuit would be less than that of the boost converter. The other advantage is higher circuit efficiency. For a traditional boost converter, the MOSFET and the diode are both hard switched. High spike current happens when the MOSFET is turned ON and reverse-recovery current happens when the diode is turned OFF, resulting in high switching losses. Due to the ZVS and ZCS operations, the turn-ON switching loss of the MOSFETs and the turn-OFF switching loss of the diodes in the proposed circuit are approximately zero. For both converters, there are turn-OFF switching losses due to the overlapping voltage and current waveforms when the MOSFETs are turned OFF. The conduction losses of the MOSFETs and diodes are analyzed as follows.

For the traditional boost converter, assuming that the self-inductance is high enough, the inductor current ripple can be ignored. The inductor current is

$$I_L \approx I_{\rm LED} \times \frac{V_o}{V_{\rm in}} = 1.6 \times \frac{124.4}{48} = 4.15{\rm A}.$$

The MOSFET current would be a rectangular waveform with a pulsewidth of DT_s. Duty ratio D is $(V_o–V_{\rm in})/V_o = (124.4 – 48)/124.4 = 0.62$. Therefore, the rms current through the MOSFET is

$$I_{S\_{\rm rms}} \approx I_L \times \sqrt{D} = 4.15 \times \sqrt{0.62} = 3.27{\rm A}.$$

The ON-resistance ($R_{ds\_{\rm on}}$) of the selected MOSFET is 60 mΩ, and the conduction loss is

$$P_{S\_{\rm con}} = R_{ds\_{\rm on}} \times I^2_{S\_{\rm rms}} = 0.06 \times 3.27^2 = 0.64{\rm W}.$$

The diode current would also be a rectangular waveform with a pulsewidth of $(1 – D)T_s$. Check the *I–V* characteristics of diode C3D10060A; when $i_D = 4.15$ A, the forward voltage drop is about 1.2 V (assuming $T_j = 75$ °C). Therefore, the conduction loss through the diode is

$$P_{D\_{\rm con}} = V_F \times I_D \times (1 - D) = 1.2 \times 4.15 \times 0.38 = 1.89{\rm W}.$$

For the proposed circuit, the switch current is nearly a trapezoidal shape, as shown in Fig. 5. The height equals I_{LM}, and the time lengths of the slope and plateau parts are T_f and T_r, respectively. The rms current is

$$I^2_{S\_{\rm rms}} \approx \frac{1}{T_s}\left[\int_0^{T_f}\left(\frac{I_{LM}}{T_f}t\right)^2 dt + \int_0^{T_r} I^2_{LM} dt\right] = \frac{I^2_{LM}T_f}{3T_s} + I^2_{LM}\frac{T_r}{T_s}.$$

I_{LM} is calculated to be 5.75 A. From (32) and (33), $T_f = 0.28T_s$ and $T_r = 0.22\ T_s$. Therefore, $I_{S\_{\rm rms}} = 3.21$ A, and the conduction loss of two MOSFETs is

$$P_{S\_{\rm con}} = 2 \times R_{ds\_{\rm on}} \times I^2_{S\_{\rm rms}} = 2 \times 0.06 \times 3.21^2 = 1.24\ {\rm W}.$$

The currents through diodes D_1 and D_2 are of triangular waveforms, as illustrated by the decreasing parts of i_{L1} and i_{L2} in Fig. 5. The peak value is also I_{LM} and decreases to zero after approximately T_f. For a time-varying diode current, the voltage across the diode is $v_D = V_{F0} + i_D R_h$, where V_{F0} is the voltage at the turn-ON point, and R_h is the forward resistance. For diode C3D10060A, $V_{F0} \approx 0.6$ V and $R_h \approx 66$ mΩ. The conduction loss of two diodes is

$$P_{D\_{\rm con}} = 2\left(V_{F0}I_{D\_{\rm avg}} + R_h I^2_{D\_{\rm rms}}\right)\frac{T_f}{T_s} = 2 \times \left[0.6 \times \frac{1}{2} \times 5.75 + 0.066 \times \left(\frac{1}{3} \times 5.75\right)^2\right] \times 0.28 = 1.1\ {\rm W}.$$

In summary, the conduction losses across MOSFETs and diodes for a traditional boost converter and the proposed circuit are 2.53 and 2.33 W, respectively. The conduction loss is almost equal. The comparison on the two converters is listed in Table IV.

TABLE IV
COMPARISON OF THE TRADITIONAL BOOST CONVERTER AND THE PROPOSED CONVERTER

Items \ Circuit	Traditional boost converter	Proposed converter
Cost	Less	More (one more active switch and one diode)
Size	Smaller	Slightly larger
Efficiency	Lower	Higher
Output voltage ripple	Higher	smaller

V. CONCLUSION

A novel dc–dc LED driver is presented. The circuit configuration mainly consists of two parallel-connected buck–boost converters that are alternatively turned ON and OFF with a short overlap time. During the overlap time, both active switches of the buck–boost converters are turned ON. A coupled inductor is used to play the role of the inductors of the buck–boost converters. The circuit operation was described, and the design equations were derived. A prototype designed for driving 200-W high-brightness LEDs was built and measured. The experimental results show that both active switches operate at ZVS and both freewheel diodes operate at ZCS, resulting in low current and voltage spikes and low switching losses. Based on the experimental results, the feasibility of the proposed interleaved converter has been verified with satisfactory performance.

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Yao-Ching Hsieh (Member, IEEE) was born in Kaohsiung, Taiwan, in 1969. He received the B.E. and M.S. degrees from National Taiwan University, Taipei, Taiwan, in 1991 and 1993, respectively, and the Ph.D. degree from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2004, all in electrical engineering.

From 2006 to 2014, he was with the Department of Electrical Engineering, National Dong Hwa University, Hualien, Taiwan. From 2014 to 2017, he was with the Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, Taipei. He is currently with the Department of Electrical Engineering, National Sun Yat-sen University. His research interests include battery-related technology, soft-switching techniques, and power converters.

Hung-Liang Cheng (Member, IEEE) was born in Chunghwa, Taiwan, in 1964. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the National Sun Yat-Sen University, Kaohsiung, Taiwan, in 1986, 1988, and 2001, respectively.

From 1988 to 2007, he was an Electronic Researcher with the Chung-Shan Institute of Science and Technology, Taoyuan, Taiwan, where he designed and developed high-power transmitters in radar and missile systems. Since February 2007, he has been with I-Shou University, Kaohsiung, where he is currently a Professor with the Department of Electrical Engineering. His current research interests include power electronic converters and electronic ballasts/drivers for lighting applications.

Dr. Cheng is a Member of the IEEE Power Electronics Society and the IEEE Industrial Electronics Society.

En-Chih Chang was born in Kaohsiung, Taiwan, in 1975. He received the B.S. degree from Feng Chia University, Taichung, Taiwan, in 1999, the M.S. degree from the National Taiwan Ocean University, Keelung, Taiwan, in 2001, and the Ph.D. degree from the National Cheng Kung University, Tainan, Taiwan, in 2008, all in electrical engineering.

He is currently a Professor with the Department of Electrical Engineering, I-Shou University, Kaohsiung, Taiwan. His current research interests include sliding-mode control, intelligent control, grey theory, and their applications in power electronics systems.

Wei-Di Huang was born in Kaohsiung, Taiwan, in 1992. He received the B.S. and M.S. degrees in electrical engineering from I-Shou University, Kaohsiung, Taiwan, in 2015 and 2018, respectively.

He is currently a Hardware Engineer with the Department of Research and Development, Zippy Technology Corporation, New Taipei City, Taiwan. His current research interests include electronic circuits for Common Redundant Power Supply (CRPS) redundant modules.