A Multichannel High-Frequency Current Link Based Isolated Auxiliary Power Supply for Medium-Voltage Applications

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***Abstract*—The auxiliary power supply (APS) is one of the critical components inside medium-voltage (MV) power converters. Besides high insulation capability and small footprint, low common-mode (CM) coupling capacitance and multichannel output are the desired features of APS in the emerging silicon-carbide-based MV converters due to their fast switching speed. This article presents the design and optimization procedure of a high-density isolated APS using an LCCL-LC resonant topology with an operating frequency of 1 MHz. The proposed design procedure attains consistent soft-switching operation under a random number of output channels. The galvanic isolation is realized by a current-fed single-turn 1 MHz transformer that can achieve a breakdown voltage of over 20 kV while maintaining a small size. Design optimization on the insulation system of the current transformer is proposed to obtain both high partial-discharge inception voltage (PDIV) and low coupling capacitance. Finally, two versions of APSs are developed, using air and silicone as dielectric materials, which can reach PDIV of over 5 and 16 kV, respectively. The corresponding coupling capacitances are 1.86 pF and 3.6 pF. Both designs can provide a maximum power of 20 W on the receiving side, and 120 W on the sending side.**

***Index Terms*—Common-mode (CM) coupling capacitance, current transformer, insulation, LCCL-LC topology, soft-switching.**

I. Introduction

THE HIGH breakdown voltages, fast switching speeds ($>$ 50 V/ns), and low switching losses provided by medium-voltage (MV) silicon-carbide (SiC) devices, e.g., 3.3 kV and 10 kV SiC MOSFETs, enable high-frequency power conversion solutions in many emerging MV applications, such as high-speed propulsion drives, solid-state transformers, and MVDC systems [1]–[10].

In such SiC-based MV power conversion systems, to ensure the device's safe operation, a high-performance auxiliary power supply (APS) system is very crucial. The APS serves as the main insulation barrier between the high-frequency-switching devices and controller ground reference, which is usually the earth ground. Due to the high-frequency switching, the elimination of partial discharge (PD) becomes another critical design factor, since it directly affects the degradation of the APS's insulation system [11]. As such, the PD inception voltage (PDIV) level should be higher than the maximum insulation stress during operation. Moreover, with the increasing switching speed and frequency, small common-mode (CM) coupling capacitance C_{CM} across the APS insulation barrier is required to minimize the CM current and reduce the electromagnetic interference (EMI) problems [12]. Finally, as shown in Fig. 1, inside the MV converter system, there are multiple auxiliary loads, including sensors, gate drivers, and local controllers. Thus, the APS should be capable of delivering reliable power to a random number of loads at different locations.

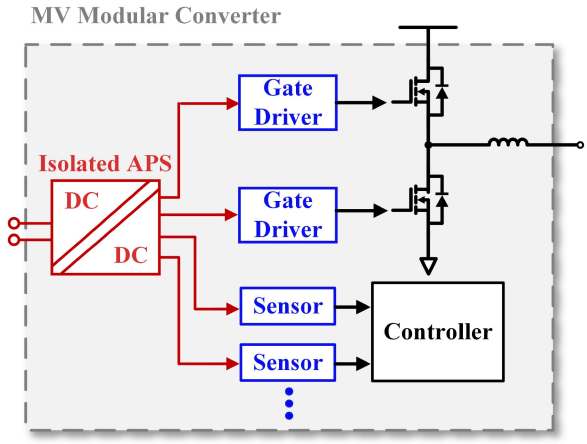

Fig. 1. Desired isolated APS architecture in a MV modular converter.

The galvanic isolation level is always the primary design consideration in the APS. In terms of the insulation schemes, APS can be categorized as either nontransformer-based or transformer-based designs. Wireless power transfer (WPT) is the most popular solution in core-less type designs due to its easy fabrication and scalable insulation level. As presented in [13]–[17], this approach can easily realize a breakdown voltage of over 20 kV with C_{CM} varying from 1.7 to 10 pF by adjusting the distance between transmitters and receivers. However, since air is used as the dielectric material in WPTs, large distance and bigger coils are needed to satisfy both insulation and power

Manuscript received March 7, 2021; revised May 24, 2021 and July 6, 2021; accepted July 17, 2021. Date of publication August 4, 2021; date of current version September 16, 2021. This work was conducted under the ARPA-E Award DE AR0001111 in the BREAKER program. Recommended for publication by Associate Editor Y. Xing. *(Corresponding author: Dong Dong.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3102055.

Digital Object Identifier 10.1109/TPEL.2021.3102055

TABLE I
DESIGN SPECIFICATIONS OF THE APS

Property	Symbol	Value
Output Voltage	V_o	24 V
Max. Output Power per Receiving Side	P_{or}	20 W
Max. Total Output Power	P_{os}	120 W
Breakdown Voltage	V_{bd}	> 20 kV
PDIV	V_{pd}	5 kV-15 kV
Coupling Capacitance	C_{CM}	< 5 pF

requirements, leading to lower power density. Spro et al. [18] and Sarrazin et al. [19] developed more compact WPT-based APSs with PCB windings. Although ultra-high breakdown voltage is realized, due to the isolated component structure, these designs cannot satisfy multiload driving requirements. As an alternative solution to the coreless design, the power over fiber, introduced in [20], has ultra-high isolation capability with negligible C_{CM} and multiload driving ability, but the efficiency is below 30% with a maximum output power of a few watts. Additionally, the laser transmitter's volume is very bulky, which is difficult to integrate into the MV converter [21].

The transformer-based APS is more popular for high-power density converter systems. For the target isolation level of few kilovolts, PCB can be utilized as the insulation media in the transformer design. A two-channel APS using a PCB-embedded transformer is developed in [22]–[24]. With the operating frequency of multimegahertz, the total volume of the APS is smaller than 3 cm^3. However, due to the high permittivity of FR4 and small core size, the maximum C_{CM} value reaches 10 pF. Alternatively, air can be used as a dielectric material. presented air-insulated transformer-based APS designs with Kapton tape wrapped around the cores. Although this design can reach an isolation voltage of more than 20 kV with a C_{CM} value lower than 2 pF, to meet the insulation requirement, a large core size is necessary. Another air-insulated design is presented in [27]–[29], and [36] by using high insulation wire passing through the center of the core. This design is able to supply multiple loads and achieve high insulation capability with ultra-low C_{CM} value, but the specific design tradeoff between insulation voltage, $C_{CM,}$ and size has not yet been addressed. To further shrink the transformer size while keeping 20 kV insulation voltage, as presented in [21], [30], and [31], solid dielectric materials such as silicone and epoxy are applied. However, compared to the air-insulated design, the drawback for this type of APS is that the C_{CM} value is slightly increased, and the output power is limited.

It can be clearly seen that a design tradeoff exists among several features, especially for high PDIV, small C_{CM}, and small footprint. Therefore, a design optimization procedure is needed to find the optimal circuit topology and operation, component sizing, and coordinate insulation. To provide sufficient auxiliary power to the SiC-based high-frequency MV power converters with multiple devices and sensors at different locations, the specifications shown in Table I are used in this article as the APS design target.

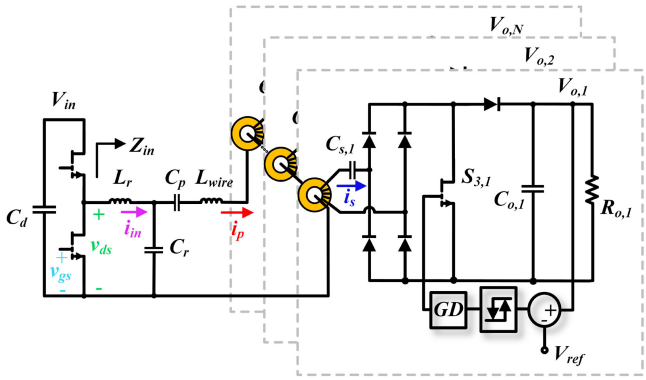

Fig. 2. LCCL-LC resonant converter with hysteresis controller and wire inductance.

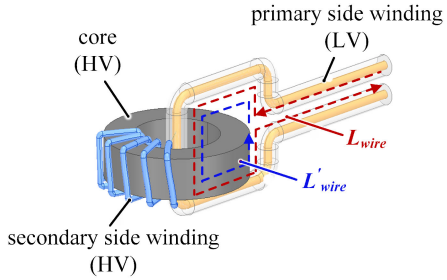

Fig. 3. Three-dimensional model of proposed transformer design with labeled wire inductance.

This article is organized as follows. An overview of the soft-switching resonant type current-transformer-based APS system is presented in Section II. Then, a transformer optimization process will be proposed in Section III. Section IV discusses the analysis of different insulation design approaches. Among all designs, regarding insulation capability, C_{CM}, and manufacturability, two designs using different dielectric materials are selected and developed in hardware. In Section V, the experimental results of the two designs are provided. Finally, Section VI offers the conclusion based on the main results.

II. APS CIRCUIT TOPOLOGY AND DESIGN

As shown in Fig. 2, to supply multiple loads at different locations, a current link-based APS solution with a single sending circuit and multiple receiving circuits are adopted. The LCCL-LC soft-switching resonant converter topology operating at the megahertz range is selected as it can deliver a constant high-frequency current to the receiving regulators via a very small current transformer [32]–[35]. As shown in Fig. 3, in order to realize low C_{CM}, high insulation level within a small size, and ease of installation, a single-turn transformer is designed. However, with the traditional design of LCCL-LC topology, zero-voltage switching (ZVS) cannot be guaranteed all the time for the sending-side devices because the device turn-off current is highly affected by the load conditions, like the number of channels and wiring shapes. Therefore, a new design approach of the LCCL-LC resonant converter suitable for multichannel receiving loads is proposed in this section.

A. Effects of Parasitic Inductance and Load Conditions on ZVS Realization

With the predetermined switching frequency f_s and current bus i_p values based on transformer optimization which will be covered in the next section, the resonant frequency, formed by L_r and C_r, is designed to be the same as the switching frequency [27], [28], [32]. The L_r and C_r values can be calculated as

$$L_r = \frac{V_{in}}{\pi^2 f_s \left|i_p\right|} \tag{1}$$

$$C_r = \frac{1}{(2\pi f_s)^2 L_r}. \tag{2}$$

In the traditional design method, C_s is used to compensate for the secondary side leakage inductance and C_p is used to tune the total input impedance Z_{in}, so that the turn-OFF current i_{in} is able to fully discharge the device's output capacitors C_{oss} according to (3) during the deadtime t_d to achieve ZVS

$$\left|i_{in}\right| = \frac{2V_{in}}{\pi \left|Z_{in}\right|} \geq \frac{2C_{oss}V_{in}}{t_d}. \tag{3}$$

However, as the number of loads varies, the additional stray inductance L_{wire}, labeled in Fig. 3, introduced by the primary-side wiring configuration and length can affect the circuit operation especially when the converter operates at high frequency and drives multiple loads simultaneously. Even though C_p is designed with a certain margin, the total input impedance will be affected on both magnitude and phase by L_{wire}. Ref Yan *et al.* [27] provide a more detailed discussion and offers one example comparing the effect of L_{wire} from 1 nH to 1 μH on ZVS realization. When L_{wire} increases to 0.4 μH, the system loses ZVS.

In addition, the load conditions also impact the soft-switching realization. As analyzed in [27], when the short-circuit condition happened on load, Z_{in}, dominated by the L_r and C_r at this condition, will drop to approximately zero. Therefore, the device's current will become extremely large, which can damage the converter.

B. Proposed Design Method

To overcome the load-dependent turn-OFF current caused by uncertain wire stray inductance and short-circuit conditions, a new LCCL-LC design methodology is proposed.

First, the primary side wire needs to adopt the co-axial or twisted configuration to reduce the wiring inductance due to variation of the length [27]. Then, as shown in Fig. 3, the L'_{wire} is generated from the wiring loop created around each current transformer core and can be estimated based on the loop area. In this condition, the variation of total parasitic inductance L_{wire} depends on the change of the number of loads N and L'_{wire}. As such, instead of using C_p, C_s can be used for impedance compensation, so each receiving side can be individually compensated. The selection of C_s will compensate the secondary side leakage inductance L_{sk}, magnetizing inductance L_m, $L'_{wire,}$ and primary side leakage inductance L_{pk} as

$$\left|Z_{pk}\left(f_s\right) + Z_{L'_{wire}(f_s)} + Z_m\left(f_s\right) \parallel \frac{\left(Z_{sk}\left(f_s\right) + Z_{C_s}\left(f_s\right)\right)}{n^2}\right| = 0. \tag{4}$$

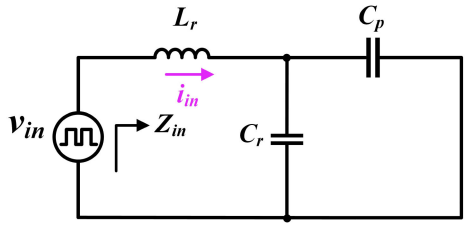

Fig. 4. Equivalent circuit of the proposed design method after C_s compensation.

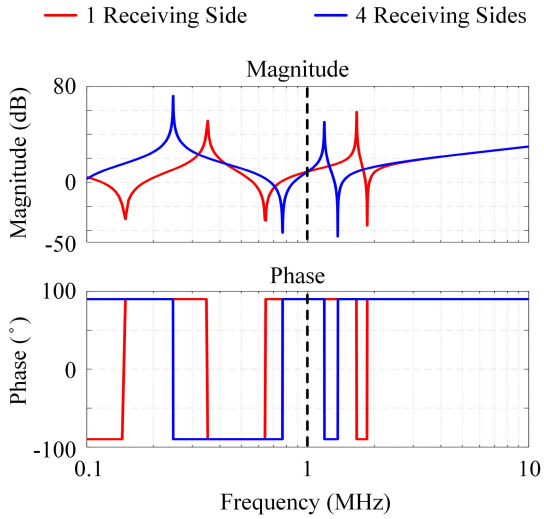

Fig. 5. Total input impedance of designed APS under the short-load condition using the proposed compensation method.

In the high-frequency range, the total impedance is primarily dominated by the passive components. The resistive load on the receiving circuit only offers a damping effect at each resonant point and will not essentially change the circuit performance. Hence, the short-circuit condition of $R_o = 0$ is used as the analysis scenario in the proposed circuit design. As shown in Fig. 4, the equivalent circuit after C_s compensation only contains three components regardless of the number of loads. This leads to a load-independent input impedance Z_{in} that can be calculated as

$$Z_{in}\left(f_s\right) = Z_{L_r}\left(f_s\right) + Z_{C_r}\left(f_s\right) \parallel Z_{C_p}\left(f_s\right). \tag{5}$$

According to (1) and (2), L_r and C_r values are designed based on the current source amplitude and switching frequency. As a result, Z_{in} only depends on C_p at f_s and is able to be determined based on the desired turn-OFF current. Then, referring to (5), C_p value can be derived.

As shown in Fig. 5, with a fixed C_p value, the total input impedance is constant at f_s with a varied number of loads. To further verify the effect of the resistive load on the operation of the resonant tank, time-domain simulations with driving loads

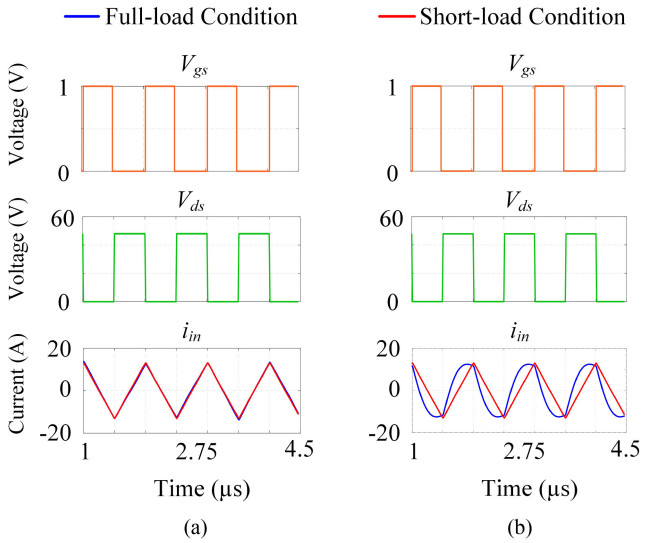

Fig. 6. Time-domain waveforms of the designed APS using the proposed compensation method with (a) one receiving side and (b) four receiving sides.

of 0 and 80 W are performed. As the results shown in Fig. 6, i_{in} is constant at turn-OFF instant. Therefore, load-independent turn-OFF current is achieved. A more specific analysis of the proposed design method can be founded in [27].

C. Voltage Regulation Design

To maintain a constant output voltage over a wide load range, a current-fed switching network with a voltage regulation is designed on each receiving side. As shown in Fig. 2, the hysteresis controller is selected due to its simple structure and excellent dynamic response. In normal operation, the control switch S_3 turns ON and OFF when the output voltage reaches the upper and lower voltage boundaries respectively. With a large C_o value, the operating frequency of S_3 is very low compared to the main switching frequency f_s. When an open circuit happens, S_3 turns ON all the time to bypass the faulty load while not interfering with other load operations.

II. Transformer Design Optimization

Referring to [27], [28], and [36], a toroid core without an air gap is selected for the best magnetic coupling to shrink the transformer size. The primary side winding is designed with a single turn using a 20 kV-insulated wire through the center of the core while the secondary side windings are designed with litz wire shown in Fig. 3, which are tightly bundled together to greatly reduce C_{CM} value [26]. In this section, the transformer design process will be discussed based on the given structure to achieve both insulation and C_{CM} targets.

A. Maximum E-field Model

In the MV system, PD-free design is important because severe PDs will reduce the lifetime of the designed product [11]. However, in real applications, PDIV is difficult to be accurately predicted because it is affected by both transformer geometries and testing environments, such as atmosphere and humidity.

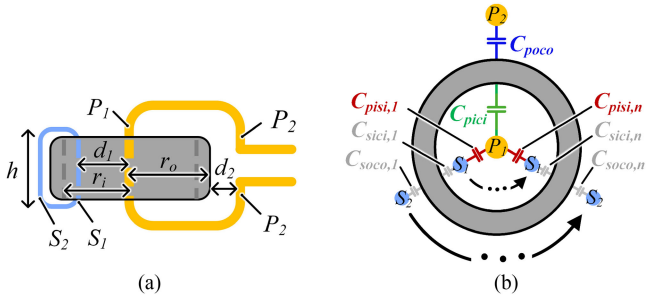

Fig. 7. (a) Side view of the proposed transformer structure without the insulating layer of primary side winding. (b) Top view of the proposed transformer structure without the insulating-layer of primary side winding.

Instead, the maximum E-field inside the transformer can be modeled and used as a design metric to realize PD-free. In the design, the maximum E-field is controlled less than 2 kV/mm in standard air to allow the effective ionization coefficient less than zero. The assumption here is that electrons detached from negative ions in the ambient air are the dominant initial electron source for discharges [40].

As shown in Fig. 3, the primary side winding is connected to the ground potential, and both secondary side windings and core are on high voltage potential levels. To simplify the calculation, the E-field distortion around the bending corner of the secondary side windings is not considered in the model. As a result, the concentric cylinder model can be implemented to estimate the E-field distribution inside the transformer. Then, the maximum E-field can be estimated as

$$E_{max} = \frac{V_{pd}}{r_{pi} \ln\left(\frac{d_1}{r_{pi}}\right)} \tag{6}$$

where V_{pd} is the desired PDIV level. r_{pi} is the radius of the primary side wire and d_1 is the distance from the center of the core to the secondary side winding. If $r_s << d_1$, then d_1 can be substituted by r_i, which is the inner radius of the core as shown in Fig. 7(a). For the air-insulated design, E_{max} boundary is selected to be 2 kV/mm to allow sufficient margin.

B. Proposed C_{CM} Model

Due to the fast-transient speed of SiC MOSFETs, a CM current is usually induced via C_{CM}, which can cause EMI problems [37]. Therefore, C_{CM} value becomes critical and needs to be precisely predicted during transformer development. Hu *et al.* [28] introduce a modeling method for toroid core by calculating the total electric field energy stored in each side of windings. However, complicated math calculation is required. Thus, a simple C_{CM} model based on core geometries, including three different coupling capacitors, is proposed in this session. To simplify the model calculation, the model does not include the insulating layer of the primary side wire.

As shown in Fig. 7(b), the first coupling capacitor, C_{pisi} represents the total capacitance generated between the inner primary side wire P_1 and secondary side wires S_1 directly through the air. By adding all $C_{pisi,n}$, the capacitance between P_1 and each $S_{1,n}$ together, C_{pisi} can be simply derived. Since the secondary

TABLE II
PARAMETERS OF TRANSFORMER SAMPLE

Parameters	Value
Transformer Inner Radius	7.5 mm
Transformer Outer Radius	12.5 mm
Transformer Height	7 mm

side wires are compactly winded around the core, $C_{pisi,n}$ can be modeled as a capacitance between two parallel wires

$$C_{pisi,n} = \frac{2\pi\varepsilon_o\varepsilon_r h}{\ln\left(\frac{(d_1-r_p)(d_1-r_s)}{r_p r_s}\right)} \tag{7}$$

where ε_r is the relative permittivity of the air, h is the length of S_1, and r_p and r_s are the radius of primary and secondary side wire conductors, respectively.

Besides coupling directly through the air between P_1 and S_1 the indirect coupling path from P_1 to core and then from the core to S_1 generates another two capacitors C_{pici} and $C_{sici,n}$ respectively, shown in Fig. 7(b). Assuming the ferrite core is a good conductor, C_{pici} can be calculated as

$$C_{pici} = \frac{2\pi\varepsilon_o\varepsilon_r h}{\ln\left(\frac{r_i}{r_p}\right)} \tag{8}$$

where r_i is the core inner radius.

Due to the negligible distance between the core and S_1, $C_{sici,n}$ becomes infinitely large. Moreover, C_{pici} and $C_{sici,n}$ are in series connection, so $C_{sici,n}$ can be ignored in this model. With the same analysis, C_{sopo}, the coupling capacitance between the core and S_2 can be ignored as well.

The coupling between P_2 and S_1 creates C_{poco} and C_{sici} . Due to the insulation requirement, P_2 is a certain distance away from the core, so C_{poco}, the capacitance between P_2 and the core, cannot be ignored in this model. Thus, the total capacitance on this coupling path is dominated by C_{poco}. Assuming the core is a good conductor, C_{poco} can be considered as the capacitance between two parallel cylinders

$$C_{poco} = \frac{2\pi\varepsilon_o\varepsilon_r h}{\ln\left(\frac{(r_o+d_r-r_p)\cdot d_2}{r_p r_o}\right)} \tag{9}$$

where r_o is the outer radius of the core and d_2 is the distance from the center of P_2 to the outer cylindrical surface of the core.

Finally, between P_2 and S_2, there are two coupling paths. One is directly coupled through the air and another one is indirectly coupled through the core. However, in this design, the capacitance created by the direct coupling is ignored because the distance between P_2 and S_2 through the air is large, leading to an extremely small capacitance. Although for the indirect coupling path, two capacitors $C_{sici,n,}$ and C_{poco} are generated, they are analyzed in the previous cases. Therefore, the total CM coupling capacitance, C_{CM} is

$$C_{CM} = n \cdot C_{pisi} + C_{pici} + C_{poco} \tag{10}$$

where n is the secondary side turn numbers.

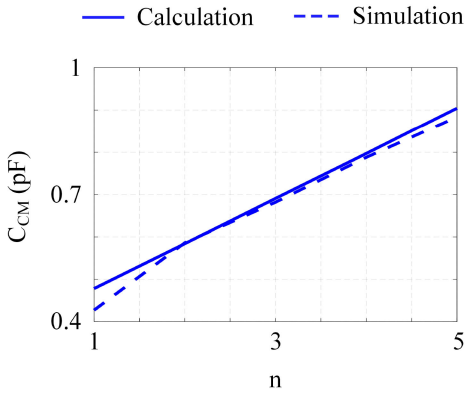

Fig. 8. Comparison between the calculated C_{CM} and Q3D simulated C_{CM} values.

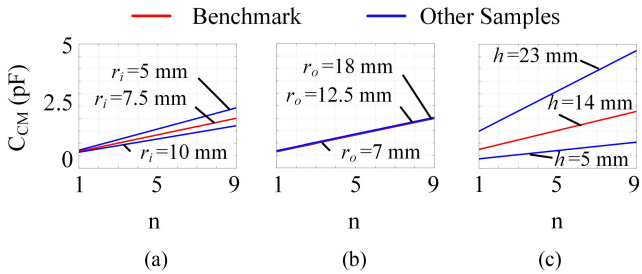

Fig. 9. Calculated C_{CM} value versus secondary side turn number with transformer (a) r_i = 5–10 mm, r_o = 15 mm, and h = 14 mm. (b) r_o = 7–18 mm, r_i = 7.5 mm, and h = 14 mm. (c) h = 5-23 mm, r_i = 7.5 mm, and r_o = 15 mm.

TABLE III
TRANSFORMER DESIGN SPECIFICATIONS

Parameters	Value
Transformer Height	14 mm
Transformer Outer Radius	$\leqslant$12.5 mm
Transformer Volume	$\leqslant$3.6 cm^3
PDIV	5 kV-15 kV
Coupling Capacitance	$\leqslant$ 1 pF
Switching Frequency (f_s)	$\geqslant$500 kHz
Secondary Side Current (i_s(rms))	1.4 A

This proposed model can be verified with Q3D simulation with sample parameters shown in Table II. As illustrated in Fig. 8, high accuracy can be realized by the model.

To implement the proposed C_{CM} model to the transformer design, the relationship between C_{CM} and transformer geometries needs to be further analyzed. Using the core designed in [28] as a benchmark, seven different transformer samples are compared. Based on the results illustrated in Fig. 9, with the same turn number, transformer height has the largest impact on C_{CM}, and transformer outer radius has the least impact on C_{CM}. Additionally, increasing the turn number, n will also increase the C_{CM} value. Therefore, to realize a small C_{CM} value, a low-profile transformer with a small turn number is preferred.

C. Transformer Design

Table III shows the transformer design specifications. To minimize the overall converter size, the switching frequency

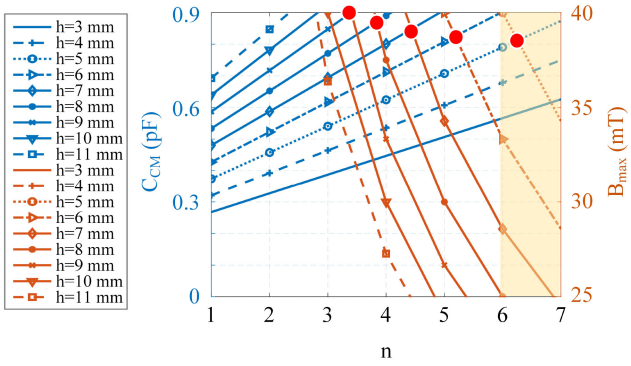

Fig. 10. Calculation results of B_{max} (plotted in orange) and C_{CM} (plotted in blue) under the switching frequency of 1 MHz.

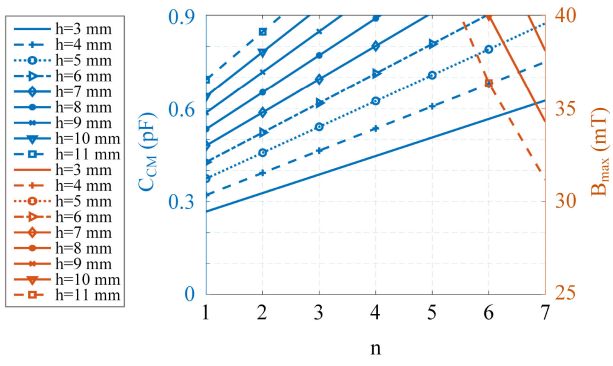

Fig. 11. Calculation results of B_{max} (plotted in orange) and C_{CM} (plotted in blue) under the switching frequency of 500 kHz.

is designed to be higher than 500 kHz. Consequently, ML91S from Hitachi is selected as the core material due to its excellent high-frequency performance [38]. Based on the current rating of primary and secondary side wires, the maximum turn ratio is limited to 1:7.

Since the transformer outer radius has a direct impact on the converter size but has less effect on PDIV and C_{CM} value, it can be determined first. In this APS design, the footprint is less concerned than the other two requirements, so the transformer outer radius is designed to be the maximum value of 12.5 mm. In this condition, the transformer inner radius and height can be optimized to achieve high PDIV and low C_{CM} while remaining low core loss. According to (6), to reach the minimum PDIV of 5 kV, the inner radius is required to be 7.3 mm. Considering the manufacturability as well as C_{CM} value, the transformer inner radius is selected to be the minimum available value of 7.5 mm. Consequently, a minimum C_{CM} value can be realized by designing a low-profile core.

To determine the transformer height, turn ratios as well as the operating frequency, the maximum flux density, B_{max} is introduced as the fourth boundary in the transformer design. Suggested by Hitachi, the B_{max} for ML91S is better to be designed within 50 mT [38]. To avoid overheating and over-design problems, the B_{max} range is determined between 25 and 40 mT, which can be calculated as

$$B_{max} = \frac{V_o D T_s}{2 n A_c} \tag{11}$$

where T_s is the switching period. D is the duty ratio which is normally 0.5 for a resonant converter and A_c is the cross-sectional area of the core.

Due to the volume and B_{max} restrictions, the transformer height is constrained between 3 and 11 mm. Furthermore, according to the simulation results, the silicone insulating layer of the primary side wire will cause an additional 10% increase in the C_{CM} value compared to the calculated value. Thus, to achieve the target C_{CM} value of 1 pF, in the following design process, 0.9 pF becomes the upper boundary of C_{CM} during the calculation. Figs. 10 and 11 illustrate the calculation results of C_{CM} and B_{max} with various core heights and turn numbers under the switching frequency of 1 MHz and 500 kHz respectively. The available core height and turn number that satisfy both C_{CM} and B_{max} requirements exist, when an intersection point caused by two lines with the same marker but different colors, appears. Then, an integer turn number is necessary to be found to further narrow down the solution list. Under the switching frequency of 1 MHz, there are few possible solutions labeled with red dots. As an example, when $h = 5$ mm, the available turn number range is covered by the yellow box, but only $n = 6$ and 7 can be regarded as potential solutions for the transformer design. However, when $h = 9$ mm, there is no available integer turn number, so it is not in the final solution list. Moreover, according to Fig. 11, there is no available solution under the switching frequency of 500 kHz. Following the same analysis process for other switching frequencies, solutions only exist under 900 kHz and 1 MHz. Considering the design of the resonant components in the circuit, 1 MHz is selected. Then, to ensure enough turning margin for the resonant components during the aforementioned circuit design and easy fabrication, the final transformer is designed with parameters shown in Table IV.

TABLE IV
DESIGNED TRANSFORMER PARAMETERS

Parameters	Value
Transformer Height	7 mm
Transformer Outer Radius	12.5 mm
Transformer Inner Radius	7.5 mm
Turn Ratio	1:5
Core Material	ML91S
Switching Frequency (f_s)	1 MHz

IV. INSULATION DESIGNS

To achieve breakdown voltage over 20 kV, the primary side wire only needs to provide a sufficiently long distance between the exposed conductor and core, since both the core and secondary side wire connect to a high voltage potential. However, it cannot prevent system degradation because PD will happen at a lower insulated voltage level [11], [39]. Thus, to maintain a long lifetime of APS, a PD-free insulation system design is desired. Although in the previous session, PDIV has been briefly discussed, this section will introduce more solutions using different E-field stress control techniques and insulation materials based on the transformer developed above, but not all solutions are able to reach the desired PDIV. The first four

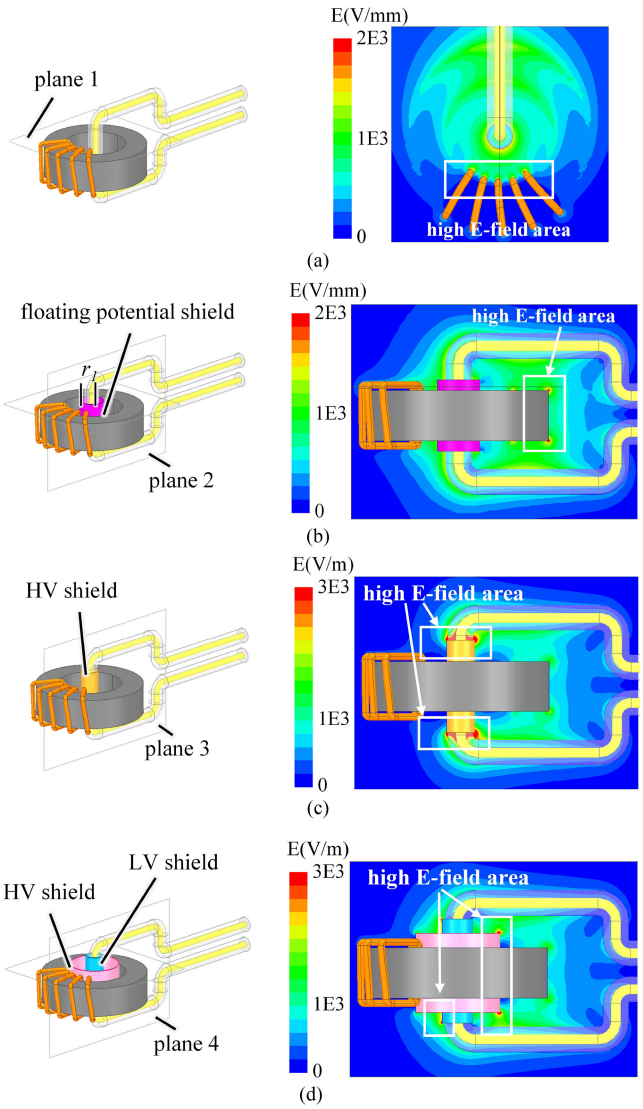

Fig. 12. Three-dimensional views of the transformer air-insulated system design and FEM E-field simulation results using (a) the basic structure, (b) conductive shield with floating potential, (c) single HV conductive shield, and (d) double conductive shields.

designs use air as insulation media with a PDIV design target of 5 kV ac. 2 kV/mm is selected as the critical value for E-field strength to evaluate each design solution. The last three designs adopt silicone as an insulation material to further increase the design target to 15 kV. In this case, 8 kV/mm is the E-field boundary to determine if the solution meets the design target. All insulation solutions can be extended to other designs.

A. Air-Insulated Solutions

Without additional shielding structure, Fig. 12(a) presents the most basic insulation design by using a developed transformer only. To analyze the E-field distribution, 3-D FEM simulation is operated with voltages assigned as shown in Fig. 3. Under 5 kV excitation, the highest E-field stress happens at the bending points of outer windings on the secondary side. This is caused by a small radius of selected litz wire and a sudden change of routing direction. However, the highest E-field within the transformer does not exceed 2 kV/mm. Thus, this design can reach PDIV of 5 kV, which proves the design analysis discussed previously. Besides qualified PDIV level, this method can achieve low C_{CM} value as discussed above. Furthermore, considering the assembly process, easy manufacturing and installation are other important benefits for such a structure.

To further improve the PDIV level, a conductive shield with floating potential is added around the primary side wire as shown in Fig. 12(b). In this case, the shield can sense a different voltage depending on the distance r_1 from the insulating layer to the shield, so the E-field inside the transformer can be reshaped more uniformly. Fig. 12(b) shows the example that achieves the lowest E-field using such a method. Under 5 kV excitation and $r_1 = 3$ mm, the maximum E-filed occurs at core edges. Thus, in a real application, the core needs to be rounded off. However, the E-field distribution is highly sensitive to the shield position. Any position mismatch will lead to design failure. Thus, this method is difficult to be implemented in real life.

Applying the shield directly to the surface of the primary side wire with a fixed high voltage potential can avoid sensitive position problems and additionally utilize the insulation capability of the insulating layer. Although the voltage strength of the insulating layer is much higher than air, due to the abrupt break of shield terminals, a server E-field problem is induced at shield terminals as shown in Fig. 12(c), which exceeds the breakdown field of air. Extra stress grading layers introduced in [11] can be designed in this condition but it will reduce wire flexibility and increase installation difficulty.

A shielding structure with a uniformly distributed E-field is necessary. To achieve so, as shown in Fig. 12(d), placing a shield with high voltage potential closed to the secondary side windings and a low voltage shield to the surface of the primary side wire. However, same as the previous method, the maximum E-field at both shields' terminals exceeds the air breakdown field value from the side view. Therefore, this design is also not applicable.

B. Silicone-Insulated Solutions

To further increase PDIV to reach the 15 kV target without enlarging core size, solid potting materials can be applied as the new insulation media. Considering the voltage strength, relative permittivity, thermal conductivity, and viscosity, SilGel612 from Wacker is selected and used in the following designs.

As shown in Fig. 13(a), core and litz wire are completely potted in silicone and a majority of the primary side wire is exposed in the air. As such, ultralow C_{CM} of 1.43 pF at 10 kHz can be achieved according to the Q3D simulation result. However, this structure cannot meet the PDIV design target. Under 15 kV excitation, the E-field at the triple point, i.e., junction of air, silicone, and primary side wire exceeds the air breakdown field value due to abrupt dielectric material change.

To reduce the E-field at the triple point without complex termination design. A stress-cone structure using silicone material can be applied as shown in Fig. 13(b). In this case, the high E-field area is constrained within the potted structure, and the E-field stress in the air especially at the triple point is greatly

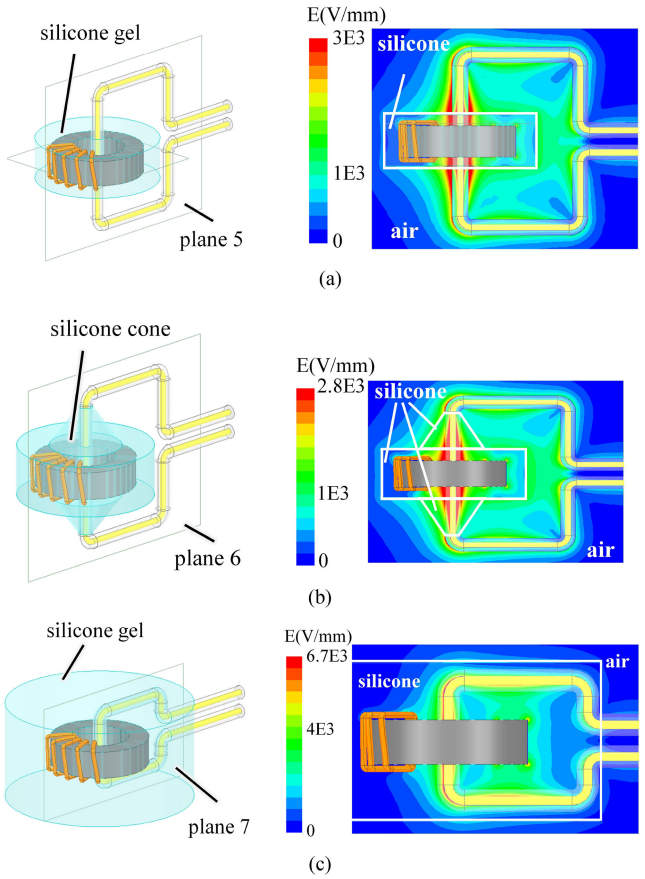

Fig. 13. 3-D views of the transformer silicone-insulated system design and FEM E-field simulation results using (a) semi-potting method, (b) stress cone terminals structure, and (c) fully potted transformer method.

reduced. Although based on the simulation result, the maximum E-field in the air is 2.79 kV/mm which is higher than the desired critical value, by further increasing the height of the stress cone, a smooth E-field transient with a maximum value below 2 kV/mm can be realized. However, the drawback of this design is that the isolated transformer will occupy more space when integrated with other circuits, and C_{CM} value will increase.

Fig. 13(c) introduces a fully potted transformer structure to solve both triple point and integration issues. Inside the potted structure, the primary side wire forms a local loop to satisfy the insulation capability. When the primary side wire comes out from silicone gel, two terminals are tightly placed together to reduce the EMI problem as well as loop inductance. According to the simulation result, with 15 kV excitation, the maximum E-field inside silicone reaches 6.7 kV/mm, which is below the critical design boundary, so the target can be achieved. To be noticed, the maximum field strength in air is smaller than 1 kV/mm without any termination requirement because the winded primary side wire naturally forms a low voltage shield at one side of the potted structure. Thus, this design can maintain high insulation capability without any termination required. However, due to the fully potted structure, C_{CM} increases to 2.22 pF based on the Q3D simulation result.

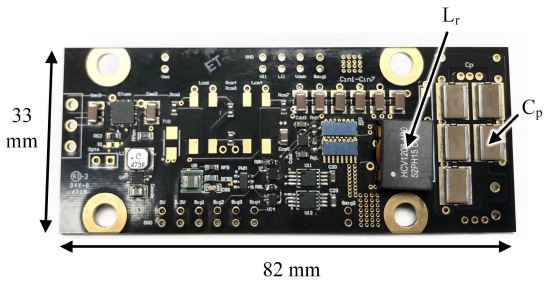

Fig. 14. Hardware prototype of sending side circuitry.

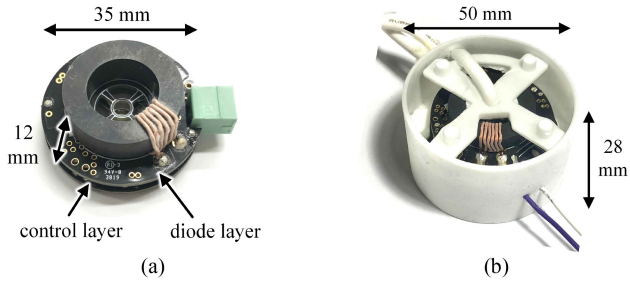

Fig. 15. Hardware prototypes of (a) air-insulated receiving side circuitry and (b) silicone-insulated receiving side circuitry.

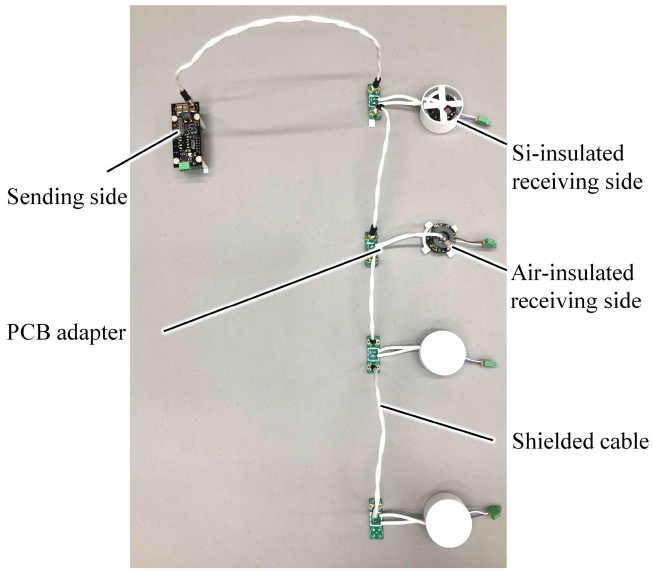

Fig. 16. Assembled current-transformer-based APS system.

V. Experimental Results

The prototype of sending side circuitry is shown in Fig. 14 and is able to drive a maximum of 120 W. To verify the proposed design and approaches, considering manufacturing ability and insulation capability, as shown in Fig. 15, an air-insulated design and silicone-insulated design are developed. GaN devices from EPC is chosen as the main power switching device and the resonant inductor is also a commercial component. Since the operating frequency is 1 MHz, both the sending side and receiving sides are able to achieve a small size. The assembled system is shown in Fig. 16. To reduce the EMI problem, a shielded cable with one conductor surrounded by return paths is used

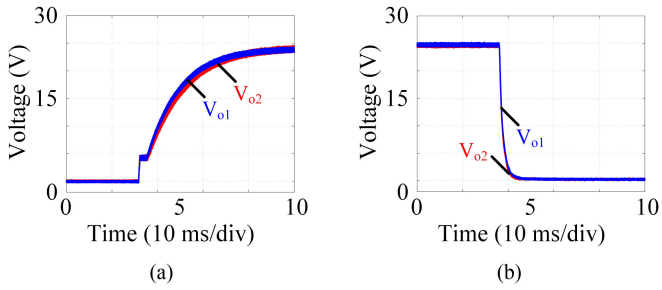

Fig. 17. (a) Startup and (b) turn-OFF processes with 80 W output power.

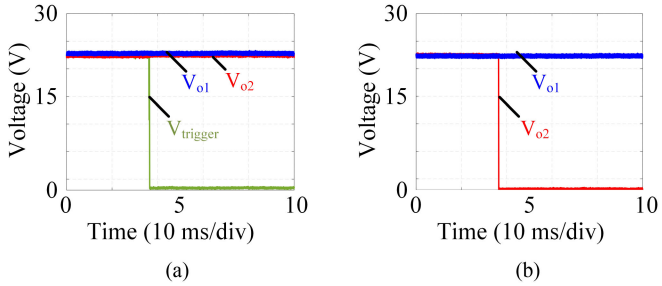

Fig. 18. (a) Open-circuit response and (b) shorts-circuit response.

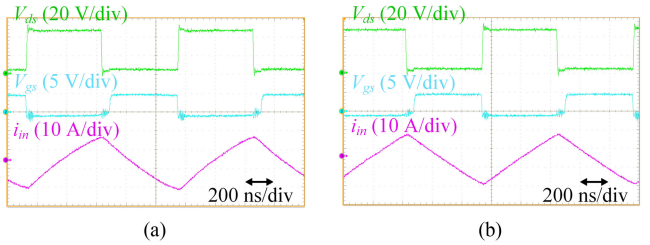

Fig. 19. ZVS verification for one load case with (a) 20 W output and (b) short-load condition.

to connect all receiving sides, including both air-insulated and silicone-insulated designs.

A. Transient Responses

Fig. 17 illustrates the APS output responses during the startup and turn-OFF period with a total output power of 80 W. All driving loads can gain power or lose power simultaneously, and no overshoot or undershoot happened. Also, the APS has a wide input range. It is able to output 24 V when the input voltage reaches 36 V under heavy load conditions. To ensure all circuit components are in the rated operation range, the maximum input voltage of the design APS is set to 60 V. During load failures, the current-fed switching network can protect the load without interrupting other load operations. As shown in Fig. 18, the output of failed load responses fast. Thus, the functionality of the feedback loop is verified.

B. ZVS Verification

Figs. 19 and 20 show the steady-state experiment results under either full load or shorted-load conditions for a different number of loads. Using the suggested winding method and proposed circuit design approach, ZVS is easily achieved with a constant

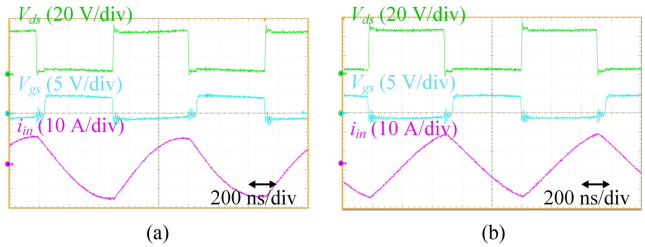

Fig. 20. ZVS verification for four loads case with (a) 80 W output and (b) short-load condition.

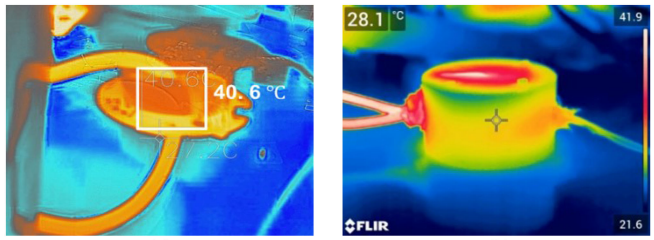

Fig. 21. Thermal test results of (a) the air-insulated design and (b) the silicone-insulated design.

current value at the turn-OFF instant. Therefore, the proposed compensation method can guarantee ZVS all the time with a load-independent turn-OFF current.

C. Thermal Verification

To verify the thermal performance for both designs, 30-min continuous tests were conducted. Each receiving side circuit operates at the full-load condition of 20 W with conventional cool conditions. As shown in Fig. 21(a), the core in air-insulated design reaches a maximum of 41 °C and the case of the silicone-insulated design reaches 28.1 °C, which indicates the core inside silicone has a maximum of 67 °C. Furthermore, the temperatures for all other circuit components are under the rating temperature. Therefore, both designs do not have thermal issues.

D. Insulation Test

In the insulation test, the completed receiving side of APS is excited by a 60 Hz ac source as shown in Fig. 22. Both high-frequency current transformer and PD detector are used to measure the PD signals, and the measurement results are close. With the threshold discharge value of 10 pC, the air-insulated design is able to achieve PDIV of 5.47 kV and the silicone-insulated design can achieve PDIV of 16.4 kV shown in Figs. 23 and 24. Fig. 25 indicates the PD pattern under 20 kV ac excitations. The average PD level is 30 pC, which demonstrates the breakdown voltage of the designed APS is above 20 kV.

E. C_{CM} Verification

Impedance analyzer Agilent 4294A is used to measure the coupling capacitance. Fig. 26 shows the measured results of the air-insulated design. With only the transformer, the measured value is close to the calculated and simulated values of 1 pF.

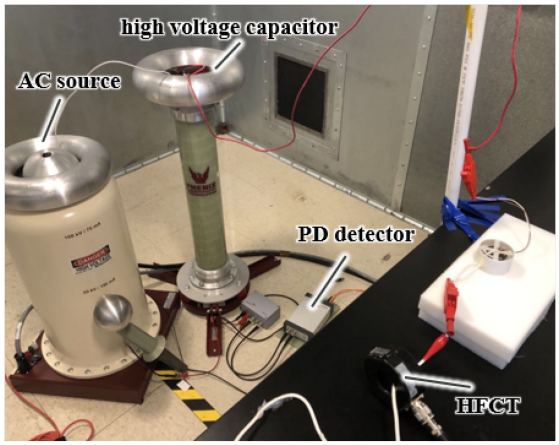

Fig. 22. Setup for insulation test.

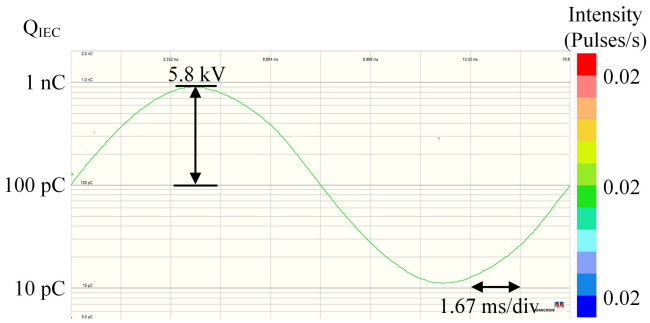

Fig. 23. PD test result for air-insulated design.

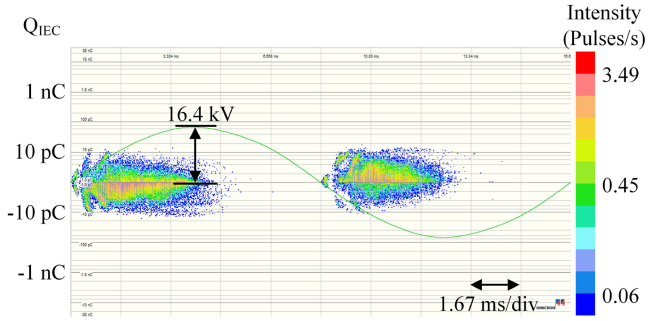

Fig. 24. PD test result for silicone-insulated design.

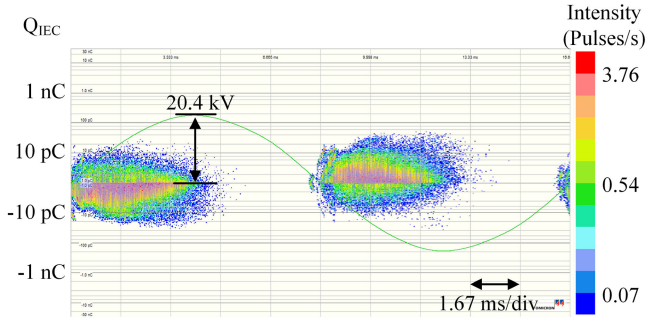

Fig. 25. Insulation test result with 20 kV excitation.

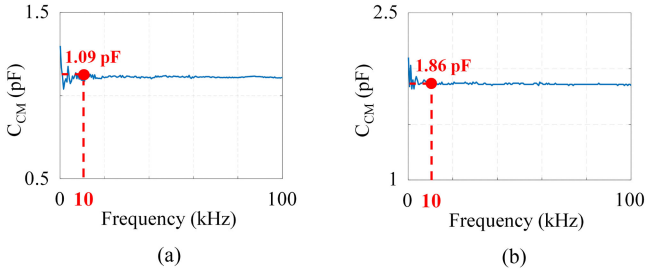

Fig. 26. Coupling capacitance measurement results of (a) air-insulated transformer only and (b) air-insulated transformer and PCBs.

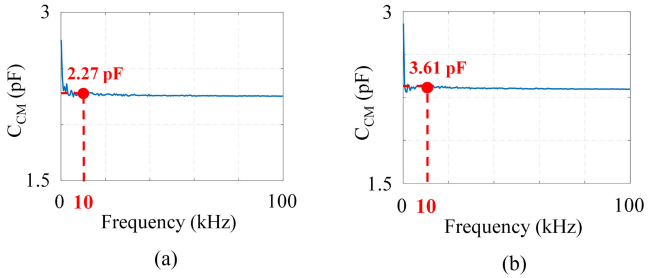

Fig. 27. Coupling capacitance measurement results of (a) silicone-insulated transformer only and (b) silicone-insulated transformer and PCBs.

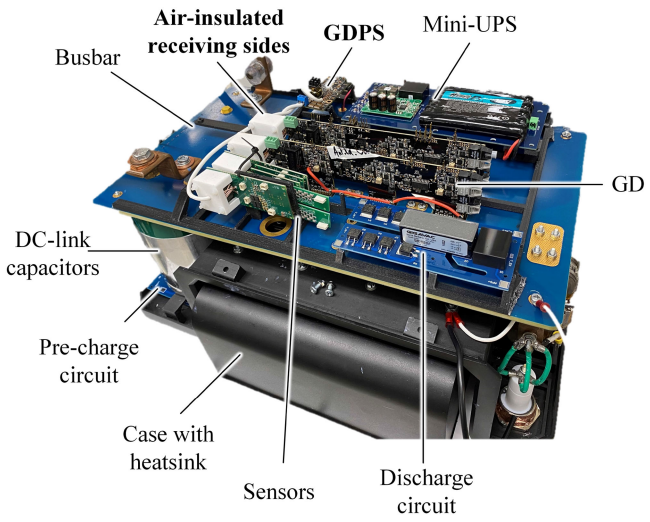

Fig. 28. Hardware prototype of a 10-kV SiC-based modular converter.

However, adding the receiving side PCBs will increase the coupling capacitance to nearly 1.9 pF, because an additional coupling capacitance is created by the overlapping area between the primary side wire and PCBs. This phenomenon is also valid for the silicone-insulated design as the result shown in Fig. 27. Overall, the air-insulated design can achieve below 2 pF and the silicone-insulated design reaches below 5 pF.

F. MV System Test

Fig. 28 indicates a 10-kV SiC MOSFET-based modular converter cell using an air-insulated design for gate drivers and sensors power supply. To verify the APS's performance in the MV system, a 6-kV continuous test in buck configuration with

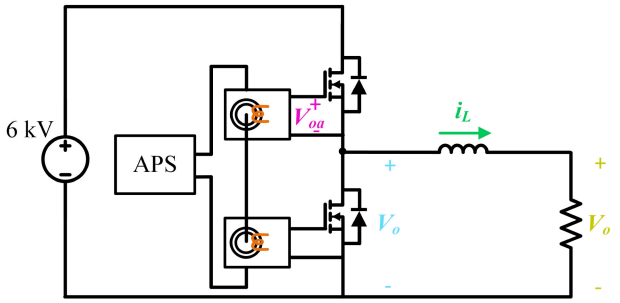

Fig. 29. Schematics of the tested buck converter.

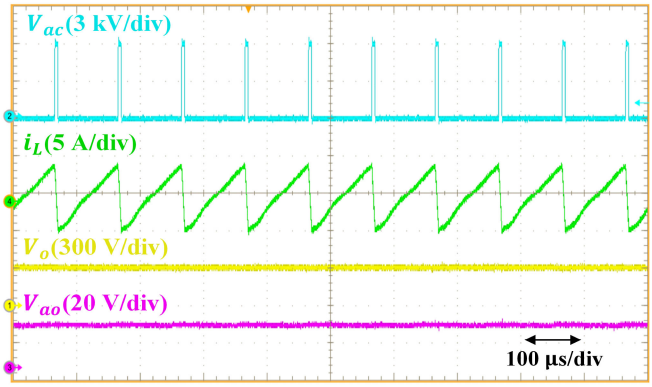

Fig. 30. Test waveforms of the designed APS in a 6-kV buck converter.

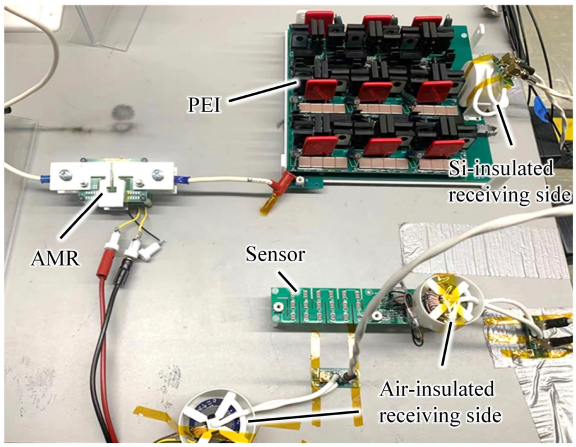

Fig. 31. Hardware setup of a 12-kV IGBT-based circuit breaker.

a switching frequency of 10 kHz is conducted as shown in Fig. 29. According to Fig. 30, the APS is able to provide a constant voltage without any spikes to gate drivers in a high dv/dt system, and no thermal issue was observed during 3 h test period. Additionally, the designed APS is validated in different MV tests in the converter, and no voltage shift or degradation in the APS output voltage is observed. More system-level test results can be found in [41].

Fig. 31 shows another MV application using the designed APS: MV solid-state power electronics interrupter (PEI) as dc circuit breaker. According to Fig. 32, the silicone-insulated APS is used to energize the gate-drivers in a PEI with a 12-kV

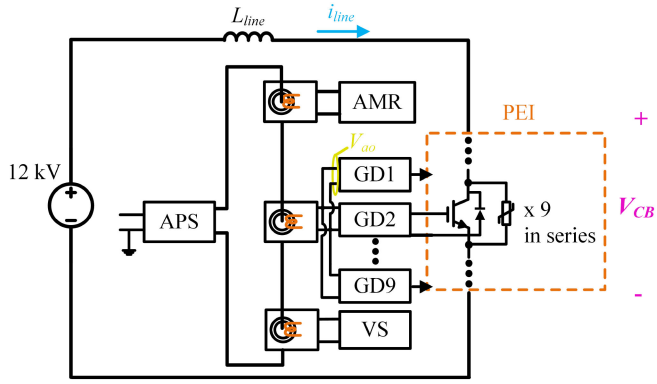

Fig. 32. Schematic of dc circuit breaker test setup.

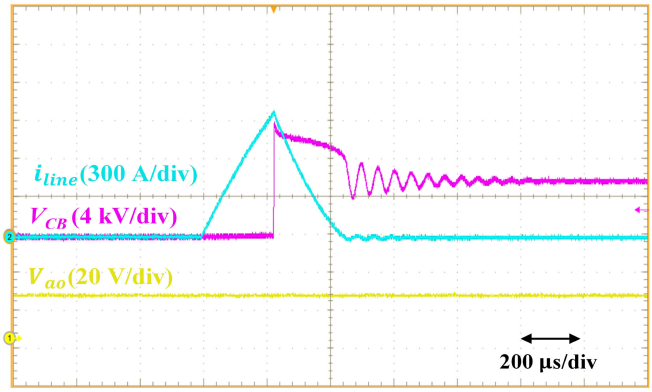

Fig. 33. Test waveforms of designed APS in a 12-kV circuit breaker circuit.

clamping voltage level, while the air-insulated APSs are powering a voltage sensor and an AMR. The PEI is constructed by stacking nine 1.7 kV IGBT devices. From the testing result shown in Fig. 33, the APS can deliver a stable voltage and power during such high voltage and current switching periods. The test is repeatable without any insulation degradation and thermal issue.

VI. Conclusion

This article presents a comprehensive high-density multi-channel APS design, including transformer optimization, LCCL-LC resonant circuit design, and insulated schemes. New C_{CM} and PDIV models for toroid core are proposed and applied to the transformer design in order to obtain the optimal core geometries. The optimized transformer size is only 25 mm wide and 7 mm tall, and it can deliver over 20 W with a comfortable thermal margin. To realize ZVS regardless of load conditions and parasitic inductance, a new circuit design procedure is presented in this article, so that constant turn-OFF current is realized and validated by experiment results. Regarding insulation designs, two receiving sides of APS with different PDIV levels were built to verify the proposed design methodologies. Both designs can achieve a breakdown voltage of over 20 kV. With the transformer inner diameter of 15 mm, the air-insulated design can reach 5.5 kV PD-free with C_{CM} of 1.86 pF, and the silicone-insulated design can achieve 16.4 kV PD-free with C_{CM} of 3.6 pF. The

APS system can be easily scaled up with a random number of loads and is tolerant of short-circuit or open-circuit faults on any of the receiving sides.

ACKNOWLEDGMENT

The authors thank the ARPA-E for their financial support.

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