Letters

A Modular Multilevel Converter Topology With Novel Middle Submodules to Reduce Capacitor Voltage Fluctuations

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***Abstract*—This letter proposes a modified topology of modular multilevel converter for medium-voltage applications, which can reduce the ac-voltage fluctuation in the submodule (SM) capacitor at low-frequency operation. A novel structure of middle SM is inserted between the upper and lower arms, which has lesser count of components compared with the existing ones, leading to the reduction in cost and power losses. At the low operating frequency, furthermore, the middle SM can attenuate the power fluctuation in arms by distributing the high-frequency power components. Therefore, the SM capacitor voltage fluctuation is significantly alleviated without imposing the common-mode voltage on the ac side. The effectiveness of the proposed topology has been verified by experimental results.**

***Index Terms*—Common-mode voltage, low-frequency operation, modular multilevel converter (MMC), SM capacitor voltage fluctuation.**

I. Introduction

RECENTLY, modular multilevel converters (MMCs), which consist of series connections of modular submodules (SMs), have garnered substantial attention due to their various merits such as modularity, scalability, fault-tolerant operation, and low-harmonic content of output voltage [1]. Therefore, several applications of MMCs have been introduced in medium- to high-voltage industrial applications [2]. However, there are a few challenges regarding the topology of MMCs that have to be overcome. One of them is that the peak-to-peak fluctuation of SM capacitor voltage is proportional to the output current level and inversely proportional to the fundamental frequency [3], [4]. It leads to a large voltage fluctuation in the SM capacitor, which causes performance deterioration of MMCs at low-frequency operation.

A conventional solution involves using the sinusoidal-wave method [4], where high-frequency voltages and ac-circulating currents are injected into the phase legs. This method ensures that the low-frequency power fluctuations in the arms are reduced during low-frequency operations, which results in the attenuation of SM capacitor voltage fluctuation. However, the common-mode voltage (CMV), which is proportional to the injected high-frequency voltage, is imposed on the ac side [5].

Meanwhile, modifications in MMC topology have been introduced [6], [7] where one SM is saved in per phase unlike that of the conventional MMC [1], [3]. It has been shown that the SM capacitor voltage fluctuation can be considerably reduced compared with that of the conventional MMC. However, the voltage fluctuation is still large during low-frequency operation [7]. It is only reduced further by injecting high-frequency CMV and ac circulating currents [6].

Enhanced topologies of MMCs with a middle SM placed between the upper and lower arms in one phase have been presented [5], [8]. The power imbalance due to low-frequency power fluctuation between both arms is transferred through the middle SM, which results in the reduction of SM capacitor voltage fluctuation without injecting the CMV. In [5], the middle SM consists of six switching devices and one capacitor, whereas four switching devices and two capacitors are featured in [8]. However, the suggested topology has been verified only at the rated fundamental-frequency operation. In addition, the number of components used could be potentially decreased to reduce the cost and power losses.

In this letter, a modified topology for MMC is proposed, where the SM capacitor voltage fluctuation can be alleviated during low-frequency operation. In the proposed topology, a novel middle SM, which consists of four switching devices and one capacitor, is placed between the upper and lower arms. It has less components compared with the conventional ones. Thus, the cost and power loss can be reduced. The middle SM is controlled to generate the high-frequency voltages, which is used to cancel out the injected high-frequency voltages in the upper and lower arms. Therefore, no CMV is imposed on the ac side. Under low-frequency operation, the high-frequency voltage can be utilized to interact with the ac-circulating current injected into the leg to alleviate the power fluctuation between both arms. As a result, the SM capacitor voltage fluctuation can be reduced. To verify the effectiveness of the proposed topology, a three-phase prototype is built and tested.

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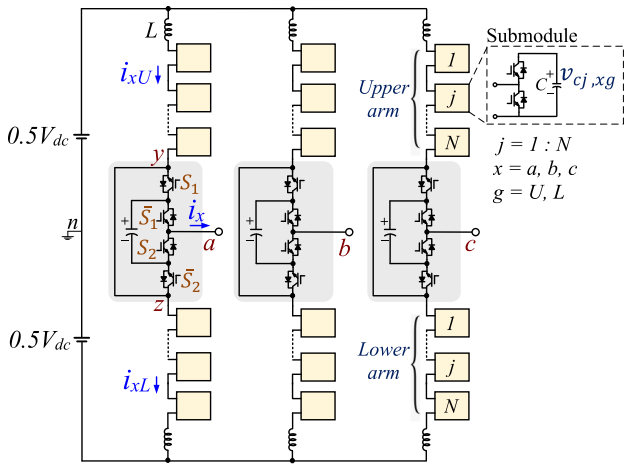

Fig. 1. Circuit configuration of the proposed topology.

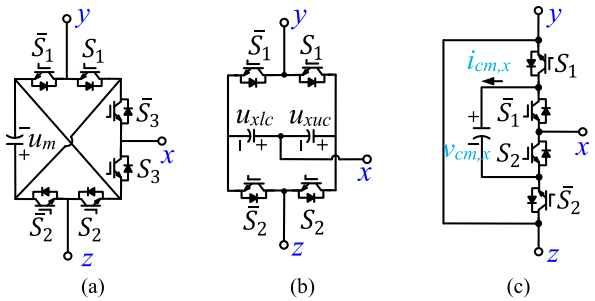

Fig. 2. Circuit configurations of middle SM. (a) Circuit in [5]. (b) Circuit in [8]. (c) Proposed circuit.

II. Modified MMC With Novel Middle SM

A. Circuit Structure

Fig. 1 shows the circuit structure of the proposed topology, where one leg consists of an upper arm, a lower arm, and a middle SM. The configuration of both arms consists of a series connection of modular cells and arm inductor, which is identical to that of the conventional MMC. In addition, an auxiliary circuit is added at the middle node between both arms and ac output side. Therefore, the load is connected at the output terminals of middle SMs in three legs.

Fig. 2 shows the circuit configurations of middle SMs, which are implemented in the conventional and proposed topologies. Fig. 2(a) shows the circuit configuration for conventional topology. This configuration features six switching devices and one capacitor in the middle SM [5]. Fig. 2(b) shows another conventional topology where four switching devices and two capacitors have been used [8]; here, the voltage stress on switching devices is two times higher than that in the SMs of arms. This leads to an increase in the number of switching devices used.

To reduce the cost and power losses of the existing MMCs while maintaining its attributes, the proposed middle SM with four switching devices and one capacitor is used as shown in Fig. 2(c). The switching devices and capacitor of middle SM have an identical voltage rating and capacitance to the ones in both arms.

TABLE I
Swithing States of Middle SM

Switching states	u_{yx}	u_{xz}
$S_1 = S_2 =$ "0"	- $v_{cm,x}$	$v_{cm,x}$
$S_1 = S_2 =$ "1"	$v_{cm,x}$	- $v_{cm,x}$

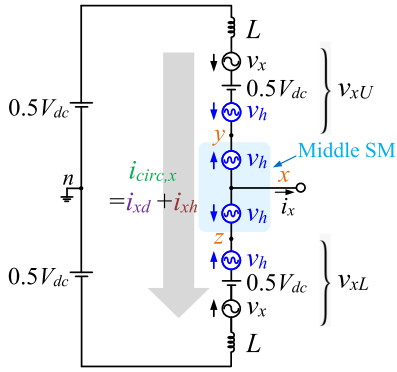

Fig. 3. Per-phase equivalent of a leg.

B. Operating Principle

To alleviate the SM capacitor voltage fluctuation, in the proposed topology, the high-frequency voltage v_h is also intentionally injected into upper and lower arms as applied in the sinusoidal-wave method [4]. The upper and lower arm voltages (v_{xU} and v_{xL}) are expressed, respectively, as

$$v_{xU} = 0.5V_{dc} - v_x - v_h \tag{1}$$

$$v_{xL} = 0.5V_{dc} + v_x + v_h \tag{2}$$

where v_x and V_{dc} is the output voltage and dc voltage, respectively. However, it is different from the method in [4] that, to avoid imposing the CMV on the ac side, two high-frequency voltages (v_h) in upper and lower arms can be cancelled out by the proposed middle SM. To achieve the cancellation, in Fig. 1, the middle SM should be controlled to generate v_h at its output terminals (v_{yx} and v_{xz}), which has the opposite polarity in the corresponding arm. So, v_{yx} and v_{xz} are expressed, respectively, as

$$v_{yx} = v_h \tag{3}$$

$$v_{xz} = -v_h. \tag{4}$$

According to the circuit configuration of the proposed middle SM shown in Fig. 2(c), in Table I, the switching states are listed together with the corresponding terminal voltage. u_{yx} is the output voltage of middle SM in the upper arms, which is opposite to v_{xz}, the output voltage of middle SM in the lower arms.

To simplify the description of operating principle, the per-phase equivalent circuit of a leg is shown in Fig. 3, where v_{xU} and v_{xL} include the fundamental-frequency (v_x), dc ($0.5V_{dc}$), and high-frequency (v_h) components. The equivalent circuit of middle SM is also simplified by v_h component at v_{yx} and v_{xz} with opposite polarity. Based on this arrangement, v_h has no effect on the output voltage waveform. During operation, an ac-circulating current (i_{xh}) is controlled to flow through the

leg, apart from the existing dc-circulating current (i_{xd}). The interaction between i_{xh} and v_h generates low-frequency power in arm for negating the inherent one, which is due to the interaction between the dc input voltage ($0.5V_{dc}$) and output current (i_x). Accordingly, the low-frequency power fluctuation can be reduced and the SM capacitor voltage fluctuation becomes lower.

C. Mathematical Analysis for Reducing the SM Capacitor Voltage Fluctuation

In (1)–(4), v_x and v_h are expressed, respectively, as

$$v_x = V_o \sin(\omega t + \varphi_x) \tag{5}$$

$$v_h = V_h \sin(\omega_h t) = v^*_{cx,m}(1-m)\sin(\omega_h t) \tag{6}$$

where V_o and V_h represent the amplitudes of each quantity, ω and ω_h are the angular frequencies of the fundamental and high-frequency components, respectively, φ_x is the initial phase angle, $v^*_{cx,m}$ is the middle SM capacitor voltage reference, and m is a modulation index. In addition, the upper and lower arm currents (i_{xU} and i_{xL}) are expressed as

$$i_{xU} = 0.5i_x + i_{circ,x} = 0.5i_x + i_{xd} + i_{xh} \tag{7}$$

$$i_{xL} = -0.5i_x + i_{circ,x} = -0.5i_x + i_{xd} + i_{xh} \tag{8}$$

where $i_{circ,x}$ is the circulating current flowing through the leg. i_{circ} includes the dc-circulating and ac-circulating currents (i_{xd} and i_{xh}), where i_{xd} is used to control the phase average SM capacitor voltage following the reference and i_{xh} is applied to alleviate the SM capacitor voltage fluctuation. i_{xh} is expressed as

$$i_{xh} = I_{xh} \sin(\omega_h t) \tag{9}$$

where I_{xh} is the amplitude of ac-circulating current.

The instantaneous power of the upper arm p_{xU} can be calculated by multiplying (1) and (7) as

$$p_{xU} = (0.5V_{dc} - v_x - v_h)(0.5i_x + i_{xd} + i_{xh}). \tag{10}$$

It is noted that the large ac-voltage fluctuation on SM capacitor is caused mainly due to the low-frequency power fluctuation. From (10), the low-frequency power fluctuation p_{xU_low} is derived as

$$p_{xU\_low} = 0.5V_{dc}i_{xd} - 0.5v_x i_x + 0.25V_{dc}i_x - v_x i_{xd} - 0.5V_h I_{xh}. \tag{11}$$

In (11), the first and second terms negate each other since the powers on the dc input side and ac output side are balanced. From these two terms, the dc-circulating current is derived as

$$i_{xd} = \frac{v_x i_x}{V_{dc}}. \tag{12}$$

Substituting (12) into (11) yields

$$p_{xU\_low} = 0.25V_{dc}i_x - v_x i_{xd} - 0.5V_h I_{xh}. \tag{13}$$

In (13), the first and second terms on the right-hand side are the main causes of large SM capacitor voltage fluctuation since they incur large power fluctuation with the fundamental frequency. To minimize the voltage fluctuation, p_{xU_low} should be suppressed, where the first and second terms are negated by the third term as

$$0.5V_h I_{xh} = 0.25V_{dc}i_x - v_x i_{xd}. \tag{14}$$

From (14), I_{xh} is derived as

$$I_{xh} = \frac{0.5V_{dc}i_x - 2v_x i_{xd}}{V_h}. \tag{15}$$

By substituting (12) into (15), the ac-circulating current i_{xh} can be obtained as

$$i_{xh} = I_{xh}\sin(\omega_h t) = \frac{1}{V_h}\left(0.5V_{dc} - \frac{2v_x^2}{V_{dc}}\right) i_x \sin(\omega_h t). \tag{16}$$

As a result, the low-frequency power fluctuation on each arm is mitigated by injecting i_{xh}, which leads to the reduction of SM capacitor voltage fluctuation.

To analyze the voltage fluctuation on the middle SM capacitor, the current flowing through the middle SM capacitor in Fig. 2(c) is achieved as

$$i_{cm,x} = (S_1 - \overline{S}_1)i_x = (2S_1 - 1)i_x. \tag{17}$$

In (17), S_1 is controlled mainly by the injected high-frequency voltage v_h with a neglect of the compensating voltage of middle SM balancing control. By normalizing v_h in (6) by $v^*_{cx,m}$ and substituting it into S_1 in (17), $i_{cm,x}$ can be expressed as

$$i_{cm,x} \approx (1-m)\sin(\omega_h t) i_x. \tag{18}$$

The output current i_x is expressed as

$$i_x = I_o \sin(\omega t + \varphi_x - \phi) \tag{19}$$

where I_o is the amplitude and φ is the phase angle between output voltage and current. Substituting (19) into (18), $i_{cm,x}$ is expressed as

$$i_{cm,x} \approx I_o(1-m)\sin(\omega_h t)\sin(\omega t + \varphi_x - \phi). \tag{20}$$

It can be seen that $i_{cm,x}$ includes only high-frequency components, which causes the middle SM capacitor ($v_{cm,x}$) to be charged and discharged within a short interval. Hence, the ac-voltage fluctuation in the middle SM capacitor is low.

III. Experimental Results

An experimental study has been conducted to verify the proposed topology. Fig. 4 shows a photo of the hardware prototype at the laboratory, where 24 SMs and 3 middle SMs are set up. In Table II, the system parameters for experiment are listed.

Fig. 5 shows the performances of the conventional MMC and the proposed topology with the fundamental frequency (f_o) of 12.5 Hz. It can be seen that there are large ac–voltage fluctuations (27.5 V) in the SM capacitors used in the conventional MMC as shown in Fig. 5(a), which are caused by the large low-frequency power fluctuations in arms. Therefore, the three-phase output current (i_{abc}) becomes distorted. Conversely, in the performance of the proposed topology as shown in Fig. 5(b), the SM capacitor voltage fluctuation is alleviated to approximately 7.5 V and i_{abc} is sinusoidal. It can be seen that the ac-voltage fluctuation on SM capacitor consists of high-frequency components

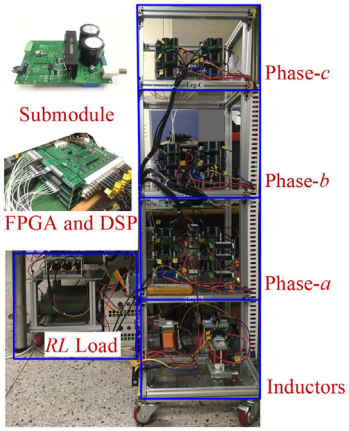

Fig. 4. Hardware prototype of the proposed topology.

TABLE II
SYSTEM PARAMETERS FOR EXPERIMENT

Parameters	Symbol	Value
Converter		
DC-link voltage	V_{dc}	200 V
Number of SMs per arm	N	4
SM capacitor voltage reference	v_c^*	50 V
Middle SM voltage reference	$v_{cx,m}^*$	50 V
Arm inductance	L	1 mH
SM capacitance	C	2500 μF
Rated frequency	f_o	50 Hz
Carrier frequency	f_c	4000 Hz
High frequency	f_h	400 Hz
RL Load		
Resistance of RL load	R_l	2 Ω and 5 Ω
Inductance of RL load	L_l	6 mH

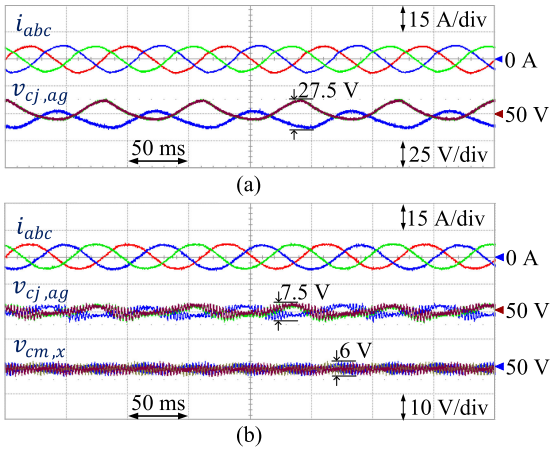

Fig. 5. Three-phase output current and SM capacitor voltages at $f_o = 12.5$ Hz. (a) Conventional MMC. (b) Proposed topology.

apart from the fundamental-frequency one, which is due to the injection of high-frequency components. In addition, since the current flowing through the middle SM capacitor consists of high-frequency components only, $v_{cm,x}$ is well balanced at 50 V with a fluctuation of 6 V.

In Fig. 6, the peak voltage stresses on switching devices of middle SM are shown. The values on S_1 and S_2 are approximately 50 V each, equal to the middle SM capacitor

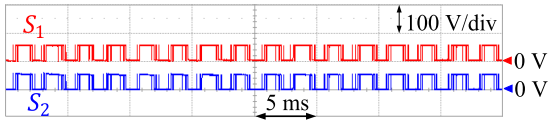

Fig. 6. Peak voltage stresses on switches of the middle SM.

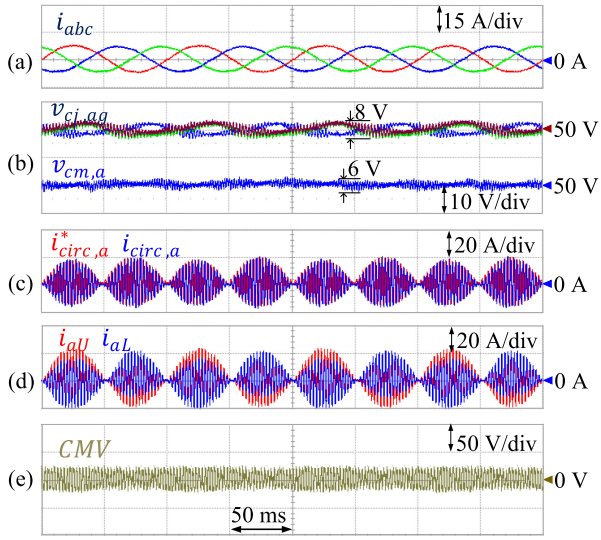

Fig. 7. Performance of the proposed topology at $f_o = 10$ Hz. (a) Three-phase output current. (b) SM and middle SM capacitor voltages. (c) Circulating current. (d) Arm currents. (e) Common-mode voltage.

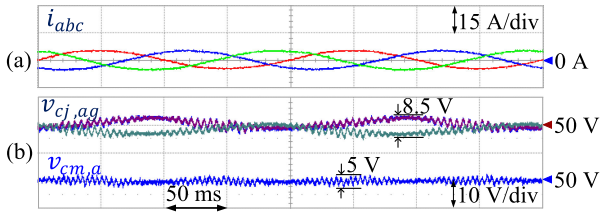

Fig. 8. Performance of the proposed topology at $f_o = 5$ Hz. (a) Three-phase output current. (b) SM and middle SM capacitor voltages.

voltage. Considering this, it can be inferred that the voltage rating and capacitance of components implemented in the middle SM are identical to those of components in both arms.

Fig. 7 illustrates the performance of the proposed topology with f_o of 10 Hz. The sinusoidal waveforms of three-phase output currents are obtained in Fig. 7(a), where its amplitude is about 8 A. Fig. 7(b) shows the balancing performance of the SM capacitors, which is controlled at 50 V with the peak-to-peak value of 8 V. The middle SM capacitor voltage ($v_{cm,a}$) is also balanced well at 50 V with the fluctuation of 6 V. It confirms that $v_{cm,a}$ is charged and discharged within a short interval as discussed in (14).

Fig. 7(c) shows the circulating current $i_{circ,a}$, which includes the dc-circulating and ac-circulating currents (i_{xd} and i_{xh}). The arm currents and CMV are shown in Fig. 7(d) and (e), respectively, where the CMV is about ±25 V. In addition, the performance of the proposed topology with f_o of 5 Hz is shown in Fig. 8, where the voltage fluctuations in SM capacitors and middle SM capacitor are mitigated appropriately. It is noted that

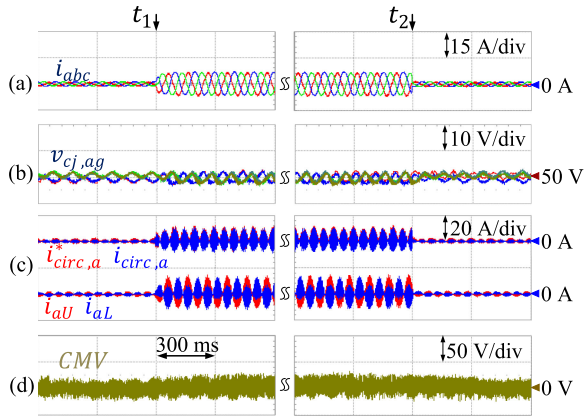

Fig. 9. Performance of the proposed topology under load change condition. (a) Three-phase output current. (b) SM capacitor voltages. (c) Circulating current. (d) Arm currents. (e) Common-mode voltage.

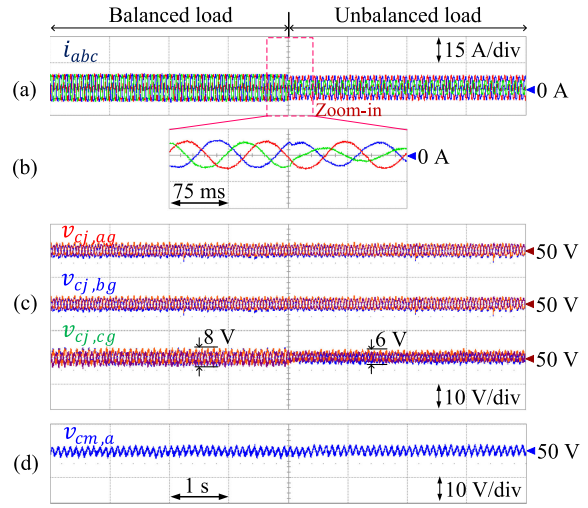

Fig. 10. Performance of the proposed topology under unbalanced load condition. (a) Three-phase output current. (b) Zoom-in waveforms. (c) SM capacitor voltages. (d) Middle SM capacitor voltages.

the voltage fluctuation on the middle SM capacitor depends on $i_{cm,x}$ in (20), which is proportional to the amplitude of output current I_o. Hence, the voltage fluctuation on middle SM capacitor (5 V) is lower than that (6 V) of in Fig. 7 (b), since I_o is about 5 A.

Fig. 9 shows the performance of the proposed topology in transient conditions, where the load power is abruptly changed from low load to high load and then returned to low load at t_1 and t_2, respectively, with $f_o = 10$ Hz. Fig. 9(a) shows the three-phase output current with an amplitude of 8 A at high load. The SM capacitor voltages are shown in Fig. 9(b), which is balanced at 50 V with low voltage fluctuations. In Fig. 9(c), amplitudes of the circulating current and arm currents are increased when the load is applied to reduce the low-frequency power fluctuation. Fig. 9(d) shows the CMV, which remains unchanged during operation.

Fig. 10 demonstrates performance of the proposed topology under unbalanced load condition with $f_o = 10$ Hz, where an additional 4 Ω resistor is connected in phase-c. In Fig. 10(a), the amplitude of i_c is decreased from 8 to 4.5 A, whereas the

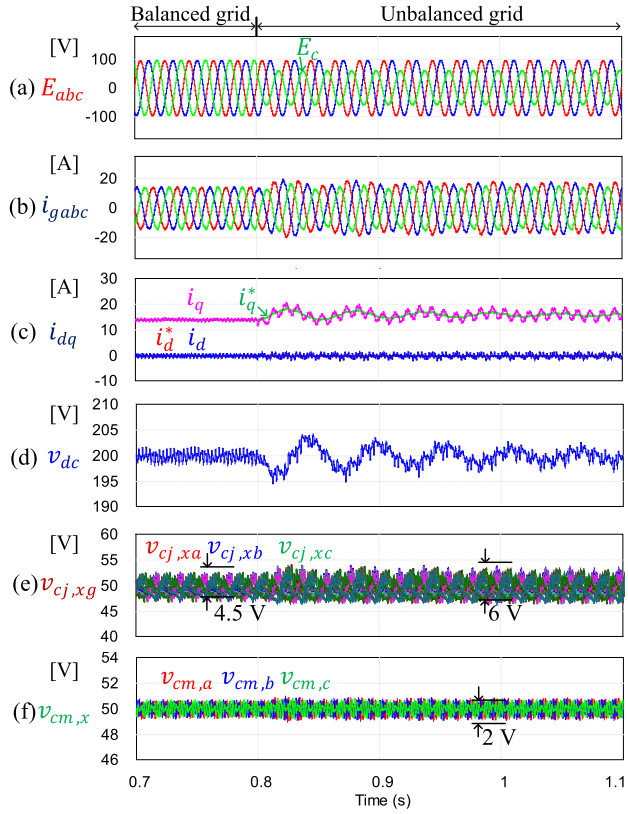

Fig. 11. Performance of the proposed topology under unbalanced grid condition (simulation). (a) Grid voltage. (b) Grid current. (c) dq-axis converter currents. (d) DC-link voltage. (e) SM capacitor voltages. (f) Middle SM capacitor voltages.

amplitudes of other phase currents are maintained. It can be seen that the voltage balancing performances of SM capacitors and middle SM capacitors are not affected by the unbalanced loads. At the unbalanced condition, the voltage fluctuation on SM capacitor of phase-c is decreased from 8 to 6 V as shown in Fig. 10(c). It is caused by the reduction of the amplitude of i_c.

In addition to the inverter operation of the proposed topology, its operation as a grid converter is also investigated. Fig. 11 illustrates the control performance of the proposed topology, where the voltage amplitude of phase-c (E_c) is decreased by 40% at $t = 0.8$ s as shown in Fig. 11(a). Fig. 11(b) and (c) show the grid phase currents and dq-axis quantities in synchronous reference frame, which are distorted under grid unbalance condition since no particular control scheme is applied to eliminate this. Accordingly, the dc-link voltage has ripple components as shown in Fig. 11(d). However, the voltage balancing performances on SM capacitors and middle SM capacitors are still kept well with little fluctuations as shown in Fig. 11(e) and (f), respectively.

To evaluate the system efficiency, the power losses of the conventional and proposed topologies have been analyzed, where the Infineon's IGBT IKW20N60T is used [9]. The conduction and switching losses have been evaluated using Thermal Modules in PSIM [10]. Fig. 12 shows the power loss comparison at various operating frequencies (f_o) between the conventional and proposed topologies. Conv[5]_con, Conv[8]_con, Conv[5]_sw, and Conv[8]_sw mean the conduction and switching losses of

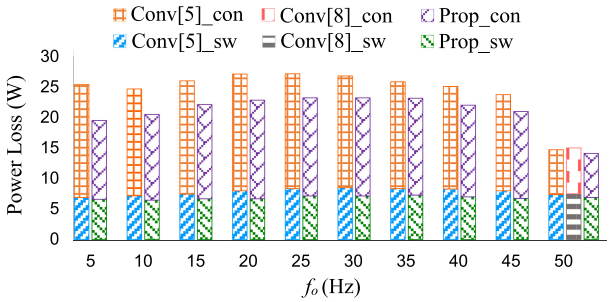

Fig. 12. Power loss comparison at various operating frequencies (f_o) between the conventional and proposed topologies.

the conventional topologies [5] and [8], respectively; Prop_con and Prop_sw denote those of the proposed topology.

In the proposed topology, the middle SM has less components compared with those of the conventional topologies, which results in lower total power loss. Since the topology in [8] is usually used for operating at the rated frequency (50 Hz), its power loss has not been investigated at low frequencies. In [5] and proposed topology, owing to natural balancing of SM capacitor voltage under the rated-frequency operation, there is no injection of the high-frequency component into the leg. It leads to lower power loss compared with the topology in [8], where a second-order harmonic current is injected. With this injection, the SM capacitor voltage fluctuation in [8] is lower than that of in Huang *et al.* [5] and proposed topology under the rated-frequency operation.

IV. Conclusion

In this letter, a modified topology of MMC has been proposed, where the SM capacitor voltage fluctuation has been mitigated at low-frequency operation. In the proposed topology, a novel middle SM is suggested that uses lesser components compared with that of the existing topologies; the proposed technology can reduce costs and power losses. The middle SM has been controlled to produce high-frequency voltages, which have polarities opposite to those injected into the upper and lower arms. Based on this arrangement, the ac-circulating current has been injected into the leg, which facilitates the reduction of the low-frequency power fluctuation in the arms. Therefore, the voltage fluctuation in SM capacitors has been alleviated without imposing the CMV on the ac side. The feasibility of the proposed topology has been verified through experimental results using a hardware prototype.

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