A Mathematical Design Approach to Volumetric Optimization of EMI Filter and Modeling of CM Noise Sources in a Three-Phase PFC

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***Abstract*—Designing an efficient, compact, and optimized electromagnetic interference (EMI) filter for the next generation high-frequency switched mode power converter while maintaining a small form factor with high power density, requires adequate research and development effort. This article presents a systematic as well as unified approach to design the EMI filter for any power electronic converter, particularly for three-phase ac–dc active boost rectifier systems. Since the differential mode (DM) filter stage consumes a major part of the EMI filter volume and weight, DM filter design optimization is a necessary yet challenging task to attain a higher power density. This article theoretically demonstrates the design steps for choosing the appropriate filter component values and number of filter stages to achieve the smallest volume of the DM EMI filter. Furthermore, to design an optimized common mode (CM) filter stage, a research effort has been made for estimation of the CM noise corner frequencies followed by multiconstraint volume optimization through a detailed mathematical noise modeling of the converter. While the validation of the proposed design methodology is done through MATLAB simulation, an experimental verification is also performed by designing the optimized EMI filter for a 2.3-kW proof of concept of a three-phase boost power factor correction converter to comply with the stringent EMI requirements of DO-160F standard.**

***Index Terms*—AC-DC power converters, electromagnetic interference, pulse width modulation converters.**

I. Introduction

FOR THE emerging fields of power electronics such as: Avionics or marine applications, the modern ac–dc rectifier systems like active boost power factor correction (PFC) converters [1]–[4] need to comply with stringent requirements in terms of efficiency, reliability, volume, weight, line harmonics, and finally electromagnetic interference (EMI) [5]–[7]. To protect the ac mains from the electromagnetic emissions originating from the high-frequency switching of such converters and to comply with the respective harmonic standards, common mode (CM) and differential mode (DM) front-end EMI filters are imperatively needed.

While there are works that discuss the DM filter design for a certain power converter topology, a few studies [8]–[15] have been done to showcase the systematic CM filter design approach. It is challenging to design the adequate CM filter for any converter including the three phase PFC rectifiers due to the difficulty in identification and quantification of the CM noise sources. A few research have been carried out to model the CM noise sources in single phase PFCs [8], [9] and to identify their ways of propagation in three phase rectifier systems [10]–[16]. But these works fail to incorporate the CM noise models within the filter design methodology. An approach to identify the relation between the CM noise spectrum and the noise sources in a three phase PFC is made in [18], but it does not include the estimation of amplitudes and frequencies of different CM noise components that are necessary to design the CM filter. To address the abovementioned limitations, a CM noise corner frequency estimation-based approach is adopted in this article to design an optimized CM filter for a three-phase PFC rectifier. The article presents all the possible CM noise corner frequencies by identifying the resonating circuit paths, through which the noise current can flow to the earth. Furthermore, through a constrained design optimization approach, this work accounts for the maximum allowable ground leakage current that often acts as a stringent constraint for the power converter used in avionics and space applications, which is not covered in any of the previous works. This sets an upper bound on the total CM filter capacitance in the filter design stage.

On the other hand, although some studies have been carried out to estimate the emitted DM noise [17], [18] and attenuate them by employing specific single or multistage DM filter, a systematic design approach that takes care of the following aspects is still missing: 1) selection of the optimum *LC* component values for minimum per-stage filter volume, 2) optimum count of filter stages considering power factor constraint and attenuation requirement, and 3) accurate volumetric model of filter components. The work in [18] demonstrates a simplified approach to design the optimum DM EMI filter based on estimated DM noise voltage at the filter design frequency. However, theoretically estimated DM noise amplitudes at switching frequency harmonics do not match with the real hardware as the noise model does

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not account for side band harmonics and circuit nonidealities, such as: Device or circuit parasitics. Therefore, in this work, the experimentally measured unfiltered EMI spectrum is taken as a more reliable design input for the filter synthesis process, which leads to the elimination of design errors and hence yields to a more precise and optimized design.

The presence of power stage nonidealities in any power converter, such as: stray inductances, parasitic capacitances of switching devices, and inter/intra winding capacitances of the inductor/transformer give rise to voltage- and current-mode EMI noise sources that tend to propagate toward the ac grid and/or chassis (or potential earth), resulting in increased leakage current and grid pollution. Compared to Si devices, the wide bandgap (WBG) devices, such as: gallium nitride (GaN) and silicon carbide (SiC) have higher dv/dt and di/dt switching transient rates. Therefore, the noise peak amplitudes in the EMI spectrum would be even higher for WBG-based power converters. The noise attenuation requirement that needs to be met by the EMI filter stage in a WBG-based power converter is likely to be higher than a Si-based design at the same switching frequency, which makes the filter bulkier and heavier in a WBG-based design. Notably, one of the major motivations of using WBG semiconductor technology is to perform a high-density power conversion while also enhancing the efficiency. With that said, although the power converter stage can be made higher power dense with WBG employment, the front-end EMI filter volume and weight tend to be higher, which, may not give us a significant net benefit of power density. Therefore, there needs to be significant research focus on EMI filter volumetric optimization for enabling WBG-based high-density power conversion, which is highly overlooked in the current research. Volume- and weight-optimized filter design solutions are critical for EMI stringent applications with power density being the priority, such as: Power electronics for avionics and space because a stricter noise attenuation requirement naturally makes the filter to be bulkier and heavier. Since the DM filter components contribute to a major part of the converter size and weight [13], [18], DM EMI filter power density improvement is as critical as that of the power conversion stage. Although a few techniques on volume optimization for the DM filter have been proposed in [13] and [18], the accuracy of the filter optimization process is largely compromised due to improper formulation of the quantitative cost functions, corresponding to the volume of the DM filter stages. This article presents a multiobjective constrained design optimization methodology for volume minimization of the DM filter. Through a comprehensive evaluation, we hereby propose a precise volumetric cost function model, in which, the volumes of passive components (i.e., toroidal core filter inductors, film type X capacitors) are quantified as a scaled linear combination of current/voltage, element value and the stored energy. Further, in this work, a rigorous mathematical formulation between the optimum count of filter stages and resultant filter volume for a given attenuation requirement is established and presented graphically.

The major contributions of the work are as follows.

1) Presentation of a unified and systematic approach for designing an optimized EMI filter for a three-phase ac–dc power converter.

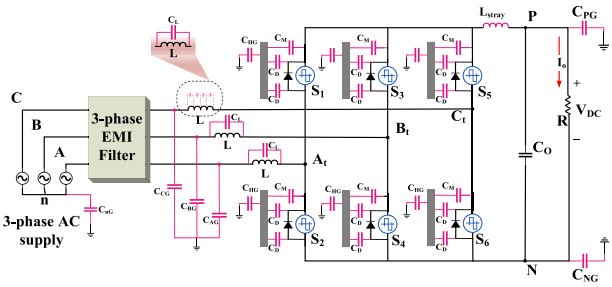

Fig. 1. 3-phase boost PFC rectifier noise model with LISN.

2) Successful identification and modeling of CM noise sources in a three phase PFC rectifier.
3) Accurate estimation of the CM noise corner frequencies and mathematically corelating them to the CM EMI spectrum.
4) A unified and generalized multiconstraint design methodology accounting for all constraints, such as: Maximum common mode leakage current and input power factor at light load operations, in the EMI filter design strategy.
5) Error variance minimization-based statistical modeling that quantitatively corelates the DM filter components volume with rated current/voltage and filter element values.
6) Multiobjective constrained volume optimization of the DM and CM filters based on the proposed volumetric models of the filter elements.

This article is organized as follows. Section II presents the modeling of different parasitic CM and DM noise sources that are present in a three-phase boost PFC rectifier. Comprehensive filter design methodologies are introduced and analyzed in Section III. Section IV describes a multiobjective constrained design optimization-based volume minimization technique for the DM filter. The filter design process is validated through simulations and experimental results, presented in Section V. Finally, Section VI concludes this article.

II. Parasitic Noise Sources and Their Modeling in a Three-Phase PFC

A key step for an effective design of an EMI filter stage for a power converter, is to effectively model the parasitic noises, generated from the circuit operation. EMI noise sources in a three-phase PFC converter mainly originate from several stray capacitances such as semiconductor–heat sink capacitance, heat sink-to–ground capacitance, and dc link-to-ground parasitic capacitances and stray inductances due to PCB traces and physical connecting cables. Fig. 1 shows the different possible sources of parasitic noises in a three-phase active boost rectifier, in which the parasitic components are shown in red color to distinguish from power stage components. The stray capacitances of the MOSFET's drain to the heat sink and the antiparallel diode's cathode to the heat sink are denoted by C_M and C_D,respectively. There is an additional capacitance (C_{HG}) that appears between the heat sink and the ground, if the heat sink is not grounded externally. The presence of these three vital capacitances along with PCB trace and device's lead inductance L_{stray} produce a very high-frequency overriding signal on the switching pulses

and shift the CM noise level up in the EMI spectrum. The interwinding capacitances of the line inductors will also affect the EMI performance of the converter at high switching frequency. To include that in the noise model, we have assumed a lumped value of such capacitances (C_L) and placed it across the line inductor L. C_{PG} and C_{NG} are the parasitic capacitances from the dc link positive and negative terminals to the ground, respectively. All the three input phases will have parasitic capacitances developed between the phase and the protective earth, which are shown as C_{AG}, C_{BG}, and C_{CG}. To establish a CM noise model of the converter, each MOSFET is replaced by a combination of a bipolar square-pulsed voltage source of the same frequency as the switching frequency and the drain-to-source capacitance C_{ds}. The dc link capacitor C_o is modeled as short-circuit as it will provide minimal impedance at the switching frequency and its higher order harmonics.

From the summarized noise model, it can be shown that a significant amount of EMI noise is generated from the heat sink connected to the semiconductors. According to Fig. 1, irrespective of the polarity of the phase current, the parasitic capacitance between the semiconductor switch and the protective earth can be expressed as

$$C_{\mathrm{SWG}} = \begin{cases} (C_M + C_D);\ \text{HeatSink is Grounded} \\ \left[\frac{C_{HG}.(C_M+C_D)}{C_{HG}+C_M+C_D}\right] =\sim C_{HG};\ \text{HeatSink is Floating.} \end{cases} \tag{1}$$

When the heat sink is connected to the earth, there is no existence of C_{HG}, and only C_M and C_D appear across the device and the ground. On the contrary, if the heat sink is left floating, the total capacitance between the switching device's drain node and ground becomes C_{HG} as C_{HG} is far less than $(C_M + C_D)$. This analysis shows that the impedance provided by C_{SWG} to the high-frequency ground noise current will be higher if the heat sink is grounded, compared to the case when it is left floating. In most of the power electronic applications, the heat sink is connected to the earth for safety reasons, leading to a higher amount of ground leakage current due to the formation of resonating CM path.

In addition, there are parasitic capacitances from phase to ground, which are not same for all three phases; rather, the parasitic values depend on the instantaneous switching combination of the three half-bridges. To design the EMI filter stage, it is important to determine the frequencies of the resonant oscillations caused by the parasitic parameters; thus, the related equations governing these oscillation frequencies are presented in Table I. The corner frequencies of the CM filter stage are determined from the parasitic resonance frequencies, which are difficult to be calculated deterministically, but they could be calculated with a reasonably high accuracy using the proposed noise modeling equations (Table I). Such CM noise modeling approach can be used for any converter topology undergoing switching events, because the switching device parasitic capacitances or the interwinding capacitances, and stray inductances can be modeled for any power converter similarly as shown in our example of three phase PFC.

TABLE I
CM NOISE CORNER/RESONANT FREQUENCY ESTIMATION

Estimated Resonant Frequencies	Approximate Resonant Frequency Value		Assumed Parameter Values
	Heat Sink Grounded	Heat Sink Floating	
$f_{noise1} = \frac{1}{2\pi\sqrt{LC_{SWG}}}$	$\sim 650kHz$	$\sim 2.52MHz$	$C_o = 100uF$ $L = 400uH$ $C_D + C_M = \sim 150pF$ $C_{HG} = \sim 10pF$ $L_{stray} = \sim 10nH$ C_{NG} or $C_{PG} = \sim 500pF$ $C_{AG} or C_{BG} = \sim 20pF$
$f_{noise2} = \frac{1}{2\pi\sqrt{L(kC_{SWG} + C_{NG} + C_{PG})}}$	$\sim 235kHz$	$\sim 250kHz$	
$f_{noise3} = \frac{1}{2\pi\sqrt{L(kC_{SWG} + C_{NG} + C_{PG} + C_{AG})}}$	$\sim 233kHz$	$\sim 248kHz$	
$f_{noise4} = \frac{1}{2\pi\sqrt{L_{stray}C_{SWG}k}}$	$\sim \frac{130}{\sqrt{k}} MHz$	$\sim \frac{503}{\sqrt{k}} MHz$	

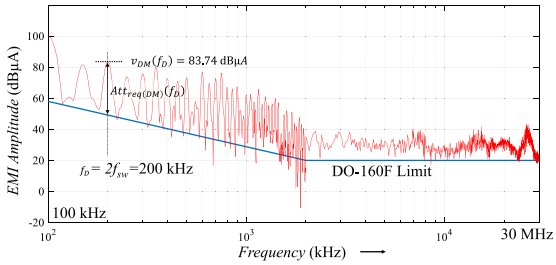

Fig. 2. Unfiltered EMI spectrum of the 3-phase boost PFC under study.

In a three-phase boost active rectifier circuit, the input boost line inductance L takes part in resonance with line–ground parasitic capacitances and semiconductor parasitics, generating the noise corner/resonant frequencies: f_{noise1}, f_{noise2}, and f_{noise3}. The value of "k" could be 1 or 2, depending on the number of conducting high-side switches in the PFC converter. Also, the stray PCB inductance and the device parasitics will provide another resonant frequency f_{noise4}, which is much higher than the other noise frequencies. The corner frequency estimation shows if the heatsink is grounded, which is the case for most of the converters, the order of the noise frequencies on the EMI spectrum will be: $f_{\mathrm{noise4}} > f_{\mathrm{noise1}} > f_{\mathrm{noise2}} > f_{\mathrm{noise3}}$. As per the calculation, f_{noise4} is found to be higher than 30 MHz and hence, falls outside the conducted EMI standard range. As the noise2 and noise3 appear at relatively lower resonating frequency, these can be partly attenuated by the DM filter stage along with CM stage. Therefore, f_{noise1} can be one suitable choice of resonant frequency for the CM filter design as it is greater than the DM noise frequencies. Also, the other high-frequency resonant oscillations should be significantly attenuated through the CM filter implementation if the filter is designed to attenuate the f_{noise1} frequency component.

In this work, an ANSYS based Q3D simulation has been carried out to extract the parasitic models of the converter power stage including stray inductances. Calculation of the possible resonant frequencies from the extracted L and C values suggests appearance of CM noise peaks at 2.37, 8.1, 15.3, 28.6 MHz, and higher order multiples. Validation of our claimed correlation between the converter circuit parasitics model and the CM mode EMI spectrum can be found from the unfiltered EMI spectrum of the converter, shown in Fig. 2. It shows prominent CM noise

peaks appearing at 2.3, 15 MHz that match closely with the model outcomes, and thus, verifies our parasitic modeling of the converter power stage.

III. EMI Filter Design Approach

In this article, the filter design is performed based on the specifications of a three-phase boost PFC, with an input of a three-phase alternator with variable frequency (360–800 Hz), typically used in shipboard and aircraft applications. Target for the filter design is to meet the EMI standard requirements according to DO-160F. The DM and CM EMI filter design approach for such a converter is separately shown below.

A. DM Filter Design

The EMI noise spectrum of any power converter will exhibit DM noise peaks at the switching frequency and its higher order harmonics. Each of such harmonics will need different level of attenuations to comply with the specific EMI standard. Therefore, for a given switching frequency (100 kHz in this design), making an appropriate choice of the DM filter corner frequency is the first important design step for a DM filter design. Next step would be to determine the attenuation requirement profile as a function of frequency. For the converter-under-test (CUT), the EMI amplitude spectrum of the converter without any filtering action is shown in Fig. 2, which implies that the highest peak of 84 dBμA occurs at 200 kHz in the conducted EMI band. Other peaks are located at the higher multiples of the switching frequency. Therefore, the attenuation requirement for the DM noises, as mentioned in (2), are obtained by subtracting the conducted EMI standard DO-160F from the spectrum without any filter with a design margin. As our converter is intended to be used for avionics application holding harsh environments, looking at the aspects of system reliability and satisfactory EMI performance under the case of health degradation of power stage components, a $\sim$15-dB buffer margin is introduced in the attenuation requirement calculation for the DM filter stage.

$$\begin{aligned}&\mathrm{Att}_{\mathrm{req}(DM)}\,(f_D)\,[dB]\\&= v_{DM}\,(f_D)\,[dB\cdot\mu A] - \mathrm{Limit}(f_D)[dB\cdot\mu A] + \mathrm{Margin}[dB]\\&= 50\,dB\;\;(at\;\;f_D = \;200\,kHz)\,.\end{aligned}\tag{2}$$

Also, our proposed filter design optimization methodology is adaptable toward any adjustable margin that can be decided by the designer. Choosing a different value of margin only changes the attenuation requirement, while not affecting the mathematical steps of the design optimization process.

Now, a DM filter that can deliver at least the required attenuation, $\mathrm{Att}_{\mathrm{req}(DM)}$, at the design frequency f_D needs to be designed. Determining the f_D is straightforward and in most cases, it would be the switching frequency or its higher order harmonic ($f_D = mf_{sw}$, m = +ve integer), whichever peak appears first in the EMI spectrum. In our design example, the converter switching frequency is kept as 100 kHz. Hence, the switching harmonic that appears first in the EMI spectrum within the DO-160F EMI standard range (that starts from 150 kHz), has a frequency of 200 kHz, i.e., the 2nd switching harmonic.

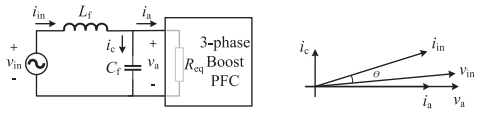

Fig. 3. Distortion of grid side input phase current due to a single *LC* filter stage before a PFC circuit.

Therefore, the design frequency (f_D) for the DM filter is chosen as 200 kHz.

In case of the DM filter design, while meeting the required attenuation, another crucial aspect to consider is the displacement of input phase currents due to the added filter components, specifically the phase-to-phase X-type capacitors. In case of any power converter with a front-end PFC circuit as shown in the Fig. 3, the PFC input phase currents (i_a) and voltages (v_a) are in phase due to a high-bandwidth current controller. However, due to the input side DM filter stage, comprising of lumped L_f and C_f , the input phase current (i_{in}) shows a displacement of angle Θ with respect to the input phase voltage (v_{in}) , which will result in power factor degradation. A calculation using the phasor diagram, shown in Fig. 3, leads to the following relationship between the filter components and the phase displacement angle:

$$\frac{2\pi f_{\mathrm{line}}}{R_{eq}}\left[L_f - {R_{eq}}^2 C_f + {R_{eq}}^2 {C_f}^2 L_f (2\pi f_{\mathrm{line}})^2\right] = \tan\Theta\tag{3}$$

where f_{line} is the line frequency i.e., 60 Hz and R_{eq} represents input impedance of the PFC and its following power stage, respectively, which as a whole is resistive in nature under a proper PFC action. R_{eq} can be represented as the ratio of voltage and current peaks of phase "A," $R_{eq} = (v_{pk,\mathrm{high}}/i_{pk,\mathrm{low}})$. To ensure a maximum allowable phase displacement of $\Theta_{\max}$, a maximum allowable filter capacitor size must be determined keeping the worst condition in mind. The relation in (4) as shown at the bottom of the next page, sets the worst-case condition, where R_{eq} is maximized to find the solution for maximum filter capacitor size, $C_{f,\max}$, which is shown in (5) as shown at the bottom of the next page.

In (4) and (5), IDF denotes the input displacement factor, which is the cosine of angle between fundamental input phase voltage and fundamental input phase current. $v_{pk,\mathrm{high}}$ is the peak value of maximum possible phase voltage, and $i_{pk,\mathrm{low}}$ is the minimum possible peak value of phase current at a certain load condition. If the maximum phase displacement needs to be limited to 5° (i.e., IDF = 0.996) at the rated output power, the total DM filter capacitors are limited to a total capacitance value of C_D = 3.5 μF per phase, as obtained from (5) considering $i_{pk,\mathrm{low}}$ and $v_{pk,\mathrm{high}}$ values to be 4.28 A and 358 V, from the specifications of the converter. For a multistage cascaded configuration of DM filter, the parallel combination of all the capacitances, required per stage, must not exceed 2.63 μF to meet a PF requirement of > 0.996.

Fig. 4 shows the EMI filter circuit topology that is used in this work. Here, the DM filter stage comprises of total six decoupled line inductors and six line-line X capacitors connected in a star fashion, and the CM stage has a set of

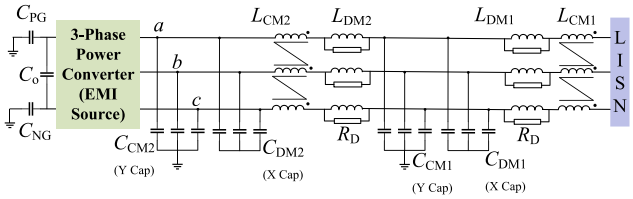

Fig. 4. EMI circuit topology used for 3-phase boost PFC in regulated transformer rectifier unit (RTRU).

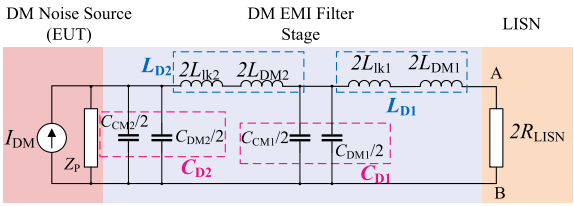

Fig. 5. DM equivalent of the EMI filter for 3-phase boost PFC.

two CM chokes and six line-ground Y capacitors. For synthesizing the DM filter parameters, the per phase equivalent circuit of the filter, as shown in Fig. 5, needs to be analyzed. Here, the DM noise source in the converter is modeled as a current-mode noise source I_{DM} with a parallel impedance Z_P that equivalently represents the pulse width modulation (PWM) converter. Furthermore, for the simplicity of analysis, we assume the following: The input-side impedance offered by both Y-capacitances and the effective series inductive path should be very large in comparison with the total line impedance stabilization network (LISN) in order to complete a DM noise path, i.e., $\omega \cdot 2(\mathrm{L_{DM1}} + \mathrm{L_{DM2}} + L_{lk1} + L_{lk2}) \gg 2R_{\mathrm{LISN}}$, where R_{LISN}, L_{lk1}, and L_{lk2} represent the LISN impedance, per phase leakage inductances for the CM chokes $\mathrm{L_{CM1}}$ and $\mathrm{L_{CM2}}$, respectively. Keeping these assumptions in mind, the per phase DM equivalent circuit can be treated as two back-to-back *LC* filter stages, where the two equivalent DM inductors are obtained as $\mathrm{L_{D1}} = 2(\mathrm{L_{DM1}} + L_{lk1})$ and $\mathrm{L_{D2}} = 2(\mathrm{L_{DM2}} + L_{lk2})$. Besides, two equivalent DM capacitors can be represented as $C_{D1} = (\mathrm{C}_{DM1} + C_{CM1})/2$ and $C_{D2} = (\mathrm{C}_{DM2} + C_{CM2})/2$. Therefore, on the basis of abovementioned assumptions and parameter values, the DM filter cutoff frequencies can be determined as $f_{\mathrm{R,D1}} = 1/(2\pi\sqrt{L_{D1}C_{D1}})$ and $f_{\mathrm{R,D2}} = 1/(2\pi\sqrt{L_{D2}C_{D2}})$. Thus, the total attenuation provided by the whole DM filter stage at a design frequency of f_{D} can be obtained as

$$\mathrm{Att}_{DM}\,(f_D)\ [dB] = 40\log\left(\frac{f_D}{f_{\mathrm{R,D1}}}\right) + 40\log\left(\frac{f_D}{f_{\mathrm{R,D2}}}\right) dB \tag{6}$$

which should surplus the required amount of noise attenuation at f_{D} frequency, $\mathrm{Att}_{\mathrm{req}(DM)}(f_D)[dB]$.

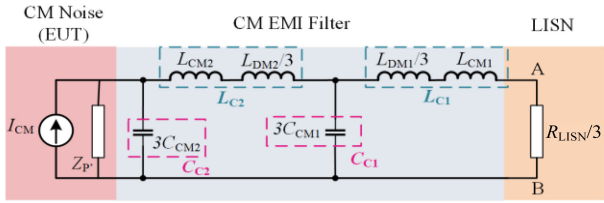

Fig. 6. CM equivalent of the EMI filter for 3-phase boost PFC.

B. CM Filter Design

An effective CM noise modeling approach has been adopted in this work, as mentioned in Section II, to estimate all possible CM noise corner frequencies. These estimated noise frequencies can be experimentally verified from the EMI spectrum of the power stage. To simplify the filter design analysis a per phase CM equivalent circuit of the whole EMI filter (Fig. 4) topology is obtained in Fig. 6. Here, the CM noise source in the converter is modeled as a noise current source I_{CM} with a parallel impedance $Z_P{}'$ that equivalently represents the PWM converter. To analyze this circuit, one critical assumption is that the equivalent CM impedance should be very large in comparison with the LISN impedance when all the phases contain CM noise, i.e., $\omega(L_{CM1} + L_{CM2} + L_{DM1}/3 + L_{DM2}/3) \gg R_{\mathrm{LISN}}/3$. Thus, the two equivalent CM inductors can be obtained as $L_{C1} = (L_{DM1}/3 + L_{CM1})$ and $L_{C2} = (L_{DM2}/3 + L_{CM2})$. Thereby, the CM noise returns to the ground or the protective earth through the two equivalent CM inductances L_{C1} and L_{C2} and two equivalent CM capacitances C_{C1} and C_{C2}. As shown in Fig. 6, the equivalent capacitors can be formed with the three line-ground Y capacitors (C_{CM}), which are parallel in the CM equivalent circuit: $C_{C1} = 3C_{CM1}$ and $C_{C2} = 3C_{CM2}$. This two-stage *LC* filter (Fig. 6) has two corner frequencies at $f_{\mathrm{R,C1}} = 1/(2\pi\sqrt{L_{C1}C_{C1}})$ and $f_{\mathrm{R,C2}} = 1/(2\pi\sqrt{L_{C2}C_{C2}})$, providing a total filter attenuation of $[40\log(f_D/f_{\mathrm{R,C1}}) + 40\log(f_D/f_{\mathrm{R,C2}})]\ dB$ to a CM noise of f_D frequency.

Thus, an appropriate choice of the CM filter stage corner frequency is critical to optimize the filter design. In this work, the CM corner frequency is chosen as f_{noise1} among all possible resonant frequencies shown in Table I. Although it is challenging to determine the exact value of corner frequency unlike the DM equivalent, a good approximation to start the design could be obtained by plugging in the parasitic parameters with the correct order of magnitudes in the estimated noise frequency formulas given in Table I.

$$\frac{2\pi f_{\mathrm{line}}}{(v_{pk,\mathrm{high}}/i_{pk,\mathrm{low}})}\left[L_f - (v_{pk,\mathrm{high}}/i_{pk,\mathrm{low}})^2 C_f + (2\pi f_{\mathrm{line}})^2 (v_{pk,\mathrm{high}}/i_{pk,\mathrm{low}})^2 C_f{}^2 L_f\right] \geq -\tan[\cos^{-1}(\mathrm{IDF_{min}})] \tag{4}$$

$$C_{f,\max} = \frac{1}{2(2\pi f_{\mathrm{line}})^2 L_f}\left[1 - \sqrt{1 - \frac{8\pi f_{\mathrm{line}} L_f i_{pk,\mathrm{low}}}{v_{pk,\mathrm{high}}}.\left(\begin{array}{c} tan[\cos^{-1}(\mathrm{IDF_{min}})] \\ +\frac{2\pi f_{\mathrm{line}} L_f i_{pk,\mathrm{low}}}{v_{pk,\mathrm{high}}} \end{array}\right)}\right] \tag{5}$$

TABLE II
COMPARISON OF DIFFERENT FILM-TYPE DM CAPACITOR VOLUME MODELS

Capacitor Volume Models	*Decision Variables*	*Coefficient of Decision Variables*				*Model Accuracy (%)*
		C [cm³/μF]	*V* [cm³/V]	*CV²* [cm³/(μF·V²)]	*Const.* [cm³]	
Model 1	CV^2, Constant	-	-	5.597×10^{-5}	1.49	96.49
Model 2	V, CV^2, Constant	-	5.853×10^{-3}	5.608×10^{-5}	1.63	96.98
Model 3	C, CV^2, Constant	1.646	-	4.941×10^{-5}	1.305	97.80
Model 4	C, V, CV^2	2.186	3.01×10^{-3}	4.668×10^{-5}	0	98.01

IV. VOLUMETRIC OPTIMIZATION OF DM AND CM FILTER STAGES

From the DM filter design approach presented in the previous section it is evident that the *LC* filter component values are decided from the required DM noise attenuation level. But there are multiple possible combinations of filter inductor (L_D) and capacitor (C_D) that can attain the same attenuation at a certain design frequency f_D. This uncertainty calls for choosing the optimized L_D and C_D values, which will lead to the minimum DM filter volume because the DM filter contributes to most of the EMI filter stage weight and volume. It is proven that for multistage DM filter the volume will be minimum if the *L–C* component values of all the stages are kept the same [13]. Considering that, to minimize the total DM filter volume, the quantitative cost function models for the volumes of the per-stage inductors and capacitors are required. In the proposed filter volume optimization method, the filter components (*L*, *C*) are considered lossless as they contribute to minimal portion of the total power loss in the three phase PFC converter. The thermal management volume as well as the system dimension are largely decided by the total power loss, which mostly occurs in the power stage components including the switching devices, boost inductors, etc. Due to low power loss per component, forced convection alone can be sufficient to establish a thermal equilibrium in the EMI filter stage of the converter. Thus, designing the EMI filter under the smallest volume using our proposed process is often not influenced by the existing or required thermal management system or the dimension of the converter power stage.

Though in general practice, the filter inductor or capacitor volume is considered to be proportional to the stored energy, a more accurate volumetric cost function model while accounting for other combination of system variables is necessary to carry out the filter optimization task. In this article, we have compared four different regression models of the filter capacitor volume considering different combinations of the chosen decision variables, i.e., rated voltage (*V*), capacitance (*C*), a scaled factor of the stored energy (CV^2), and a constant factor; as shown in Table II. For example, in model 4, the capacitor volume is approximated as

$$V_c = k_c \cdot C + k_c' \cdot V + k_c'' \cdot C \cdot V^2 \tag{7}$$

where the coefficients k_c, k_c', and k_c'' describe the proportionality of capacitor volume with the capacitance, the rated voltage, and the stored energy, respectively. After preparing an archive of commercially available film type X-capacitors datasheets of 310, 400, and 530-Vac voltage ratings from different manufacturers, a complete dataset is generated to fit the models using the variance minimization method. This process outputs the value of the coefficients k_c, k_c', and k_c'' or any constant factors, mentioned in Table II. It is found that if the capacitor volume model is built with all the three decision variables (*C, V, and* CV^2), the model accuracy turns out the highest. Thus, model-4 is found to be the most precise fit for the filter capacitor volume quantification, as shown in Fig. 7.

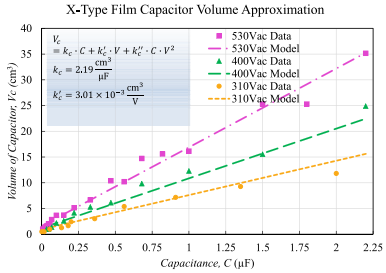

Fig. 7. Proposed DM capacitor volume model: Model 4.

TABLE III
COMPARISON OF DIFFERENT TOROID CORE DM INDUCTOR VOLUME MODELS

Capacitor Volume Models	*Decision Variables*	*Coefficient of Decision Variables*				*Model Accuracy (%)*
		L [cm³/mH]	*I* [cm³/A]	*LI²* [cm³/(mH·A²)]	*Const.* [cm³]	
Model 1	LI^2, Constant	-	-	0.285	0	91.93
Model 2	L, LI^2, Constant	0	-	0.259	3.18	94.07
Model 3	I, LI^2, Constant	-	0.311	0.246	1.125	94.79
Model 4	L, I, LI^2, Constant	0.91	0.38	0.237	0.36	95.66

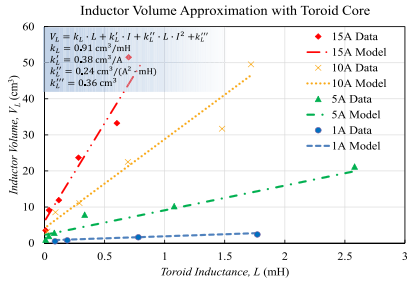

Fig. 8. Proposed DM inductor volume model: Model 4.

In a similar fashion, the toroidal core filter inductor volume is also modeled in four different ways, as can be found in Table III. It is found that the filter inductor volume can be best modeled as

$$V_L = k_L \cdot L + k_L' \cdot I + k_L'' \cdot L \cdot I^2 + k_L''' \tag{8}$$

where k_L, k_L', k_L'', and k_L''' are the coefficients of the inductance (*L*), rated current of the designed inductor (*I*), the scaled factor of the stored energy (LI^2), and a constant factor, respectively. The percentage accuracies of the different filter inductor volume models conclude that while the inductor volume majorly depends on the stored energy, its inductance and the rated current also have significant effects on its volume. Thus, in this work, we have approximated filter inductor volume using model 4 (the best fit candidate), as graphically depicted in Fig. 8.

Considering the DM filter components of each filter stage to be equal (i.e., $L_{DM1} = L_{DM2}$; $C_{DM1} = C_{DM2}$, and $L_{D1} = L_{D2} = L_D$; $C_{D1} = C_{D2} = C_D$), the total volume of the DM filter for N_f filter stages can be expressed as

$$V_{f,DM} = 3 \cdot (V_{L_{DM}} + V_{C_{DM}}) \cdot N_f \tag{9}$$

where $V_{L_{DM}}$ and $V_{C_{DM}}$ are the volumes of each L_{DM1} and each C_{DM1}, respectively, which can be expressed similarly as done in (7) and (8). To attain minimum filter volume, $V_{f,DM}$ is to be minimized with a constraint of the required level of attenuation as shown in (6). The DM *LC* filter (Fig. 5) attenuation considering N_f filter stages can be expressed as

$$\mathrm{Att}_{DM}(f_D) = (2\pi f_D)^{2N_f} \cdot (L_D \cdot C_D)^{N_f}. \tag{10}$$

Assuming the CM filter capacitances (C_{CM}) do not contribute much to the C_D because of their lower value in general, C_D can be assumed to be $C_{DM}/2$. Similarly, ignoring the contribution of the leakage inductance of the CM choke in DM inductance, L_D can be represented as $L_{\mathrm{D}} = 2L_{DM}$. Considering these, total DM filter attenuation of (10) becomes

$$\mathrm{Att}_{DM}(f_D) = (2\pi f_D)^{2N_f} \cdot (L_{DM} \cdot C_{DM})^{2N_f} \geq Att_{DM,\mathrm{req}}. \tag{11}$$

Minimizing (9) while satisfying the constraints given by (7), (8), and (11) outputs the optimized values of the filter components as

$$L_{DM,\mathrm{opt}} = \sqrt{\frac{\sqrt[N_f]{\mathrm{Att}_{DM,\mathrm{req}}} \cdot (k_c'' V^2 + k_c)}{(2\pi f_D)^2 \cdot (k_L + k_L'' I^2)}} \tag{12}$$

$$C_{DM,\mathrm{opt}} = \sqrt{\frac{\sqrt[N_f]{Att_{DM,\mathrm{req}}} \cdot (k_L'' I^2 + k_L)}{(2\pi f_D)^2 \cdot (k_c + k_c'' V^2)}}. \tag{13}$$

This shows that the optimized values of the DM filter stage components depend on the required amount of attenuation ($Att_{DM,\mathrm{req}}$), number of filter stages (N_f), the rated filter capacitor voltage, and the rated current of the designed filter inductor.

Using (12) and (13), the optimized volume of the whole DM filter can be expressed as

$$V_{f,DM,\mathrm{opt}} = 3N_f \left(k_L' I + k_C' V + k_L'''\right) + 6N_f \sqrt{\frac{\sqrt[N_f]{Att_{DM,\mathrm{req}}} \cdot (k_c'' V^2 + k_c) \cdot (k_L + k_L'' I^2)}{(2\pi f_D)^2}}. \tag{14}$$

In order to validate this proposed filter volume optimization method, a design effort is made to optimize the DM EMI filter of a 2.3-kW three-phase boost PFC converter switching at 100 kHz (f_{sw}), as discussed in Section III. With the following available information ($\mathrm{Att}_{DM,\mathrm{req}} = 50$ dB or $10^{\frac{50}{20}} = 316.2$; $f_D = 200$ kHz; $I = 15$ A; $V = 310$ Vac) and using the governing equations (12)–(13), the DM filter *LC* components can be synthesized for a given number of filter stage. However, filter stage count should also be incorporated within the volumetric optimization problem, so that global minima of filter volume can be reached for an optimum synthesized design space (N_f^*, C_{DM}^*, L_{DM}^*).

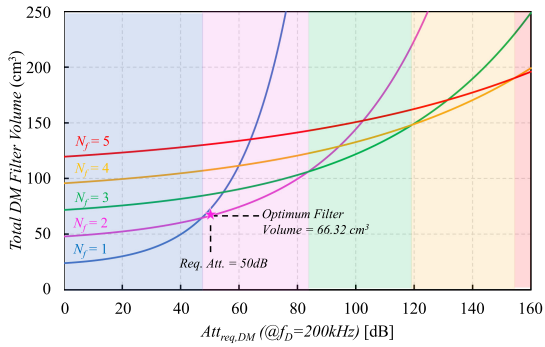

Fig. 9. Optimized DM filter volume for varying attenuation requirements ($\mathrm{Att}_{\mathrm{req},DM}$) and different number of filter stages (N_f).

To study the dependency of DM filter volume ($V_{f,DM,\mathrm{opt}}$) on N_f, a characterization study is performed between $V_{f,DM,\mathrm{opt}}$ and the required attenuation ($\mathrm{Att}_{\mathrm{req},DM}(f_D)$), at a design frequency of 200 kHz while sweep ing N_f from 1 to 5. Fig. 9 shows the optimal DM filter volume as a function of attenuation requirement ($Att_{\mathrm{req},DM}$) for different number of filter stages (N_f). It can be concluded that the optimum number of filter stage increases in steps, as the attenuation requirement becomes more stringent. Furthermore, Fig. 9 also suggest that a two-staged DM filter will be the best choice for our design targeting minimum volume.

Table IV depicts the optimized DM EMI filter component values as per our requirement for different filter stages using (12)–(13). We hereby consider the maximum tolerable displacement angle for the PFC as 5°, which imposes a constraint on the total allowable DM filter capacitor per phase and per filter stage ($C_{D,\max}$) and thereby limits the sample size of C_{DM} in the volume optimization technique. It is clear from the data presented in the table that for a 50-dBμA attenuation requirement at 200-kHz design frequency, the minimum DM filter volume is obtained as 66.32 cm^3, if a two-staged filter is employed with *L-C* values of 37.2 μH and 302.7 nF.

Results from the proposed volumetric minimization procedure are also presented through DM filter volume and attenuation surface plots in Fig. 10. The volume surfaces are built depending on the developed inductor and capacitor volume models using an extensive dataset, shown in (7) and (8). It can be found that all the (L_{DM}, C_{DM}) combinations that satisfy the 50-dBμA attenuation requirement are present on the parabolic periphery on the attenuation surface. Looking from this analysis perspective, we find the optimal (L_{DM}, C_{DM}) cross-section point using the color map, which indicates the minimum possible DM filter volume to be 66.3 cm^3 for $N_f = 2$ in our design.

The CM filter stage of the power converter can be optimized similarly as done for the DM stage with the help of the mathematically derived volumetric models of the filter components. The CM *LC* filter (Fig. 6) attenuation considering N_f filter stages needs to be higher than the required attenuation level at the design frequency, which can be expressed as

$$g_1(L_C, C_C, N_f) = \mathrm{Att}_{CM}(f_D) = (2\pi f_D)^{2N_f} \cdot (L_C \cdot C_C)^{N_f} > \mathrm{Att}_{CM,\mathrm{req}} \tag{15}$$

TABLE IV
OPTIMIZED DM FILTER COMPONENT VALUES FOR DIFFERENT NUMBERS OF FILTER STAGES

f_{sw}	f_D	$Att_{req(DM)}$	N_f	$L_{DM,opt}$[1]	$C_{DM,opt}$[1]	$V_{f,opt}$	L_D or $2L_{DM,opt}$	C_D or $C_{DM,opt}/2$	Total allowable $C_{D,max}$ *	Allowable $C_{DM,opt(max)}$ or $2{\cdot}C_{D,max}/N_f$	Total Displacement Angle
(kHz)	(kHz)	(dB)		(μH)	(nF)	(cm^3)	(μH)	(nF)	(μF)	(μF)	(°)
100	200	50	1	156.9	1276.6	72.15	313.8	638.3	2.63	5.26	1.16
100	200	50	2	37.2	302.7	66.32	74.4	151.4	2.6	2.6	0.55
100	200	50	3	23.0	187.4	85.63	46.1	93.7	2.592	1.728	0.51
100	200	50	4	18.1	147.4	107.77	36.2	73.7	2.59	1.295	0.54

[1]LDM and CDM are optimized for an inductor current rating and capacitor voltage rating of 15 A and 310 Vac respectively.
*Total allowable $C_{D,\max}$ is calculated based on the maximum displacement angle of 5°, $v_{pk,\text{high}}$ & $i_{pk,\text{low}}$ of 384 V and 4.3 A, respectively.

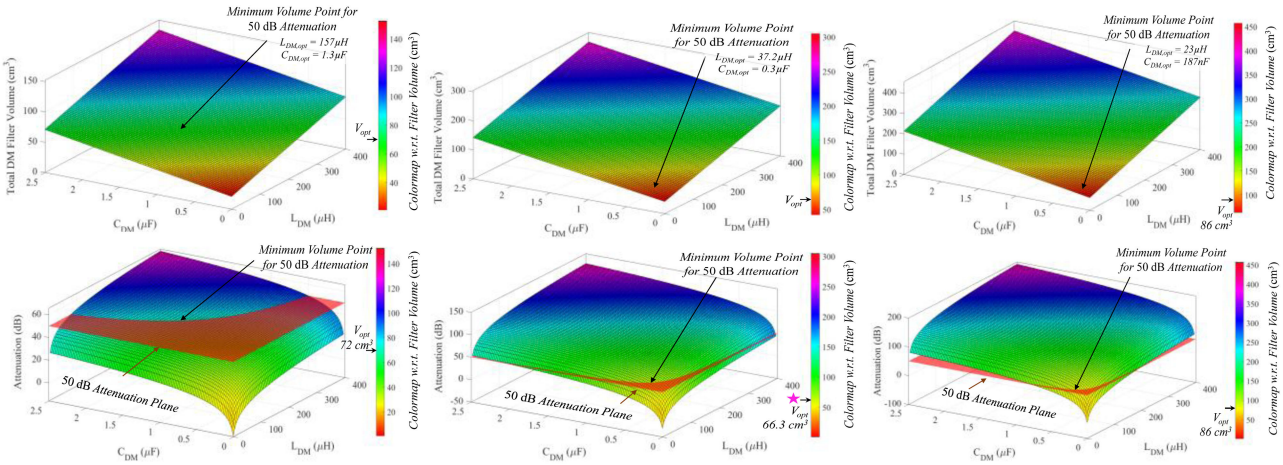

Fig. 10. DM filter volume and attenuation surface plots obtaining minimum filter volume points for different filter stages. (a) $N_f = 1$. (b) $N_f = 2$. (c) $N_f = 3$.

where $C_C = C_{C1} = C_{C2}$ and $L_C = L_{C1} = L_{C2}$.

While designing the CM filter stage, the maximum allowable leakage current flowing to the earth or converter chassis becomes an important design constraint. Due to the safety reasons, the maximum value of protective conductor current, as specified in the regulation IEC 60990, will limit the total CM capacitance in the following way: $C_{CM,\max} = \frac{I_{\text{leak},\max}}{2\pi f_{\text{grid}} V_{ph-ph}}$, where f_{grid} is the grid frequency; V_{ph-ph} is the phase-to-phase rms voltage; $I_{\text{leak},\max}$ is maximum leakage current allowed. Under a selection of "N_f" stage volume optimized *LC* filter, each CM capacitor needs to follow the constraint, shown as follows:

$$g_2\ (C_{CM}) = C_{CM} - \frac{C_{CM,\max}}{N_f} < 0. \tag{16}$$

The cost function to be minimized is the total CM filter volume, expressed as: $V_{f,\,CM} = f\,(C_{CM},\ L_{CM},\ N_f) = 3 \cdot (V_{L_{CM}} + V_{C_{CM}}) \cdot N_f$, where inductor and capacitor volumes have been modeled earlier as function of filter elements and current/voltage ratings. Using the method of Lagrange multipliers, we formulate the following Lagrangian function:

$$L\ (C_{CM},\ L_{CM},\ N_f,\ \lambda_1, \lambda_2) = f\,(C_{CM},\ L_{CM},\ N_f) - \lambda_1 . g_1\,(L_{CM},\ C_{CM},\ N_f) - \lambda_2 . g_2\,(C_{CM})\,. \tag{17}$$

For global minimization, any direction perpendicular to all gradients of the constraints is also perpendicular to the gradient of the function. Another way, we can state that the directional derivative of the function is 0 in every feasible direction. The method generalizes readily to functions on five variables: $\nabla_{C_{CM},\ L_{CM},\ N_f,\ \lambda_1, \lambda_2} L\ (C_{CM},\ L_{CM},\ N_f,\ \lambda_1, \lambda_2) = 0$, which amounts to solving five equations in five unknowns, resulting in the optimal solution set for the CM filter *LC* parameters and optimum number of stages. Results from the proposed volumetric minimization procedure leads to an optimized two-staged CM filter for our design with filter parameter values of $C_{CM} = 3.9\ nF$ and $L_{CM} = 1.76\ mH$.

Finally, summarizing the proposed unified approach for a constrained design optimization of a three-phase front-end EMI filter, a comprehensive flowchart is presented in Fig. 11.

V. EXPERIMENTAL RESULTS

For concept validation purpose, a laboratory prototype of a 2.3-kW three-phase boost PFC converter integrated with the EMI filter stage for avionics application is designed, developed, and tested. The employed EMI filter stage, as shown in Fig. 3, is comprised of two *LC* filter stages ($N_f = 2$) with optimized DM components values, fetched from Table IV.

Figs. 12 and 13 show the simulated DM (from 150 kHz to 5 MHz) and CM (from 3 to 25 MHz) EMI spectrums of the converter integrated with the filter circuit, respectively. The simulated spectrum stays below the DO-160F conducted EMI

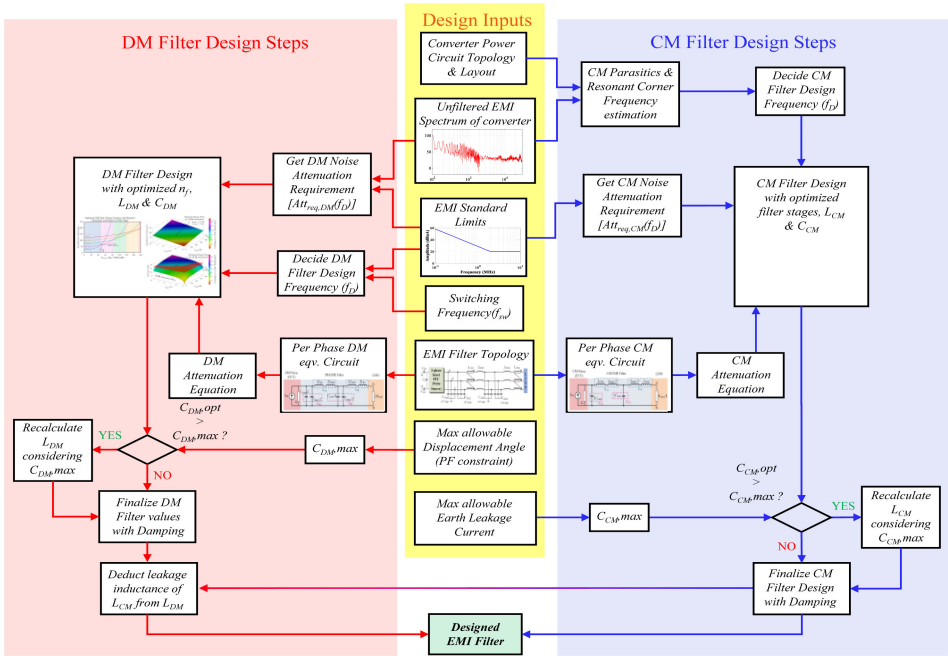

Fig. 11. DM and CM EMI filter design steps shown in a flowchart.

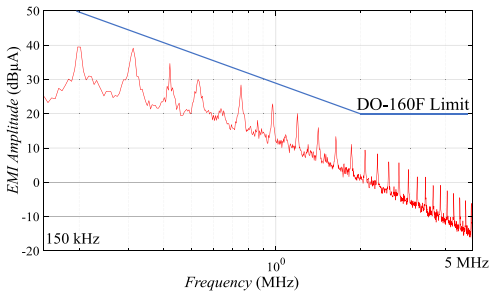

Fig. 12. Simulated DM noise spectrum after filtering action.

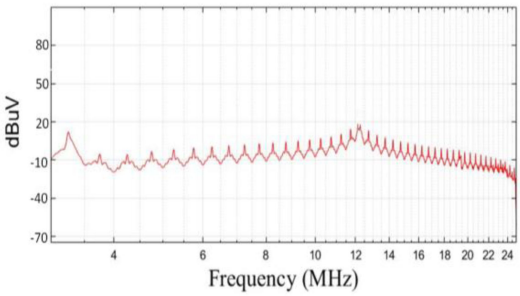

Fig. 13. Simulated CM EMI spectrum with filtering action.

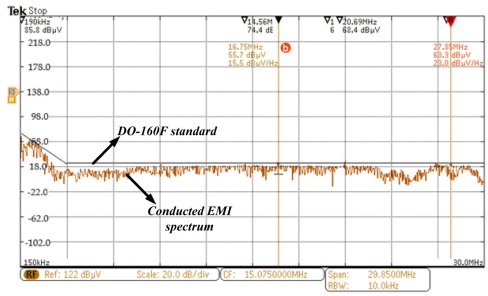

Fig. 14. Hardware EMI spectrum satisfying DO-160F EMI standard.

standard while maintaining a margin of over 3 dB, thus verifying the EMC compliance. Furthermore, the experimentally obtained conducted EMI performance of the converter, integrated with the filter stage, is demonstrated in Fig. 14 for the whole spectrum range from 150 kHz to 30 MHz. The result establishes the EMI performance to satisfy the DO-160F standard within its whole frequency range.

To verify the usefulness of the proposed volume optimization technique, we present a comparison between the designed filter stage with other state-of-the-art (SOA) counterparts for three-phase PFC conversion in Table V. The comparison data suggest that our designed filter has been able to achieve a 12.12% and 10.53% less volume than the filters reported in [14] and [15], respectively, which upholds the benefits of utilizing our proposed volume-optimized filter design procedure. Moreover, the total volume of our employed DM filter components is measured as 61.45 cm^3, which was predicted through our volumetric model to be 66.31 cm^3. Therefore, this proves the accuracy of the proposed DM filter volume estimation model.

Fig. 15 represents the experimental waveforms for the input phase currents i_A, i_B, phase "A" voltage $v_{A\text{-}n}$, and the output dc link voltage v_{DC} of the designed PFC-EMI integrated stage. An input power factor of 0.998 and a THD of 4.1% are measured from the reported results. The power conversion efficiency of the combined EMI and PFC stage is measured as 98.92%, whereas the standalone EMI stage efficiency is 99.7%.

TABLE V
COMPARISON OF DESIGNED EMI FILTERS FOR THREE PHASE BOOST PFC

EMI Filter Designs	*Component*	*Value*	*Quantities*	*Specs*	*DM Filter Component Volume* (cm^3)		*Total EMI Filter Board Volume* (cm^3)
					Predicted	*Measured*	*Measured*
[11]	X-capacitor	0.22µF	3	Film capacitor, 530V AC	68.9 cm^3	–	–
	Y-capacitor	4.7nF	7	Film capacitor, 330V AC			
	CM Choke	1.4mH	2	W409 core, Iron based; Bmax = 1.2T			
	DM Choke	400µH	1	T90 core (90% Tungsten)			
[12]	X-capacitor	0.33µF	6	X2 Film capacitor, 310Vac	69.56 cm^3	67.92 cm^3	203 cm^3
	Y-capacitor	4.7nF	6	Y Film capacitor, 310Vac			
	CM Choke	1.5mH	2				
	DM Choke	70µH	6				
Our Design	X-capacitor	0.33µF	6	X2 Film capacitor, 310Vac	66.31 cm^3	61.45cm^3	158 cm^3
	Y-capacitor	3.9nF	6	Y Film capacitor, 310Vac			
	CM Choke	1.76mH	2				
	DM Choke	37µH	6				

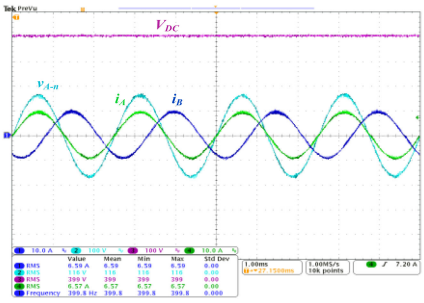

Fig. 15. Waveforms of the 3-phase active boost PFC converter integrated with EMI Stage: $V_{DC} = 400$ V; $V_{A\text{-}n} = 115$ V (rms); $P_{\text{out}} = 2.3$ kW.

VI. CONCLUSION

This work presents a rigorous and comprehensive procedure for the EMI filter design for any power converter with a primary example of a three-phase boost PFC rectifier unit used in avionics applications. To optimize the overall filter volume, the article mathematically demonstrates a volume optimization technique of the DM and CM EMI filter based on the derived volumetric models of the filter components – inductor (L_D) and capacitor (C_D). This analysis shows the filter volume primarily depends on the noise attenuation requirement (Att_{req}), the design frequency (f_D), the number of filter stages (N_f), the rated voltage for C_D, and the rated current for L_D. The unfiltered EMI spectrum of any power stage would give the required attenuation profile and hence the noise attenuation criteria at the design frequency, based on which the filter parameters are selected and then optimized while satisfying the design constraints. Therefore, due to the generic nature, the proposed filter design optimization strategy can be applied to any power converter topology with modified design constraints, according to the converter application and design demand.

Based on our analysis, for a given DM noise attenuation requirement of 50 dB, a globally optimized DM filter for our PFC converter with $N_f = 2$ will have a total volume of 66.31 cm^3, whereas an intuitive design with $N_f = 1$ and $N_f = 3$ will lead to a volume of 72.15 and 85.63 cm^3, which are 8.8% and 29.1% higher than the optimized result, respectively. Extension of the proposed volume minimization method to the CM filter stage leads to an optimized two-staged CM filter for our design with filter parameter values of $C_{CM} = 3.9$ nF and $L_{CM} = 1.76$ mH. Thus, the application of our volumetric optimization technique results in the total EMI filter board volume of 158 cm^3, which is 22.1% less than reported in the existing literature. Experimental measurements of conducted EMI spectrum are performed with a proof-of-concept of 2.3-kW ac–dc active boost PFC-EMI integrated stage operating at 100-kHz switching frequency, which exhibits a thorough compliance with the conducted EMI standard DO-160F while maintaining a sufficient margin. The volumetric comparison of the designed filter with similar SOA filters for the same application, reported in the literature, shows a clear advantage of the proposed multiobjective optimization technique. With the proposed EMI solutions, the PFC converter maintains an efficiency of 98.92% with an input power factor of 0.998, hence signifying a good power quality.

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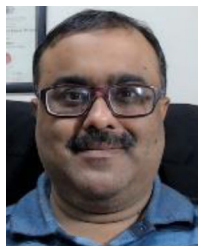

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