Letters

A High-Power Step-Up DC/DC Converter Dedicated to DC Offshore Wind Farms

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***Abstract*—In this letter, a high-power step-up dc/dc converter dedicated to dc offshore wind farms is proposed, with the combination of half-bridge submodules, thyristors, diodes, and transformer. Compared with the other promising dc/dc topologies, the device numbers, costs, losses, and energy storage requirement are greatly reduced. The operation principle is introduced. The effectiveness and validity are confirmed by simulation and experimental results.**

***Index Terms*—DC/DC converter, dc offshore wind farms, diodes, thyristors, soft switching.**

I. Introduction

As ONE of the key renewable energy sources, offshore wind continued its accelerated growth of installed capacity over the last few years, and is of great development potential in the future. It is expected that future offshore wind farm will have an average offshore distance of 100 km and power rating over 1000 MW [1], [2]. The dc offshore wind farm using medium-voltage dc (MVdc) collection and high-voltage dc (HVdc) transmission is regarded as the promising solution for future large-scale system, since it reduces the number and types of equipment as well as the size and footprint of the offshore platform, and it also reduces the cable losses of the collection system [3], [4]. However, a high-power dc/dc converter is indispensable to step up the MVdc voltage and transmit the power to the shore through HVdc cables.

There are many technical hurdles and requirements associated with this dc/dc converter: high power rating (hundred MW), high step-up ratio, large current stress at the MVdc side (tens of kA), high voltage stress at the HVdc side (hundreds of kV), unidirectional power flow, and requirements of compactness and light weight. At MV level, resonant switched-capacitor dc/dc converter with cascaded modules has been extensively investigated [5], but the incremental voltage stress of the switches as well as capacitors and the large resonant current stress hinder its application to high voltage and large power. In [6], series connected thyristors are employed to form a three-phase step-up resonant dc/dc converter (SRdc) with an LCL tank, so as to take advantage of the high power capability of thyristors. But all the components in this circuit have to be rated to withstand both the high current stress of MV side and the high voltage stress of HV side, particularly considering the resonant waveforms with higher peak values, which results in low device utilization rate and high conduction loss. On the other hand, the dc solid-state transformer concept with input series output series connection of dual active bridge has attracted research interest [7]. However, the main problem associated with the dc solid-state transformer when employed beyond MV level is the employment of a massive number of transformers and their onerous requirement for high insulation. This difficulty can be avoided by involving modular multilevel converter based front-to-front dc/dc converters (MMC-FTF) [8], as the requirements of HV level and large power rating can be easily satisfied [9]. However, the semiconductor count and submodule (SM) capacitor size of MMC are very significant, leading to high cost and heavy weight. To reduce the number of semiconductors, a novel dc/dc converter (named as TLC-MMC) is proposed in [10], combining two-level converters in parallel on the MV side and one MMC on the HV side. But the series connection of IGCTs, employment of multiple high-insulation transformers, and the large SM capacitor size would still be the concern.

To tackle the remaining technical challenges, this letter proposes a novel high-power step-up dc/dc converter concept (HSdc), by combining the arm cascaded by SMs with the thyristor and diode valves. As a result, it inherits the merits of low conduction loss and high-power density of the thyristor and diode, and the high controllability of the voltage and current waveforms of the arm. Compared with the topology in [10], HSdc can reduce SM numbers by around 50% since three arms of MMC are replaced by series-connected diodes, meanwhile, the energy storage requirement of SM capacitance is also significantly reduced. Therefore, compactness, light weight, low cost, and high efficiency are the merits of the proposed HSdc.

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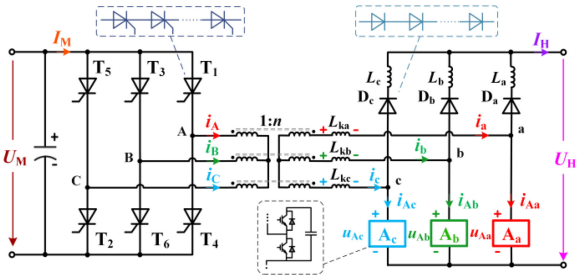

Fig. 1. Circuit configuration of the proposed HSdc.

II. Principle of Operation

A. Circuit Configuration

Fig. 1 depicts the circuit configuration of the proposed HSdc. It consists of top thyristor valves (T_1, T_3, and T_5) and bottom thyristor valves (T_4, T_6, and T_2) in MVdc side, one wye-wye connected 1:n ($n < U_H/U_M$) three-phase transformer and three diode valves (D_a, D_b, and D_c) as well as three arms (A_a, A_b, and A_c) in HVdc side. Each arm is formed by N series-connected half-bridge SMs. The terms U_M and I_M are the voltage and current of the MVdc side, U_H and I_H are the voltage and current of the HVdc side, respectively. L_{kj} and L_j (j = a, b, c) are the leakage inductances of transformer and buffer inductances, respectively.

B. Operation Principle

The sketched operation waveforms of the proposed HSdc are shown in Fig. 2. T_1∼T_6 and D_a∼D_c are sequentially conducted for taking turns to carry I_M and I_H, respectively. Meanwhile, the currents of T_1∼T_6 (i_{T1}∼i_{T6}) and D_a∼D_c (i_{Da}∼i_{Dc}) are shaped as identical but interleaved trapezoid waveforms, which helps synthesize continuous dc currents at both MVdc and HVdc sides, i.e., $I_M = i_{T1} + i_{T3} + i_{T5}$ and $I_H = i_{Da} + i_{Db} + i_{Dc}$, as shown in Fig. 2(b) and (d), respectively. In each operation cycle (T), there are two types of operation stages, i.e., *holding stage* (both thyristor currents and diode currents hold their values) and *commutation stage* (currents of thyristor and diode commutate between two phases). Since, there are six thyristor valves and three diode valves; *commutation stage* appears nine times per cycle. At the end of each *commutation stage*, a *holding stage* is followed, so as to ensure symmetrical three-phase transformer current waveforms. During the *holding stage*, one top thyristor, one bottom thyristor, and one diode are in on-state. An example circuit is shown in Fig. 3(a). The power is directly transferred through transformer to the HVdc side. Meanwhile, to regulate the dc voltage or power, one arm needs to sustain the voltage difference ($U_H - nU_M > 0$) and another arm sustains the current difference ($I_M/n - I_H > 0$). For *thyristor commutation*, the currents are controlled by the arm voltages which produce opposite voltage (U_T) across corresponding leakage inductors L_{kj} of the two phases, as shown in Fig. 2(c). As a result, one thyristor current rises from 0 to I_M, whereas the other falls from I_M to 0 with the same rate. Afterwards, a *holding stage* is followed, in which a negative voltage is imposed across thyristor for a certain time T_q to ensure its reliable turn-OFF. On the other hand, for *diode commutation*, the currents are commutated between the two phases by producing opposite voltage U_D across the buffer inductors L_j, as shown in Fig. 2(e). Besides, during the *commutation stage*, transformer current of the third phase should not be affected. This is realized by appropriately adjusting arm voltage of the third phase, maintaining zero voltage across its leakage inductor. The detailed analysis of the HSdc during [t_0∼t_6] are further described as follows.

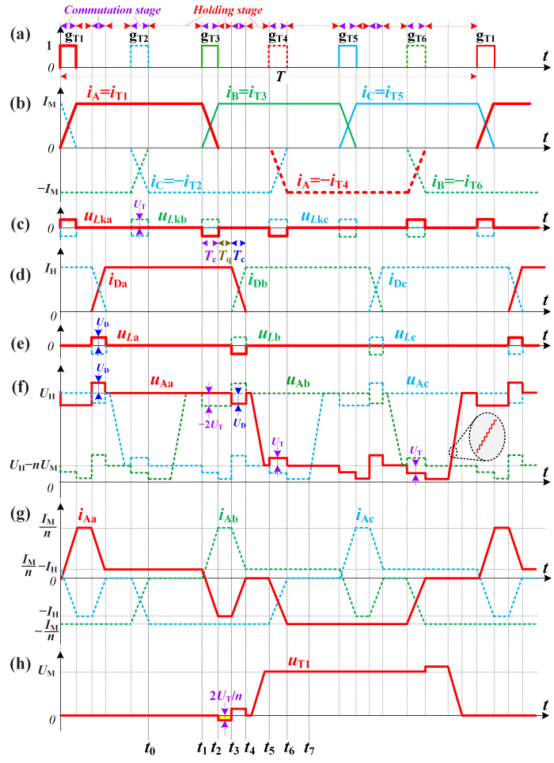

Fig. 2. Principle waveforms of the proposed HSdc. (a) Firing signals of T_1∼T_6. (b) Three-phase transformer currents. (c) Leakage inductor voltages. (d) Diode currents. (e) Buffer inductor voltages. (f) Arm voltages. (g) Arm currents. (h) Voltage of T_1.

Holding Stage I [$t_0 \sim t_1$]: The corresponding circuit is shown in Fig. 3(a). T_1, T_2 and D_a are in on-state. The transformer currents of phase a and phase c are opposite, i.e., $i_a = -i_c = I_M/n$. Meanwhile, i_a mainly flows through D_a forming the HVdc current I_H while A_a would sustain the remaining small current difference $I_M/n - I_H$. On the other hand, as the phase-to-phase voltage u_{ac} should be kept as nU_M, A_c needs to sustain the voltage difference $U_H - nU_M$. Besides, the voltage of A_b (u_{Ab}) is gradually ramped up to U_H to be ready for thyristor commutation. To avoid causing excessive du/dt in thyristors, the SMs are switched sequentially. It is noteworthy that due to $i_b = 0$, zero-current switching (ZCS) for the SMs in A_b is realized.

Thyristor Commutation Stage I [$t_1 \sim t_2$]: As u_{Ab} has been built up to U_H at t_1, the phase-to-phase voltage u_{AB} is zero, hence, T_3 can be softly triggered on with zero-voltage switching (ZVS). Afterwards, as shown in Fig. 3(b), T_1 and T_3 are both in on-state, u_{Ab} is adjusted to $U_H - 2U_T$, resulting in a phase-to-phase voltage of $u_{ba} = -2U_T$. The u_{ba} is shared by the

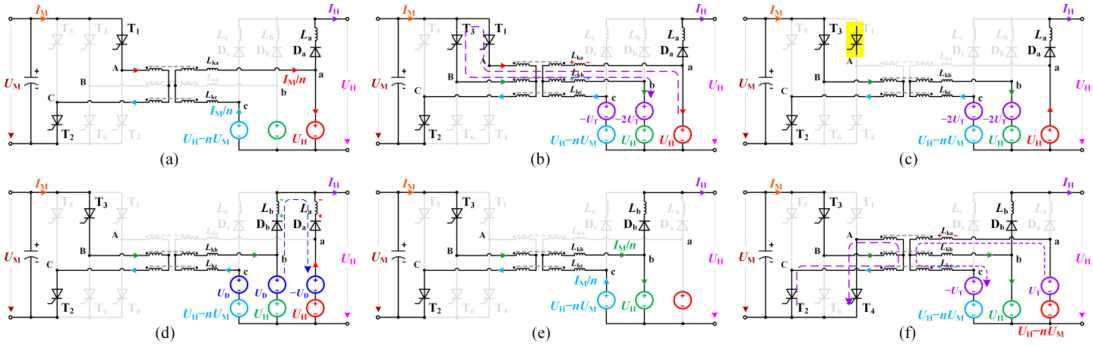

Fig. 3. Current paths of the HSdc during different time intervals. (a) $[t_0 \sim t_1]$. (b) $[t_1 \sim t_2]$. (c) $[t_2 \sim t_3]$. (d) $[t_3 \sim t_4]$. (e) $[t_4 \sim t_5]$. (f) $[t_5 \sim t_6]$.

transformer leakage inductances $L_{\rm ka}$ and $L_{\rm kb}$, which means $u_{L\rm ka} = -U_{\rm T}$ and $u_{L\rm kb} = U_{\rm T}$, respectively. As a result, $i_{\rm T3}$ rises from 0 to $I_{\rm M}$, whereas $i_{\rm T1}$ falls from $I_{\rm M}$ to 0 with the same rate. Meanwhile, $u_{\rm Ac}$ is adjusted to $U_{\rm H} - nU_{\rm M} - U_{\rm T}$ to ensure $u_{L\rm kc} = 0$, so as to hold $i_{\rm T2}$ as constant $-I_{\rm M}$.

Holding Stage II [$t_2 \sim t_3$]: After $i_{\rm T1}$ falls to zero, $u_{\rm ba} = -2U_{\rm T}$ will be retained as a negative voltage for a hold-off time $T_{\rm q}$ to ensure $\rm T_1$ turns OFF reliably, as shown in Fig. 3(c).

Diode Commutation Stage [$t_3 \sim t_4$]: As shown in Fig. 3(d), $u_{\rm Aa}$ and $u_{\rm Ab}$ are adjusted to $U_{\rm H} - U_{\rm D}$ and $U_{\rm H} + U_{\rm D}$, respectively, which produces opposite voltage on $L_{\rm a}$ and $L_{\rm b}$, i.e., $u_{L\rm b} = -u_{L\rm a} = U_{\rm D}$. As a result, $i_{\rm Da}$ falls while $i_{\rm Db}$ rises linearly, and $I_{\rm H}$ remains constant. On the other hand, $\rm A_c$ is adjusted to $U_{\rm H} - nU_{\rm M} + U_{\rm D}$, maintaining zero voltage across $L_{\rm kb}$ and $L_{\rm kc}$, which means the transformer currents $i_{\rm b}$ and $i_{\rm c}$ are not affected.

Holding Stage III [$t_4 \sim t_5$]: As shown in Fig. 3(e), similar to the *holding stage I*, $i_{\rm b}$ and $i_{\rm c}$ are opposite, i.e., $i_{\rm b} = -i_{\rm c} = I_{\rm M}/n$. $\rm A_b$ sustains the small current difference $I_{\rm M}/n - I_{\rm H}$, and $\rm A_c$ sustains the voltage difference $U_{\rm H} - nU_{\rm M}$. $u_{\rm Aa}$ is gradually ramped down to $U_{\rm H} - nU_{\rm M}$ with ZCS of the SMs.

Thyristor Commutation Stage II [$t_5 \sim t_6$]: Similar to the *Thyristor commutation stage I*, $\rm T_4$ is softly turned on with ZVS, since the phase-to-phase voltage $u_{\rm ac}$ is zero at t_5. Afterwards, as shown in Fig. 3(f), $u_{\rm Aa}$ and $u_{\rm Ac}$ are adjusted to $U_{\rm H} - nU_{\rm M} + U_{\rm T}$ and $U_{\rm H} - nU_{\rm M} - U_{\rm T}$, respectively, which produces opposite voltage $U_{\rm T}$ upon $L_{\rm ka}$ and $L_{\rm kc}$, i.e., $u_{L\rm kc} = -u_{L\rm ka} = U_{\rm T}$. As a result, $i_{\rm T2}$ and $i_{\rm T4}$ commutate linearly. After $i_{\rm T2}$ falls to zero, $u_{\rm ca} = -2U_{\rm T}$ will be retained as a negative voltage to ensure $\rm T_2$ turns OFF reliably. Due to symmetry of the waveforms, the analyses of the other time durations are not repeated here.

From the abovementioned analysis, the ZVS as well as the reliable turn-OFF for $\rm T_1 \sim T_6$ and continuous dc currents ($I_{\rm M}$ and $I_{\rm H}$) are guaranteed with the help of the coordination of three-phase arms. The ZCS for the SMs is realized during the arm voltage ramping up and down processes.

On the other hand, the SM capacitors should tolerate the energy fluctuation (integration of $u_{{\rm A}j} \times i_{{\rm A}j}$) of each arm. Hence, the capacitance of SM capacitors can be derived as

$$C_{\rm SM} \geq \frac{P\left[\left(\frac{U_{\rm H}}{nU_{\rm M}} - 1\right)T + 3\left(T_{\rm c} + T_{\rm q}\right)\right]}{6NU_{\rm C}^2\varepsilon} \tag{1}$$

where P is the transferred power, $T_{\rm c}$ is the commutation time, $U_{\rm C}$ is the rated SM-capacitor voltage, and ε is the relative voltage ripple. From waveforms of the arm voltage and arm current in Fig. 2, it can be observed that when the arm voltage is high, the arm current is relatively small; when the arm current is relatively large, the arm voltage remains small. Hence, energy storage requirement of the SM capacitors is relieved.

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Simulation	Experiment
Power rating P	150MW	2.4kW
HVDC voltage $U_{\rm H}$	400kV	400V
MVDC voltage $U_{\rm M}$	50kV	150V
SM capacitor voltage $U_{\rm C}$	2.2kV	100V
SM number per arm N	216	6
SM capacitance $C_{\rm SM}$	0.58mF	1.88mF
SM voltage ripple ε	±10%	±1.5%
Operation frequency f(=1/T)	150Hz	150Hz
Turns ratio 1:n	1:6.8	1:2
Leakage inductance L_{kj}	10mH	3mH
Buffer inductance L_j	10mH	5.3mH
Commutation time $T_{\rm c}$	300μs	300μs
Hold-off time $T_{\rm q}$	120μs	300μs

III. CASE STUDY AND PERFORMANCE EVALUATION

A. Simulation and Experimental Results

To verify the validity of the proposed HSdc, a simulation rated at 50 kV/400 kV, 150 MW is performed. There are 216 SMs per arm, and the rated SM voltage is 2.2 kV. The turn's ratio of transformer n is 6.8. The fast thyristors KK3500-40[11] are employed whose turn-OFF time is around 50∼70 μs. Hence, the hold-OFF time $T_{\rm q}$ is set as 120 μs with certain margin. More detailed parameters are summarized in Table I. Fig. 4 demonstrates the steady-state waveforms of HSdc. The transformer currents [shown in Fig. 4(b)] and diode currents [shown in Fig. 4(c)] were controlled as identical but interleaved trapezoid waveforms, which synthesizes continuous dc currents $I_{\rm M}$ (3 kA) and $I_{\rm H}$ (375 A), as shown in Fig. 4(a). Meanwhile, during the thyristor commutation and diode commutation between two phases, transformer current of the third phase was not affected. As shown in Fig. 4(c) and (d), when the arm voltage $u_{\rm Aa}$ was held as 400 kV, its arm current $i_{\rm Aa}$ was the small current difference (3 kA/6.8 − 375 A = 66 A), whereas, when $u_{\rm Aa}$ was held as 60 kV (voltage difference 400 kV–6.8 × 50 kV), it carried the transformer current $i_{\rm Aa}$ = –441A. Besides, during $u_{\rm Aa}$ ramping down and up processes, du/dt stress was limited and the SMs were switched with ZCS due to $i_{\rm Aa} = 0$. Moreover, as shown in

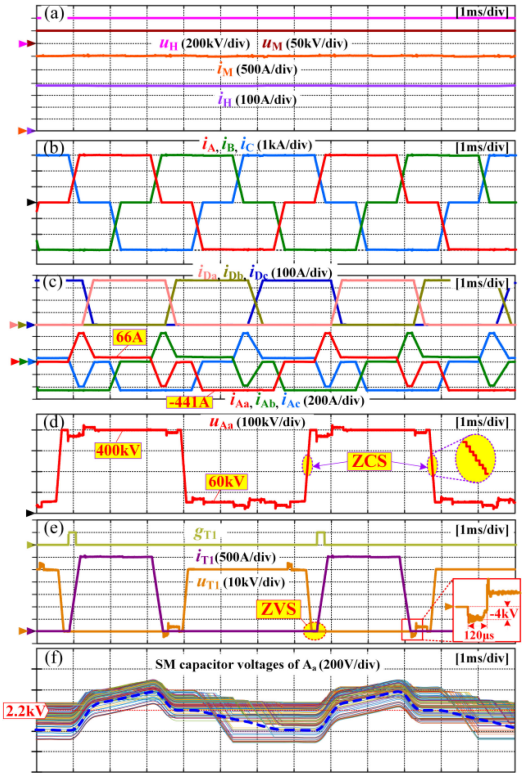

Fig. 4. Simulation results of the proposed HSdc. (a) Voltages (U_H and U_M) and currents (I_H and I_M) of the two dc sides. (b) Transformer currents (i_A, i_B, and i_C). (c) Diodes currents (i_{Da}, i_{Db}, and i_{Dc}) and arm currents (i_{Aa}, i_{Ab}, and i_{Ac}). (d) Voltage of A_a (u_{Aa}). (e) Firing signal (g_{T1}), voltage (u_{T1}) and current (i_{T1}) of thyristor T_1. (f) SM capacitor voltages of A_a.

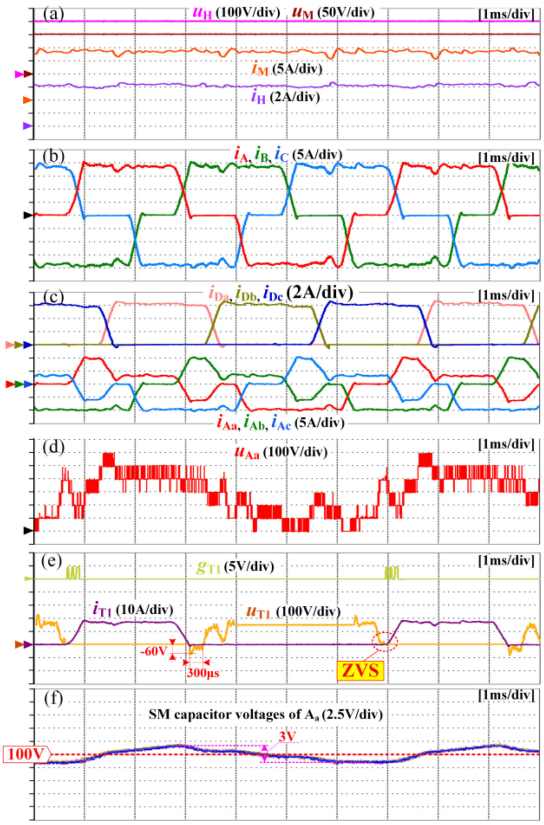

Fig. 5. Experimental results of the proposed HSdc. (a) Voltages (U_H and U_M) and currents (I_H and I_M) of the two dc sides. (b) Transformer currents (i_A, i_B, and i_C). (c) Diodes currents (i_{Da}, i_{Db}, and i_{Dc}) and arm currents (i_{Aa}, i_{Ab}, and i_{Ac}). (d) Voltage of A_a (u_{Aa}). (e) Firing signal (g_{T1}), voltage (u_{T1}) and current (i_{T1}) of thyristor T_1. (f) SM capacitor voltages of A_a.

Fig. 4(e), the thyristor T_1 was turned ON smoothly with ZVS, and after i_{T1} decreased to zero, a negative voltage around -4 kV was applied across T_1 for 120 μs, which ensures its reliable turn-OFF. The 216 SM capacitor voltages of A_a are depicted in Fig. 4(f), which were well balanced around 2.2 kV. It should be mentioned that the average capacitor voltage of these 216 SMs is also shown in Fig. 4(f) by blue dashed line. As can be seen, the relative voltage ripple was kept as $\pm 10\%$, which is coincident with the theoretical analysis value.

Moreover, a downscaled HSdc prototype rated at 150 V/400 V, 2.4 kW has been built and tested to further verify the HSdc concept. There are six SMs per arm and the TT120N16SOF thyristors are employed whose turn-OFF time is 200 μs. The specifications are also listed in Table I. The experimental results are shown in Fig. 5, which is consistent with simulation results. However, since the limited number of SMs, the HSdc generates voltage waveform with much less voltage steps, as shown in Fig. 5(d). As a result, the transformer currents and diode currents are not ideal trapezoids, which exists some visible switching-frequency current harmonics.

B. Comparison With SRDC [6], MMC-FTF [8], and TLC-MMC [10]

For comparison of the proposed HSdc with SRdc, MMC-FTF, and TLC-MMC, the simulation parameters in Table I are selected as a specific case study and the calculated results are listed in Table II. The ABB-5SNA0650J450300 (4.5 kV) IGBTs are employed in the SMs of HV side, whereas the Infineon-D471N90T diodes (9 kV) and ABB-5SDF08H6005 diodes (5.5 kV fast recovery diode) are adopted forming the diode valves of HSdc and SRdc, respectively. For the MV side, the ABB-5SNA3000K452300 IGBT (4.5 kV) and ABB-5SHX26L4520 IGCT (4.5 kV) are selected for MMC-FTF and TLC-MMC, respectively, whereas the thyristors KK3500-40 (4 kV/3.5 kA) are adopted for HSdc and SRdc. To minimize the energy storage requirement, the maximum switching frequency [$f_{s,max} = 1/(6T_q)$] of SRdc is selected as 1388 Hz. Besides, for the MMC-FTF and TLC-MMC dc/dc converters, the power factor is assumed as unity to minimize their current stress. As can be seen from Table II, in terms of the MV-side device, the current stresses are similar apart from SRdc. For the HV-side, the IGBT current stresses of the latter three topologies are also similar, but the diodes current stress of SRdc is much greater than that of HSdc. On the other hand, compared with SRdc, the MV-side device number of the HSdc is reduced to one-eighth. While compared with MMC-FTF and TLC-MMC, no matter for the MV-side or for the HV-side, the device number of the HSdc is lower. Therefore, the total installed device capacity (assessed by device number times current stress and voltage stress) is around 13.9%, 58.9%, and 76.3% of SRdc, MMC-FTF, and

TABLE II
COMPARISON OF HSDC WITH EXISTING DC/DC TOPOLOGIES

Parameters	SRDC	MMC-FTF	TLC-MMC	HSDC
Number, product type and costs of devices in MV-side	1200 (Thy.) KK3500-40 1200×$200	276 (IGBT) ABB-5SNA3000K452300 276×$9918	138 (IGCT) ABB-5SHX 26L4520 138×$4586	**150 (Thy.)** KK3500-40 **150×$200**
Current stress of MV-side device (A)	4720	3353	3142	**3000**
Number, product type and costs of IGBTs in HV-side	–	2592 ABB-5SNA0650J450300 2592×$1685	2592 ABB-5SNA0650J450300 2592×$1685	**1296** 5SNA0650J450300 **1296×$1685**
Current stress of HV-side IGBT (A)	–	419	433	441
Number, product type and costs of diodes in HV-side	876 ABB-5SDF08H6005 876×$976	–	–	**267** Infineon-D471N90T **267×$647**
Current stress of HV-side Diode (A)	3120	–	–	**375**
Total installed device capacity (GW)	18.84	4.43	3.42	**2.61**
Device costs (million $)	1.1	7.1	5.0	**2.4**
Energy storage (kJ/MW)	12.8	18.5	10.0	**6.1**

Notes:
1. The device cost can be searched in "https://octopart.com/" and [11].
2. The voltage derating factor of all the devices is set as 0.5.

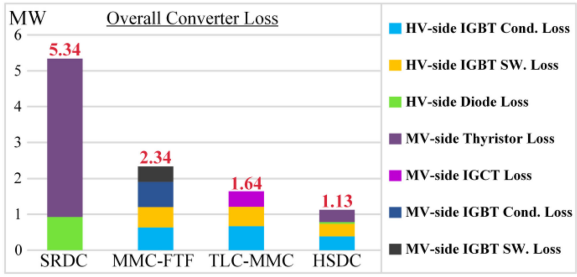

Fig. 6. Loss comparison of HSdc with SRdc, MMC-FTF and TLC-MMC.

TLC-MMC, respectively. Since costs of the thyristor and diode are much lower than IGBT and IGCT, the total device costs of HSdc is around 33.8% and 48% of MMC-FTF and TLC-MMC, respectively. Moreover, the total energy storage of capacitors represented by kJ per MW is also listed in Table II. As can be seen, the energy storage requirement of HSdc is conspicuously reduced, which is an attractive characteristic for the compact and lightweight offshore wind farms application.

On the other hand, the converter losses are evaluated based on the rated parameters and datasheets of the selected devices. Since the HSdc should control the trapezoidal currents, the SM switching frequency of HSdc is set as 330 Hz, whereas the SM switching frequencies of MMC-FTF and TLC-MMC are 200 Hz. The calculated results are shown in Fig. 6. For SRdc, a large number of thyristors results in significant conduction loss (around eight times that of HSdc), and high turn-OFF di/dt (122A/ μs due to the resonant waveform) causes the thyristor reverse recovery loss also considerable (around 1.45 MW). In terms of MMC-FTF and TLC-MMC, the MV side loss of TLC-MMC is lower than that of MMC-FTF due to the soft switching of IGCT. However, the HV side loss is still large. With respect to the proposed HSdc, since the IGBT number is around 50% of TLC-MMC, the conduction loss is reduced around 45%. Meanwhile, the ZCS for the IGBTs of HSDC is realized during the arm voltage ramping up and down processes, resulting in much lower IGBT switching loss than that of TLC-MMC. Moreover, owing to the ZVS and low turn-OFF di/dt (10A/ μs for thyristors and 1.25 A/μs for diodes) as well as the lower on-state voltage drop of thyristors and diodes, their losses are relatively small. Therefore, the overall loss can be reduced by 78.8%, 51.8%, and 31.3% compared to SRdc, MMC-FTF, and TLC-MMC, respectively.

IV. CONCLUSION

Targeted at dc offshore wind farms, a high-power step-up dc/dc is proposed in this letter. By appropriately controlling the arms, commutation of the thyristors and diodes is realized and smooth dc currents are ensured without any filtering effort. The effectiveness is confirmed by both simulation and experimental results. Compared with state-of-the-art dc/dc converters, it shows that the HSdc has the merits of lower cost, lower energy storage requirement, and higher efficiency.

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