Three-Phase Modular Multilevel Converter With Optimized Capacitor Sizing for Low-Voltage Applications

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***Abstract*—High capacitance requirement is a major concern of modular multilevel converters (MMCs) when applied to medium- or low-voltage systems. This article presents the design procedure and development of a modified MMC topology for low-voltage applications. With respect to the conventional MMC topologies, the proposed structure is designed and optimized to have a relatively low capacitance requirement. The switching states, modulation, control, and design procedure of the different parameters, including submodule capacitor and arm inductor, are investigated in this article. Moreover, the control scheme is presented to achieve regulation of the output voltage and the circulating current. The outcomes of this study are verified by simulation and experimental results.**

***Index Terms*—Capacitor voltage ripple, circulating current injection, modular multilevel converter (MMC), multilevel inverters.**

I. Introduction

MULTILEVEL inverters are drawing significant attention due to their smaller filter size [2], lower switching losses[3], reduced electromagnetic interference (EMI) [4], and higher power quality [5], which make them useful for a variety of applications ranging from low-voltage (LV) applications [6], [7] to high-power high-voltage (HV) converters for photovoltaic (PV) and wind power systems [8], [9].

These multilevel topologies are commonly classified into three main groups: neutral-point clamped (NPC), flying capacitor (FC), and cascaded topologies, which is subdivided into modular multilevel converter (MMC) and cascaded H-bridge (CHB) [6].

For LV applications, the FC, NPC, or a derived solution such as T-type NPC are commonly used [10]. Nevertheless, NPC topologies suffer from some drawbacks including the following.

1) NPC topologies with a high number of levels (more than three) are possible, but the complexity and cost is high for LV industrial applications.
2) The losses not only increases with the increasing number of levels but also unevenly distributes between the inner and outer devices as well [6].
3) Overvoltage can appear across the switches, as the switches are not clamped directly to the dc-link capacitors. Therefore, the stray inductance (due to the long commutation loops) can limit the operation in case of high current or high variation of current (di/dt).

In order to increase the efficiency, enhance the reliability, and reduce EMI, MMC with several submodules (SMs) can be used for LV applications in order to share the voltage using lower rated components. As each SM of the MMC can be realized with a capacitor in parallel with a series connection of two switches, the stray inductance can be minimized even using a standard and relatively cheap module assembly.

Despite the aforementioned merits of the MMCs, there are a set of challenging issues, the main ones include the following:

1) higher control complexity;
2) need of balancing the SM capacitors voltage requiring increased control complexity if each SM is controlled by a separate unit and the communication is required with the central unit;
3) higher SM capacitance compared to other multilevel converter topologies; for example, according to [11], the SM capacitor occupies two-thirds from the SM overall size.

The MMC has been proposed recently for LV systems [12]–[16]. Analysis for a five-level Si MOSFET-based MMC is presented in [12]–[14] as an alternative to the two-level insulated gate bipolar transistors (IGBT)-based converter for LV dc distribution networks. Moreover, experimental results, provided in [16], show that the efficiency of the MOSFET-based MMC can be further improved by connecting devices in parallel. In [15], a detailed study for the different possible approaches, that can be used to reduce the required capacitance, is provided.

The most crucial issue with the MMC is the high amount of required capacitance. There are many solutions, proposed in the literature, to reduce the needed amount of capacitance either by control or hardware approaches [1], [17]–[26].

Regarding the control solutions, the voltage oscillation of the capacitors can be reduced by injecting a fixed or an optimized [18] amount of second-order harmonics in the

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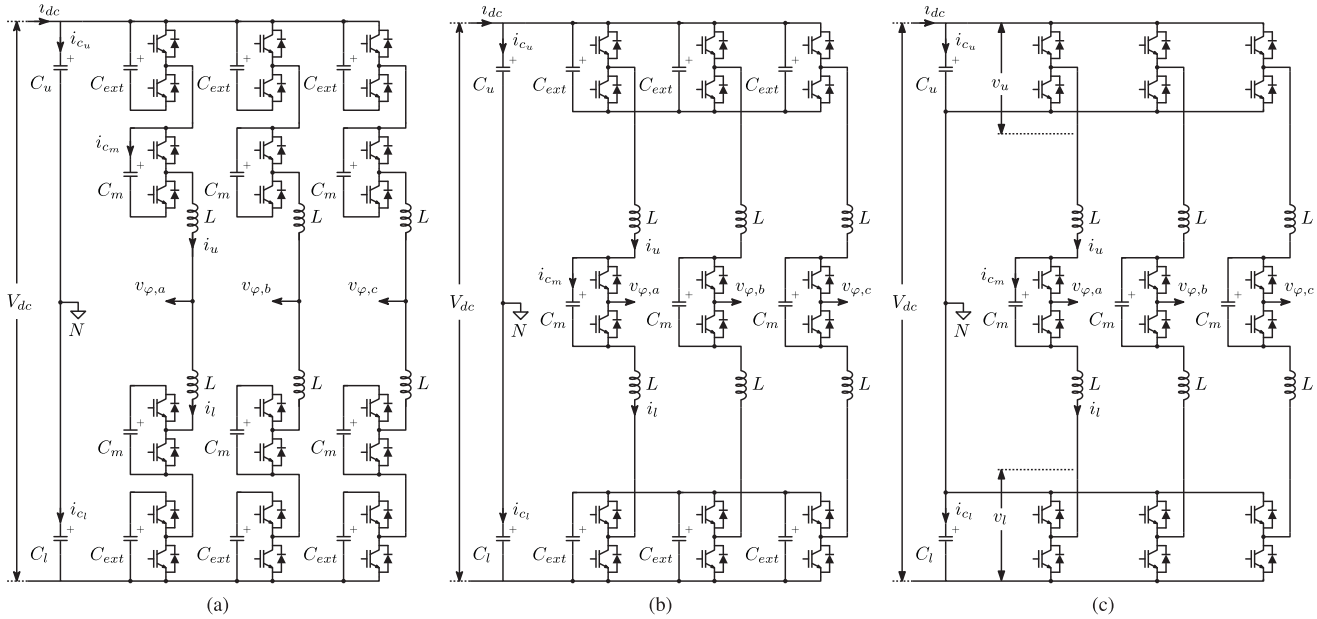

Fig. 1. (a) Conventional three-phase MMC with two SMs per arm. (b) Modified three-phase MMC proposed in [1] with two SMs per arm and a middle SM. (c) Proposed three-phase three-level MMC.

circulating current. The second-order circulating current reference can be generated online from the instantaneous values of the output current and the modulation signal [20]. As the injection of the circulating current affects the efficiency, its amplitude can be optimized as a tradeoff between voltage ripple reduction and efficiency improvement [21]. Beside the voltage boosting capability, full-bridge SMs give more capabilities to further reduce the ripple due to the negative voltage state [25] but with additional cost and size. Circulating current injection can eliminate only the first-order component of the capacitor voltage in case of half-bridge SMs. However, with full-bridge SMs, the second-order component can also be eliminated [23], which has a substantial contribution to the voltage ripple. Furthermore, third-order harmonic voltage injection can contribute to the voltage ripple reduction [27].

On the other hand, modifications to the topology can reduce the total amount of capacitance. An MMC structure with a middle SM can reduce the number of SMs of a three-phase MMC by three (one in every phase) [19] for the same number of output voltage levels. The approach proposed by [1] can further reduce the capacitance by connecting the external SM from each arm in every phase of a three-phase converter to the corresponding SMs in the other two phases. However, the circulating current control and its effect on the capacitance sizing are not well discussed. The proposed MMC structure in [24] reduces the required capacitance but with a significant increase in the component count and control complexity. An additional full-bridge SM in the ac side, proposed in [22], can reduce the voltage ripple by redistributing the power between the SMs.

This article proposes a modified MMC converter topology for LV systems, that is applicable for low, medium, as well as high power. The proposed topology (a filed patent [28]) reduces the number of components, and the capacitance requirement as well, for the same number of output voltage levels. In particular, a three-level configuration is analyzed and compared with the recent state-of-the-art MMC structures. Moreover, the tradeoff between the minimum rms value of the arm current (maximum efficiency) and the minimum capacitance size is discussed. Experimental results using a laboratory-scale prototype are provided to demonstrate the validity of the proposed topology.

The rest of this article is structured as follows. Section II introduces the proposed MMC structure, its principle of operation, and the used modulation scheme. Experimental results are presented and discussed in Section IV. Finally, Section V concludes this article.

II. Principle of Operation, Modulation, and Steady-State Analysis of the Proposed MMC Converter

A. Proposed MMC Structure

A three-phase three-level MMC is reported in Fig. 1(a). The dc bus voltage ($V_{\rm dc}$) is assumed to be fixed. Each leg of the MMC has two arms (an upper arm and a lower arm) with two SMs per arm. Each SM, in the half-bridge MMC variant, comprises two IGBT units connected in series, and a capacitor. The upper and the lower arms of the same leg are coupled to an output ac terminal of the leg through the inductance (L). The arm voltage is controlled by bypassing or inserting the SM's capacitor into the circuit.

Moreover, the direct current, supplied by the converter's dc link, splits equally into the three phases. The alternating current also splits equally into the upper and the lower arms of each phase. The number of levels of the output voltage of a three-phase inverter is three if phase voltage to neutral is considered, or five, if the line voltage is considered.

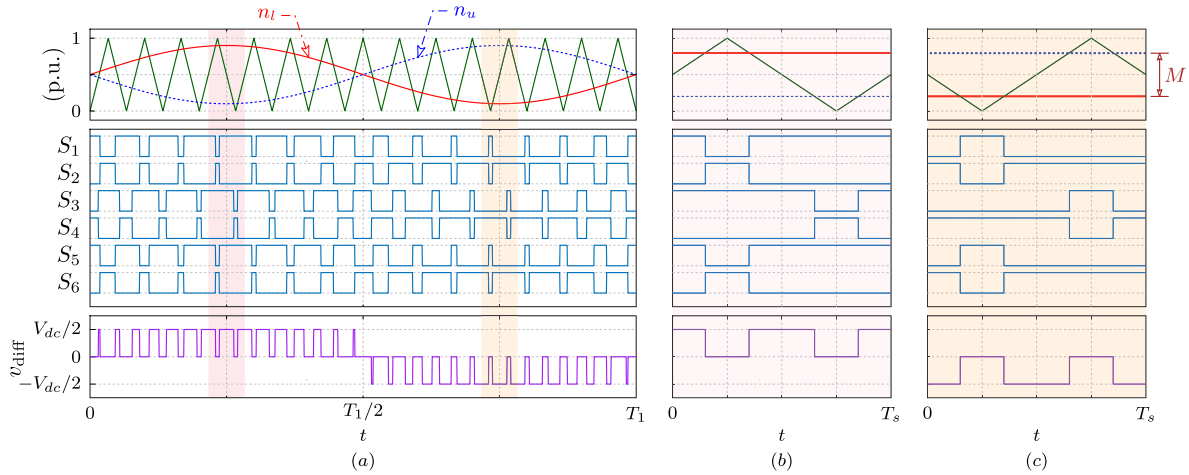

Fig. 2. Modulation technique for the proposed MMC topology. (a) Reference, carriers, gate signals for switches S_1 to S_6, and the resultant differential voltage (v_{diff}). (b) Zoom for one switching cycle when v_{diff} is positive. (c) Zoom for one switching cycle when v_{diff} is negative, where $v_{\text{diff}} = v_l - v_u$.

In order to reduce the SM capacitance, the MMC scheme, shown in Fig. 1(b), is proposed in [1]. Each external capacitor (C_{ext}) in every arm of a phase is connected to the other two corresponding capacitors in the other two phases. Moreover, a middle SM is employed to reduce the required number of SMs/arm by one. The idea of employing a middle SM is originally proposed by [19]. The sum of the three currents is flowing through the external capacitors; therefore, the pulsating current is reduced. This proposed solution can significantly reduce the required capacitance of the external SM of each arm. However, the capacitance reduction obtained from those solutions does not make the MMC a feasible solution for an LV application, where still high capacitance relative to the existing topologies, such as FC and NPC, is required.

Motivated by the aforementioned challenges, a three-phase three-level MMC structure, shown in Fig. 1(c), is proposed in this article. Each leg is composed of three SMs, namely, an upper, a lower, and a middle SM.

The three upper SMs are supplied from the dc-link capacitor (C_u). Similarly, the three lower SMs are connected to the dc-link capacitor (C_l). This feature is very advantageous for three-phase four-wire ($3\Phi - 4\,W$) systems. In this way, the two bulky dc-link capacitors, usually already present in $3\Phi - 4\,W$ systems, are inherently integrated into the structure. The adoption of the proposed MMC structure allows a significant reduction in the number of components and the overall converter size.

It is worth mentioning that the reduction of the capacitance requirements and the number of components either of the modified or the proposed MMC come at the expense of the converter redundancy and modularity, where the optimum choice depends on the application requirements. Moreover, increasing the number of levels beyond three by increasing the number of SMs in each arm is possible; however, each extra SM requires very large capacitance compared with the upper, lower, and middle SMs.

The topology variation between the proposed Fig. 1(c) and 1(b) implies a different converter operation, as outlined hereafter.

TABLE I
SWITCHING STATES OF THE PROPOSED MMC TOPOLOGY

Switching State	S_1	S_2	S_3	S_4	S_5	S_6	v_{diff}	i_{c_m}
P_1	**1**	**0**	**1**	**0**	**1**	**0**	$\frac{V_{dc}}{2}$	$-i_\varphi/2$
P_2	0	0	1	0	1	0		$-i_\varphi$
P_3	1	0	1	0	0	0		0
O_1	0	0	0	1	1	0	0	0
O_2	0	1	1	0	0	0		0
O_3	**1**	**0**	**0**	**1**	**1**	**0**		$i_\varphi/2$
O_4	**0**	**1**	**1**	**0**	**0**	**1**		$-i_\varphi/2$
O_5	0	0	1	0	0	1		$-i_\varphi$
O_6	1	0	0	1	0	0		i_φ
N_1	**0**	**1**	**0**	**1**	**0**	**1**	$-\frac{V_{dc}}{2}$	$i_\varphi/2$
N_2	0	0	0	1	0	1		0
N_3	0	1	0	1	0	0		i_φ

B. Modulation

The phase-shifted carriers (PSCs) modulation technique is the most suitable for the MMC with a low number of SMs/arm [29]. The carriers driving the SMs of the same arm are π phase shifted. The two carriers of the upper arm are $\pi/2$ phase shifted from the corresponding ones of the lower arm [29].

The modulation technique used to drive the three SMs in each arm, for the proposed structure, is driven from the PSCs modulation, as shown in Fig. 2. Two π-shifted reference signals are used. The first one is used to drive the upper and the lower SMs, while the other one is used to drive the middle SM.

C. Switching States and Gate Signal Generation

Table I and Fig. 3 show the different possible switching states of the proposed MMC. The circulating current can be controlled using the upper and the lower SMs; therefore, the switching

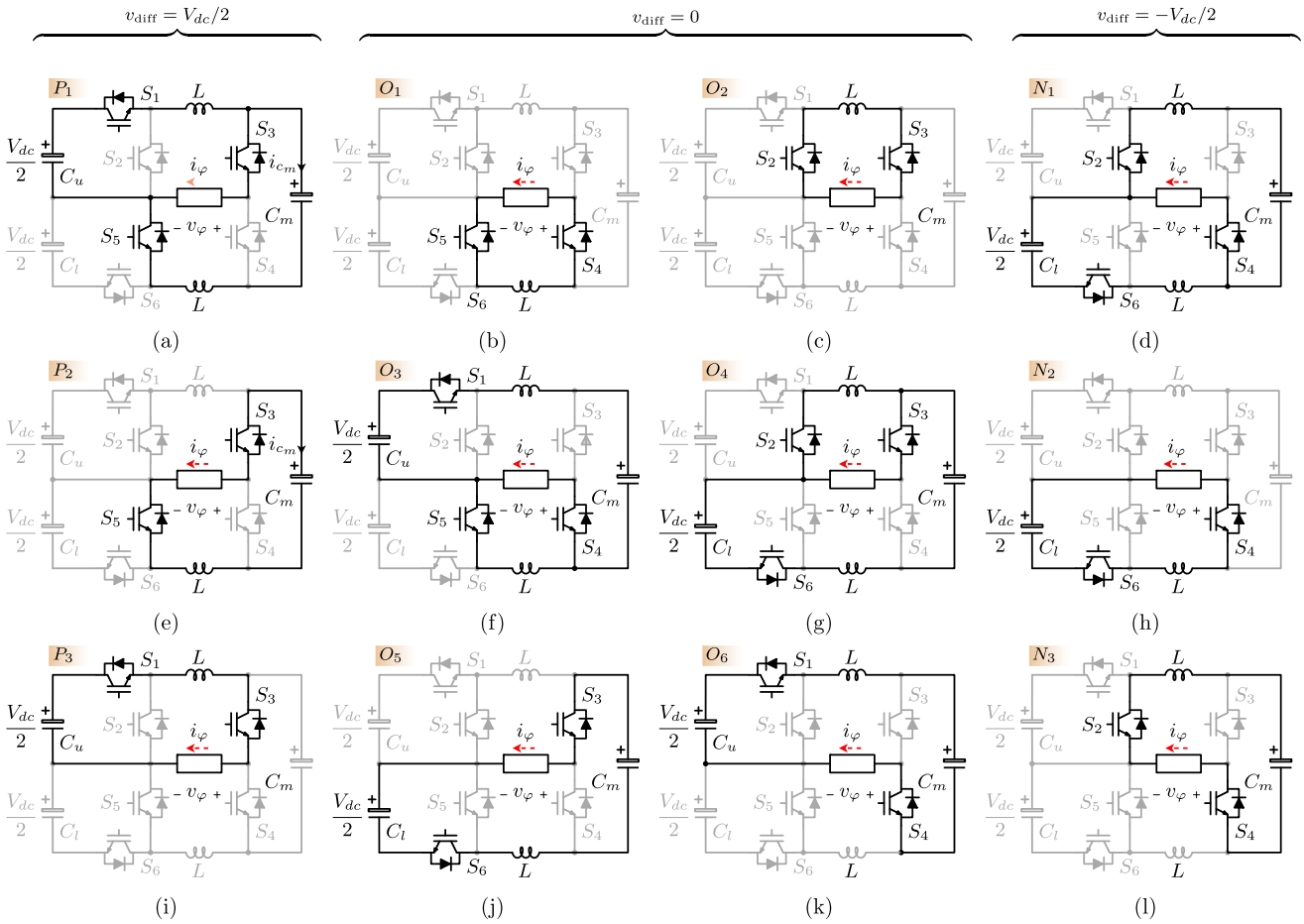

Fig. 3. Switching states of the proposed three-level MMC.

states, in which S_1 and S_2 or S_5 and S_6 are both OFF, are avoided. Accordingly, the highlighted switching states in Table I are chosen. In order to generate an output phase voltage (v_φ) of $+V_{\text{dc}}/2$, the switches S_1, S_3, and S_5 are turned ON, while S_2, S_4, and S_6 are turned OFF, as shown in Fig. 3(a). The zero level can be obtained by either turning ON S_2, S_3, and S_6, or turning ON S_1, S_4, and S_5, as shown in Fig. 3(g) and (f), respectively. For a negative level ($-V_{\text{dc}}/2$), the switches S_2, S_4, and S_6 are turned ON, while S_1, S_3, and S_5 are turned OFF, as shown in Fig. 3(d).

The generation of the gate signals for the six switches in each phase is shown in Fig. 4. The common-mode differential voltage reference (v^*_{com}) is used to control the common-mode circulating current, as discussed later in this section.

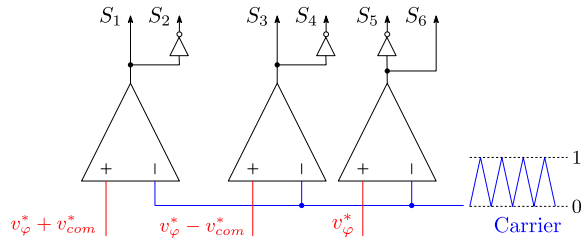

Fig. 4. Gate signal generation for the six switches in each phase. Note that v^*_φ is the differential phase voltage reference, while v^*_{com} is the common-mode voltage reference.

D. Low-Frequency Analysis and Design Procedure

Assuming a balanced three-phase system, the output phase voltages of the MMC ($v_{\varphi,a}, v_{\varphi,b}, v_{\varphi,c}$) are expressed by

$$\begin{bmatrix} v_{\varphi,a} \\ v_{\varphi,b} \\ v_{\varphi,c} \end{bmatrix} = \frac{MV_{\text{dc}}}{2} \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - 2\pi/3) \\ \cos(\omega t + 2\pi/3) \end{bmatrix} \tag{1}$$

where ω is the line angular frequency and M is the modulation index.

The output phase currents are expressed by

$$\begin{bmatrix} i_{\varphi,a} \\ i_{\varphi,b} \\ i_{\varphi,c} \end{bmatrix} = \hat{i}_\varphi \begin{bmatrix} \cos(\omega t - \varphi) \\ \cos(\omega t - 2\pi/3 - \varphi) \\ \cos(\omega t + 2\pi/3 - \varphi) \end{bmatrix} \tag{2}$$

where φ is the load power factor angle, and $\hat{i}_\varphi$ is the peak value of the phase currents.

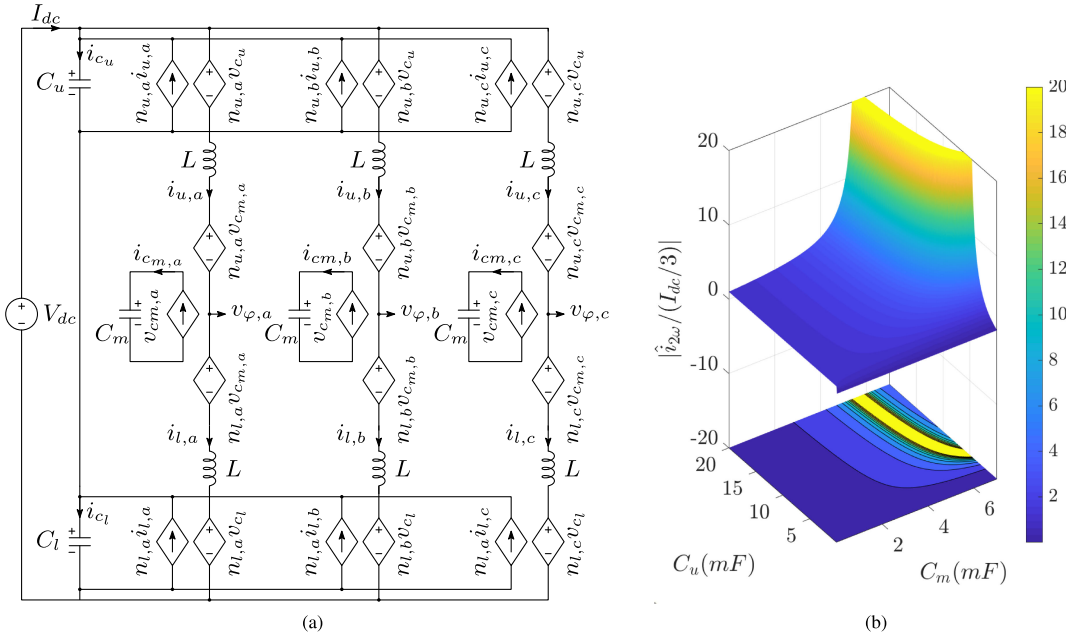

Fig. 5. Low-frequency analysis for the proposed three-phase MMC topology. (a) Average model. (b) Relative amplitude of the second-order component of the circulating current as a function of the SMs capacitance.

In order to generate the output voltages in (1), the insertion (modulation) indices of the upper arm SMs (n_u) and the ones of the lower arm (n_l) are calculated from

$$\begin{bmatrix} n_{u,a} \\ n_{u,b} \\ n_{u,c} \end{bmatrix} = \frac{1}{2} - \frac{M}{2} \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - 2\pi/3) \\ \cos(\omega t + 2\pi/3) \end{bmatrix}$$
$$\begin{bmatrix} n_{l,a} \\ n_{l,b} \\ n_{l,c} \end{bmatrix} = \frac{1}{2} + \frac{M}{2} \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - 2\pi/3) \\ \cos(\omega t + 2\pi/3) \end{bmatrix}. \tag{3}$$

The output phase current is split equally between the upper and the lower arms. Therefore, the upper arm currents and the lower arm currents are composed of two terms: a differential current, which is half the output phase current, and a common-mode one (i_{circ}), circulating through the converter.

Accordingly, the upper arm currents ($i_{u,a}, i_{u,b}, i_{u,c}$) and the lower arm currents ($i_{l,a}, i_{l,b}, i_{l,c}$) can be defined, noting that the circulating currents in the three MMC are negative sequence [30], as

$$\begin{bmatrix} i_{u,a} \\ i_{u,b} \\ i_{u,c} \end{bmatrix} = \overbrace{\frac{I_{\text{dc}}}{3} + \hat{i}_{\text{circ},2\omega} \begin{bmatrix} \cos(2\omega t + \varphi_2) \\ \cos(2\omega t + 2\pi/3 + \varphi_2) \\ \cos(2\omega t - 2\pi/3 + \varphi_2) \end{bmatrix}}^{i_{\text{circ}}} + \underbrace{\frac{\hat{i}_\varphi}{2} \begin{bmatrix} \cos(\omega t - \varphi) \\ \cos(\omega t - 2\pi/3 - \varphi) \\ \cos(\omega t + 2\pi/3 - \varphi) \end{bmatrix}}_{i_\varphi/2} \tag{4}$$

$$\begin{bmatrix} i_{l,a} \\ i_{l,b} \\ i_{l,c} \end{bmatrix} = \overbrace{\frac{I_{\text{dc}}}{3} + \hat{i}_{\text{circ},2\omega} \begin{bmatrix} \cos(2\omega t + \varphi_2) \\ \cos(2\omega t + 2\pi/3 + \varphi_2) \\ \cos(2\omega t - 2\pi/3 + \varphi_2) \end{bmatrix}}^{i_{\text{circ}}} \underbrace{- \frac{\hat{i}_\varphi}{2} \begin{bmatrix} \cos(\omega t - \varphi) \\ \cos(\omega t - 2\pi/3 - \varphi) \\ \cos(\omega t + 2\pi/3 - \varphi) \end{bmatrix}}_{-i_\varphi/2} \tag{5}$$

where I_{dc} is the total dc current drawn from the dc power supply, $\hat{i}_{\text{circ},2\omega}$ is the amplitude of the second-order component of the arm current, and φ_2 is its phase shift.

The term (I_{dc}) is dependent on the power delivered by the inverter, which is the total output power (P_{out}), which can be expressed, under the assumption of unity efficiency, as

$$I_{\text{dc}} = \frac{P_{\text{out}}}{V_{\text{dc}}} = \frac{3M\hat{i}_\varphi}{4}\cos(\varphi). \tag{6}$$

Fig. 5(a) shows the average model of the proposed structure based on the model reported in [31], assuming a relatively high switching frequency.

Applying Kirchhoff's current law at the upper terminal of the capacitor C_u and substituting (3), (4) and (6), the capacitor current (i_{c_u}) and voltage (v_{c_u}) of the upper dc-link capacitor

(C_u) are expressed as

$$\begin{aligned} i_{c_u} &= I_{\text{dc}} - (1-n_{u,a})i_{u,a} - (1-n_{u,b})i_{u,b} - (1-n_{u,c})i_{u,c} \\ &= -\frac{3M\hat{i}_{\text{circ},2\omega}}{4}\cos(3\omega t+\varphi_2) \\ v_{c_u} &= \frac{V_{\text{dc}}}{2} - \frac{M\hat{i}_{\text{circ},2\omega}}{4\omega C_u}\sin(3\omega t+\varphi_2). \end{aligned} \tag{7}$$

Similarly, the capacitor current (i_{c_l}) and voltage (v_{c_l}) of the lower dc-link capacitor (C_l) can be calculated from

$$\begin{aligned} i_{c_l} &= I_{\text{dc}} - (1-n_{l,a})i_{l,a} - (1-n_{l,b})i_{l,b} - (1-n_{l,c})i_{l,c} \\ &= \frac{3M\hat{i}_{\text{circ},2\omega}}{4}\cos(3\omega t+\varphi_2), \\ v_{c_l} &= \frac{V_{dc}}{2} + \frac{M\hat{i}_{\text{circ},2\omega}}{4\omega C_l}\sin(3\omega t+\varphi_2). \end{aligned} \tag{8}$$

From (7) and (8), it can be noted that the capacitor voltage of the upper and the lower SMs, beside the dc component, have only a third-order component that depends on the magnitude of the circulating current ($\hat{i}_{2\omega}$).

The middle capacitor current (i_{c_m}) and voltage (v_{c_m}) are expressed as

$$\begin{aligned} i_{c_m} &= \hat{i}_{\text{circ},2\omega}\cos(2\omega t+\varphi_2) - \frac{M\hat{i}_{\varphi}}{4}\cos(2\omega t-\varphi), \\ v_{c_m} &= \frac{V_{dc}}{2} + \frac{\hat{i}_{\text{circ},2\omega}}{2\omega C_m}\sin(2\omega t+\varphi_2) - \frac{M\hat{i}_{\varphi}}{8\omega C_m}\sin(2\omega t-\varphi). \end{aligned} \tag{9}$$

From the average model shown in Fig. 5(a), the circulating current (i_{circ}) can be calculated from

$$i_{\text{circ}} = \frac{1}{2\,L}\int \left(V_{dc} - n_{u,a}v_{c_u} - v_{c_m} - n_{l,a}v_{c_l}\right) dt. \tag{10}$$

By substituting (3) and (7)–(9) into (10), the amplitude and the phase of the second-order component of the circulating current can be calculated from

$$\hat{i}_{\text{circ},2\omega} = \left[\frac{1}{\left(\frac{M^2}{4}\frac{C_m}{C_u} - 8C_mL\omega^2\right)+1}\right]\frac{M\hat{i}_{\varphi}}{4} \tag{11}$$

$$\varphi_2 = -\varphi \tag{12}$$

where the upper SMs capacitance (C_u) and the lower SMs capacitance (C_l) are assumed to be equal.

Substituting (12) into (7)–(9), the peak-to-peak voltage ripple of the upper (ΔV_{c_u}), the lower (ΔV_{c_l}), and the middle (ΔV_{c_m}) capacitors can be expressed as

$$\begin{aligned} \Delta V_{c_u} &= \Delta V_{c_l} = \frac{M\hat{i}_{\text{circ},2\omega}}{2\omega C_u} \\ \Delta V_{c_m} &= \frac{1}{\omega C_m}\left|\hat{i}_{\text{circ},2\omega} - \frac{M\hat{i}_{\varphi}}{4}\right| \end{aligned} \tag{13}$$

where $|.|$ denotes the absolute value.

TABLE II
RELATIONSHIP BETWEEN THE CIRCULATING CURRENT OF PHASE a AND THE VOLTAGE RIPPLES OF THE DIFFERENT CAPACITORS

$i_{circ,2\omega}$	ΔV
0	$\Delta V_{c_u} = \Delta V_{c_l} = 0$ $\Delta V_{c_m} = \frac{M\hat{i}_{\varphi}}{4\omega C_m}$
$\frac{M\hat{i}_{\varphi}}{4}cos(2\omega t-\varphi)$	$\Delta V_{c_u} = \Delta V_{c_l} = \frac{M^2\hat{i}_{\varphi}}{8\omega C_u}$ $\Delta V_{c_m} = 0$

TABLE III
SPECIFICATIONS OF THE SIMULATED THREE-PHASE MMC CONVERTER

Rated power (S)	30 kVA
Input voltage (V_{dc})	800 V
Output line voltage (V_{φ})	400_{rms} V
Line frequency (f_1)	50 Hz
Switching frequency (f_s)	10 kHz
Arm inductance (L)	240 μH
Upper SM capacitance (C_u)	12 mF
Lower SM capacitance (C_l)	12 mF
Middle SM capacitance (C_m)	300 μF
Output filter capacitance (C_f)	325 μF

From (11) and (13), it can be noted that in the absence of circulating current control, both the arm inductance and the SM capacitance values influence the circulating current, and accordingly, the capacitor voltage ripple. Moreover, a resonance could happen at certain values. Fig. 5(b) shows the relative amplitude of the second-order circulating current as a function of C_u and C_m using the parameters adopted in Table III.

In order to limit the amplitude of the second-order circulating current, it has to be controlled. In this case, its amplitude and phase depend on the adopted control strategy.

According to (13), two extreme cases for the second-order component of the circulating current ($\hat{i}_{\text{circ},2\omega}$) can be identified. On the one hand, if $\hat{i}_{\text{circ},2\omega}$ is controlled to be zero, the peak-to-peak capacitor voltage ripple for the upper and the lower SM capacitors becomes, theoretically, zero, while the one of the middle SM capacitor reaches its maximum. On the other hand, if $\hat{i}_{\text{circ},2\omega}$ is controlled to be $M\hat{i}_{\varphi}/4$, the peak-to-peak capacitor voltage ripple for the upper and the lower SM capacitors reaches its maximum, while the one of the middle SM capacitor becomes, theoretically, zero. From the capacitor requirement standpoint, this is the most interesting solution as the two bulky capacitors at the dc side are already present in $3\Phi - 4\,W$ systems. Table II summarizes the relationship between the circulating current and the voltage ripple. The circulating current can be controlled to

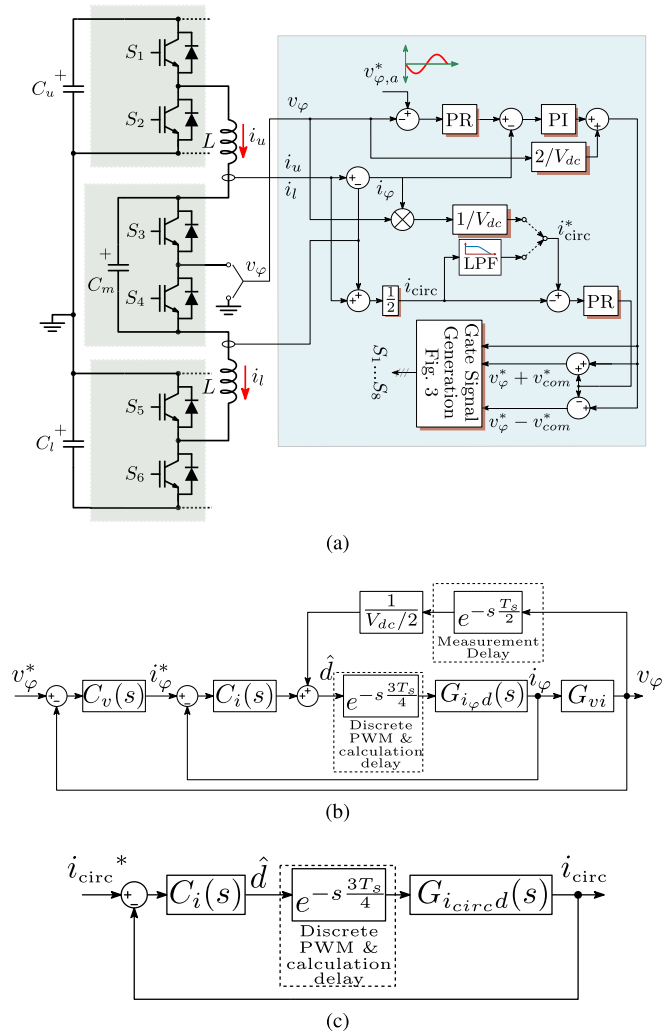

Fig. 6. Closed-loop control diagram for the proposed MMC. (a) Control scheme of the proposed topology. (b) Block diagram for the linearized model of the output voltage loop. (c) Block diagram for the linearized model of the circulating current loop.

achieve an optimum solution for SM capacitance and losses (i.e., the peak value of the arm current).

E. Control Design

Fig. 6(a) depicts the control diagram used to control the output phase voltage and the circulating current control. A single-loop voltage regulator is possible; however, multiloop voltage control with an inner current loop can actively damp the output filter resonance oscillation [32]. Moreover, it provides overcurrent protection during faults or abnormal conditions [33].

1) Output Voltage Control: The voltage control loop includes an inner current loop with a simple proportional-integral (PI) regulator and a feed-forward from the output voltage in order to damp the resonance oscillation. The difference between the upper arm current (i_u) and the lower arm current (i_l) is utilized as a feedback for the inner current loop. The transfer function of the PI regulator is

$$C_{i_\varphi} = k_{p,i_\varphi} + k_{i,i_\varphi}\frac{1}{s} \tag{14}$$

where k_{p,i_φ} and k_{i,i_φ} are the proportional and the integral gains, respectively.

In a stationary reference frame, a simple PI regulator is not enough to eliminate the steady-state error of a sinusoidal reference; therefore, a proportional-resonant (PR) regulator is used with a resonant frequency at the line frequency (f_1). The transfer function of the PR regulator can be expressed as

$$C_{v,v_\varphi} = k_{p,v_\varphi} + k_{r,v_\varphi}\frac{s}{s^2+\omega_1^2} \tag{15}$$

where k_{p,v_φ} and k_{r,v_φ} are the proportional and the resonant gains, respectively. The control parameters are designed according to the linearized model shown in Fig. 6(b).

2) Circulating Current Control: As discussed in Section II-D, the circulating current affects the converter's efficiency and the capacitor voltage oscillation; therefore, it has to be controlled. Similar to the output voltage control, as the PI regulator does not provide enough gain at the double line frequency, a PR regulator in the stationary reference frame with a resonant frequency at $2f_1$ is adopted. The transfer function of the circulating current PR regulator is expressed as

$$C_{i,\text{circ}} = k_{p,\text{circ}} + k_{r,\text{circ}}\frac{s}{s^2+(2\omega_1)^2}, \tag{16}$$

where $k_{p,\text{circ}}$ and $k_{r,\text{circ}}$ are the proportional and the resonant gains, respectively. The control parameters are designed according to the linearized model shown in Fig. 6(c).

As seen in Table II, for maximum efficiency (minimum arm current), the second-order harmonic of the circulating current has to be eliminated. In this case, the voltage ripple of the middle capacitor reaches its maximum. On the other hand, for minimum voltage ripple (less middle capacitance), a second-order harmonic needs to be injected.

The single-phase apparent power can be written as

$$\begin{aligned} S_{\text{ph}} = v_\varphi i_\varphi &= \frac{\hat{v}_\varphi \hat{i}_\varphi}{2}\cos(\varphi) + \frac{\hat{v}_\varphi \hat{i}_\varphi}{2}\cos(2\omega t - \varphi) \\ &= \frac{MV_{\text{dc}}\hat{i}_\varphi}{4}\cos(\varphi) + \frac{MV_{dc}\hat{i}_\varphi}{4}\cos(2\omega t - \varphi). \end{aligned} \tag{17}$$

By substituting (6) and (12) into (4), the circulating current can be rewritten as

$$i_{\text{circ}} = \frac{M\hat{i}_\varphi}{4}\cos(\varphi) + \hat{i}_{\text{circ},2\omega}\cos(2\omega t - \varphi). \tag{18}$$

By inspection of (17), (18), and Table II, it can be noted that the reference current of the circulating current in the second-order injection mode can be generated from the instantaneous value of the single-phase apparent power divided by V_{dc}. If a constant circulating current is required, only a low-pass filter for the circulating current is needed as shown in Fig. 6(a).

III. Simulation Results

A $230\,V_{rms}$30-kVA simulation model with the parameters listed in Table III has been developed to verify the performance of the proposed topology, in which an output voltage control is implemented. Three different conditions are considered for the circulating current control: control disabled; current reference generated from the output phase voltage, as previously discussed in Section II-E2; and constant circulating current. The three case studies are discussed in details in the following.

A. Open-Loop Circulating Current Control

Fig. 7(a) shows the simulation results with a disabled circulating current control. The arm current is mainly composed of a first-order harmonic and a dc component, as well as an uncontrolled second-order harmonic. As discussed before, the magnitude and phase of first-order harmonic are directly related to the output current. However, the magnitude of the second-order component is related to the circuit parameters, i.e., the arm inductance (L), the dc-side capacitance (C_u), and the middle capacitance (C_m). The peak value of the circulating current can be estimated as the sum of the dc-component reported in Fig. 7(a) (i.e., 17.2 A) and the amplitude of the second-order component calculated with (11), where parameters listed in Table III are adopted. An analytical value of 30 A is obtained, which is very close to the results obtained by the simulation (i.e., 29.1 A). It is clear also from the simulation results that the capacitor current of the upper and the lower capacitors is composed mainly of high-frequency components, as well as a third-order harmonic with the amplitude calculated from (7).

B. Circulating Current Injection Control

With an enabled circulating current control, similar results can be obtained by injecting a second-order harmonic where the reference current is generated by (17) divided by V_{dc}. Simulation results for this mode of operation are shown in Fig. 7(b). The reference current can be multiplied by a factor ranging from 0 to 1.0 to have a specific voltage ripple in the middle capacitance. By lowering the amplitude of second-order harmonic, the peak arm current becomes lower, but the voltage ripple in the middle capacitor increases, hence, a larger capacitance is needed.

C. Constant Circulating Current Control

The minimum arm current amplitude is obtained by setting the amplitude of the second-order component to 0. In this case, the voltage ripple of the middle capacitor becomes maximum. Simulation results for this mode of operation are shown in Fig. 7(c). By considering relationship (13), the peak-to-peak voltage ripple is found to be around 155 V. The error between the analytical calculation and the obtained results is only about 2%.

D. Energy Storage Requirement

The middle capacitor's voltage ripple in the modified MMC is higher due to the higher voltage ripple of the external capacitors. For example, with a second-order injection in the circulating current, the load is supplied mostly from the upper arm during the positive half cycle, as shown in Fig. 8; therefore, the external capacitor's voltage ripple of the upper arm is reflected on the middle capacitor's voltage. Similarly, the external capacitor's voltage ripple of the lower arm is reflected on the middle capacitor's voltage during the negative half cycle of the load. As the upper and lower SMs of the proposed MMC is supplied from the dc-link capacitors, the middle capacitor's voltage ripple is minimal.

The MMC's energy storage requirements depend on the amplitude of the second-order component injected in the circulating current. Fig. 9 shows a comparison between the three topologies: the conventional, the modified, and the proposed MMC using a simulation with the same input and output parameters. The capacitor voltage ripple is kept 10% of the average capacitor voltage in all the cases. Fig. 9(a) shows the variation of the required capacitance for the external SMs (C_{ext}), in the conventional and the modified MMC, versus the circulating current injection ratio ($k_{circ,2\omega}$), where $k_{circ,2\omega} = \hat{i}_{circ,2\omega}/(M\hat{i}_{\varphi}/4)$. Fig. 9(b) shows the variation of the required capacitance for the middle SMs (C_m) with the variation of $k_{circ,2\omega}$. According to Table II, which is also applicable for the modified MMC, with the increase of the circulating current injection ratio, the voltage ripple of the capacitors supplying the external SMs increases, while the voltage ripple of the middle capacitors decreases. For the same voltage ripple, the proposed topology requires less middle capacitance compared with the modified one; for example, at $k_{circ,2\omega} = 1$, a capacitance of 63μF is needed in the modified capacitance while a 34μF is required for the proposed one. Fig. 9(c) and 9(d) shows the rms and peak values of the arm currents, respectively. The rms and peak values of the arm currents increase with the increase of $k_{circ,2\omega}$.

The total stored energy, excluding the dc-link capacitors, is taken as a measure of the overall capacitance requirements in the case of the modified and the proposed MMC topologies respect to the conventional MMC. The total stored energy of the three topologies is expressed as

$$\begin{aligned} E_{conv} &= 6\left(\frac{1}{2}C_m\left(\frac{V_{dc}}{2}\right)^2\right) + 6\left(\frac{1}{2}C_{ext}\left(\frac{V_{dc}}{2}\right)^2\right) \\ E_{modified} &= 3\left(\frac{1}{2}C_m\left(\frac{V_{dc}}{2}\right)^2\right) + 6\left(\frac{1}{2}C_{ext}\left(\frac{V_{dc}}{2}\right)^2\right) \\ E_{proposed} &= 3\left(\frac{1}{2}C_m\left(\frac{V_{dc}}{2}\right)^2\right) \end{aligned} \tag{19}$$

where it has been assumed that the bulky dc capacitors are already present in the system and they are not included in the comparison, as present in all three solutions. The reduction of the total stored energy is shown in Fig. 9(e). At constant circulating current ($k_{circ,2\omega} = 0$), a relatively small capacitance is required for (C_{ext}) in the case of the modified MMC; therefore, the reduction achieved by the modified and the proposed MMC topologies respect to the conventional one are close to each

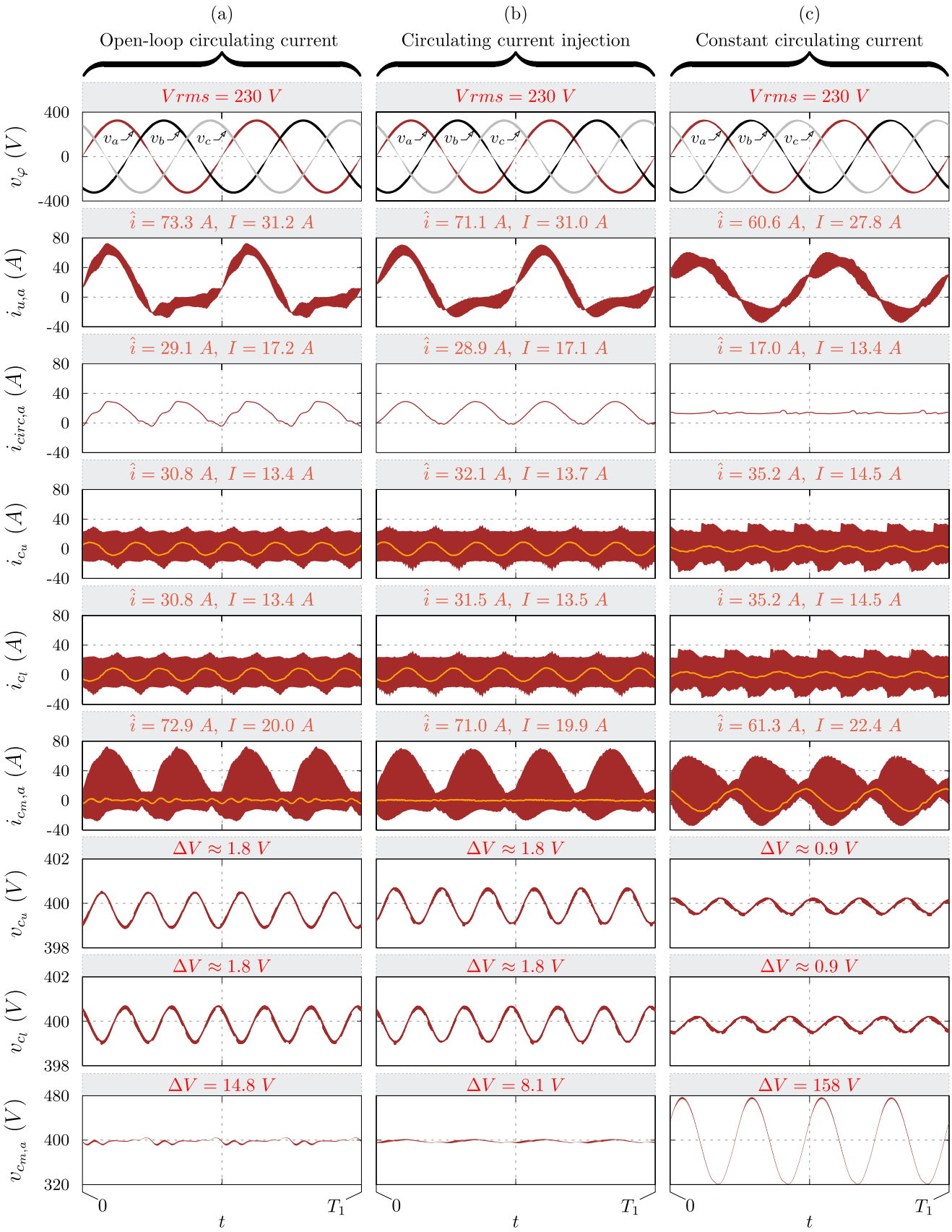

Fig. 7. Simulation results for the proposed topology. Note that ΔV, I, and $\hat{i}$ are the peak-to-peak voltage ripple, the rms current, and the peak current, respectively. T_1 is the fundamental period of the output voltage. The orange waveforms are the low-frequency components.

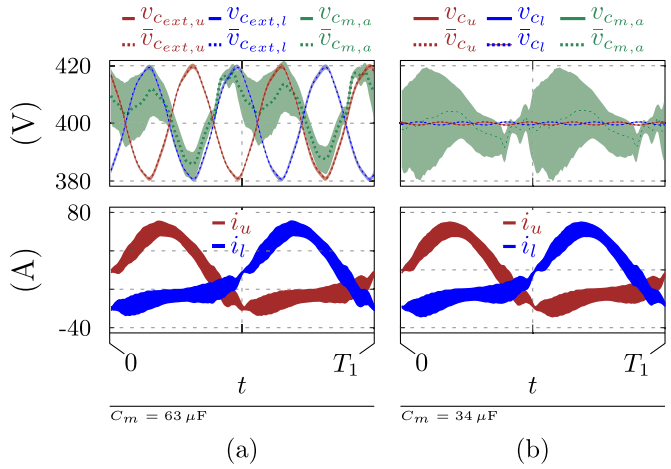

Fig. 8. Comparison between the voltage ripple of the middle capacitor with a second-order injection in the circulating current of (a) modified MMC and (b) proposed MMC.

other (86.7% and 87.3%, respectively). With the increase of $k_{\text{circ},2\omega}$, more capacitance is needed for the external SMs while less capacitance is required for the middle ones. Accordingly, the reduction obtained by the proposed topology becomes more with an increase of $k_{\text{circ},2\omega}$. The obtained reduction of the total stored energy is 90%, at $k_{\text{circ},2\omega} = 1$, concerning the modified MMC and 99.5% with respect to the conventional one. It is worth mentioning that the number of components is also significantly reduced from nine capacitors to three capacitors. Determining a solution that minimizes the capacitance and the rms current (converter losses) requires a tradeoff where the performance indexes are weighted according to a specific application and design requirements.

E. Comparison With State-of-the-Art LV Topologies

The stray inductance of long commutation loops in the three-level topologies such as 3L-NPC, 3L-FC, and T-type impose a practical limitation on application to LV high-current applications. Due to the long commutation loop, potentially destructive HV overshoots appear across the semiconductor devices [34], [35].

The main interesting characteristic of the proposed structure is the smaller commutation loops compared to 3L-NPC, 3L-FC, and T-type. This feature reduces the voltage overshoot over the switches, reduces the converter EMI, and increases the power capability due to the smaller loop inductance. However, it is worthy to compare the number of passive and active components of the proposed topology to the state-of-the-art LV topologies. Table IV shows a comparison between different three-level topologies considering the number of switches, capacitors, inductors, and maximum switch voltage.

The proposed structure requires the same number of semiconductors as the NPC. It should be noted that the switches of the active NPC (ANPC) must be overrated due to the voltage overshoot. One more inductor is required for the proposed MMC; however, these two inductors reduce the input current

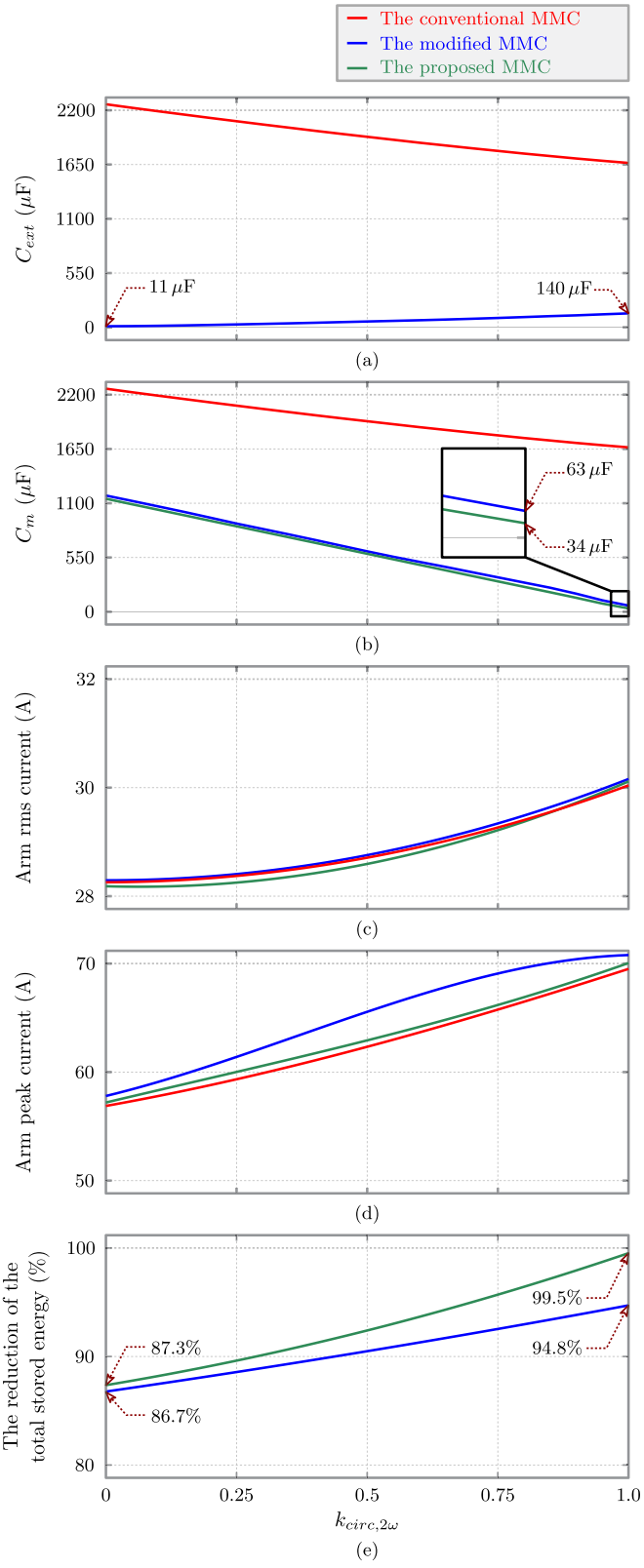

Fig. 9. Comparison between the three topologies: the conventional, the modified, and the proposed topologies. (a) External capacitance (C_{ext}). (b) Middle capacitance (C_m). (c) Arm rms current. (d) Arm peak current. (e) Reduction of the total stored energy of the modified and the proposed topologies respect to the conventional one.

TABLE IV
COMPARISON BETWEEN 3L-ANPC, 3 L T-TYPE, 3L-FC AND THE PROPOSED MMC

	3L T-type	3L-FC	3L-ANPC	Proposed MMC
No. of switches	4	4	6	6
Max. switch voltage	V_{dc}	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
No. of capacitors	2	3	2	3
No. of inductors	1 (61 A_{pk})	1 (61 A_{pk})	1 (61 A_{pk})	2 (43 A_{pk})

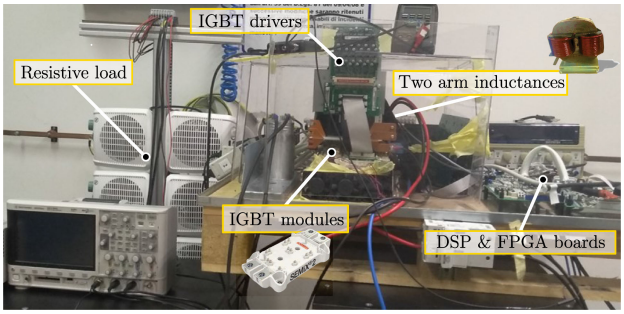

Fig. 10. Picture of the single-phase prototype.

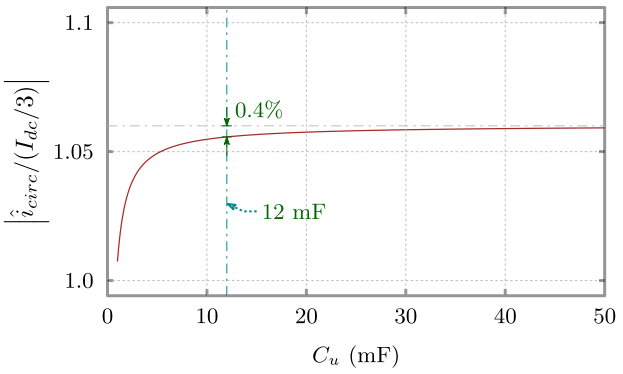

Fig. 11. Relationship between the dc-side capacitance and the relative amplitude of the second-order component of the circulating current.

ripple and limit the current in case of fault. Moreover, the peak current of the arm inductors is lower in the case of the proposed MMC, as shown in Table IV.

IV. EXPERIMENTAL VALIDATION

The experimental setup, aimed at validating the performance of the proposed topology, is shown in Fig. 10. Fig. 11 shows the relationship between the dc-side capacitance and the relative amplitude of the second-order component of the circulating current substituting the simulation parameters in Table V into (11). It can be noted that the effect of increasing the dc-side capacitance, above the 12 mF used in the simulation, is minimal. Therefore, the analysis and simulation results reported in this article can be validated using a single-phase MMC prototype using two fixed dc voltage sources.

An LV single-phase prototype of the proposed MMC converter has been developed to validate the analytical analysis and simulations experimentally. The inverter is supplied with a dc voltage of 800 V and an output resistive load is considered. The parameters are listed in Table V. As shown in Fig. 6(a), the phase includes three half-bridge SMs. Each SM consists of a SEMIKRON SSEMiX402GB066HDs IGBT Module rated at 600 V and 400 A, and a capacitor. Two voltage sources, 400 V each, are used to supply the upper and the lower SMs, while a 300 μF is used to supply the middle one.

TABLE V
SPECIFICATIONS OF THE SINGLE-PHASE MMC EXPERIMENTAL SYSTEM

Input voltage (V_{dc})	600 V
Output phase voltage (V_{φ})	150_{rms} V
Line frequency (f_1)	50 Hz
Switching frequency (f_s)	10 kHz
Arm inductance (L)	240 μH
Middle SM capacitance (C_m)	300 μF
Output filter capacitance (C_f)	325 μF

A DSP-based board is used for implementing the controllers and generating the references and the switching signals for the three SMs, while a field-programmable gate array board is used to generate the switching signals for every single IGBT with an appropriate dead time. The output voltage and the arm currents are measured, sampled, and sent to the DSP board for control and protection purposes.

The three modes of operation, discussed using simulation in Section III, are experimentally validated. The adopted output voltage control is reported in Fig. 6(b). Unlike the simulation results, the voltage of the upper and the lower SMs are fixed as they are directly supplied from the dc supply; therefore, their voltage ripples are negligible. The dc-side capacitance, for dc/ac converters, is mostly designed to have a large capacitance; therefore, the most critical design factor for this topology is the middle capacitor.

The following two test cases are considered: 1) unity load factor where a 25-Ω resistor is utilized, and 2) 0.79 lagging power factor where a 25 Ω in parallel with a 100-μF capacitor are used. Fig. 12(a) shows the experimental results in the case of disabled circulating current control. The voltage ripple of the middle capacitors is close to what is expected from the simulation. Fig. 12(b) shows the experimental results with the controlled constant circulating current. The experimental results with injecting controlled second-order harmonics in the circulating current are reported in Fig. 12(c). The voltage ripple of the middle capacitor, the peak, and rms value of the arm current, and consequently, the converter efficiency are affected by the circulating current control. Fig. 12(d)–(f) shows the experimental results with open-loop, constant, and second-order injection of the circulating current, respectively, at 0.79 load power factor.

The peak-to-peak voltage ripple of the middle capacitor, calculated from (13), is around 43.6 V and 55.4 with the unity and 0.79 lagging power factor, respectively, which are close to the values 47.25 and 57.6 V obtained in Fig. 12(b) and (e).

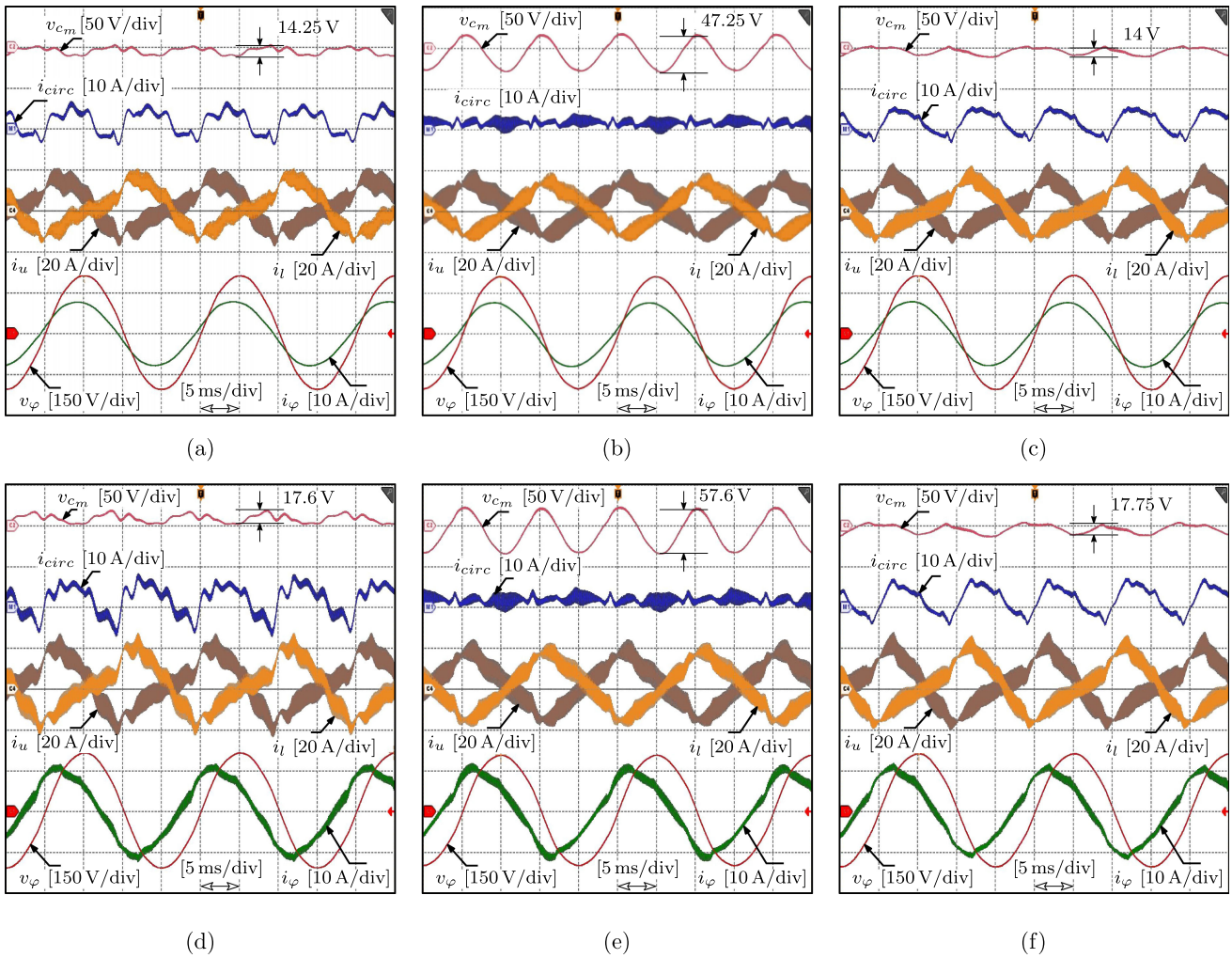

Fig. 12. Experimental results: unity power factor with (a) disabled circulating current control; (b) constant circulating current; (c) second-order circulating current injection; 0.79 lagging power factor with (d) disabled circulating current control; (e) constant circulating current; and (f) second-order circulating current injection.

V. Conclusion

This article has introduced a modified MMC topology for LV applications. The MMC topology is known to be an efficient one for HV applications and some medium-voltage ones. However, the main issue is the large capacitance requirement. Therefore, this article aims to reduce the capacitance requirement while keeping the benefits of the MMC structure. The effectiveness of the proposed topology and the provided analysis and design procedure are confirmed by simulation and experimental results. It is proved that the capacitance requirement of the proposed topology is significantly smaller. Instead of 12 capacitors as in the conventional MMC or nine capacitors as in a modified MMC topology, only three capacitors are needed, if it is assumed that the two bulky dc-link capacitors are already present in the $3\Phi - 4$ W system. Moreover, the middle capacitance is reduced in the proposed topology respect to the modified one (about half in the case of circulating current injection). Furthermore, the operation can be optimized between the two extreme points, that is, the minimum capacitance and the maximum efficiency by proper injection of second-order harmonics in the circulating current.

In the case of injecting a second-order harmonic in the circulating current, excluding the two dc-link capacitors, only three capacitors of 34 μF are needed instead of the 12 capacitors of 2260 μF required in the conventional MMC. Accordingly, the total stored energy is reduced up to 99.5% with respect to the conventional MMC and 90% concerning the modified one.

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