Switching-Cell Buck–Boost AC–AC Converter With Common-Ground and Noninverting/Inverting Operations

Hafiz Furqan Ahmed, Mohamed Shawky El Moursi, *Senior Member, IEEE*, Bashar Zahawi, *Senior Member, IEEE*, Khalifa Al Hosani, *Senior Member, IEEE*, and Ashraf Ali Khan, *Member, IEEE*

***Abstract*—This article proposes a switching-cell-based bipolar buck–boost ac–ac converter that can provide multiple modes of operation, including noninverting buck operation, noninverting boost operation, inverting buck–boost operation, and adjustable noninverting buck–boost operation with two control duty ratios. Each fundamental switching-cell in the proposed converter is composed of a unidirectional buck circuit with no short-circuit or open-circuit problems, increasing its robustness. Hence, safe commutation is naturally realized without the use of *RC* snubbers or soft-commutation strategies, removing the need for pulsewidth modulation deadtimes. External fast recovery diodes are utilized, avoiding the high-frequency conduction of MOSFET's body diodes and eliminating their slow reverse recovery problem and corresponding power loss. The proposed converter shares a common ground between input and output ports, offers support for reactive loads, draws continuous sinusoidal current from ac mains, and delivers a continuous output current. The converter is suitable for ac voltage regulation applications, notably as a dynamic voltage restorer, compensating extensive magnitudes of both grid voltage sags and swells. Circuit operation and analysis are provided for all the proposed modes of operation. Experimental results obtained using a 400-W laboratory-scale hardware verify the theoretical analysis.**

***Index Terms*—AC–AC converter, buck–boost operation, commutation issue, dynamic voltage restorer (DVR), inverting and noninverting operation, switching-cell (SC).**

Manuscript received January 3, 2021; revised April 6, 2021; accepted May 30, 2021. Date of publication June 9, 2021; date of current version August 16, 2021. This work was supported by the Khalifa University of Science and Technology under Award CIRA-2018-37. Recommended for publication by Associate Editor J. C. Clare. *(Corresponding author: Mohamed Shawky El Moursi.)*

Hafiz Furqan Ahmed, Bashar Zahawi, and Khalifa Al Hosani are with the Advanced Power and Energy Center, Department of Electrical Engineering and Computer Science, Khalifa University, Abu Dhabi 127788, UAE (e-mail: furqanhmd164@gmail.com; bashar.zahawi@ku.ac.ae; khalifa.halhosani@ku.ac.ae).

Mohamed Shawky El Moursi is with the Advanced Power and Energy Center, Department of Electrical Engineering and Computer Science, Khalifa University, Abu Dhabi 127788, UAE, and also with the Faculty of Engineering, Mansoura University, Mansoura 35516, Egypt (e-mail: mohamed.elmoursi@ku.ac.ae).

Ashraf Ali Khan is with the Department of Electrical and Computer Engineering, Faculty of Engineering and Applied Science, Memorial University of Newfoundland, St. John's, NL A1C 5S7, Canada (e-mail: ashrafak@mun.ca).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3087811.

Digital Object Identifier 10.1109/TPEL.2021.3087811

I. Introduction

DUE to the integration of renewable energy, growing load diversity, and the presence of a plethora of disturbance sources, the power grid is vulnerable to various voltage volatility issues such as voltage sag/swell, voltage flicker, and three-phase voltage unbalance [1]. AC–AC converter-based series voltage compensators [2]–[5] are a promising solution to provide a stable ac voltage to sensitive electronic equipment and industrial loads, operating under grid voltage disruptions. Fig. 1(a) shows a field-upgradable transformer (FUT) based ac voltage regulator [3], [4], consisting of a modified medium-voltage (MV) distribution transformer with additional low voltage taps (with $\pm$5–10% voltage settings) and a partially rated direct ac–ac converter with a shared terminal between input and output ports. Relays R_1 and R_2 connect the converter inputs to the positive and negative taps ($\pm v_{XN}$), respectively, injecting positive and negative output voltages ($\pm v_{\rm conv}$) in series with the line voltage v_{LN}, and provide secondary-side voltage ($v_{\rm SEC}$) regulation within a typical range of $\pm$5–10%. Fig. 1(b) shows the configuration of a dynamic voltage restorer (DVR) [5] based on a direct ac–ac converter. The converter injects positive and negative series voltages ($\pm v_{\rm conv}$) through tapped-winding (voltage injection) transformer and connection switches S_1, S_2, providing regulation for both grid voltage sags and swells.

Direct pulsewidth modulation (PWM) ac–ac converters [6]–[10] are a preferred choice for grid voltage regulation due to their simple topology/control, smaller size, and single power conversion process without requiring sizeable dc-link capacitors. However, typical buck, boost, and buck–boost ac–ac converters [6]–[10] can produce only noninverting or inverting outputs. Therefore, they require additional negative tapped-windings and connection relays/switches (see Fig. 1) for negative voltage injection. This makes the total size and cost of the system uneconomical [11].

To resolve this, numerous efforts have been devoted to the development of bipolar output ac–ac converters [12]–[18]. Impedance-source (ZS) network-based ac–ac converters [10], [12]–[14] have been proposed with noninverting boost (NIBo) and inverting buck–boost (IBB) voltage capability. However, besides requiring a large number of inductors and capacitors, they are unable to mitigate shallow voltage sags (below 50%) due

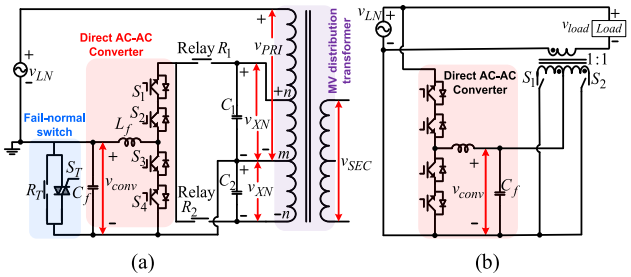

Fig. 1. Series voltage compensators. (a) FUT [3], [4]. (b) DVR [5].

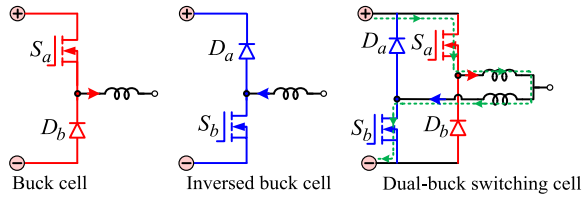

Fig. 2. SC structure [21].

to the unavailability of a noninverting buck (NIBu) operation. A nondifferential ac chopper-based bipolar ac–ac converter has also been proposed [15]. However, this requires eight active switches and provides only voltage buck operation. AC–AC converters with bipolar buck–boost voltage operation have been proposed in [16] and [17]. Nevertheless, the modulation signals and operation of these circuits are somewhat complex. Also, the lack of common-ground sharing between input and output ports makes them unsuitable for application as a FUT [see Fig. 1(a)] while increasing the insulation requirement of the voltage injection transformer for application as a DVR [see Fig. 1(b)] [18]. A unified PWM ac–ac converter was proposed [18] with bipolar voltage operation and a shared common ground between input and output. However, this has discontinuous input and output currents and cannot produce a NIBo output. All of the aforementioned bipolar ac–ac converters [12]–[18] are susceptible to a voltage source short-circuit and/or interruption of inductor current due to switch overlap and deadtimes, respectively, resulting in commutation issues. This decreases their reliability and requires *RC* snubbers or soft-commutation strategies along with PWM switching deadtimes for safe operation, each with its own disadvantages [19], [20].

A switching-cell (SC) structure was proposed in [21] consisting of buck and inversed buck cells connected in parallel, as shown in Fig. 2, which can naturally overcome the voltage source short-circuit problem. SC-based ac–ac converters have been developed [8], [19], [20], [24]–[28] with the following salient features; high robustness with no short-circuit or open-circuit issues, no need of *RC* snubbers or soft-commutation strategies, removal of PWM deadtimes (and related duty ratio loss), and high-quality output voltage/current waveforms. In addition, external fast recovery diodes are used to avoid high-frequency conduction of MOSFET's body diodes and the associated problems of significant reverse recovery loss, EMI noises, and MOSFET damage risk [22], [23]. However, SC-based buck, boost, and IBB ac–ac converters in [8], [19], [20], [24], and [25] have a unipolar output and, therefore, can only compensate a

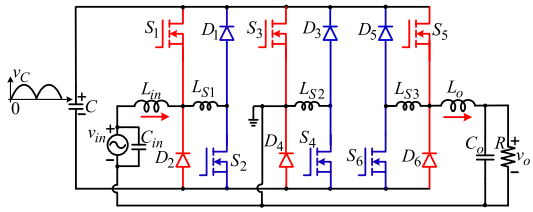

Fig. 3. Proposed SC bipolar buck–boost ac–ac converter.

voltage sag or swell. A high-frequency isolated bipolar SC ac–ac converter was proposed in [26]. However, this can provide only a double-buck operation in which the output voltage is limited to half of the input voltage. A hybrid SC version of a nondifferential ac chopper-based bipolar ac–ac converter [15] was proposed in [27]. But, this provides only voltage buck operation and can, thus, compensate only shallow voltage sags. It also requires twice the inductance of the original circuit in [15], while the input current remains discontinuous. An SC noninverting/inverting ac–ac converter has been proposed [28] with buck–boost voltage capability for application as a DVR. However, this circuit is devoid of NIBo operation, limiting the voltage sag mitigation range to below 50%. It also needs a large number of switching devices and its magnetic utilization is low (only 50%). Moreover, the input current is always discontinuous, while the output current is discontinuous for all modes of operation except the NIBu mode. All of these SC ac–ac converters have floating input and output ports, and thus cannot be used in FUT applications. They also increase the insulation requirement of the voltage injection transformer when employed in DVR applications.

In this article, an SC ac-ac converter is proposed with bipolar buck–boost voltage operations. It combines the functionality of basic NIBu, NIBo, and IBB converters, producing voltage gains of d_a, 1/(1-d_b), and $-d_c$/(1-d_c), respectively. In addition, it can provide adjustable noninverting buck–boost (ANIBB) operation with a voltage gain of d_a/(1-d_b), with independent control of buck (d_a) and boost (d_a) duty ratios. The proposed converter is secured against shoot-through and open-circuit risks, and thus, naturally realizes safe commutation without requiring *RC* snubbers or soft-commutation switching techniques. It also utilizes external fast recovery diodes to stop high-frequency conduction of MOSFET's body diodes and avoid related issues. The proposed converter provides the following advantages over existing bipolar SC ac–ac converter topologies: fewer active switches, higher magnetic utilization, continuous input and output currents, provision of NIBo operation to compensate voltage sags of above 50%, and common-ground sharing between input and output.

II. Proposed SC Buck–Boost AC–AC Converter

The circuit diagram of the proposed converter is shown in Fig. 3. It is comprised of second-order input/output filters ($L_{\rm in}C_{\rm in}/L_oC_o$), a small value film capacitor *C*, and three pairs of buck and inversed buck (dual-buck) SCs (see Fig. 2) with small value shoot-through preventing inductors (L_{S1}, L_{S2}, and L_{S3}) connected at the midpoints of each pair. A MOSFET is connected in series with an external fast recovery diode to realize each buck-cell (S_1D_2, S_3D_4, S_5D_6) and inversed buck-cell (S_2D_1,

TABLE I
COMPARISON WITH SC AC–AC CONVERTERS

Parameters	SC IBB converter [8]	Bipolar SC converter [27]	SC inv./non-inv. converter [28]	Proposed bipolar SC converter
Voltage gain G (v_o/v_{in})	$\frac{d}{1-d}$	$d_1 - d_2$	d_1, $-d_2/(1-d_2)$, $(2d_3\text{-}1)/d_3$	d_a, $1/(1\text{-}d_b)$, $-d_c/(1-d_c)$, $d_a/(1-d_b)$
Availability of NIBu, NIBo, IBu and IBo operations	NIBu: No NIBo: No IBu: Yes IBo: Yes	NIBu: Yes NIBo: No IBu: Yes IBo: No	NIBu: Yes NIBo: No IBu: Yes IBo: Yes	NIBu: Yes NIBo: Yes IBu: Yes IBo: Yes
No. of switches	$4(S_1-S_4)$	$8(S_1-S_8)$	$8\ (S_1-S_8)$	$6\ (S_1-S_6)$
No. of diodes	$4(D_1-D_4)$	$4(D_1-D_4)$	$8\ (D_1-D_8)$	$6\ (D_1-D_6)$
No of Energy storing/ bypass capacitors	$2\ (C_1, C_2)$	$2\ (C_1, C_2)$	$4\ (C_1-C_4)$	$1\ (C)$
No. of inductors and their values	$2\ (L_1, L_2)$, Large	$2\ (L_1, L_2)$, Large	$4\ (L_1-L_4)$, Large	$2\ (L_{in}, L_o)$, Large; $3\ (L_{S1}-L_{S3})$, Very small
Magnetic utilization	Low (50%)	Low (50%)	Low (50%)	High (~100%)
Commutation issue	No	No	No	No
Continuity of input current	Quasi-Continuous	Discont.	Discont.	Continuous
Continuity of output current	Quasi-Continuous	Continuous	Discont.	Continuous
Require input filter inductor	Yes	Yes	Yes	No
Common-grounding	No	No	No	Yes
Compensation of voltage sag/swell	Sag: above & below 50% Swell: No	Sag: Below 50% Swell: Full	Sag: Below 50% Swell: Full	Sag: above & below 50% Swell: Full
Isolation transformer is required for series voltage injection	Yes	Yes	Yes	No
Insulation requirements of isolation transformer	High	High	High	Relatively low

*NIBu (noninverting buck), NIBo (noninverting boost), IBu (inverting buck), IBo (inverting boost).

S_4D_3, S_6D_5). Table I provides a comparison with existing SC ac–ac converters [8], [27], [28]. The proposed converter can provide both voltage buck and boost operations for non-inverting and inverting outputs; a feature not possessed by the counterpart SC converters. Also, unlike the counterpart SC converters in which half of the large inductors are inactive for each input/output half-cycle, the main inductors $L_{\rm in}$ and L_o in the proposed converter are fully utilized with one or two small value inductors L_{S1}, L_{S2}, L_{S3} also providing filtering in each half-cycle, improving its magnetic utilization.

Fig. 4(a) shows the equivalent circuit of the proposed converter during overlap time when all switches are turned ON. The short-circuit of the input voltage source $v_{\rm in}$ and output capacitor C_o is avoided by inductors $L_{\rm in}$ and L_o, respectively. The shoot-through of capacitor C is also protected by inductors L_{S1}, L_{S2}, and L_{S3}. Fig. 4(b) shows the equivalent circuit during deadtime when the switches are turned OFF. As observed, the inductor currents flow through capacitor C (which acts as a natural snubber) and external freewheeling diodes without any interruptions, avoiding switch voltage overshoots. Moreover, the voltages of all MOSFETs and diodes are clamped by capacitor C.

III. NIBU OPERATION

Fig. 5 shows the switch modulation strategy for NIBu operation. Switches S_1–S_4 are line frequency switches that are modulated according to the polarity of the input voltage $v_{\rm in}$.

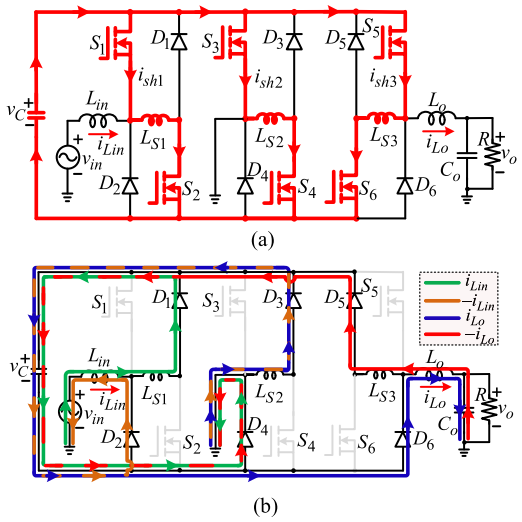

Fig. 4. Proposed converter during (a) overlap time and (b) dead time.

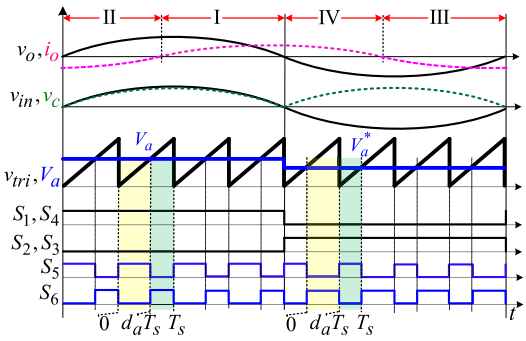

Fig. 5. Switch modulation strategy for NIBu operation.

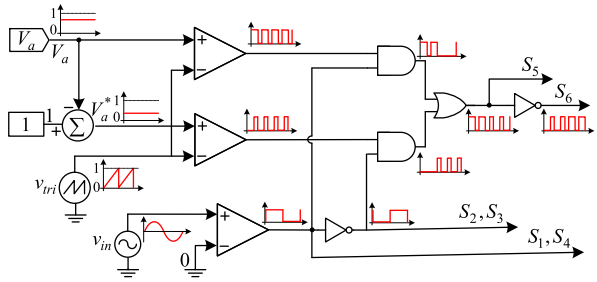

Fig. 6. Block diagram of switch modulation signals generation for NIBu operation.

For $v_{\rm in} > 0$, switches S_1, S_4 are fully turned ON and S_2, S_3 are fully turned OFF, and vice versa. Switches S_5, S_6 are modulated at high frequency in a complementary manner by comparing a reference signal V_a with high-frequency saw-tooth carrier signal $v_{\rm tri}$. For $v_{\rm in} > 0$, switch S_5 is turned ON for an interval d_aT_s (when $V_a > v_{\rm tri}$), and its complementary switch S_6 conducts for an interval $(1-d_a)T_s$ (when $V_a < v_{\rm tri}$). For $v_{\rm in} < 0$, the ON-times (and functions) of switches S_5 and S_6 are interchanged (S_5 now conducts for duration of $(1-d_a)T_s$), as obtained by comparing the modified reference signal $V_a^*(=1-V_a)$ with $v_{\rm tri}$. Fig. 6 shows the block diagram of switch modulation signals

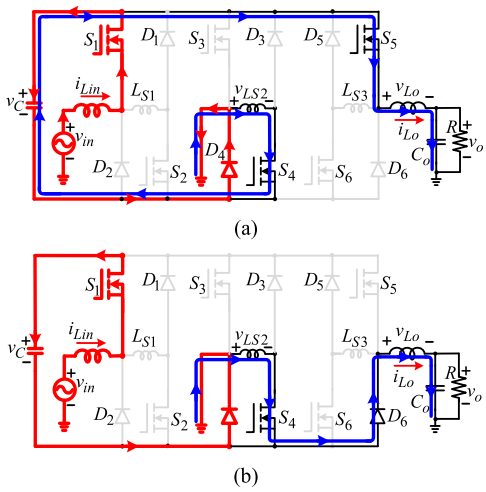

Fig. 7. Equivalent circuits in Sector-I $(v_o > 0, i_o > 0)$ for NIBu operation. (a) Interval-1. (b) Interval-2.

generation for NIBu operation (see Fig. 5). A sinusoidal input voltage $v_{\rm in}$ is compared with 0 to generate a line-frequency control signal to modulate switches S_1, S_4, while its inverted signal modulates switches S_2, S_3. A reference signal $V_a$is compared with carrier signal $v_{\rm tri}$ to generate the PWM signal with ON-time of d_aT_s. The reference signal V_a is subtracted from 1 and the modified reference signal V_a^* is compared with $v_{\rm tri}$ to generate a complementary PWM signal with an ON-time of $(1-d_a)T_s$. These signals are fed to a combination of AND and OR logic gates along with line-frequency logic signals (obtained by comparing $v_{\rm in}$ with 0) to generate a PWM signal with ON-times of d_aT_s and $(1-d_a)T_s$ for $v_{\rm in} > 0$ and $v_{\rm in} < 0$, respectively, to modulate switch S_5, while its inverted PWM signal modulates switch S_6.

For nonunity power factor (reactive load) operation, Sector-I $(v_o > 0, i_o > 0)$ and Sector-II $(v_o > 0, i_o < 0)$ exist for $v_o > 0$, while Sector-III $(v_o < 0, i_o < 0)$ and Sector-IV $(v_o\langle 0, i_o\rangle 0)$ exist for $v_o < 0$. Circuit operation is discussed for $v_{\rm in} > 0$:

The equivalent circuits for Sector-I are shown in Fig. 7. S_1 and S_4 are fully ON, and $v_{\rm in}$ is applied across the input filter $L_{\rm in}C_{\rm in}$, $v_c = v_{\rm in}$.

A. Interval-1 [0–d_aT_s]

S_5 is ON and S_6 is OFF [see Fig. 7(a)]. Input source $v_{\rm in}$ provides energy to L_o and the load. L_{S2} is in series with L_o. i_{Lo} increases linearly with a slope as given by

$$\frac{di_{Lo}}{dt} = \frac{v_{\rm in} - v_o}{L_{S2} + L_o}. \tag{1}$$

B. Interval-2 [d_aT_s–T_s]

S_5 is OFF and S_6 is ON [see Fig. 7(b)]. $v_{\rm in}$ is disconnected from the main circuit but provides power to the input filter $L_{\rm in}C_{\rm in}$, and the input current remains continuous. The energy stored in L_{S2} and L_o is released to the load. i_{Lo} decreases with the slope

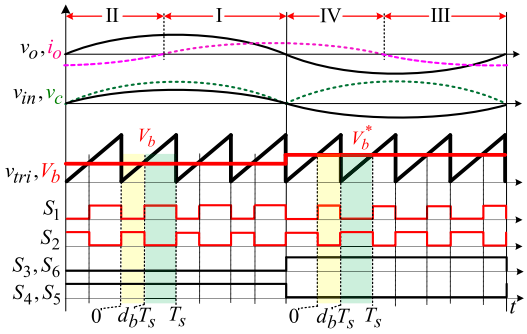

Fig. 8. Switch modulation strategy for NIBo operation.

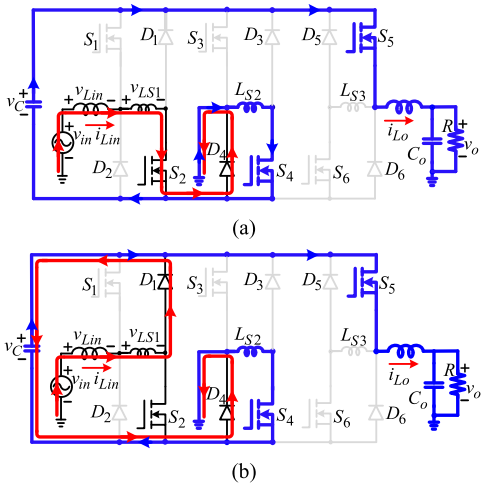

Fig. 9. Equivalent circuits in Sector-I $(v_o > 0, i_o > 0)$ for NIBo operation. (a) Interval-1. (b) Interval-2.

as given by

$$\frac{di_{Lo}}{dt} = \frac{-v_o}{L_{S2} + L_o}. \tag{2}$$

Operation in Sector-II occurs for nonunity power factor load when the output current is reversed $(i_o < 0)$. The bidirectional switching devices (MOSFETs with external free-wheeling diodes) provide current paths to reversed currents $-i_{\rm Lin}$ and $-i_{Lo}$, making the proposed converter compatible with reactive loads.

The voltage gain $M_a(= v_o/v_{\rm in})$ for NIBu operation is obtained from (1) and (2) as

$$M_a = \frac{v_o}{v_{\rm in}} = d_a. \tag{3}$$

IV. Noninverting Boost Operation

Fig. 8 shows the switch modulation strategy, and Fig. 9 shows the equivalent circuits for Sector-I. S_1 and S_2 are now high-frequency complementary switches that conduct for the duration of d_bT_s for $v_{\rm in} < 0$ and $v_{\rm in} > 0$, respectively. S_3–S_6 become line frequency switches.

For $v_{\rm in} > 0$, S_4 and S_5 are completely ON. A *CLC* filter (CL_oC_o) is created at the output by capacitors C, C_o and inductor L_o, $v_c = v_o$. L_{S2} is in series with L_o and contributes to its inductance.

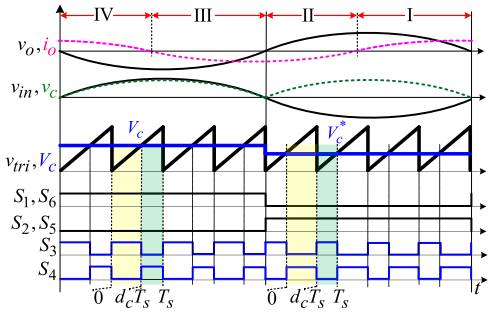

Fig. 10. Switch modulation strategy for IBB operation.

A. Interval-1 [0–d_bT_s]

S_2 is ON and S_1 is OFF [see Fig. 9(a)]. Input source v_{in} provides energy to L_o and the load. L_{S1} is in series with L_{in} and participates in the filtering of input current

$$\frac{di_{Lin}}{dt} = \frac{v_{\text{in}}}{L_{S1} + L_{\text{in}}}, \quad \frac{dv_C}{dt} = \frac{-i_o}{C}. \tag{4}$$

B. Interval-2 [d_bT_s–T_s]

S_2 is OFF and S_1 is ON [see Fig. 9(b)]. Input source v_{in} and L_{in} provide energy to capacitor C and the load. Circuit equations are given by

$$\frac{di_{Lin}}{dt} = \frac{v_{\text{in}} - v_o}{L_{S1} + L_{\text{in}}}; \quad \frac{dv_C}{dt} = \frac{i_{Lin} - i_o}{C}. \tag{5}$$

The voltage gain M_b for NIBo operation is obtained as

$$M_b = \frac{v_o}{v_{\text{in}}} = \frac{1}{1 - d_b}. \tag{6}$$

V. IBB Operation

The switch modulation strategy for IBB operation is shown in Fig. 10. S_3 and S_4 become high-frequency complementary switches. S_1, S_2, S_5, and S_5 are line-frequency switches. S_1 and S_6 are completely turned ON for $v_{\text{in}} > 0$. The equivalent circuits for operation in Sector-III ($v_{\text{in}} > 0, v_o < 0, i_o < 0$) are shown in Fig. 11.

A. Interval-1 [0–d_cT_s]

S_3 is ON and S_4 is OFF [see Fig. 11(a)]. L_{in} stores energy from the input source v_{in}. Capacitor C provides energy to L_o and the load. L_{S3} is in series with L_o and adds to its inductance

$$\frac{di_{Lin}}{dt} = \frac{v_{\text{in}}}{L_{\text{in}}}; \quad \frac{di_{Lo}}{dt} = \frac{v_C - v_o}{L_{S3} + L_o}; \quad \frac{dv_C}{dt} = \frac{-i_o}{C}. \tag{7}$$

B. Interval-2 [d_cT_s–T_s]

S_3 is OFF and S_4 is ON [see Fig. 11(b)]. Input source v_{in} and L_{in} provide energy to capacitor C. L_o provides energy to the load

$$\frac{di_{Lin}}{dt} = \frac{v_{\text{in}} - v_C}{L_{\text{in}}}; \quad \frac{di_{Lo}}{dt} = \frac{-v_o}{L_{S3} + L_o}; \quad \frac{dv_C}{dt} = \frac{i_{Lin}}{C}. \tag{8}$$

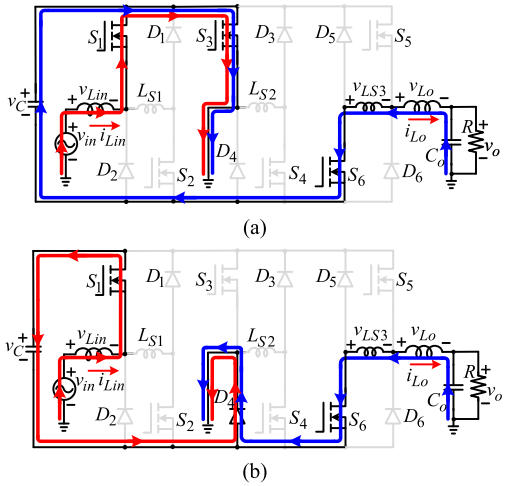

Fig. 11. Equivalent circuits in Sector-III ($v_o < 0, i_o < 0$) for IBB operation. (a) Interval-1. (b) Interval-2.

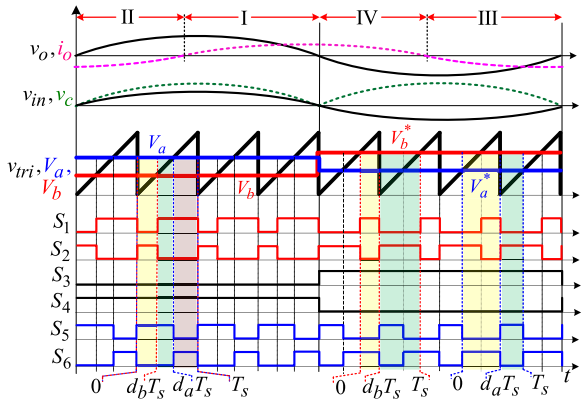

Fig. 12. Switch modulation strategy for ANIBB operation.

The voltage gain M_C for IBB operation is given by

$$G_c = \frac{v_o}{v_{\text{in}}} = -\frac{d_c}{1 - d_c}. \tag{9}$$

From (11), buck operation occurs for $d_c < 0.5$ and boost operation is obtained for $d_c > 0.5$.

VI. ANIBB Operation

Fig. 12 shows the switch modulation strategy for ANIBB operation. S_4 is completely turned ON for $v_{\text{in}} > 0$ and its complementary switch S_3 conducts for $v_{\text{in}} < 0$. Switches S_5, S_6 are modulated as in NIBu operation (see Fig. 5) by comparing references V_a and V_a^* with v_{tri}. Switches S_1, S_2 are modulated as in NIBo operation (see Fig. 8) by comparing references V_b and V_b^* with v_{tri}. The buck duty ratio d_a (ON-time of S_5) and boost duty ratio d_b (ON-time of S_2) can be adjusted independently, providing an extra control degree of freedom when regulating the output voltage.

The equivalent circuits for operation in Sector-1 are shown in Fig. 13 for $d_a > d_b$.

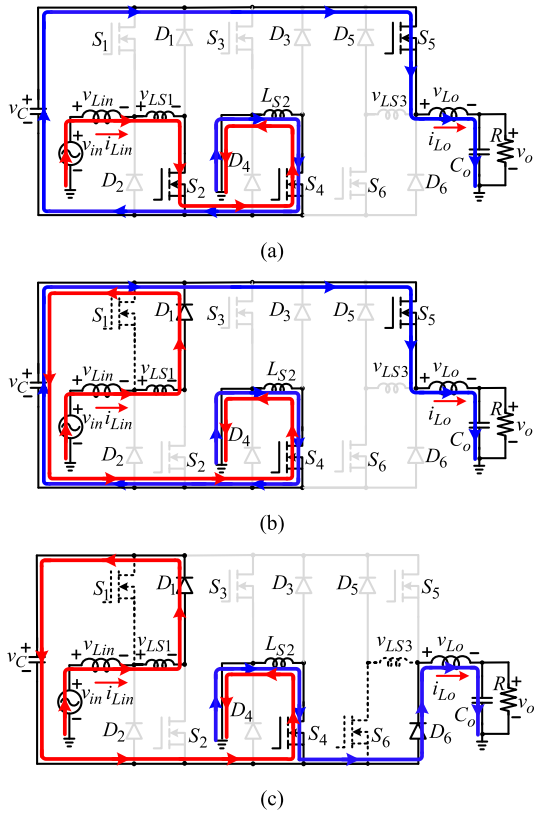

Fig. 13. Equivalent circuits in Sector-I ($v_o > 0, i_o > 0$) for ANIBB operation. (a) Interval-1. (b) Interval-2. (c) Interval-3.

A. Interval-1 [0–d_bT_s]

S_2, S_5 are ON and S_1, S_6 are OFF [see Fig. 13(a)]. Input source v_{in} provides energy to L_{in}. Capacitor C provides energy to L_o and the load

$$\frac{di_{Lin}}{dt} = \frac{v_{\text{in}}}{L_{S1} + L_{\text{in}}}; \quad \frac{di_{Lo}}{dt} = \frac{v_C - v_o}{L_{S2} + L_o}; \quad \frac{dv_C}{dt} = \frac{-i_o}{C}. \tag{10}$$

B. Interval-2 [d_bT_s–d_aT_s]

S_2 is OFF and S_1 is ON [see Fig. 13(b)]. S_5 remains ON (and S_6 remains OFF) as in the previous interval. Input source v_{in} and L_{in} charge capacitor C. Meanwhile, capacitor C also keeps providing energy to L_o and the load

$$\frac{di_{Lin}}{dt} = \frac{v_{\text{in}} - v_C}{L_{S1} + L_{\text{in}}}; \quad \frac{di_{Lo}}{dt} = \frac{v_C - v_o}{L_{S2} + L_o}; \quad \frac{dv_C}{dt} = \frac{i_{Lin} - i_o}{C}. \tag{11}$$

C. Interval-3 [d_aT_s–T_s]

S_5 is OFF and S_6 is ON [see Fig. 13(c)]. S_2 remains OFF and S_1 remains ON. Input source v_{in} and L_{in} keep charging C. L_o provides energy to the load

$$\frac{di_{Lin}}{dt} = \frac{v_{\text{in}} - v_C}{L_{S1} + L_{\text{in}}}; \quad \frac{di_{Lo}}{dt} = \frac{v_o}{L_{S2} + L_o}; \quad \frac{dv_C}{dt} = \frac{i_{Lin}}{C}. \tag{12}$$

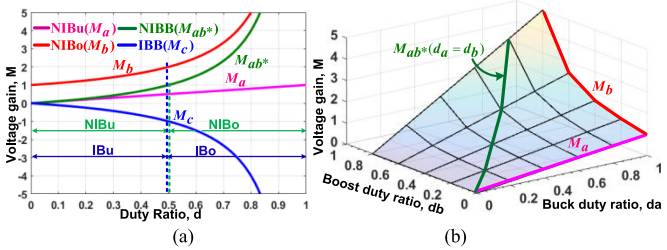

Fig. 14. Voltage gain versus duty ratio plots. (a) NIBu, NIBo, IBB, and NIBB operations. (a) ANIBB operation with two duty ratio controls.

The voltage gain M_{ab} in ANIBB operation is given by

$$M_{ab} = \frac{v_o}{v_{\text{in}}} = \frac{d_a}{1 - d_b}. \tag{13}$$

From (13), the voltage gain M_{ab} in ANIBB operation is the product of voltage gains for NIBu operation ($M_a = d_a$) and NIBo operation ($M_b = 1/(1 - d_b)$, i.e., $M_{ab} = M_a \cdot M_b$.

Fig. 14(a) shows the voltage gain (M) versus duty ratio (d) plots for NIBu, NIBo, IBB, and NIBB (same as ANIBB operation for $d_a = d_b$) operations. The voltage gain for ANIBB is plotted in Fig. 14(b) against variations in d_a and d_b. The resultant graph is a 3-D surface, providing numerous different combinations of d_a and d_b to achieve a certain voltage gain. The gain lines M_a, M_b and M_{ab*} are special cases for ANIBB operation when $d_b = 0$, $d_a = 1$, and $d_a = d_b$, respectively.

VII. Component Design/Selection Guidelines and Comparative Evaluation

Table II provides the component voltage/current stresses and ripples for the proposed converter. Component design/selection criteria for the proposed converter are discussed in this section, together with comparisons with counterpart SC buck–boost ac–ac converters [8], [28].

A. Switching Devices Voltage Stresses

Voltage stresses v_{SD} of switches and diodes are given by

$$\begin{cases} v_{SD-\text{NIBu}} = \frac{v_o}{M}; & \text{Proposed, [28]} \\ v_{SD-\text{NIBo}} = v_o; & \text{Proposed} \\ v_{SD-\text{IBB}} = \left(1 + \frac{1}{M}\right) v_o & \text{Proposed, [8], [28]} \\ v_{SD-\text{ANIBB}} = \frac{M_b}{M_{ab}} v_o; & \text{Proposed.} \end{cases} \tag{14}$$

Fig. 15(a) shows the normalized switching device voltage stresses v_{SD}/v_o versus voltage gain M for the proposed converter (in NIBu, NIBo, and IBB operations) and the counterpart converters [8], [28]. As observed, the proposed converter has the lowest device voltage stresses for the complete buck–boost gain range for combined NIBu–NIBo operations. v_{SD} is maximum for minimum M. Fig. 15(b) shows v_{SD}/v_o of the proposed converter for ANIBB operation plotted against variations in boost gain M_b and converter gain M_{ab}. For the same M_{ab} ($= M_a.M_b$), v_{SD}/v_o increases when M_b increases. This is because a decrease in M_a means that a higher capacitor C voltage v_C ($=v_{SD}$) is required to produce the same output voltage v_o ($=v_C.M_a$). Also, a smaller v_{SD}/v_o can be achieved than in IBB operation

TABLE II
COMPONENT VOLTAGE/CURRENT STRESSES AND RIPPLES FOR THE PROPOSED CONVERTER

Parameters	$G=f(d)$	Switch/Diode voltages, v_{SD}	Switch/Diode Currents, i_{SD}	Inductor current, i_L	Inductor current ripples, Δi_L	Voltage across capacitor, v_C	Capacitor voltage ripples, Δv_C
NIBu Operation	d_a	$v_{SD1-SD6} = v_{in}$	$i_{SD1-SD4} = i_{in}$ $i_{SD5,SD6} = i_o$	$i_{Lin,Ls1} = i_{in}$ $i_{Lin,Ls2,3} = i_o$	$\Delta i_{Lo} = \frac{(v_{in}-v_o)d_aT}{L_o}$	$v_{Cin,C} = v_{in}$ $v_{Co} = v_o$	$\Delta v_C \approx 0$
NIBo Operation	$\frac{1}{1-d_b}$	$v_{SD1-SD6} = v_o$	$i_{SD1-SD4} = i_{in}$ $i_{SD5,SD6} = i_o$	$i_{Lin,Ls1} = i_{in}$ $i_{Lin,Ls2,3} = i_o$	$\Delta i_{Lin} = \frac{v_{in}d_bT}{L_o}$	$v_{Cin} = v_{in}$ $v_{Co,C} = v_o$	$\Delta v_C = \frac{i_o d_b T}{C}$
IBB Operation	$-\frac{d_c}{1-d_c}$	$v_{SD1-SD6} = v_{in} + v_o$	$i_{SD1,SD2} = i_{in,}$ $i_{SD3,SD4} = i_{in} + i_o$ $i_{SD5,SD6} = i_o$	$i_{Lin,Ls1} = i_{in}$ $i_{Lin,Ls2,3} = i_o$	$\Delta i_{Lin} = \frac{v_{in}d_cT}{L_{in}}$ $\Delta i_{Lo} = \frac{v_o(1-d_c)T}{L_o}$	$v_{Cin} = v_{in}$ $v_{Co} = v_o$ $v_C = v_{in} + v_o$	$\Delta v_C = \frac{i_o d_c T}{C}$
ANIBB Operation	$\frac{d_a}{1-d_b}$	$v_{SD1-SD6} = \frac{v_o}{d_a}$	$i_{SD1,SD2} = i_{in,}$ $i_{SD3,SD4} = i_{in} + i_o$ $i_{SD5,SD6} = i_o$	$i_{Lin,Ls1} = i_{in}$ $i_{Lin,Ls2,3} = i_o$	$\Delta i_{Lin} = \frac{v_{in}d_bT}{L_{in}}$ $\Delta i_{Lo} = \frac{v_o(1-d_a)T}{L_o}$	$v_{Cin} = v_{in}$ $v_{Co} = v_o$ $v_C = \frac{v_o}{d_a}$	$\Delta v_C = \frac{i_o d_b T}{C}$

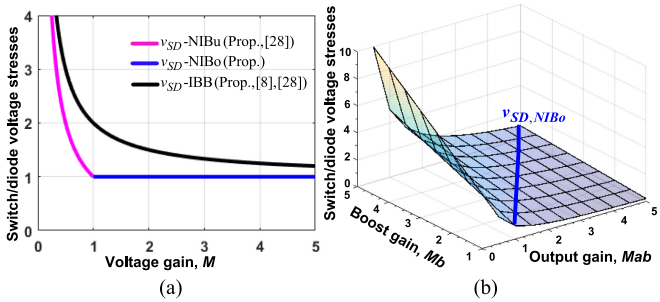

Fig. 15. Normalized switch/diode voltage stresses. (a) Proposed and counterpart converters in [8] and [28]. ANIBB operation of the proposed converter.

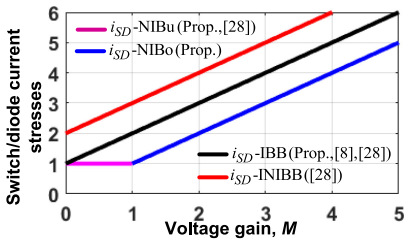

Fig. 16. Normalized switch/diode current stresses.

[see Fig. 15(a)] when $d_a > d_b$ ($M_a > 1 - 1/M_b$). The blue line shows the v_{SD}/v_o for $M_a = M_{ab}$ (i.e., $M_a = 1$), which is the same as in the NIBo operation [see Fig. 15(a)].

B. Switching Devices Current Stresses

Current stresses i_{SD} of switches and diodes are given by

$$\begin{cases} i_{SD-\mathrm{NIBu}} = i_o; & \text{Proposed, [28]} \\ i_{SD-\mathrm{NIBo}} = i_o\, M; & \text{Proposed} \\ i_{SD-(\mathrm{AN})\mathrm{IBB}} = (1+M)\, i_o; & \text{Proposed, [8], [28]} \\ i_{SD-\mathrm{INIBB}} = (2+M)\, i_o; & \text{[28]}. \end{cases} \tag{15}$$

Normalized device current stresses i_{SD}/i_o for the proposed converter, [8], and [28] are plotted in Fig. 16. The devices experience maximum current stresses for maximum gain M. Again, the proposed converter provides the lowest current stresses for combined NIBu–NIBo operations, whereas [28] has the highest current stresses for its INIBB operation. Unlike the counterpart SC converters, the presence of efficient combined NIBu–NIBo operations in the proposed converter (with the least device voltage and current stresses) makes it a more suitable candidate for application as a direct ac–ac voltage regulator.

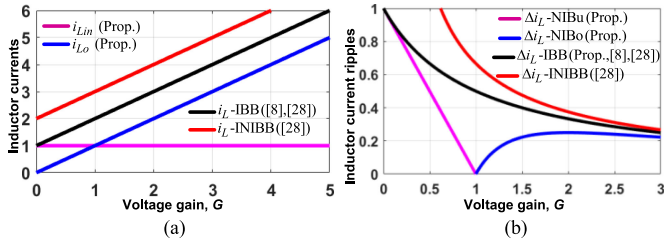

Fig. 17. Inductor stresses and ripples. (a) Current stresses. (b) Current ripples.

C. Inductors

For all operating modes, the main inductors L_{in} and L_o of the proposed converter carry currents i_{in} and i_o, respectively. Inductors L_1, L_2in [8] are required to carry $i_{\mathrm{in}} + i_o$. Inductors $L_1 - L_4$ in [28] have to handle currents of $i_{\mathrm{in}} + i_o$ and $i_{\mathrm{in}} + 2i_o$ for IBB and INIBB operations, respectively. From the i_L/i_o plots in Fig. 17(a), the inductors in the proposed converter have smaller current handling requirements.

Inductor current ripples Δi_L can be expressed as

$$\begin{cases} \Delta i_{L-\mathrm{NIBo}} = \dfrac{M-1}{M^2}\dfrac{v_o}{f_s L_{\mathrm{in}}}; & \text{Proposed} \\ \Delta i_{L-\mathrm{NIBu}} = (1-M)\dfrac{v_o}{f_s L_{\mathrm{in}}}; & \text{Proposed, [28]} \\ \Delta i_{L-\mathrm{IBB}} = \dfrac{1}{(1+M)}\dfrac{v_o}{f_s L_{\mathrm{in}}}; & \text{Proposed, [8], [28]} \\ \Delta i_{L-\mathrm{INIBB}} = \dfrac{(1+M)}{M\,(2+M)}\dfrac{v_o}{f_s L_{\mathrm{in}}}; & \text{[28]} \end{cases} \tag{16}$$

where, $f_s = 1/T_s$ is the switching frequency. Fig. 17(b) shows the normalized inductor current ripples $\Delta i_L\,/k$ ($k = v_o/f_s L$) versus voltage gain M. The inductors in the proposed converter have least $\Delta i_L\,/k$ for combined NIBu–NIBo operations. Maximum Δi_L occurs at the minimum value of M (maximum v_{in}), and the inductor values can be selected to contain Δi_L within the allowable limit.

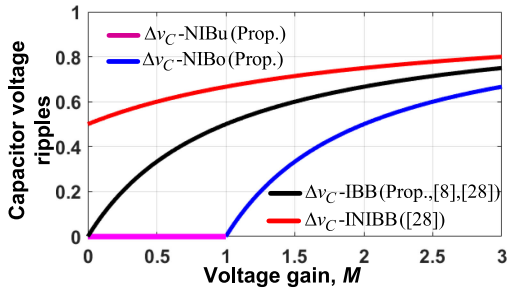

Fig. 18. Capacitor voltage ripples.

D. Capacitors

Apart from the input and output filter capacitors $(C_{\rm in}, C_o)$, the proposed converter requires one small value capacitor C, [8] requires two capacitors. and [28] requires four capacitors. In addition to providing filtering and energy transfer, the capacitor C in the proposed converter acts as a natural snubber, offering a path for inductor current during dead time [see Fig. 4(b)]. It also clamps the voltages of the switching devices, protecting them against voltage overshoots. Capacitor voltage stresses v_C are the same as switch voltage stresses, plotted in Fig. 15.

Capacitor voltage ripples Δv_C are given by

$$\begin{cases} \Delta v_{C-\rm NIBu} = 0; & \text{Proposed} \\ \Delta v_{C-\rm NIBo} = \dfrac{M-1}{M}\dfrac{\sqrt{2}P_o}{f_s\,C}; & \text{Proposed} \\ \Delta v_{C-\rm IBB} = \dfrac{M}{M+1}\dfrac{\sqrt{2}P_o}{f_s\,C}; & \text{Proposed, [8], [28]} \\ \Delta v_{C-\rm INIBB} = \dfrac{M+1}{M+2}\dfrac{\sqrt{2}P_o}{f_s\,C}; & \text{[28]}. \end{cases} \tag{17}$$

Fig. 18 shows the plots of normalized capacitor voltage ripples $\Delta i_C/k'$ ($k' = \sqrt{2}P_o/f_s\,C$) against the voltage gain M. The proposed converter has the lowest Δi_C (and minimum capacitance requirement) for NIBu and NIBo operations, while [28] has the highest Δi_C in INIBB operation. Maximum Δi_C occurs at maximum M (minimum $v_{\rm in}$), which determines the capacitor values.

VIII. Application as DVR and FUT

The proposed converter combines the functionality of the basic noninverting buck converter (NIBu operation), noninverting boost converter (NIBo operation), inverting buck–boost/Cuk converter (IBB operation), and noninverting buck–boost converter (ANIBB operation with $d_a = d_b$). This makes the proposed converter a potential candidate for numerous applications.

1) It can be employed as a fully-rated direct ac–ac voltage regulator in which the input and output are connected in shunt with the ac mains and load, respectively. The proposed NIBu and NIBo operations can regulate the ac output voltage for a wide range of high and low inputs, respectively, with lower component stresses and higher efficiency than a typical IBB (or Cuk) ac–ac converter.

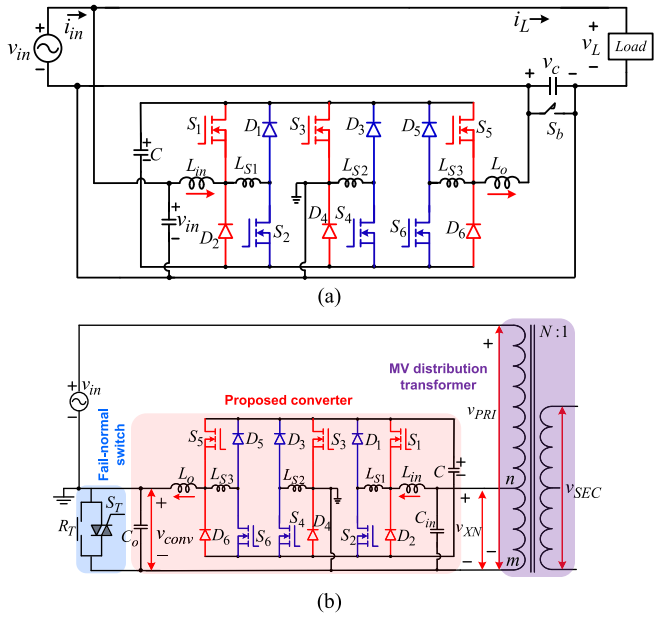

Fig. 19. Application of the proposed converter as a series voltage compensator. (a) DVR. (b) FUT.

2) IBB and NIBB (ANIBB operation with $d_a = d_b$) operations of the proposed converter can together provide step-changed frequency output (similar to a single-phase MC [29]). This step-variable frequency operation makes the proposed converter suitable for application as a traction converter [30], high step-up ac–dc converter [31], etc.

3) Bipolar buck–boost operations make the proposed converter suitable for application as a partially rated series voltage compensator such as DVR and FUT, as discussed in the following.

A. Application as DVR

The conventional DVR, based on the basic buck ac–ac converter as shown in Fig. 1(b), has the following limitations.

1) A line-frequency tapped winding transformer is required together with connection switches S_1 and S_2 to inject negative series voltages, which makes the cost and volume of the system uneconomical [11].
2) The step-down voltage operation of the buck ac–ac converter limits the voltage sag compensation range, i.e., voltage sags of only up to 50% can be mitigated.
3) PWM dead times based soft-commutations strategies or *RC* snubbers are required to overcome the commutation problem of the buck ac–ac converter.

Existing SC ac–ac converters [8], [19], [20], [24]–[28] have floating input and output ports, and therefore, they inevitably require an external line-frequency transformer for series voltage injection. The floating input and output also increase the insulation requirements of the injection transformer [18].

The configuration of a DVR based on the proposed converter is shown in Fig. 19(a). The input of the converter is directly fed from the ac line $v_{\rm in}$, and its output $v_{\rm conv}$ is connected in series with the ac line and the load. Due to the common-ground sharing

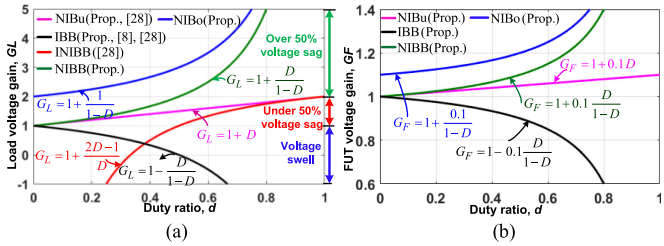

Fig. 20. Voltage gain plots. (a) DVR. (b) FUT.

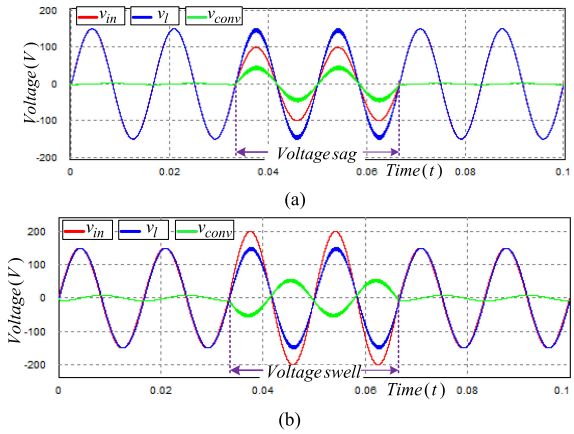

Fig. 21. Simulation results of the proposed DVR. (a) Voltage sag compensation. (b) Voltage swell compensation.

feature of the proposed converter, an external line frequency transformer is not required for series voltage injection. Also, if an external transformer was to be added for the purpose of electrical isolation and protection, its insulation requirement would be relatively lower [18].

The load voltage gains G_L of the DVRs are given by

$$\begin{cases} G_{L-\text{NIBu}} = \frac{v_o}{v_{in}} = 1 + d; & \text{Proposed, [28]} \\ G_{L-\text{NIBo}} = \frac{v_o}{v_{\text{in}}} = 1 + \frac{1}{1-d}; & \text{Proposed} \\ G_{L-\text{IBB}} = \frac{v_o}{v_{\text{in}}} = 1 - \frac{d}{1-d}; & \text{Proposed, [8], [28]} \\ G_{L-\text{ANIBB}} = \frac{v_o}{v_{\text{in}}} = 1 + \frac{d}{1-d}; & \\ G_{L-\text{INIBB}} = \frac{v_o}{v_{\text{in}}} = 1 + \frac{2d-1}{d}; & \text{Proposed [28].} \end{cases} \tag{18}$$

The load voltage gain G_L is plotted in Fig. 20(a). The proposed converter can compensate voltage sags of below and above 50% through combined NIBu–NIBo or ANIBB operation, and a complete range of voltage swell is mitigated through IBB operation. In contrast, the converter presented in [8] can compensate only voltage sag or swell, and that in [28] can compensate only shallow voltage sags (below 50%). Fig. 21 shows the simulation results of the proposed DVR. Fig. 21(a) shows the waveforms of the line voltage v_{in}, load voltage v_l, and converter output injected voltage v_{conv} for a voltage sag condition when v_{in} decreases from 110 V_{rms} to 70 V_{rms}. The converter feeds a positive series voltage through ANIBB operation, and v_l is maintained at 110 V_{rms}. Fig. 21(b) shows the same waveforms in the event of a voltage swell when v_{in} increases to 150 V_{rms}. The converter feeds a negative series voltage ($-v_{\text{conv}}$) through IBB operation, and the load voltage is again regulated.

B. Application as FUT

Existing FUTs [3], [4], based on a buck ac–ac converter [see Fig. 1(a)], have the following shortcomings.

1) Negative (low frequency) tap windings ($-v_{XN}$) are required together with switching relays R_1 and R_2 to inject a negative voltage for high input ac line voltages. This increases the cost of the system and the switching of the relays adds control complexity and operational delays [4].
2) The maximum voltage compensation range is limited to the available tapped-winding voltage ($\pm v_{XN}$). For instance, with a tapped-winding voltage setting of $\pm 5\%$, the compensation range is limited to 5%.
3) Due to the commutation issues of the employed ac–ac converter, current-based soft-commutation switching is used for safe commutation [4]. Moreover, the FUT utilizes lossy snubber circuits to provide a path for the line current during false commutation, along with input fuses and varistors for protection against current shoot-through and voltage spikes, respectively.

The counterpart SC ac–ac converters [8], [19], [20], [24]–[28] with their floating inputs and outputs would require an additional transformer for series voltage injection, which is not a feasible approach as the MV distribution transformer of the FUT already provides electrical isolation.

Fig. 18(b) shows the configuration of a FUT [2], [3] based on the proposed converter. The input of the converter is fed from the positive low voltage tapped-winding with an $x\%$ voltage setting ($v_{XN} = x\%.v_{in}$), and its output (v_{conv}) is connected in series with the distribution line (v_{in}) and primary winding (v_{PRI}) of the MV distribution transformer. Due to the bipolar voltage injection capability of the proposed converter, the negative tapped winding and connection relays R_1, R_2 [see Fig. 1(a)] are not required.

By assuming a tap settings of 10% ($v_{XN} = x\% \cdot v_{\text{in}}$), the voltage gain G_F ($v_{\text{SEC}}/v_{\text{in}}$) of the proposed FUT is plotted against the converter duty ratio in Fig. 19(b). The combined NIBu–NIBo or NIBB operations can regulate v_{SEC} when v_{in} is lower than the nominal value, whereas IBB operation can provide regulation for overvoltages. In addition, buck–boost operations can compensate for higher voltage magnitudes (below 0.9 and above 1.1) than the actual tap settings (of 10%).

The above features of the proposed DVR and FUT and the fact that the proposed topology is the only reported SC-based direct ac–ac converter with common grounding between the input and output ports make it an attractive choice for applications as a FUT or DVR.

IX. Experimental Results

A 400-VA hardware prototype was built and tested. The design parameters and operating conditions of the experimental test circuit are provided in Table III. Experiments were performed without using *RC* snubbers or soft-commutation switching techniques, validating the natural safe-commutation feature of the proposed converter.

Figs. 22 and 23 show the experimental waveforms during NIBu operation for an *RL* load, with $v_{\text{in}} = 150\,\text{V}_{\text{rms}}$, $v_o =$

TABLE III
EXPERIMENTAL SPECIFICATIONS

Output voltage (v_o)	155 V_{peak}/ 60 Hz
Input ac voltage (v_{in})	70~150 V_{rms}
Output load power (P_o)	400 VA
Switching frequency (f_s)	50 kHz
MOSFETs ($S_1 - S_6$)	47N60CFD
External Diodes ($D_1 - D_6$)	RHRG3060
Capacitors (C_{in}, C, C_o)	(1.5 µF , 3 µF, 1.5 µF)
Inductors ($L_{in}, L_o, L_{S1} - L_{S3}$)	(400 uH, 300 uH, 30 µH)
Load (RL)	30 Ω + 30 mH

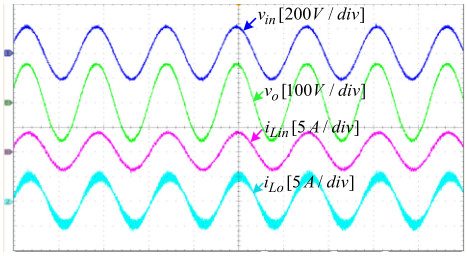

Fig. 22. Measured waveforms of input/output voltages and inductor currents during NIBu operating mode $v_{\rm in} = 150\ {\rm V_{rms}}$.

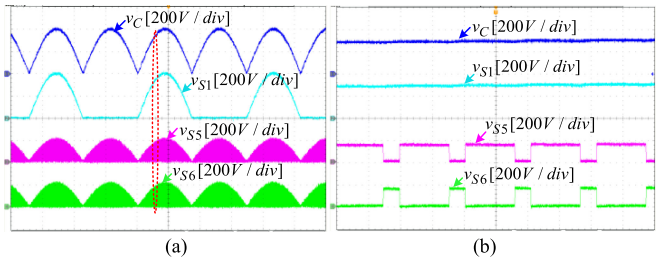

Fig. 23. Measured waveforms during NIBu operating mode $v_{\rm in} = 150\ {\rm V_{rms}}$. (a) Component voltage stresses. (b) Enlarged waveforms of (a).

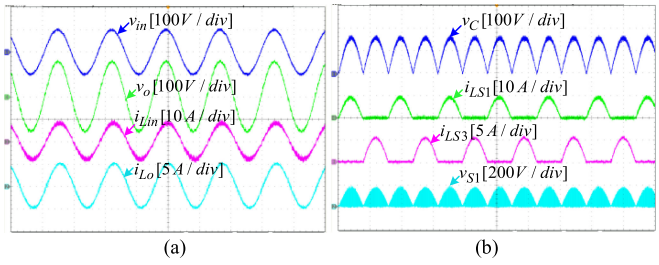

Fig. 24. Measured waveforms during NIBo operating mode $v_{\rm in} = 70\ {\rm V_{rms}}$. (a) Input/output voltages and inductor currents. (b) Component stresses.

$110\ {\rm V_{rms}}$, and $d_a = 0.73$. Fig. 22 shows the waveforms of input and output voltages ($v_{\rm in}$ and v_o) and input and output inductor currents (i_{Lin} and i_{Lo}). Continuous sinusoidal input current (i_{Lin}) is obtained due to the input *LC* filter formed by $L_{\rm in}$ and *C*. Fig. 23(a) shows the voltage stresses of capacitor *C* and switches S_1, S_5, and S_6. The enlarged waveforms of component voltage stresses [see Fig. 23(a)] are shown in Fig. 23(b). The peak capacitor *C* voltage is around 212 V, equal to the peak value of $v_{\rm in}$, clamping the switch voltage stresses. Fig. 24 shows the experimental waveforms for NIBo operation with $v_{\rm in} = 70\ {\rm V_{rms}}$ and

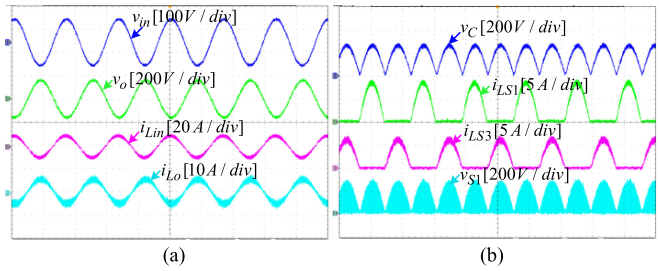

Fig. 25. Measured waveforms during IBB (boost) operating mode $v_{\rm in} = 70\ {\rm V_{rms}}$. (a) Input/output voltages and inductor currents. (b) Component stresses.

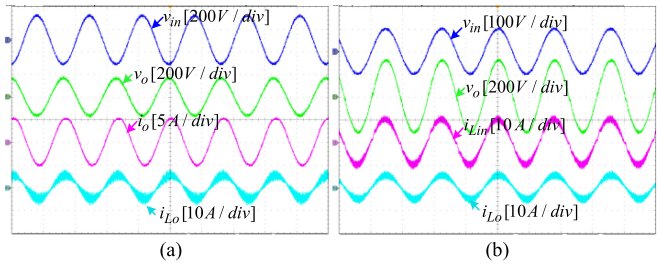

Fig. 26. Measured waveforms of input/output voltages and inductor currents. (a) IBB (buck) operation. (b) NIBB (boost) operation.

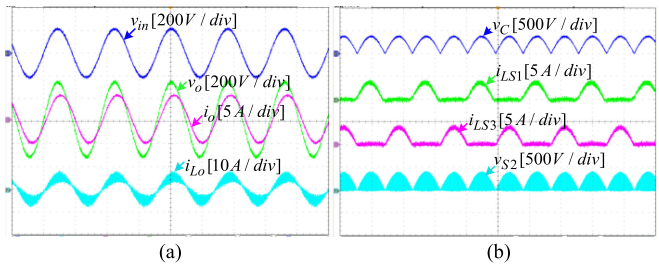

Fig. 27. Measured waveforms during ANIBB (buck) operating mode $v_{\rm in} = 150\ {\rm V_{rms}}$. (a) Input/output voltages and currents. (b) Component stresses.

$d_b = 0.36$. Fig. 24(a) shows the $v_{\rm in}$, v_o, i_{Lin} and i_{Lo}waveforms. As observed, i_{Lo} has a negligible ripple component due to the presence of the output *CLC* filter created by *C*, L_o, and C_o. Fig. 24(b) shows the voltage stresses of capacitor *C* and switch S_1, as well as the inductor L_{S1}, L_{S3} currents. The peak voltage stresses of the capacitor and switches are about 155 V, equal to the peak value of v_o. Fig. 25 shows the experimental waveforms for the IBB (boost) operation with $v_{\rm in} = 70\ {\rm V_{rms}}$ and $d_c = 0.61$. Fig. 25(a) shows the experimental waveforms of $v_{\rm in}$, v_o, i_{Lin}, and i_{Lo}. Fig. 25(b) shows the voltage stresses of capacitor *C* and switch S_1, together with inductor L_{S1}, L_{S3} currents. The observed voltage stresses of the capacitor and switches become larger in IBB operation compared to NIBu and NIBo operations as the components have to sustain the sum of the input and output voltages. Fig. 26(a) and (b) shows the waveforms of $v_{\rm in}$, v_o, i_{Lin} (or i_o), and i_{Lo} for IBB operation ($v_{\rm in} = 150\ {\rm V_{rms}}$, $d_c = 0.43$) and ANIBB operation ($v_{\rm in} = 70\ {\rm V_{rms}}$, $d_a = d_b = 0.61$), respectively. Fig. 27 shows the experimental waveforms for ANIBB (buck) operation with $v_{\rm in} = 150\ {\rm V_{rms}}$, $d_a = d_b = 0.43$. Fig. 27(a) shows the waveforms of $v_{\rm in}$, v_o, i_{Lo}, and i_o. Fig. 27(b)

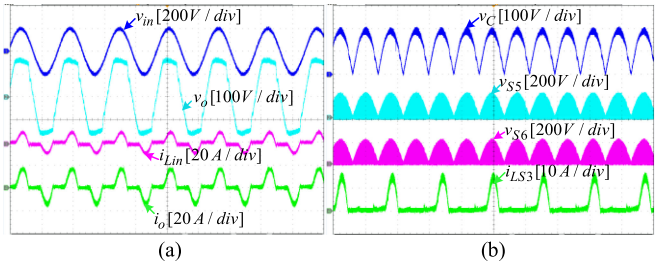

Fig. 28. Measured waveforms during NIBu operating mode with nonlinear load $v_{\rm in} = 150\ {\rm V_{rms}}$. (a) Input/output voltages and inductor currents. (b) Component stresses.

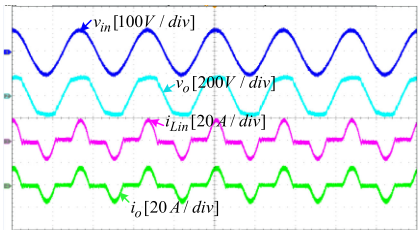

Fig. 29. Measured waveforms of input/output voltages and inductor currents during NIBo operating mode with nonlinear load, $v_{\rm in} = 70\ {\rm V_{rms}}$.

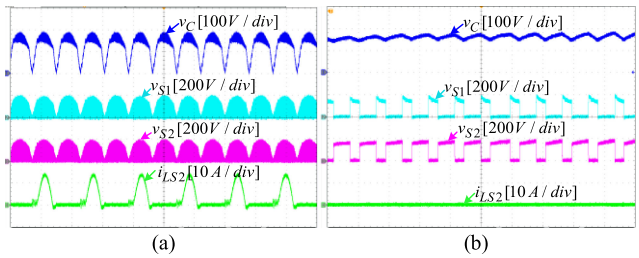

Fig. 30. Measured waveforms during NIBu operating mode with nonlinear load $v_{\rm in} = 70\ {\rm V_{rms}}$. (a) Component voltage/current stresses. (b) Enlarged waveforms of (a).

shows the voltage stresses of capacitor C and switch S_2, and the inductor currents i_{LS1}, i_{LS3}.

Figs. 28–30 show the experimental results for a nonlinear load composed of a full-wave diode rectifier followed by an output capacitor $C_f = 1.5\ \mu{\rm F}$ and resistor $R = 30\ \Omega$. Fig. 28 shows the experimental waveforms during NIBu operation for a nonlinear load, with $v_{\rm in} = 150\ {\rm V_{rms}}$ and $d_a = 0.73$. Fig. 28(a) shows the waveforms of $v_{\rm in}$, v_o, i_{Lin}, and i_o. Fig. 28(b) shows the voltage stresses of capacitor C and switches S_5, S_6 and inductor L_{S3} current. Figs. 29 and 30 show the experimental waveforms during NIBo operation for the nonlinear load with $v_{\rm in} = 70\ {\rm V_{rms}}$ and $d_a = 0.36$. Fig. 29 shows the waveforms of $v_{\rm in}$, v_o, i_{Lin}, and i_{Lo}. Fig. 30(a) shows the voltage stresses of capacitor C and switches S_1, S_2 and the current through the inductor L_{S2}. Fig. 30(b) shows the enlarged switching-frequency waveforms of Fig. 30(a).

The closed-loop experimental results of the proposed ac–ac converter-based DVR are shown in Figs. 31–33. Fig. 31(a) and (b) shows the experimental results for a voltage sag of 36% when the line voltage is decreased from its optimal value of 110 to 70 $\rm V_{rms}$. Fig. 31(a) shows the ac line voltage $v_{\rm in}$, load voltage v_l,

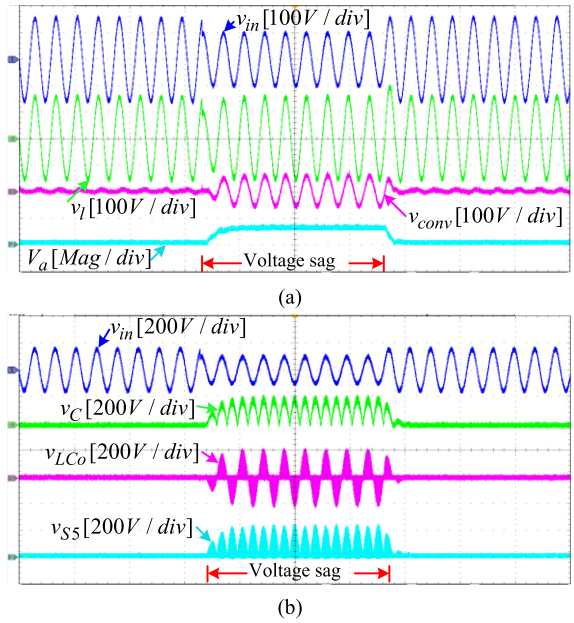

Fig. 31. Close-loop control results for compensation of the low magnitude of a voltage sag. (a) AC line voltage, load voltage, converter output voltage, and control duty ratio. (b) Component voltage stresses.

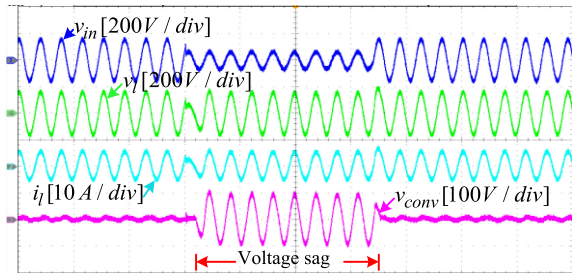

Fig. 32. Close-loop control results of ac line voltage, load voltage/current, and converter output voltage for compensation of a deep voltage sag.

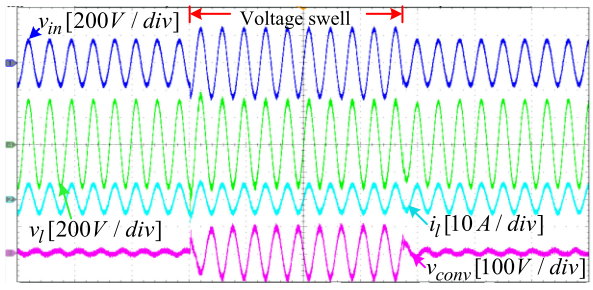

Fig. 33. Close-loop control results of ac line voltage, load voltage/current, and converter output voltage for compensation of a grid voltage swell.

the injected voltage of converter $v_{\rm conv}$, and the control reference signal V_a (see Fig. 5). As observed, once a voltage sag occurs, the converter operates in NIBu mode and the control reference V_a is dynamically adjusted through feedback control to inject the positive series voltage $v_{\rm conv}$, stabilizing the load voltage v_l. Fig. 31(b) shows the waveforms of the unfiltered output voltage of the converter v_{LCo} and the voltage stresses of capacitor C and switch S_5. Fig. 32 shows the experimental waveforms of $v_{\rm in}$, v_l,

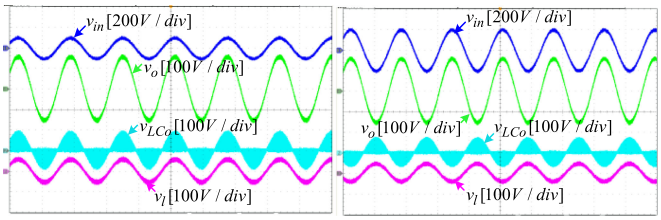

Fig. 34. Experimental results as FUT. (a) Low-line voltage condition. (b) High-line voltage condition.

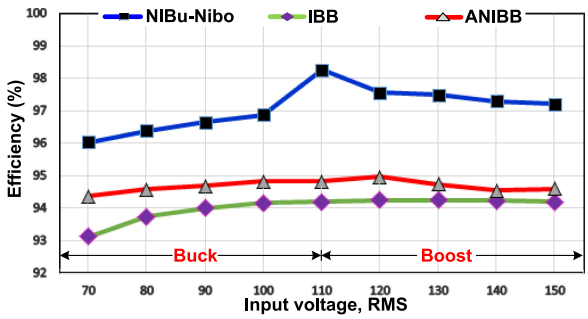

Fig. 35. Experimental efficiency of the proposed converter.

$v_{\rm conv}$, and load current i_l for a deep voltage sag of 64% when the line voltage v_l is reduced to 40 $V_{\rm rms}$. The converter operates in NIBo mode to inject the required positive series voltage to compensate for the load voltage. Fig. 33 shows the waveforms of $v_{\rm in}$, v_l, i_l, and $v_{\rm conv}$ for a voltage swell of 36% when the line voltage is increased to 150 $V_{\rm rms}$. The converter operates in IBB mode, injecting the required negative series voltage, and hence, provides compensation for the voltage swell without needing a tapped-winding transformer.

Fig. 34 shows the experimental results of the proposed converter when applied as a FUT. This is realized by connecting the converter input to the tapped primary winding of a three-winding transformer, and connecting its output in series with the ac line voltage and the primary winding [the same configuration as that shown in Fig. 19(b)]. Fig. 34(a) shows the input ac line voltage $v_{\rm in}$, unfiltered and filtered converter output voltages v_{LCo}, $v_{\rm conv}$, and secondary-side (load) voltage v_l for a low-line voltage condition when $v_{\rm in}$ is decreased to 80 $V_{\rm rms}$. The converter contributes a positive voltage (NIBu operation) in series with $v_{\rm in}$, and v_l is regulated to 110 $V_{\rm rms}$. Fig. 34(b) shows the same waveforms for a high-line voltage condition when $v_{\rm in}$ is increased to 150 $V_{\rm rms}$. The converter produces a negative output voltage (IBB operation) in series with $v_{\rm in}$, and v_l is regulated.

The measured efficiency of the proposed converter is plotted in Fig. 35 for different perturbations in input voltage for various operating modes for $v_o = 110\,V_{\rm rms}$ and $P_o = 400$ W. The highest efficiency occurs during NIBu–NIBo operations for $v_{\rm in} = 110\,V_{\rm rms}$ (unity gain operation) as the input source is directly connected to the load with no high-frequency switching, eliminating the corresponding MOSFET/diode switching loss and inductor core loss. An efficiency comparison with existing SC ac–ac converters [8], [27], [28] is given in Table IV. Clearly,

TABLE IV
EFFICIENCY COMPARISON

Circuit topology	Operating mode	Operating Conditions					Eff. (%)
		$v_{\rm IN}$ (V_{rms})	v_o (V_{rms})	M= v_o/v_{in}	P_o (W)	f_s (KHZ)	
[8]	IBu	170	120	0.71	460	50	93.8
	IBo	70	120	1.71	460	50	91.6
[27]	NIBu	141	98	0.7	400	18	95
	IBu	141	98	0.7	400	18	95
[28]	NIBu	141	110	0.775	300	50	97
	IBu	141	110	0.775	300	50	94
	IBo	78	110	1.4	300	50	91.6
Proposed	NIBu	150	110	0.73	400	50	97.1
	NIBo	70	110	1.57	400	50	96
	IBu	150	110	0.73	400	50	94.2
	IBo	70	110	1.57	400	50	93.1

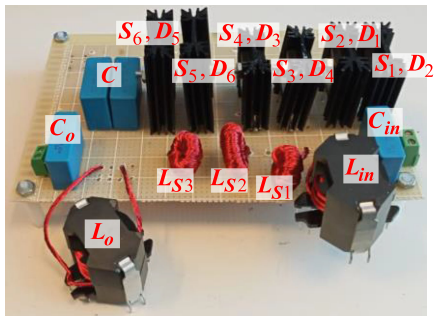

Fig. 36. Photograph of the converter hardware.

the proposed converter can provide improved efficiencies, especially for NIBu and NIBo operations. A photo of the hardware prototype of the proposed converter is shown in Fig. 36. These experimental results confirm the merits of the proposed circuit.

X. CONCLUSION

A novel SC, buck–boost, ac–ac converter is proposed with noninverting and inverting operations. Due to its versatile modes of operation, the circuit can operate as a NIBu, NIBo, IBB, and noninverting buck–boost ac–ac converter. The first three provide very simple operation with single duty ratio control, while the latter ANIBB operation provides more flexibility for adjusting the output voltage with two duty ratio controls. The proposed converter provides continuous input and output currents and supports reactive loads. In addition, the input and output ports share a common ground.

The proposed converter is very robust with natural protection from short-circuit and open-circuit problems, solving any potential commutation problems without requiring extra circuitry or complex control. It also stops the high-frequency conduction of MOSFET's body diodes and avoids the corresponding reverse recovery issues and losses. The converter is a suitable candidate for application as a direct ac–ac voltage regulator and series voltage compensator. The operating principles of the circuit are presented together with a full analysis of each operating mode. The operating characteristics and effectiveness of the proposed converter are verified experimentally using a 400-VA laboratory test circuit.

REFERENCES

[1] J. Y. Chan and J. V. Milanovi, "Assessment of the economic value of voltage sag mitigation devices to sensitive industrial plants," *IEEE Trans. Power Del.*, vol. 30, no. 6, pp. 2374–2382, Dec. 2015.

[2] S. Jothibasu and M. K. Mishra, "A control scheme for storageless DVR based on characterization of voltage sags," *IEEE Trans. Power Del.*, vol. 29, no. 5, pp. 2261–2269, Jul. 2014.

[3] D. M. Divan and A. Prasai, "Methods and systems of field upgradeable transformers," Google Patent US20 160 195 891A1, 2015.

[4] H. Chen, R. P. Kandula, A. Prasai, J. Schatz, and D. Divan, "Flexible transformers for distributed grid control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–6.

[5] H. Liu, J. Wang, and O. Kiselychnyk, "Mathematical modeling and control of a cost effective AC voltage stabilizer," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 8007–8016, Nov. 2016.

[6] F. Z. Peng, L. Chen, and F. Zhang, "Simple topologies of PWM ac–ac converters," *IEEE Power Electron. Lett.*, vol. 1, no. 1, pp. 10–13, Mar. 2003.

[7] J.-C. Wu, H.-L. Jou, K.-D. Wu, and S.-J. Jan, "Three-arm AC automatic voltage regulator," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 567–575, Feb. 2011.

[8] A. A. Khan, H. Cha, and H. F. Ahmed, "An improved single-phase direct PWM inverting buck-boost AC-AC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5384–5393, Sep. 2016.

[9] S. Sharifi, M. Monfared, and A. Nikbahar, "Highly efficient single-phase direct AC to AC converter with reduced semiconductor count," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1130–1138, Feb. 2021.

[10] X. P. Fang, Z. M. Qian, and F. Z. Peng, "Single-phase Z-source PWM ac– ac converters," *IEEE Power Electron. Lett.*, vol. 3, no. 4, pp. 121–124, Dec. 2005.

[11] J. Kaniewski, Z. Fedyczak, and G. Benysek, "AC voltage sag/swell compensator based on three-phase hybrid transformer with buck-boost matrix-reactance chopper," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3835–3846, Aug. 2014.

[12] M. K. Nguyen, Y. G. Jung, and Y. C. Lim, "Single-phase ac–ac converter based on quasi-Z-source topology," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2200–2210, Aug. 2010.

[13] R. A. M. R. Banaei, N. Jahanyari, and E. S. Najmi, "An AC Z-source converter based on gamma structure with safe-commutation strategy," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1255–1262, Feb. 2016.

[14] L. He, J. Nai, and J. Zhang, "Single-phase safe-commutation trans-Zsource ac-ac converter with continuous input current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5135–5145, Jun. 2018.

[15] C. Liu *et al.*, "Novel bipolar-type direct ac-ac converter topology based on non-differential ac choppers," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9585–9599, Oct. 2019.

[16] H. F. Ahmed, H. Cha, A. A. Khan, and H. Kim, "A novel buck–boost AC–AC converter with both inverting and noninverting operations and without commutation problem," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4241–4251, Jun. 2016.

[17] H. F. Ahmed, M. S. E. Mousri, H. Cha, K. H. A. Hosaini, and B. Zahawi, "A reliable single-phase bipolar buck-boost direct PWM AC-AC converter with continuous input/output currents," *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 10253–10265, Dec. 2020.

[18] P. Li and Y. Hu, "Unified non-inverting and inverting PWM ac-ac converter with versatile modes of operation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1137–1147, Feb. 2017.

[19] H. Shin, H. Cha, H. Kim, and D. Yoo, "Novel single-phase PWM AC-AC converters solving commutation problem using switching cell structure and coupled inductor," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2137–2147, Apr. 2015.

[20] A. A. Khan, H. Cha, and H.-G. Kim, "Three-phase three-limb coupled inductor for three-phase direct PWM AC-AC converters solving commutation problem," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 189–201, Jan. 2016.

[21] N. R. Zargari, P. D. Zargari, and G. Joos, "Two switch high performance current regulated DC/AC converter module," in *Proc. Conf. Rec. IEEE IAS Annu. Meeting*, 1995, pp. 929–934.

[22] L. Saro, K. Dierberger, and R. Redl, "High-voltage MOSFET behavior in soft-switching converters: Analysis and reliability improvements," in *Proc. 20th IEEE Telecommun. Energy Conf.*, 1998, pp. 30–40.

[23] X. D. Huang, H. J. Yu, J.-S. Lai, A. R. Hefner, and D. W. Berning, "Characterization of paralleled super junction MOSFET devices under hard and soft-switching conditions," in *Proc. 32nd IEEE Power Electron. Spec. Conf.*, 2001, pp. 2145–2150.

[24] A. A. Khan, H. Cha, and H. F. Ahmed, "High efficiency single-phase AC-AC converters without commutation problem," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5655–5665, Aug. 2016.

[25] A. A. Khan, H. Cha, and H. Kim, "Magnetic integration of discrete coupled inductors in single-phase direct PWM AC-AC converters," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2129–2138, Mar. 2016.

[26] H. F. Ahmed, H. Cha, A. A. Khan, and H. G. Kim, "A highly reliable single-phase high-frequency isolated double step-down AC–AC converter with both noninverting and inverting operations," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4878–4887, Nov./Dec. 2016.

[27] Y. Wang *et al.*, "An improved bipolar-type AC-AC converter topology based on non-differential dual-buck PWM AC choppers," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9585–9599, Oct. 2019.

[28] U. A. Khan, A. A. Khan, H. Cha, H. Kim, J. Kim, and J. Baek, "Dual buck AC–AC converter with inverting and non-inverting operations," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9432–9443, Nov. 2018.

[29] H. F. Ahmed, H. Cha, A. A. Khan, J. Kim, and J. Cho, "A single-phase buck-boost matrix converter with only six switches and without commutation problem," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1232–1244, Feb. 2017.

[30] P. Drabek, Z. Peroutka, M. Pittermann, and M. Cedl, "New configuration of traction converter with medium frequency transformer using matrix converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5041–5048, Nov. 2011.

[31] C. M. Young, M. H. Chen, S. H. Yeh, and K. H. Yuo, "A single-phase single-stage high step-up ac–dc matrix converter based on Cockcroft–Walton voltage multiplier with PFC," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4894–4905, Dec. 2012.

Hafiz Furqan Ahmed received the B.E. (with hons.) degree in electronics engineering from the National University of Sciences and Technology, Islamabad, Pakistan, in 2012, and the M.S. combined Ph.D. degrees in energy engineering (specialization in power electronics) from Kyungpook National University, Daegu, South Korea, in 2017.

He is currently working as a Postdoctoral Researcher with Khalifa University, UAE. His current research interests include grid-connected inverters and ac–ac converters for gird voltage compensation.

Mohamed Shawky El Moursi (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees from Mansoura University, Mansoura, Egypt, in 1997 and 2002, respectively, and the Ph.D. degree from the University of New Brunswick (UNB), Fredericton, NB, Canada, in 2005, all in electrical engineering.

He was a Research and Teaching Assistant with the Department of Electrical and Computer Engineering, UNB, from 2002 to 2005. He joined McGill University as a Postdoctoral Fellow with the Power Electronics Group. He joined Vestas Wind Systems, Arhus, Denmark, in the Technology R&D with the Wind Power Plant Group. He was with TRANSCO, UAE, as a Senior Study and Planning Engineer. He is currently a Professor in the Electrical Engineering and Computer Science Department, Khalifa University of Science and Technology—Masdar Campus, Abu Dhabi, UAE, and seconded to a Professor position in the Faculty of Engineering, Mansoura University, Mansoura, Egypt, and currently on leave. He was a Visiting Professor with the Massachusetts Institute of Technology, Cambridge, MA, USA. His research interests include power system, power electronics, FACTS technologies, VSC-HVDC systems, microgrid operation and control, and renewable energy systems (wind and PV) integration and interconnections.

Dr. Shawky is currently an Editor for the IEEE TRANSACTIONS ON POWER DELIVERY, IEEE TRANSACTIONS ON POWER SYSTEMS, an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, a Guest Editor for the IEEE TRANSACTIONS ON ENERGY CONVERSION, a Guest Editor-in-Chief for a special section between TPWRD and RPWRS, an Editor for IEEE POWER ENGINEERING LETTERS, a Regional Editor for *IET Renewable Power Generation* and an Associate Editor for *IET Power Electronics Journals*.

Bashar Zahawi (Senior Member, IEEE) received the B.Sc. and Ph.D. degrees in electrical and electronic engineering from Newcastle University, Newcastle upon Tyne, U.K., in 1983 and 1988, respectively.

From 1988 to 1993, he was a Design Engineer with a U.K. manufacturer of large variable speed drives and other power conversion equipment. He was appointed as a Lecturer in Electrical Engineering with the University of Manchester, Manchester, U.K., in 1994 and was a Senior Lecturer with the School of Electrical and Electronic Engineering, Newcastle University, from 2003 to 2014. Since 2014, he has been with the Department of Electrical and Computer Engineering, Khalifa University, Abu Dhabi, United Arab Emirates, where he is currently a Professor of electrical power engineering. His research interests include power conversion, renewable energy, optimization methods, and the application of nonlinear dynamical methods to electrical circuits and systems.

Dr. Zahawi was a recipient of the Crompton Premium awarded by the Institution of Electrical Engineers, U.K., and the Denny Medal awarded by the Institute of Marine Engineering, Science and Technology. He is past Chairman of the IEEE Power and Energy Society United Arab Emirates Chapter.

Khalifa Al Hosani (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Notre Dame, Notre Dame, IN, USA, in 2005 and 2007, respectively, and the Ph.D. degree in electrical and computer engineering from Ohio State University, Columbus, OH, USA, in 2011.

He is currently an Associate Professor with the Department of Electrical and Computer Engineering, Khalifa University, Abu Dhabi, United Arab Emirates. He is the Co-Founder of the Power Electronics and Advanced Sustainable Energy Center Laboratory, ADNOC Research and Innovation Center, Abu Dhabi. His research interests include a wide range of topics including nonlinear control, sliding mode control, control of power electronics, power systems stability and control, renewable energy systems modeling and control, smart grid, microgrid and distributed generation, and application of control theory to oil and gas applications.

Ashraf Ali Khan (Member, IEEE) received the B.E. (with hons.) degree in electronics engineering from the National University of Sciences and Technology (NUST), Islamabad, Pakistan, in 2012, and the M.S. combined Ph.D. degree in energy engineering (majoring in power electronics) from Kyungpook National University, Daegu, South Korea, in 2018.

From 2018 to 2020, he was a Postdoctoral Researcher and a Teaching Fellow with the University of British Columbia, Canada. He also worked as a Professor with the Okanagan College of Technology. He has been working as an Assistant Professor with the Memorial University of Newfoundland, St. John's, NL, Canada. His current research interests include high-efficiency grid-connected photovoltaic inverters, energy systems, and power factor correction circuits.

Dr. Khan was a recipient of the IEEE Best Paper Award in 2015 and the Best Researcher Awards from BK in 2015, 2016, and 2017. He has also received scholarships and awards from NICT R&D Fund Pakistan, NUST, Kyungpook National University, and BISE SWAT. He is the author or coauthor of more than 41 technical papers published in various IEEE international conferences and IEEE journals. He has served as a Chairperson at several IEEE conferences and serves as a reviewer for more than 20 international journals and conferences.