Simplified Modeling and Control of a GaN Switched-Capacitor Converters With Phase Shift Modulation

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***Abstract*—This article focuses on the modeling of a novel switched-capacitor converter with phase shift modulation, which is proposed in the previous work. This switched-capacitor converter can realize high voltage gain with high efficiency and power density based on its modular topology. However, it is difficult to build the accurate and standard models for the general form with any number of modules as the numerous passive components will result in a high order model. This problem limits the voltage regulation ability and dynamic performance of switched-capacitor converter, especially for high voltage gain application. In this article, the general steady-state model is first derived. Then, the relationship between the order of dynamic model based on the conventional method and the number of modules in converter is derived to illustrate the complexity and high computational cost. Therefore, a simplified modeling method is proposed, which can reduce the order and complexity of the system, and has considerable consistency compared with precise model. The approximate modeling method can be easily applied on general form of the converter and is friendlier for controller design. Simulation verifies the theoretical correctness of the modeling. And experiment on a prototype whose controller is designed according to the model proves the practicability.**

***Index Terms*—Average small signal model, dynamic modeling, phase shift modulation, switched-capacitor converter.**

I. Introduction

IN THE application that requires high voltage gain, like data center and electric vehicle [1], switched-capacitor converter (SCC) has some unique features and advantages [2]–[4] compared with typical isolated converter. The SCC needs no transformer to step up/down voltage. The magnetic loss is eliminated in SCC. And the weight and volume of magnetic cores is also cut down. The cost and design complexity of SCC is also reduced without magnetic components and relevant radiator. Besides, in the isolated converter with high voltage gain, the switches in low voltage side bear high current stress, which means high conduction loss or else complex parallel design. In SCC, with appropriate topology and modulation method, the current stress of switches can be much lower and uniform, which results in a superior conduction loss. Therefore, it is naturally easier for SCC to achieve high efficiency and high power density based on its circuit mechanism [5].

After years of development and research, various SCC topologies are proposed, like serial-parallel SCC [6], [7], ladder SCC [8], and Dickson SCC [9], [10]. These SCCs adopt different circuit configuration and switching sequence, as they all have respective advantages in corresponding application field. However, there are still some common inherent problems for SCCs [5], [11]. First, the voltage gain of most of the conventional SCC, like serial-parallel SCC, Fibonacci SCC, and Ladder SCC, can only be integer and is determined by the number of capacitors. The poor voltage regulation ability limits the application of SCC. Second, the absence of inductive components weakens the controllability of current in switching transient process, which means a high current surge peak and EMI problem. Third, switches in traditional SCCs work in hard-switching mode, which cause appreciable switching loss and limits the increasing of switching frequency. On the account of the above, the SCC is always cannot work independently in a convert system and not suitable for high power converter.

To solve these problems, a new class of SCCs, which is called hybrid SCC insert some small inductors into conventional SCCs [12]. These inductors can be air-core inductors or parasitic inductance of PCB wiring, so that the hybrid SCC still takes the advantages from magnet-less feature. On the other hand, these inductors solve the current spike problem and make the current waveform regular and determinable [35]. With corresponding modulation method, the voltage gain can be regulated with duty ratio [36]–[39], switching frequency [42], [48], or phase shift ratio [40]–[42]. Besides, the inductor in hybrid SCC is helpful for realizing soft-switching and higher switching frequency, which can further reduce the volume of inductor and capacitor and improve the power density of hybrid SCC [24]–[26]. Therefore, hybrid SCC becomes more popular in application from hundred watts to thousand watts.

The topology types of conventional SCC are also available for hybrid SCC [13]–[21]. Different topologies have different stress distribution of current and voltage, which influences the efficiency and power density of the converter [12], [25], [33], [34]. For example, in hybrid Dickson SCC, each switch has a low

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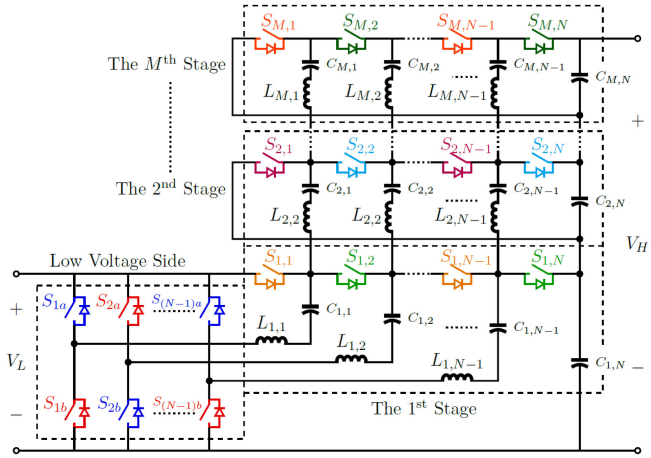

Fig. 1. Proposed SCC in general form.

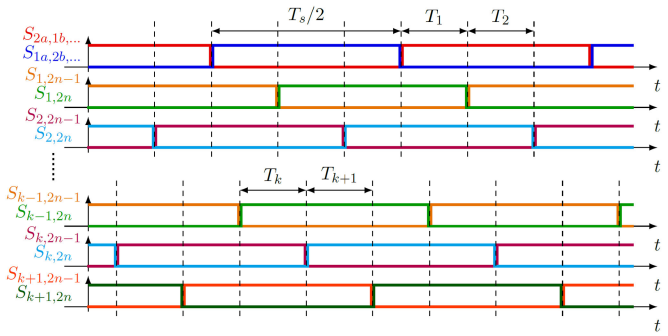

Fig. 2. Waveforms of phase shift modulation.

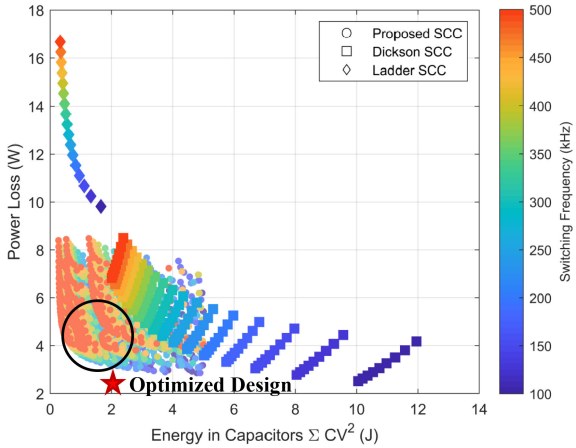

Fig. 3. Comparison with other topologies.

voltage stress and current stress of switches, but the capacitor voltage stress increase with the voltage gain. This feature is not friendly for high power density design in high voltage gain application [21]–[23]. On the contrary, ladder SCC has limited capacitor voltage stress, but larger conduction loss because of high current stress of switches [17]–[19]. By modifying the topology of the standard hybrid SCCs, the component stress can be optimized [26]–[31]. In the previous work [32], a novel SCC topology is proposed to coordinate the contradiction between different topologies. The proposed topology has both low current stress of switches and low voltage stress of capacitor. The switch voltage stress is also limited. Therefore, the proposed SCC can achieve both high efficiency and power density in high voltage gain applications.

Fig. 1 shows the general form of the proposed hybrid SCC. The converter consists of two major parts. At the left, the low voltage side part contains $(N-1)$ half bridges. At the right part, several modular stages stack up from the first stage to the *m*th stage. In each stage, there are N switches, $(N-1)$ *LC* branches and an output capacitor. N and M determine the nominal voltage gain G as (1). For the general form of the proposed SCC, the number of stages M is larger than 2. In the case that $M = 1$, the proposed SCC is equal to a hybrid Dickson SCC. Therefore, the conclusion of this article can be also applied in analysis of hybrid Dickson SCC

$$V_H = ((N-1)M+1) \cdot V_L. \tag{1}$$

On the basis of inserting inductor, different modulation method can be applied on hybrid SCC [37]–[44]. For the proposed SCC, corresponding phase shift modulation method is also proposed in [32]. According to the topology, the phase shift modulation method of the proposed hybrid SCC is also proposed in [32]. The switches are divided into $(M+1)$ groups according to their positions. In each group, switches turn ON complementarily with 50% duty ratio. Fig. 2 illustrates the timing sequential of switches in different groups. The signal of switches in the first stage shifts backward for T_1 from the switches in low voltage side. And the switches in the second stage shift backward for T_2 from the first stage, etc. $(M+1)$ groups correspond to M time delay intervals from T_1 to T_M. Then, the phase shift ratios D_k can be defined as (2). Here, T_{sw} is the switching period

$$D_k = 2T_k/T_{\text{sw}} k = 1, 2, \ldots, M. \tag{2}$$

The more detailed description and analysis of the proposed SCC can be found in [32]. And the comparison of the proposed SCC with Dickson SCC and Ladder is shown in Fig. 3. The horizontal ordinate is the total energy in the capacitors, which indicates the power density of the converter. The vertical coordinate is the total power loss. As the proposed SCC has lower capacitor voltage stress than Dickson SCC and lower switch current stress than Ladder SCC, the proposed SCC can achieve higher power density and efficiency.

To increase the applicability in industrial, SCC is supposed to require nice and stable performance for both steady state and dynamic response. The accuracy steady state and dynamic model are helpful to analysis the characteristic and stability of the SCC and guide the design of parameters in converter and controller. For SCC or hybrid SCC, the number of modules and passive components is proportional to the voltage gain. Therefore, it is important to build unified models for both steady state and dynamic, so that the models can be easily applied for any voltage

gain and the advantage of SCC can be fully taken with the standard design method based on the general steady state and dynamic model.

With the steady-state conditions, the steady-state model can be derived under certain modulation method. For the proposed SCC under phase shift modulation, the connection relationship is complex, as shown in Fig. 1, and there are many switching states in one period, as shown in Fig. 2. In the previous work, the complete steady-state model for the general form of the proposed SCC is not derived yet. In this article, the steady-state model will be proposed with a unified and clear form, which can help to determine the parameters of passive components and phase ratios in each stage.

For dynamic model of SCC, it is difficult to derive the unified model, especially for the hybrid SCC. As the capacitors and inserted inductors compose series resonant loop, the small signal model has complex expressions [45]. For different SCC topologies and modulation method, there has been an amount modeling method. For both conventional SCC without inductors [46], [47] and hybrid SCC [48]–[56], the dynamic models can be built. In general, the modeling for hybrid SCC is more difficult, as there are more passive components and the switching states are more complex with modulations. Although these models are precise, they are all applied on a SCC or hybrid SCC with certain and small number of capacitors. However, to achieve high voltage gain, the SCC is supposed to be extended to any required module numbers. At the same time, the increasing modular means more nonlinear components as capacitors and inserted inductors in hybrid SCC, which increase the order of the equations and mathematical complexity a lot. These difficulties block the modeling for SCCs, which is also a bottleneck for development of SCC.

In this article, based on the proposed hybrid SCC shown in Fig. 1, the complexity and difficulty of the small signal model based on the conventional modeling method is analyzed. Then, an approximate modeling method is proposed to solve the complexity problems. The simplifying process reveals the features of hybrid SCC and has a good accuracy compared with precise model. Therefore, the simplified model can reflect the dynamic characteristics of the proposed SCC well.

As defined in (2), the proposed SCC is a multi-input system with phase ratios for different stages. To realize the closed-loop control, the decoupling method for control variables is also designed in this article. The decoupling method is based on the small signal model, so that the proposed simplified model makes the control loop with the decoupling stage can work on real-time controllers. Both the simplified model and the controller improve the steady state and dynamic performance. The SCC with voltage regulation ability and well dynamic response can work as an independent stage in the power electronic system.

The rest of this article is organized as follows. The steady-state model will be given in Section II. Then, the dynamic model will be derived in Section III. The precise average small signal model will be given at first with the complexity analysis. And the simplifying method will be further proposed. The discussion of the models and the design of controller will be proceeded in Section IV. At last, the experiment configuration and results are shown in Section V to validate the theory. Finally, Section VI concludes this article.

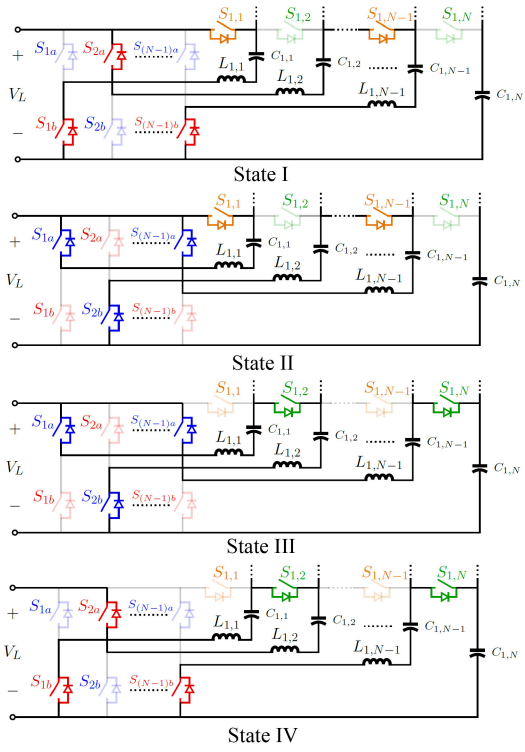

Fig. 4. Four switching states of the first stage.

II. Steady-State Model of SCC

As the proposed SCC can be decomposed into M stages and each stage have N LC branches, the steady-state model can be derived by two steps. At first, the relationship of capacitors and inductors in the same stage can be solved by the balance condition. Then, the relationship among different stages can be solved according to the steady state condition of the output capacitor $C_{k,N}$. And the relationship among input voltage, output voltage, and load can be derived at the same time.

A. Steady-State Analysis in One Stage

In the steady state, the volt-second product of inductor should keep zero in one period. For the inductors in the first stage, the voltages are only determined by the states of the switches in the low voltage side and in the first stage. So, there are four different states, as shown in Fig. 4. And according to the equivalent circuits and volt-second balance condition, the voltage of capacitors in the first stage can be expressed as

$$\begin{bmatrix} 3 & -1 & & & & \\ -1 & 2 & -1 & & & \\ & -1 & 2 & -1 & & \\ & & \ddots & \ddots & \ddots & \\ & & & -1 & 2 & -1 \\ & & & & -1 & 3 \end{bmatrix} \begin{bmatrix} V_{C_{1,1}} \\ V_{C_{1,2}} \\ V_{C_{1,3}} \\ \vdots \\ V_{C_{1,N-2}} \\ V_{C_{1,N-1}} \end{bmatrix} = \begin{bmatrix} V_L \\ 0 \\ 0 \\ \vdots \\ 0 \\ 2V_{C_{1,N}} - V_L \end{bmatrix}. \tag{3}$$

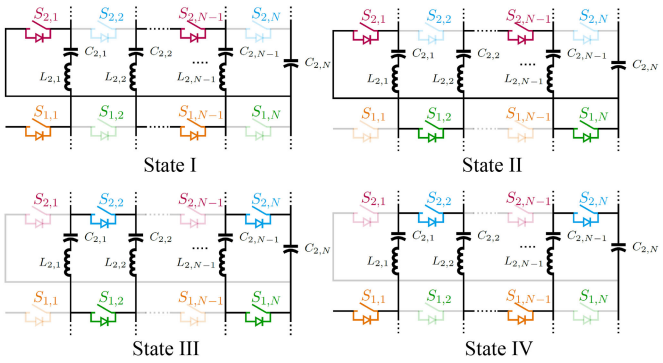

Fig. 5. Four switching states for the second stage.

The equation is independence of the duty ratio D_1. By solving the equation, the capacitor voltage can be expressed with V_L and $V_{C_{1,N}}$ as (4), which constitutes an arithmetic progression

$$V_{C_{1,j}} = \frac{2j-1}{2} V_1^* + \frac{1}{2} V_0^*. \tag{4}$$

Here, V_k^* is the standardized voltage for simplifying the equation

$$V_k^* = \begin{cases} V_L & k = 0 \\ \frac{V_{C_{1,N}} - V_L}{N-1} & k = 1 \\ \frac{V_{C_{k,N}}}{N-1} & k > 1 \end{cases}. \tag{5}$$

From the second stage to *m*th stage, there are also four switching states, as shown in Fig. 5. And the voltage of inductors is the combination of the adjacent capacitor in the same stage and the voltage from the previous stage. As the voltage of capacitor in the first stage is an arithmetic progression, the voltage from the previous stage is same for each inductor. Therefore, the voltage relationship in the *k*th, where k is larger than 2, can be expressed as

$$\begin{bmatrix} 3 & -1 & & & & \\ -1 & 2 & -1 & & & \\ & -1 & 2 & -1 & & \\ & & \ddots & \ddots & \ddots & \\ & & & -1 & 2 & -1 \\ & & & & -1 & 3 \end{bmatrix} \begin{bmatrix} V_{C_{k,1}} \\ V_{C_{k,2}} \\ V_{C_{k,3}} \\ \vdots \\ V_{C_{k,N-2}} \\ V_{C_{k,N-1}} \end{bmatrix} = (N-1) \begin{bmatrix} 2V_{k-1}^* \\ 0 \\ 0 \\ \vdots \\ 0 \\ 2V_k^* \end{bmatrix}. \tag{6}$$

Then, the steady-state voltage of capacitors in the *LC* branches of each stage can be final derived

$$V_{k,j} = \begin{cases} \frac{2j-1}{2} V_1^* + \frac{1}{2} V_0^* & 1 \le j < N, k = 1 \\ \frac{2j-1}{2} V_k^* + \frac{2(N-j)-1}{2} V_{k-1}^* & 1 \le j < N, 2 \le k \le M \end{cases}. \tag{7}$$

And the current change rate of inductors in the steady state can be also calculated. As the capacitor voltage sequence in each stage is all arithmetic, the current change rate is same in one stage

$$\frac{\mathrm{d}i_{L_{k,j},\mathrm{I}}}{\mathrm{d}t} = -\frac{\mathrm{d}i_{L_{k,j},\mathrm{III}}}{\mathrm{d}t} = \frac{V_k^* - V_{k-1}^*}{2L_k} \cdot (-1)^j$$
$$\frac{\mathrm{d}i_{L_{k,j},\mathrm{II}}}{\mathrm{d}t} = -\frac{\mathrm{d}i_{L_{k,j},\mathrm{IV}}}{\mathrm{d}t} = \frac{V_k^* + V_{k-1}^*}{2L_k} \cdot (-1)^j.$$

And the capacitors in each *LC* branches should keep the charge balance in one period. Then, the initial current in one period of any inductor $L_{k,j}$ can be solved as (8). The current expressions of inductors can, then, be obtained

$$\begin{aligned} i_{L_{k,j},0} &= -\frac{\frac{\mathrm{d}i_{L_{k,j},\mathrm{I}}}{\mathrm{d}t} \cdot (1 - D_k) + \frac{\mathrm{d}i_{L_{k,j},\mathrm{II}}}{\mathrm{d}t} \cdot D_k}{4f_s} \\ &= -\frac{V_k^* - V_{k-1}^* (1 - 2D_k)}{8 f_s L_k} \cdot (-1)^j. \end{aligned} \tag{8}$$

B. Steady-State Analysis Among Different Stages

The next step of steady-state modeling can focus on the relationship between phase shift ratio D_k, high side voltage V_H, and output power. The high side voltage is stacked by the output capacitors $C_{k,N}$, which can be analyzed by charge balance condition. Fig. 7 shows the current paths connected to $C_{k,N}$. There are five capacitors will exchange charge with $C_{k,N}$ and the total charge should be zero in one steady state period. Specially, $C_{k+1,N}$ should also obey the ampere-second balance rule, which means the sum charge flowing from $C_{k+1,N}$ to $C_{k,N}$ is zero. So, there remains four capacitors $C_{k,N-1}$, C_{k+11}, $C_{k+1,N-1}$, and C_{k+21} contribute charge to $C_{k,N}$ indeed. The current of these capacitors in *LC* branches are equal to the inductors in series with them, and in which states the current will flow into $C_{k,N}$ is controlled by switches $S_{k,N}$ and S_{k+11}.

According to the current expressions derived from steady-state analysis of each stage, the current integral of these four capacitors in available half period can be expressed as follow:

$$\begin{aligned} &\int_{T_s/2} i_{C_{k,N-1}} = \frac{D_k (1 - D_k)}{8 f_s^2 L_k} \cdot V_{k-1}^*; \int_{T_s/2} i_{C_{k+1,N-1}} \\ &= \frac{D_{k+1} (1 - D_{k+1})}{8 f_s^2 L_{k+1}} \cdot V_{k+1}^* \\ &\int_{T_s/2} i_{C_{k+1,1}} = \frac{D_{k+1} (1 - D_{k+1})}{8 f_s^2 L_{k+1}} \cdot V_k^*; \int_{T_s/2} i_{C_{k+2,1}} \\ &= \frac{D_{k+2} (1 - D_{k+2})}{8 f_s^2 L_{k+2}} \cdot V_{k+2}^*. \end{aligned} \tag{9}$$

The coefficient of V_k^* contains the inductance value L_k and phase shift ratio D_k of the corresponding stage, which has the dimension of capacitance. To simplify the expression, the equivalent capacitance C_k^* can be defined as

$$C_k^* = \frac{D_k (1 - D_k)}{8 f_s^2 L_k}. \tag{10}$$

Sum four items with signs according to the direction of current, the ampere-second balance equation of output capacitor C_k can be obtained

$$C_k^* V_{k-1}^* - C_{k+1}^* \left(V_k^* + V_{k+1}^*\right) + C_{k+2}^* V_{k+2}^* = 0. \tag{11}$$

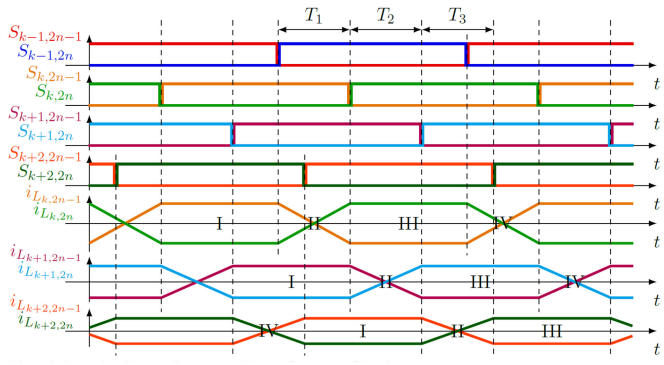

Fig. 6. Steady-state current waveforms of inductors.

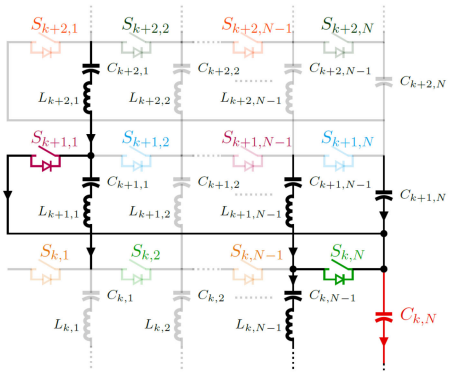

Fig. 7. Current path flowing to $C_{k,N}$.

For special $k = M-1$, there is no the $(M-1+2)$th stage, so the equation will degenerate to

$$C^*_{M-1}V^*_{M-2} - C^*_M\left(V^*_{M-1} + V^*_M\right) = 0. \tag{12}$$

And for $k = M$, there are no capacitors from other stages but the output current I_H. A fixed resistor R is supposed to connect with high side voltage V_H. So, the equation for the Mth stage changes to

$$C^*_M V^*_{M-1} - \frac{V_H}{f_s R} = 0. \tag{13}$$

The V_H can be further expressed with the standardized voltage of each stage

$$V_H = V_L + (N-1)\sum_{k=1}^{M} V^*_k. \tag{14}$$

Thus, all the ampere-second balance equations of the whole converter can be merged into the matrix form as (15) shown at the bottom of this page. The equation indicates the relationship of different stages in the converter and how the phase shift ratios will influence the voltage of each stage. Although the topology of the proposed hybrid SCC seems complex, the steady-state analysis illustrates inherent regularity as the brief and unified equations, which is help to the design of inductances and phase shift ratio for certain voltage gain and load

III. Dynamic Model of SCC

A. Complexity of Conventional Small Signal Model

In order to improve the dynamic performance and realize closed-loop control, it is essential to build the dynamic model for SCC and further design the controller. The conventional average small signal modeling method can be adopted to obtain the dynamic model of the proposed SCC. However, the number of passive components will increase with N and M. This section will illustrate the complexity of the conventional model first.

Similarly, small signal modeling starts from each single stage. For the first stage, according to steady-state equation in (3), and exerting perturbation, the small signal average current change rate in one period can be expressed as

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} \hat{i}_{L_{1,1}} \\ \hat{i}_{L_{1,2}} \\ \hat{i}_{L_{1,3}} \\ \vdots \\ \hat{i}_{L_{1,N-2}} \\ \hat{i}_{L_{1,N-1}} \end{bmatrix} = \frac{1}{4L_1}\begin{bmatrix} -3 & 1 & & & & \\ 1 & -2 & 1 & & & \\ & 1 & -2 & 1 & & \\ & & \ddots & \ddots & \ddots & \\ & & & 1 & -2 & 1 \\ & & & & 1 & -3 \end{bmatrix}\begin{bmatrix} \hat{v}_{C_{1,1}} \\ \hat{v}_{C_{1,2}} \\ \hat{v}_{C_{1,3}} \\ \vdots \\ \hat{v}_{C_{1,N-2}} \\ \hat{v}_{C_{1,N-1}} \end{bmatrix} + \begin{bmatrix} \hat{v}_L \\ 0 \\ 0 \\ \vdots \\ 0 \\ 2\hat{v}_{C_{1,N-1}} - \hat{v}_L \end{bmatrix}. \tag{16}$$

$$\begin{bmatrix} C^*_1 & -C^*_2 & -C^*_2 & C^*_3 & & & & & \\ & C^*_2 & -C^*_3 & -C^*_3 & C^*_4 & & & & \\ & & \ddots & \ddots & \ddots & \ddots & & & \\ & & & C^*_k & -C^*_{k+1} & -C^*_{k+1} & C^*_{k+2} & & \\ & & & & \ddots & \ddots & \ddots & \ddots & \\ & & & & & C^*_{M-2} & -C^*_{M-1} & -C^*_{M-1} & C^*_M \\ & & & & & & C^*_{M-1} & -C^*_M & -C^*_M \\ -\frac{1}{f_s R} & -\frac{N-1}{f_s R} & \cdots & \cdots & \cdots & \cdots & -\frac{N-1}{f_s R} & C^*_M - \frac{N-1}{f_s R} & -\frac{N-1}{f_s R} \end{bmatrix}\begin{bmatrix} V^*_0 \\ V^*_1 \\ V^*_2 \\ \vdots \\ V^*_k \\ \vdots \\ V^*_{M-2} \\ V^*_{M-1} \\ V^*_M \end{bmatrix} = \mathbf{0} \tag{15}$$

And then the small signal average voltage change of capacitors in the first stage can be derived. For capacitors from C_{11} to $C_{1,N-1}$ that are in *LC* branches, the equations contain second order terms, as shown in (17). In the coefficient matrix, $\langle s^n \rangle$ represents the polynomial with maximum order n and the specific expressions are omitted as the order of model is mainly concerned

$$\begin{bmatrix} \langle s^2\rangle & \langle s^1\rangle & & & & \\ \langle s^1\rangle & \langle s^2\rangle & \langle s^1\rangle & & & \\ & \langle s^1\rangle & \langle s^2\rangle & \langle s^1\rangle & & \\ & & \ddots & \ddots & \ddots & \\ & & & \langle s^1\rangle & \langle s^2\rangle & \langle s^1\rangle \\ & & & & \langle s^1\rangle & \langle s^2\rangle \end{bmatrix} \begin{bmatrix} \hat{v}_{C_{1,1}} \\ \hat{v}_{C_{1,2}} \\ \hat{v}_{C_{1,3}} \\ \vdots \\ \hat{v}_{C_{1,N-2}} \\ \hat{v}_{C_{1,N-1}} \end{bmatrix} = \begin{bmatrix} \langle s^1\rangle \\ \langle s^1\rangle \\ \langle s^1\rangle \\ \vdots \\ \langle s^1\rangle \\ \langle s^1\rangle \end{bmatrix} \hat{v}_L + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ \langle s^1\rangle \end{bmatrix} \hat{v}_{C_{1,N}} + \begin{bmatrix} \langle s^1\rangle \\ \langle s^1\rangle \\ \langle s^1\rangle \\ \vdots \\ \langle s^1\rangle \\ \langle s^1\rangle \end{bmatrix} \hat{d}_1. \tag{17}$$

This solution of $\hat{v}_{C_{1,j}}$ can be solved by the tridiagonal matrix algorithm as (18). The order of (18) is linear with the number of capacitors in one stage

$$\hat{v}_{C_{1,j}} = \frac{\langle s^{2N-3}\rangle}{\langle s^{2N-2}\rangle}\hat{v}_L + \frac{\langle s^{2N-3}\rangle}{\langle s^{2N-2}\rangle}\hat{v}_{C_{1,N}} + \frac{\langle s^{2N-3}\rangle}{\langle s^{2N-2}\rangle}\hat{d}_1. \tag{18}$$

However, for the second stage, the small signal expressions are related with $\hat{v}_{C_{1,j}}$ and $\hat{i}_{L_{1,j}}$ in the first stage, which is not similar with the steady-state analysis as the $\hat{v}_{C_{1,j}}$ is not an arithmetic sequence in this small signal modeling. With the similar solving process, the order of $\hat{v}_L$, $\hat{v}_{C_{1,N}}$, and $\hat{d}_1$ in the expressions for $\hat{v}_{C_{2,j}}$ will double. For the *k*th stage, the order will further increase as chain relation. And the expressions for $\hat{v}_{C_{k,j}}$ is as following:

$$\hat{v}_{C_{k,j}} = \sum_{m=1}^{k}\left(\frac{\langle s^{(k-m+1)(2N-3)}\rangle}{\langle s^{(k-m+1)(2N-2)}\rangle}\hat{v}_{C_{m,N}} + \frac{\langle s^{(k-m+1)(2N-3)}\rangle}{\langle s^{(k-m+1)(2N-2)}\rangle}\hat{d}_m\right) + \frac{\langle s^{(k-m+1)(2N-3)}\rangle}{\langle s^{(k-m+1)(2N-2)}\rangle}\hat{v}_L. \tag{19}$$

The abovementioned expressions describe the small signal model of each stage. Then, the relationship among different stages will be derived. As illustrated in Fig. 7, the current though capacitor $\hat{v}_{C_{k,N}}$ is related with the capacitor in the $(k+1)$th and $(k+2)$th stages. Therefore, the coefficient matrix of equations from $\hat{v}_{C_{1,N}}$ to $\hat{v}_{C_{M,N}}$ can be described as

$$\begin{bmatrix} \frac{\langle s^{3(2N-3)}\rangle}{\langle s^{3(2N-2)}\rangle} & \frac{\langle s^{2(2N-3)}\rangle}{\langle s^{2(2N-2)}\rangle} & \frac{\langle s^{(2N-3)}\rangle}{\langle s^{(2N-2)}\rangle} & & \\ \frac{\langle s^{4(2N-3)}\rangle}{\langle s^{4(2N-2)}\rangle} & \frac{\langle s^{3(2N-3)}\rangle}{\langle s^{3(2N-2)}\rangle} & \frac{\langle s^{2(2N-3)}\rangle}{\langle s^{2(2N-2)}\rangle} & \frac{\langle s^{(2N-3)}\rangle}{\langle s^{(2N-2)}\rangle} & \\ \vdots & \vdots & \vdots & \ddots & \\ \frac{\langle s^{(M+1)(2N-3)}\rangle}{\langle s^{(M+1)(2N-2)}\rangle} & \cdots & \cdots & \cdots & \frac{\langle s^{2(2N-3)}\rangle}{\langle s^{2(2N-2)}\rangle} \\ \frac{\langle s^{(M+2)(2N-3)}\rangle}{\langle s^{(M+2)(2N-2)}\rangle} & \cdots & \cdots & \cdots & \frac{\langle s^{3(2N-3)}\rangle}{\langle s^{3(2N-2)}\rangle} \end{bmatrix}. \tag{20}$$

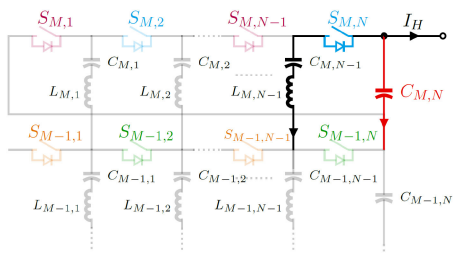

Fig. 8. Current path of $C_{M,N}$.

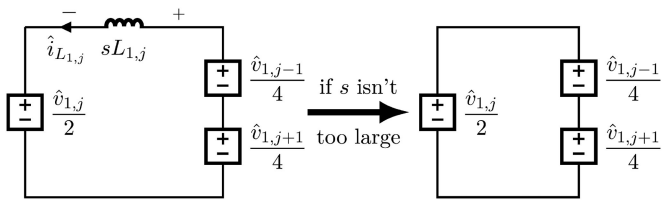

Fig. 9. Equivalent circuit of small signal equations about inductor and its simplified version.

This matrix should be solved by LU factorization or Gauss elimination method. With multiple iterations, the order of the solutions will increase with number of stages M as exponential relation. The small signal response of the output capacitor in the *k*th stage $\hat{v}_{C_{k,N}}$ can be solved as the function of the small signal perturbation of low side voltage $\hat{v}_L$ and the phase shift ratios of each stage. And the small signal response of high side voltage $\hat{v}_H$ can be obtained by sum up the $\hat{v}_{C_{k,N}}$, which is like the steady-state model

$$\hat{v}_{C_{k,N}} = f\left(\hat{v}_L, \hat{d}_1, \ldots, \hat{d}_k\right)$$

$$\hat{v}_H = \sum_{k=1}^{M}\hat{v}_{C_{k,N}} \tag{21}$$

$$\deg\left(f\left(\hat{v}_L, \hat{d}_1, \ldots, \hat{d}_k\right)\right) = a \cdot c^M \cdot (N+b). \tag{22}$$

However, the order of the final expression increases too rapidly. For example, if $N = 3$ and $M = 2$, the order of small signal model will larger than one hundred. To realize a higher voltage gain, the order of the model will be higher. Although the conventional small signal modeling method is precise, the complexity makes the modeling process very difficult and blocks the dynamic analysis of high voltage gain SCC.

B. Simplifying Method of Small Signal Modeling

The conventional small signal modeling method is precise but complex. The high order and high computation cost stop the dynamic analysis and optimization for high voltage gain SCCs. Therefore, a simplified modeling method is proposed.

Consider (16) of average inductor current change rate at first. The equation can be converted to an equivalent circuit, as shown in Fig. 9. The left side of the equation is the inductor $L_{1,j}$ and the right side is three controlled voltage sources. The voltage

across the inductor can be calculated as (23). In the proposed SCC or hybrid Dickson SCC, the inserting inductor has a very small value, which is usually tens of nH. And in the small signal analysis, the frequency range depends on the required bandwidth of controller, will not be too high. Thus, $\hat{v}_{L_{1,j}}$ is always much smaller than the controlled voltage sources and can be regard as zero in the circuit. The equation now can be simplified as (23), and the corresponding equivalent circuit is shown in the right of Fig. 9

$$\hat{v}_{L_{1,j}} = \hat{i}_{L_{1,j}} \cdot sL_1 \tag{23}$$

$$\hat{v}_{C_{1,j-1}} - 2\hat{v}_{C_{1,j}} + \hat{v}_{C_{1,j+1}} = 0. \tag{24}$$

The new approximate equation, which comes from the equivalent circuit has similar form with the steady-state equation, and can be extended to all the inductors in the first stage. In this way, the relationship of the small signal capacitor voltage can be expressed with a similar matrix

$$\begin{bmatrix} -3 & 1 & & & & \\ 1 & -2 & 1 & & & \\ & 1 & -2 & 1 & & \\ & & \ddots & \ddots & \ddots & \\ & & & 1 & -2 & 1 \\ & & & & 1 & -3 \end{bmatrix} \begin{bmatrix} \hat{v}_{C_{1,1}} \\ \hat{v}_{C_{1,2}} \\ \hat{v}_{C_{1,3}} \\ \vdots \\ \hat{v}_{C_{1,N-2}} \\ \hat{v}_{C_{1,N-1}} \end{bmatrix} = \begin{bmatrix} \hat{v}_L \\ 0 \\ 0 \\ \vdots \\ 0 \\ 2\hat{v}_{C_{1,N-1}} - \hat{v}_L \end{bmatrix}. \tag{25}$$

The solution of this equation also has the structure of arithmetic progressions, which means some conclusions can be extended in the small signal analysis

$$\hat{v}_{C_{1,j}} = \frac{2j-1}{2}\hat{v}_1^* + \frac{1}{2}\hat{v}_0^*. \tag{26}$$

The simplifying method can be adopted in other stages by making the small signal voltage across the inductor zero in the corresponding equivalent circuit. And as mentioned in Section III-A, by conventional small signal modeling, the expressions of $\hat{v}_{C_{k,j}}$ are related with the small signal expressions of other passive components, which is one of the reasons of the increment of the order. As the expressions obtained by proposed simplified small signal model method are arithmetic, the voltage difference of two adjacent point will be same as in the steady state. Therefore, the equations can be directly listed without discriminating different cases

$$\begin{bmatrix} -3 & 1 & & & & \\ 1 & -2 & 1 & & & \\ & 1 & -2 & 1 & & \\ & & \ddots & \ddots & \ddots & \\ & & & 1 & -2 & 1 \\ & & & & 1 & -3 \end{bmatrix} \begin{bmatrix} \hat{v}_{C_{k,1}} \\ \hat{v}_{C_{k,2}} \\ \hat{v}_{C_{k,3}} \\ \vdots \\ \hat{v}_{C_{k,N-2}} \\ \hat{v}_{C_{k,N-1}} \end{bmatrix} = (N-1) \begin{bmatrix} 2\hat{v}_{k-1}^* \\ 0 \\ 0 \\ \vdots \\ 0 \\ 2\hat{v}_k^* \end{bmatrix}. \tag{27}$$

Then, the small signal expressions for voltage of capacitors in each *LC* branches can be obtained, which is also arithmetic and the coefficient has no complex frequency s. The approximate method makes the use of the inductance-less feature of SCC and the small signal condition, which is credible and reasonable. Compared with precise small signal model, by ignoring the inductor voltage term in the equation because of the little inductance, the differential equation converts to algebraic equation. And the result has regular forms and the order can be reduced to zero

$$\hat{v}_{C_{k,j}} = \frac{2j-1}{2}\hat{v}_k^* + \frac{2(N-j)-1}{2}\hat{v}_{k-1}^*. \tag{28}$$

With the relationship of small signal capacitor voltage, the small signal inductor current change rate in each switching state can be calculated, which has a unified form for each inductor in each stage

$$\frac{\mathrm{d}\hat{i}_{L_{k,j},\mathrm{I}}}{\mathrm{d}t} = -\frac{\mathrm{d}\hat{i}_{L_{k,j},\mathrm{III}}}{\mathrm{d}t} = \frac{\hat{v}_k^* - \hat{v}_{k-1}^*}{2L_k} \cdot (-1)^j$$

$$\frac{\mathrm{d}\hat{i}_{L_{k,j},\mathrm{II}}}{\mathrm{d}t} = -\frac{\mathrm{d}\hat{i}_{L_{k,j},\mathrm{IV}}}{\mathrm{d}t} = \frac{\hat{v}_k^* + \hat{v}_{k-1}^*}{2L_k} \cdot (-1)^j. \tag{29}$$

However, integrating these change rates cannot get the expression of $\hat{i}_{L_{k,j}}$, as the premise of deriving these change rates is assuming $\hat{i}_{L_{1,j}} \cdot s\, L_{1,j} = 0$. The next step focus on the small signal voltage change rate of capacitors in *LC* branches. By integrating the current of inductor, perturbation, and linearization, the capacitor voltage change rate in each stage can fit into one expression

$$C_k \left\langle \frac{\mathrm{d}\hat{v}_{C_{k,j}}}{\mathrm{d}t} \right\rangle = \hat{i}_{L_{k,j}} + \frac{2\hat{v}_k^* - (2-4D_k)\,\hat{v}_{k-1}^* + 4V_{k-1}^*\hat{d}_k}{16 f_s L_k} \cdot (-1)^j. \tag{30}$$

According to (30), another equivalent circuit can be built, as shown in Fig. 10. In the equivalent circuit, three controlled current source and a current source are parallel with the capacitor $C_{k,j}$. As the expressions of the small signal voltage $\hat{v}_{C_{k,j}}$ is already known, the small signal current of inductor $\hat{i}_{L_{k,j}}$ now can be solved according to the equivalent circuit and can be used in the further derivation

$$\begin{aligned} \hat{i}_{L_{1,j}} = & \left[\frac{2j-1}{2}C_1 s - \frac{2(-1)^j}{16 f_s L_1}\right]\hat{v}_1^* \\ & + \left[\frac{1}{2}C_1 s + \frac{(2-4D_1)(-1)^j}{16 f_s L_1}\right]\hat{v}_0^* - \frac{4V_0^*(-1)^j}{16 f_s L_1}\hat{d}_1 \\ \hat{i}_{L_{k,j}} = & \left[\frac{2j-1}{2}C_k s - \frac{2(-1)^j}{16 f_s L_k}\right]\hat{v}_k^* \\ & + \left[\frac{2(N-j)-1}{2}C_k s + \frac{(2-4D_k)(-1)^j}{16 f_s L_k}\right]\hat{v}_0^* \\ & - \frac{4V_{k-1}^*(-1)^j}{16 f_s L_k}\hat{d}_k. \end{aligned} \tag{31}$$

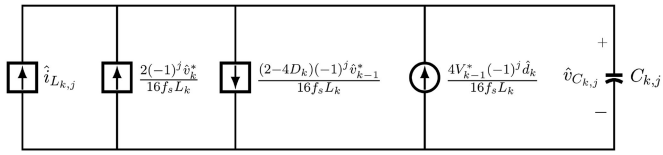

Fig. 10. Equivalent circuit of small signal equations about capacitor.

The last step is solving out the small signal voltage of output capacitors in each stage. Same as the steady state, the output capacitor $C_{k,N}$ is connected with five other capacitors as $C_{k,N-1}$, $C_{k+1,N-1}$, $C_{k+1,N}$, C_{k+11}, and C_{k+21}. The small signal average current change of capacitors in *LC* branches can be obtained by integrating the current of corresponding inductors $\hat{i}_{L_{k,j}}$ according to different switching states. Then, the expressions of $\hat{i}_{C_{k,j}}$ in different half period can be merged into one expression, which contains only small signal voltage terms, (32) shown at bottom of this page.

And the average small signal current from $C_{k+1,N}$ can be directly expressed with the average voltage change rate of $C_{k+1,N}$

$$\left\langle \hat{i}_{C_{k+1,N}} \right\rangle_{T_s} = C_{k+1} \left\langle \frac{\mathrm{d}\hat{v}_{C_{k+1,N}}}{\mathrm{d}t} \right\rangle = C_{k+1} s \hat{v}_{C_{k+1,N}}. \quad (33)$$

For $k = M-1$, it is same that the term $\langle \hat{i}_{C_{k+21}} \rangle_{\frac{T_s}{2}}$ is missed. And for $k = M$, the small signal current of load can also be expressed as

$$\hat{i}_{\mathrm{Load}} = \frac{1}{R}\left[\hat{v}_L + (N-1)\sum_{k=1}^{M} \hat{v}_k^*\right]. \quad (34)$$

Sum up the small signal current terms with the sign according to the current flowing direction, the equation about small signal capacitor voltage change rate of $C_{k,N}$ can be obtained

$$\begin{aligned} C_k \left\langle \frac{\mathrm{d}\hat{v}_{C_{k,N}}}{\mathrm{d}t} \right\rangle &= -\left\langle \hat{i}_{C_{k,N-1}} \right\rangle_{\frac{T_s}{2}} + \left\langle \hat{i}_{C_{k+1,N-1}} \right\rangle_{\frac{T_s}{2}} \\ &- \left\langle \hat{i}_{C_{k+1,1}} \right\rangle_{\frac{T_s}{2}} \\ &+ \left\langle \hat{i}_{C_{k+2,1}} \right\rangle_{\frac{T_s}{2}} + \left\langle \hat{i}_{C_{k+1,N}} \right\rangle_{T_s}. \end{aligned} \quad (35)$$

In order to simplify the final equations, some intermediate variables are defined to replace the long expressions. The coefficient of one order terms has the dimension of capacitance. By unfolding the small signal voltage expressions, an average capacitance vector can be defined for each stage

$$\bar{\boldsymbol{C}}_{\boldsymbol{1}}^* = \begin{bmatrix} \bar{C}_{1,0}^* \\ \bar{C}_{1,1}^* \\ \bar{C}_{1,2}^* \\ \bar{C}_{1,3}^* \end{bmatrix} = \frac{1}{4}\begin{bmatrix} -5C_1 \\ -(2N-4)C_2 - (6N-7)C_1 \\ (2N-3)C_3 + (6N-8)C_2 \\ C_3 \end{bmatrix} \quad (36)$$

$$\bar{\boldsymbol{C}}_{\boldsymbol{k}}^* = \begin{bmatrix} \bar{C}_{k,k-1}^* \\ \bar{C}_{k,k}^* \\ \bar{C}_{k,k+1}^* \\ \bar{C}_{k,k+2}^* \end{bmatrix} = \frac{1}{4}\begin{bmatrix} -C_k \\ -(2N-4)C_{k+1} - (6N-7)C_k \\ (2N-3)C_{k+2} + (6N-8)C_{k+1} \\ C_{k+2} \end{bmatrix}. \quad (37)$$

And the coefficient of zero order term about small signal voltage has the dimension of conductance, which can be defined as Y_k^*. And the coefficient of small signal phase shift ratio $\hat{d}_k$ has the dimension of current, which can be defined as I_k^*

$$\begin{aligned} Y_k^* &= \tfrac{D_k(1-D_k)}{8f_sL_k} I_{k,k}^* = \tfrac{(1-2D_k)V_{k-1}^*}{8f_sL_k} \\ I_{k,k+1}^* &= \tfrac{(1-2D_{k+1})\left(V_{k+1}^* + V_k^*\right)}{8f_sL_{k+1}} I_{k,k+2}^* = \tfrac{(1-2D_{k+2})V_{k+2}^*}{8f_sL_{k+2}}. \end{aligned} \quad (38)$$

Then, the matrix contains the small signal model of the whole SCC can be expressed as

$$\left(\bar{\boldsymbol{C}}^* s + \boldsymbol{Y}^*\right)\begin{bmatrix} \hat{v}_L \\ \hat{\boldsymbol{v}}^* \end{bmatrix} + \boldsymbol{I}^* \hat{\boldsymbol{d}} = \boldsymbol{0}. \quad (39)$$

Here, $\hat{\boldsymbol{v}}^*$ and $\hat{\boldsymbol{d}}^*$ is the column vector of the small signal voltage and phase shift ratio perturbation. And the coefficient matrix is the combinations of the intermedia variables defined previously, (40) and (41) shown at the bottom of next page and (42) following after bottom of next page.

It can be seen that, in the proposed simplified small signal model, the order is independent with the number of *LC* branches N, and the coefficient matrix is clearer and has much lower order, which reduce the complexity a lot and can be applied to high voltage gain more easily.

IV. Discussion of the Dynamic Model

A. Accuracy of the Simplified Model

The basis of the simplify is the little inductance, which coincides the feature of SCC. And as the required frequency range of small signal analysis depends on the controller bandwidth, the impedance of inserting inductor is negligible. Therefore, the proposed simplified method has considerable accuracy. To analyze and verify the dynamic model, transfer functions from the input voltage to the output voltage and from the phase shift ratio to the output voltage are extracted from the dynamic model

$$\begin{aligned} \left\langle \hat{i}_{C_{k,N-1}} \right\rangle_{\frac{T_s}{2}} &= \tfrac{C_k s}{2}\hat{v}_{C_{k,N-1}} - \tfrac{D_k(1-D_k)}{8f_sL_k}\hat{v}_{k-1}^* - \tfrac{(1-2D_k)V_k^*}{8f_sL_k}\hat{d}_k \\ \left\langle \hat{i}_{C_{k+1,N-1}} \right\rangle_{\frac{T_s}{2}} &= \tfrac{C_{k+1} s}{2}\hat{v}_{C_{k+1,N-1}} - \tfrac{D_{k+1}(1-D_{k+1})}{8f_sL_{k+1}}\hat{v}_k^* - \tfrac{(1-2D_{k+1})V_{k+1}^*}{8f_sL_{k+1}}\hat{d}_{k+1} \\ \left\langle \hat{i}_{C_{k+1,1}} \right\rangle_{\frac{T_s}{2}} &= \tfrac{C_{k+1} s}{2}\hat{v}_{C_{k+1,1}} + \tfrac{D_{k+1}(1-D_{k+1})}{8f_sL_{k+1}}\hat{v}_k^* + \tfrac{(1-2D_{k+1})V_k^*}{8f_sL_{k+1}}\hat{d}_{k+1} \\ \left\langle \hat{i}_{C_{k+2,1}} \right\rangle_{\frac{T_s}{2}} &= \tfrac{C_{k+2} s}{2}\hat{v}_{C_{k+2,1}} + \tfrac{D_{k+2}(1-D_{k+2})}{8f_sL_{k+2}}\hat{v}_{k+2}^* + \tfrac{(1-2D_{k+2})V_{k+2}^*}{8f_sL_{k+2}}\hat{d}_{k+2}. \end{aligned} \quad (32)$$

TABLE I
PARAMETERS OF THE PROTOTYPE

Parameter	Value
Topology	$N = 2, M = 2$
Load Resistance R	10.24Ω
Inductor in 1st layer L_1	110nH
Inductor in 2nd layer L_2	220nH
Capacitor in 1st layer $C_{1,1}$~$C_{1,3}$	500μF
Capacitor in 2nd layer $C_{2,1}$~$C_{2,3}$	500μF
Switching frequency f_s	1MHz

TABLE II
PARAMETERS OF THE PROTOTYPE

Parameter	Value
Input voltage V_{in}	12V
Output voltage V_o	60V
Output Power P_o	600W
Inductor in 1st layer L_1	42nH
Inductor in 2nd layer L_2	90nH
Capacitor in 1st layer $C_{1,1}$~$C_{1,3}$	100μF
Capacitor in 2nd layer $C_{2,1}$~$C_{2,3}$	100μF
Switching frequency f_s	300kHz
Switching Device	EPC2024
Half Bridge Driver	LMG1205
Isolated Driver	Si8271
Auxiliary Power Supply	NX1JS0505

$$G_{v_{k,N},v_L} = \frac{\hat{v}_{C_{k,N}}}{\hat{v}_L}; G_{v_H,v_L} = \sum_{k=1}^{M} G_{v_{k,N},v_L}$$

$$G_{v_{k,N},d_k} = \frac{\hat{v}_{C_{k,N}}}{\hat{d}_k}; G_{v_H,d_k} = \sum_{k=1}^{M} G_{v_{k,N},d_k}. \tag{43}$$

Fig. 11 shows the comparison between the precise model and simplified model. The modeling is based on a two-stage SCC with parameters in Table I. There are two transfer functions from input to output of two stages and four transfer functions from phase shift ratio to output. The bode plots of simplified model are almost equal to the precise model. There is only little difference at the high frequency close to 10 kHz. Generally, with reasonable parameters setting and controller bandwidth for the SCC as (44), the simplified model can realize markable accuracy with much less calculation complexity and cost

$$LCf_c^2 < 10. \tag{44}$$

A simulation model is also built in PLECS with the parameters in Table I, to verify the correctness of the mathematical model. A small step signal is exerted to input voltage and phase shift ratios, respectively. And the response is the high side voltage V_H. The simulation applies on a two-stage SCC. Figs. 12–14 show the comparison results with normalized magnitude. The step responses calculated from the transfer functions fit the simulation results well, which verified the dynamic model.

B. Effect of the SCC Parameters

The simplified model not only can be solved faster, but also reveals the relationship between dynamic performance and converter parameters with its more concise expressions.

If $M = 1$, the proposed SCC actually becomes a Dickson SCC with hybrid inductors, as shown in Fig. 15. The transfer function can also be solved out, which is the simplest form and is easy to analyze. The expressions of transfer functions are like a *RC* circuit, which conforms to the magnet-less feature of SCC. The pole point and zero point of the transfer functions is related to N, R, and C. As N and R are always determined by the

$$\bar{\boldsymbol{C}}^* = \begin{bmatrix} \bar{C}^*_{1,0} & \bar{C}^*_{1,1} & \bar{C}^*_{1,2} & \bar{C}^*_{1,3} & & & & & \\ & \bar{C}^*_{2,1} & \bar{C}^*_{2,2} & \bar{C}^*_{2,3} & \bar{C}^*_{2,4} & & & & \\ & & \ddots & \ddots & \ddots & \ddots & & & \\ & & & \bar{C}^*_{k,k-1} & \bar{C}^*_{k,k} & \bar{C}^*_{k,k+1} & \bar{C}^*_{k,k+2} & & \\ & & & & \ddots & \ddots & \ddots & \ddots & \\ & & & & & \bar{C}^*_{M-2,M-3} & \bar{C}^*_{M-2,M-2} & \bar{C}^*_{M-2,M-1} & \bar{C}^*_{M-2,M} \\ & & & & & & \bar{C}^*_{M-1,M-2} & \bar{C}^*_{M-1,M-1} & \bar{C}^*_{M-1,M} \\ & & & & & & & \bar{C}^*_{M,M-1} & \bar{C}^*_{M,M} \end{bmatrix} \tag{40}$$

$$\boldsymbol{Y}^* = \begin{bmatrix} Y^*_1 & -Y^*_2 & -Y^*_2 & Y^*_3 & & & & & \\ & Y^*_2 & -Y^*_3 & -Y^*_3 & Y^*_4 & & & & \\ & & \ddots & \ddots & \ddots & \ddots & & & \\ & & & Y^*_k & -Y^*_{k+1} & -Y^*_{k+1} & Y^*_{k+2} & & \\ & & & & \ddots & \ddots & \ddots & \ddots & \\ & & & & & Y^*_{M-2} & -Y^*_{M-1} & -Y^*_{M-1} & Y^*_M \\ & & & & & & Y^*_{M-1} & -Y^*_M & -Y^*_M \\ -\frac{1}{R} & -\frac{N-1}{R} & \cdots & \cdots & \cdots & \cdots & -\frac{N-1}{R} & Y^*_M - \frac{N-1}{R} & -\frac{N-1}{R} \end{bmatrix} \tag{41}$$

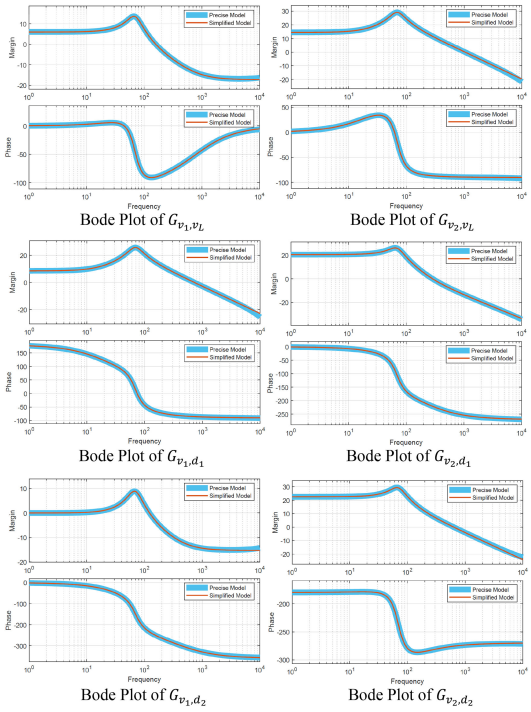

Fig. 11. Comparison of the precise model and the simplified model.

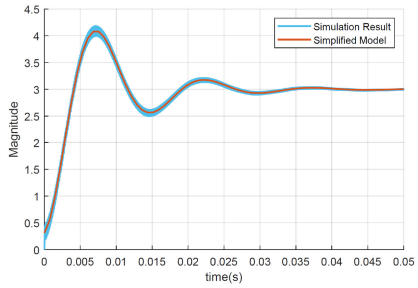

Fig. 12. Step response of G_{v_H,v_L} from simulation and model.

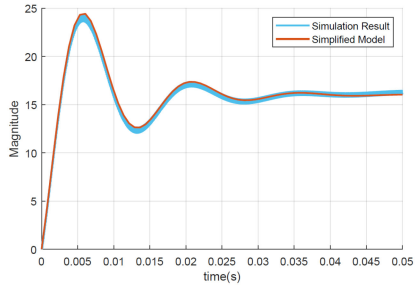

Fig. 13. Step response of G_{v_H,d_1} from simulation and model.

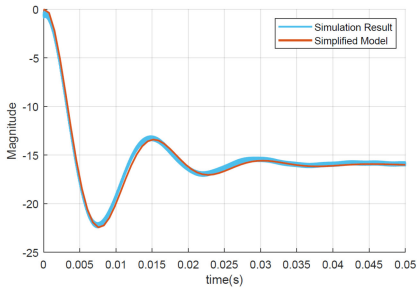

Fig. 14. Step response of G_{v_H,d_2} from simulation and model.

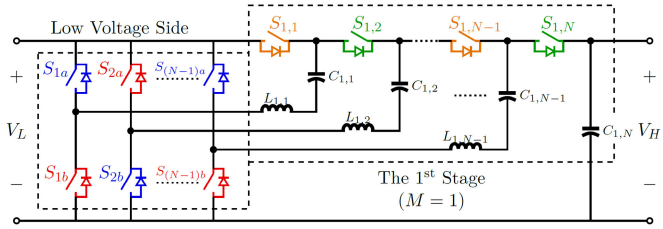

Fig. 15. Step response of G_{v_H,d_2} from simulation and model.

requirement of voltage gain and output power, the capacitance can be adjusted to change the dynamic performance. Fig. 16 shows how the capacitor value influence the bode plot of transfer function G_{v_H,v_L}. With larger capacitors, the crossing frequency will be higher, but the phase margin is same with different capacitor value. As for the transfer function G_{v_H,d_1}, it has the same pole point with the G_{v_H,v_L}, but has no zero point, which is a typical low-pass filter

$$\begin{aligned} G_{v_H,v_L} &= \frac{\frac{N-2}{4(N-1)}RC_1 s + \frac{D_1(1-D_1)R}{8f_s L_1}}{\frac{6N-7}{4(N-1)}RC_1 s + 1} \\ G_{v_H,d_1} &= \frac{\frac{(1-2D_1)R}{8f_s L_1}}{\frac{6N-7}{4(N-1)}RC_1 s + 1}. \end{aligned} \tag{45}$$

If $M = 2$, the transfer function will be a little more complicated, as there are more circuit stages and more control input variables. The transfer functions from v_L, d_1, and d_2 to v_H can be solved as below. The transfer functions have one more pole

$$\boldsymbol{I}^* = \begin{bmatrix} I^*_{1,1} & -I^*_{1,2} & I^*_{1,3} & & & & & \\ & I^*_{2,2} & -I^*_{2,3} & I^*_{2,4} & & & & \\ & & \ddots & \ddots & \ddots & & & \\ & & & I^*_{k,k} & -I^*_{k,k+1} & I^*_{k,k+2} & & \\ & & & & \ddots & \ddots & \ddots & \\ & & & & & I^*_{M-2,M-2} & -I^*_{M-2,M-1} & I^*_{M-2,M} \\ & & & & & & I^*_{M-1,M-1} & -I^*_{M-1,M} \\ & & & & & & & I^*_{M,M} \end{bmatrix}. \tag{42}$$

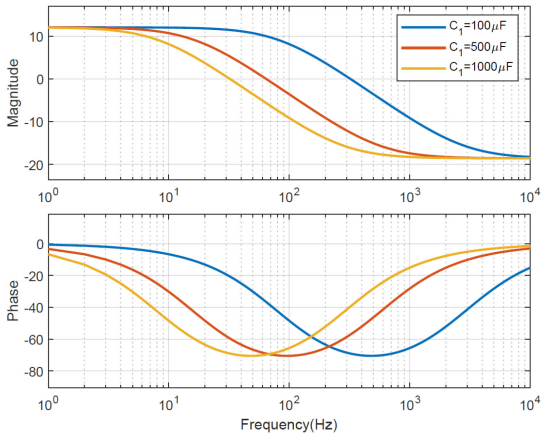

Fig. 16. Bode plot of G_{v_H,v_L} with different capacitor values ($M = 1$).

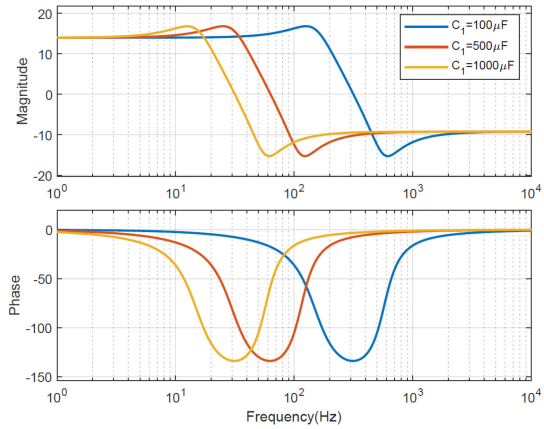

Fig. 17. Bode plot of G_{v_H,v_L} with different capacitor values ($M = 2$).

point and zero point than the case of $M = 1$

$$G_{v_H,v_L} = \frac{a_2 s^2 + a_1 s + a_0}{p_2 s^2 + p_1 s + p_0} \tag{46}$$

$$G_{v_H,d_1} = \frac{b_1 s + b_0}{p_2 s^2 + p_1 s + p_0} \tag{47}$$

$$G_{v_H,d_2} = \frac{c_1 s + c_0}{p_2 s^2 + p_1 s + p_0} \tag{48}$$

$$p_2 = \frac{(6N-7)^2 C_1 C_2 + 4(3N-5)(N-1)C_2^2}{16}$$

$$p_1 = \frac{(N-1)\left[(6N-7)C_1 + 4(2N-3)C_2\right]}{4R}; p_0$$

$$= \left(\frac{D_2(1-D_2)}{8 f_s L_2}\right)^2$$

$$a_2 = \frac{\left(6N^2 - 14N + 9\right) C_1 C_2 + 4(3N-5)(N-1)C_2^2}{16}$$

$$a_1 = \frac{(5N-6) C_2 D_1 (1-D_1)}{32 f_s L_1} - \frac{5(5N-1) C_1 D_2 (1-D_2)}{32 f_s L_2}$$

$$a_0 = \left(\frac{D_1(1-D_1)}{8 f_s L_1} + \frac{D_2(1-D_2)}{8 f_s L_2}\right) \frac{D_2(1-D_2)}{8 f_s L_2}$$

$$b_1 = \frac{2(3N-4)(N-1)(1-2D_1) C_2 V_L}{32 f_s L_1}$$

$$b_0 = \frac{(N-1)(1-2D_1) D_2 (1-D_2) V_L}{8 f_s L_1 \cdot 8 f_s L_2}$$

$$c_1 = \frac{\left[((6N-7)C_1 + 2(N-2)C_2)(V_1 - V_L) + 2(3N-4) C_2 V_2\right](1-2D_2)}{32 f_s L_2}$$

$$c_0 = -\frac{(1-2D_2) D_2 (1-D_2)(V_1 - V_L + V_2)}{(8 f_s L_2)^2}.$$

The transfer functions are also related to the parameters of the SCC. The bode plot of G_{v_H,v_L} with different capacitor values is shown in Fig. 17. The plot is similar with Fig. 16. And the added pole point and zero point increase the resonance peak and the slope. Therefore, the phase margin is less than $M = 1$. A closed-loop controller should be design to increase the phase margin. The inductance is another parameter that can be adjusted. However, in order to keep voltage gain and power unchanged, the ratio of $D_k(1-D_k)$ and L_k should be a constant. Thus, the adjustment of L_k or D_k will not influence G_{v_H,v_L}, but just change the dc gain of G_{v_H,d_k}.

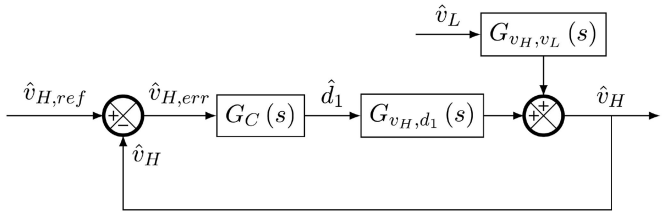

Fig. 18. Block diagram of closed-loop of SCC ($M = 1$).

C. Controller Design and Decoupling

For $M = 1$, it is easy to design the controller, as there is only one controller variable and one output voltage. So, a simple compensator $G_C(s)$ like PI controller can handle the closed-loop controller, as shown in Fig. 18.

As for the case that $M > 1$, there are M independent control variables and M output voltages. As to the dynamic model, each output variables $\hat{v}_{C_{k,N}}$ will be influenced by all phase shift ratios from $\hat{d}_1$ to $\hat{d}_M$. Therefore, to get a clear controller design, the variables should be decoupled first.

The decoupling process is also based on the proposed small signal model. The coefficient matrix $\bar{\boldsymbol{C}}^*$ can be split into a column vector $\bar{\boldsymbol{C}}_0^*$ and a square matrix $\bar{\boldsymbol{C}}_M^*$, which is same for $\boldsymbol{Y}^*$. Then, the output voltage vector $\hat{\boldsymbol{v}}^*$ can be expressed as

$$\hat{\boldsymbol{v}}^* = -\left(\bar{\boldsymbol{C}}_M^* s + \boldsymbol{Y}_M^*\right)^{-1} \left[\left(\bar{\boldsymbol{C}}_0^* s + \boldsymbol{Y}_0^*\right) \hat{v}_L + \boldsymbol{I}^* \hat{\boldsymbol{d}}\right] \tag{49}$$

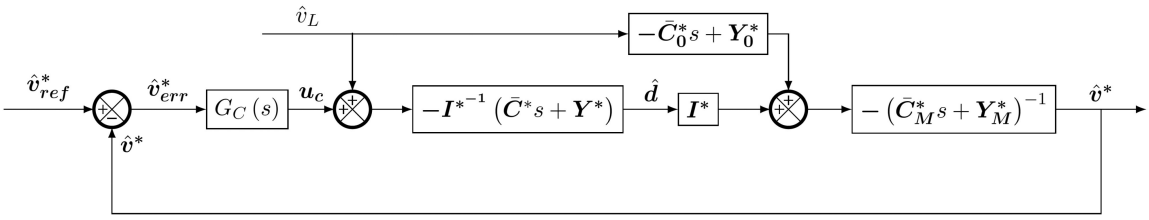

Fig. 19. Block diagram of closed-loop of SCC ($M = 2$).

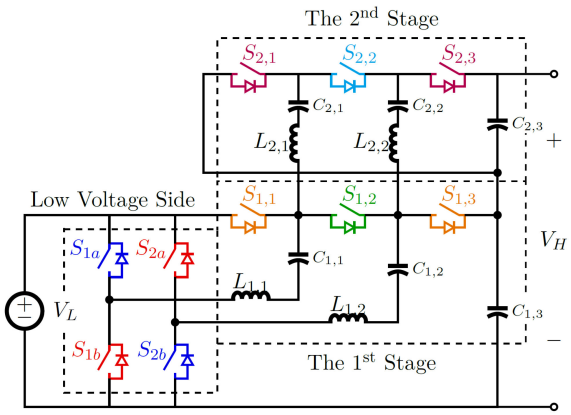

Fig. 20. Circuit of the prototype.

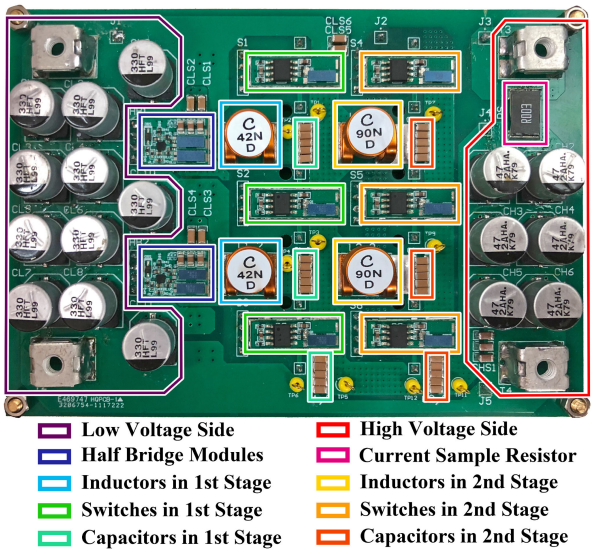

Fig. 21. Prototype of the proposed SCC.

$$\bar{C}_0^* = \begin{bmatrix} \bar{C}_{1,0}^* \\ 0 \\ \vdots \\ 0 \\ 0 \\ 0 \end{bmatrix}; \bar{C}_M^*$$

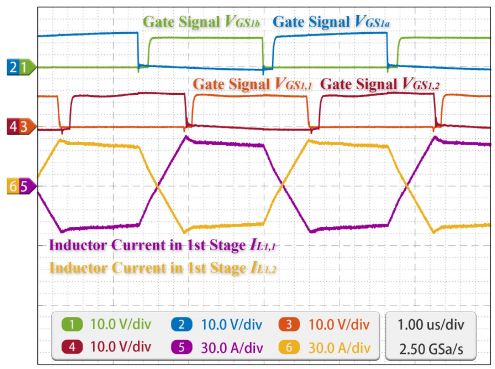

Fig. 22. Waveforms of switching signal and inductor current in first stage.

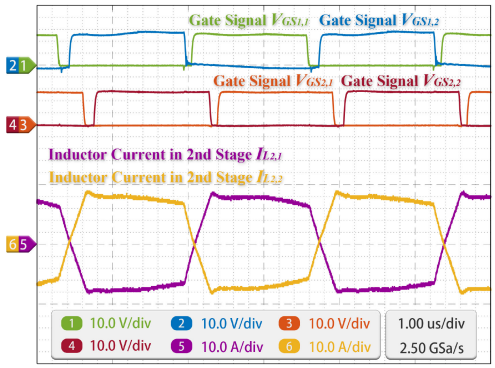

Fig. 23. Waveforms of switching signal and inductor current in second stage.

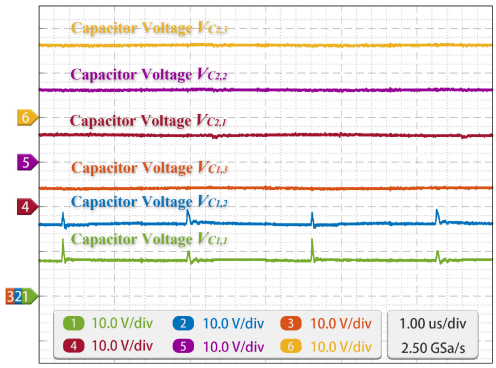

Fig. 24. Waveforms of capacitor voltage.

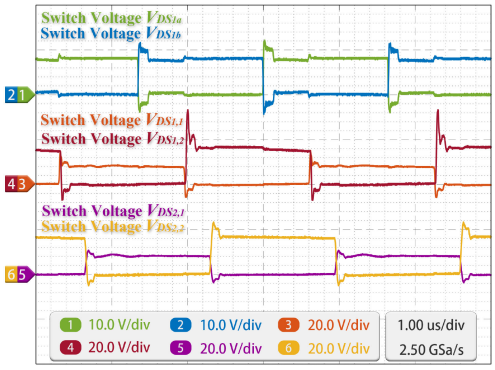

Fig. 25. Waveforms of switch voltage.

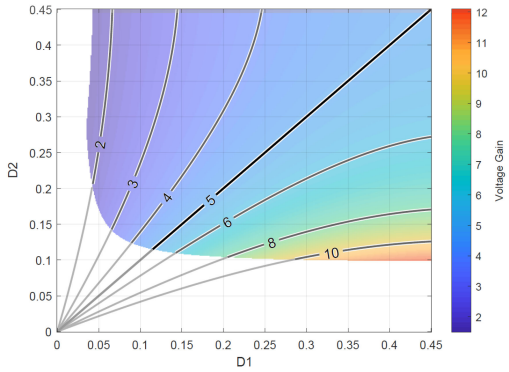

Fig. 26. Theoretical voltage gain with different D_1 and D_2.

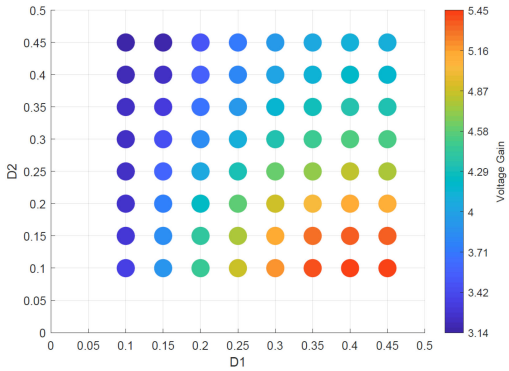

Fig. 27. Measured voltage gain with different D_1 and D_2.

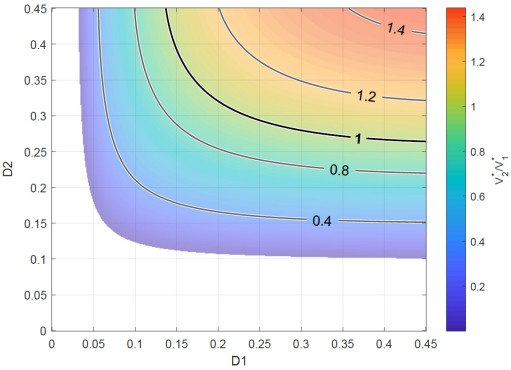

Fig. 28. Theoretical voltage ratio with different D_1 and D_2.

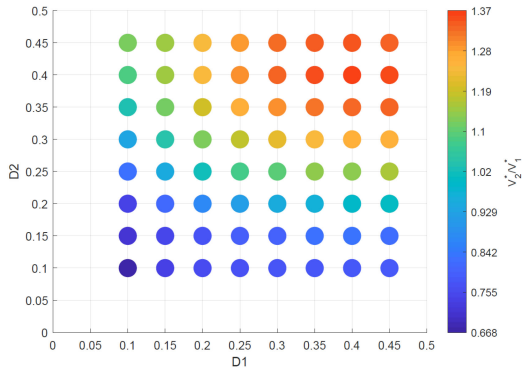

Fig. 29. Measured voltage ratio with different D_1 and D_2.

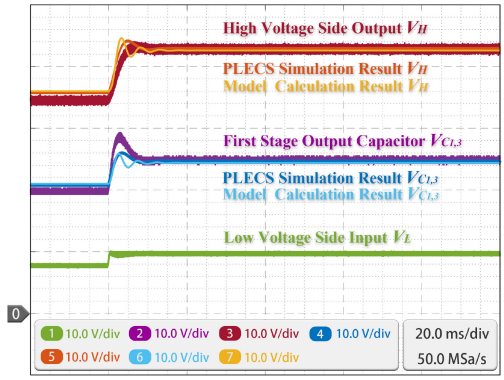

Fig. 30. Open-loop step response.

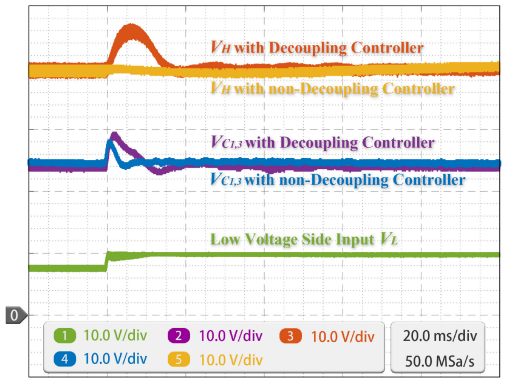

Fig. 31. Closed-loop step response.

$$= \begin{bmatrix} \bar{C}^*_{1,1} & \bar{C}^*_{1,2} & \bar{C}^*_{1,3} & & & & \\ \bar{C}^*_{2,1} & \bar{C}^*_{2,2} & \bar{C}^*_{2,3} & \bar{C}^*_{2,4} & & & \\ \ddots & & \ddots & \ddots & \ddots & & \\ & \bar{C}^*_{M-2,M-3} & \bar{C}^*_{M-2,M-2} & \bar{C}^*_{M-2,M-1} & \bar{C}^*_{M-2,M} & & \\ & & \bar{C}^*_{M-1,M-2} & \bar{C}^*_{M-1,M-1} & \bar{C}^*_{M-1,M} & & \\ & & & \bar{C}^*_{M,M-1} & \bar{C}^*_{M,M} & & \end{bmatrix} \tag{50}$$

$$\boldsymbol{I}^{*-1}=\begin{bmatrix}\frac{8f_sL_1}{(1-2D_1)V_0^*} & \frac{8f_sL_1(V_1^*+V_2^*)}{(1-2D_1)V_0^*V_1^*}\\ & \frac{8f_sL_2}{(1-2D_2)V_1^*}\end{bmatrix} \quad (53)$$

$$\boldsymbol{Y}^*=\begin{bmatrix}\frac{D_1(1-D_1)}{8f_sL_1} & -\frac{D_2(1-D_2)}{8f_sL_2} & -\frac{D_2(1-D_2)}{8f_sL_2}\\ -\frac{1}{R} & \frac{D_2(1-D_2)}{8f_sL_2}-\frac{2}{R} & -\frac{2}{R}\end{bmatrix}$$

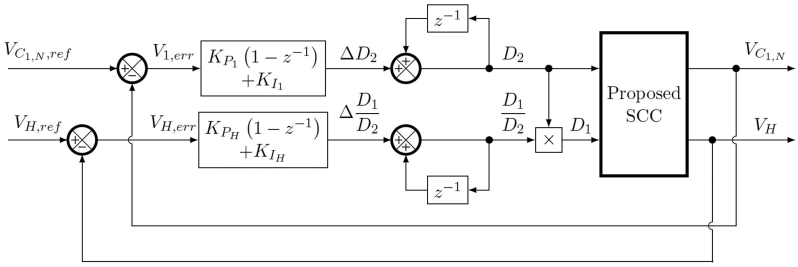

Fig. 32. Block diagram of nondecoupling closed-loop controller.

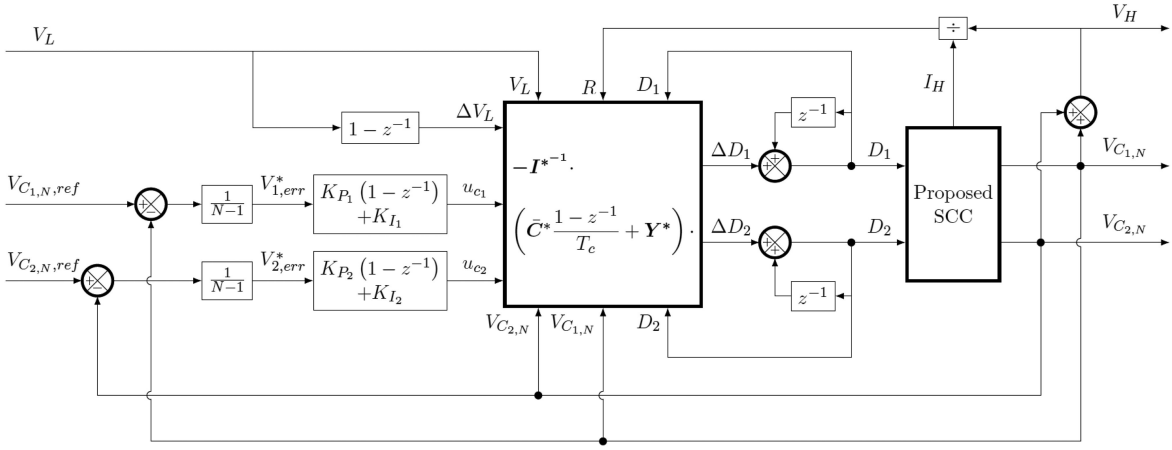

Fig. 33. Block diagram of decoupling closed-loop controller.

$$\boldsymbol{Y}_{\boldsymbol{0}}^*=\begin{bmatrix}Y_1^*\\0\\\vdots\\0\\0\\-\frac{1}{R}\end{bmatrix};\boldsymbol{Y}_{\boldsymbol{M}}^*$$

$$=\begin{bmatrix}-Y_2^* & -Y_2^* & Y_3^* & & & & \\ Y_2^* & -Y_3^* & -Y_3^* & Y_4^* & & & \\ & \ddots & \ddots & \ddots & \ddots & & \\ & & Y_{M-2}^* & -Y_{M-1}^* & -Y_{M-1}^* & Y_M^* & \\ & & & Y_{M-1}^* & -Y_M^* & -Y_M^* & \\ -\frac{N-1}{R} & \cdots & \cdots & -\frac{N-1}{R} & Y_M^*-\frac{N-1}{R} & -\frac{N-1}{R} & \end{bmatrix}. \quad (51)$$

In a closed loop, a new control variable vector $\boldsymbol{u_c}$ can be defined, whose elements are corresponding to output voltage of each stage one by one. And the actual control variable as the phase shift ratios $\hat{\boldsymbol{d}}$ can be solved from $\boldsymbol{u_c}$. And the block diagram of the controller is shown in Fig. 19. With the decoupling matrix, each output voltage of corresponding stage can be controlled independently. Besides, as shown in the (52), only the element $\bar{\boldsymbol{C}}^*$ is constant, which is determined by the topology and capacitance values. $\boldsymbol{I}^*$ and $\boldsymbol{Y}^*$ are all the function of the actual phase shift ratios D_k and output voltage $V_{C_{k,N}}$. So, the decoupling matrix should be upgraded in the real-time controller. If the dynamic model is as complex as the conventional small signal model, it is too difficult to complete the calculation. With the proposed simplified modeling method, the matrixes in the closed loop have a simple form and easy to be calculated in the controller

$$\begin{aligned}\hat{\boldsymbol{d}}&=-\boldsymbol{I}^{*^{-1}}\left[\left(\bar{\boldsymbol{C}}_{\boldsymbol{M}}^*s+\boldsymbol{Y}_{\boldsymbol{M}}^*\right)\boldsymbol{u_c}+\left(\bar{\boldsymbol{C}}_{\boldsymbol{0}}^*s+\boldsymbol{Y}_{\boldsymbol{0}}^*\right)\hat{v}_L\right]\\&=-\boldsymbol{I}^{*^{-1}}\left(\bar{\boldsymbol{C}}^*s+\boldsymbol{Y}^*\right)\begin{bmatrix}\hat{v}_L\\\boldsymbol{u_c}\end{bmatrix}.\end{aligned} \quad (52)$$

V. Experiments

A. Prototype Design

A prototype of proposed SCC is built to validate the steady state and dynamic model. The prototype has two stages and three capacitors in each stage, which means $M = 2$ and $N = 3$, as shown in Fig. 20. Thus, the nominal voltage gain of the prototype is five. The main parameters of the prototype are listed in Table I. The capacitors in each stage imply MLCC for its high capacitance density. The inductors have little inductance and imply air core inductor to reduce core loss. GaN switching devices are also adopted in the prototype to achieve higher switching frequency and less conduction loss and switching-OFF loss.

And the photograph of the prototype is shown in Fig. 21. The main components are on the top side for a compact design. And

the half bridge modules and isolated switch modules for each stage are mounted on the main board.

B. Steady-State Waveforms

To validate the steady-state characteristics of proposed SCC, the prototype works with certain input voltage V_L, phase shift ratios D_1, D_2, and load. Figs. 22 and 23 show the waveforms of the switch gate signal V_{GS} and the inductor current in the first stage and the second stage. The switches in the prototype are driven by the signal with phase shift modulation, so that the current of inductors in each stage has four states in a switching period, as analyzed in Section II. The waveforms are accord with the theoretical analysis in Fig. 6. As shown in Figs. 22 and 23, the slope of inductor current changes when corresponding switch turn OFF. Therefore, the dead band added in the practical gate signal will not influence the actual phase shift ratio.

Fig. 24 shows the capacitor voltage in the *LC* branches. For the first stage, the voltage of C_{13} is threefold of the low side voltage V_L. And the voltage of C_{11}, C_{12} are, respectively, equal to V_L and $2V_L$, which composes the arithmetic sequence as steady-state analysis. And for the second stage, the voltage of C_{21}, C_{22}, and C_{23} are all equal to twice of V_L. As the high side voltage V_H is the series of $V_{C_{13}}$ and $V_{C_{23}}$, V_H is equal to $5V_L$, which is same as the nominal voltage gain of the prototype.

Fig. 25 shows the voltage across the switches. For the half bridges, the voltage across the switches is equal to the low side voltage V_L. For the first and second stages, the voltage across switch is depending on the voltage of capacitors. As the capacitor voltage distribution in Fig. 24, the voltage across S_{11}, S_{13}, S_{21}, and S_{23} should be equal to V_L, and the voltage across S_{12} and S_{22} should be equal to $2V_L$. The switch voltage waveforms in Fig. 25 fit the steady-states analysis result. It also can be seen that, the voltage across switches is different in dead band time as the switch has reverse conduction voltage drop. The voltage drop means that all the switches in the proposed SCC are able to achieve ZVS, which is helpful to reach high switching frequency and high power density with low switching loss and high efficiency.

As steady-state analysis, the voltage gain and voltage ratio of the first and second stage is changeable with different phase shift ratio combinations. With certain low side input voltage V_L, the phase shift ratios D_1 and D_2 are adjusted in steps of 0.05. The voltage gains V_H/V_L and voltage ratios V_2^*/V_1^* are measured and plotted in Figs. 27 and 29. Compared with the theoretical results in Figs. 26 and 28, the voltage ratio measured in experiment fits the theoretical calculation well. As for the voltage gain, the distribution and trends of experimental data are accord with the theory. However, with high D_1 and low D_2 combinations, the voltage gain can be extremely high in theory. At the same time, the peak current of inductors and switches will also be much higher than usual situation, which means large conduction loss and limits the upper bound of voltage gain. This feature will not influence the voltage regulation ability and control of the proposed SCC, and means with certain stage number M and certain capacitor number N in each stage, the proposed SCC has its compatible voltage gain range. In this range, the theoretical model is available and accurate, and the converter can reach high efficiency.

C. Step Response Waveforms

The dynamic characteristic of the proposed hybrid SCC is also verified by experiments. In the experiment, after the converter entering steady state, the input voltage V_L is added with 2 V. The responses of V_H and $V_{C_{13}}$ with open loop are shown in Fig. 30. And the step response obtained from PLECS and the step response calculated from model transfer functions are also plotted. It can be seen that, the waveforms from experiment coincides the simulation results. The rising time of the step response is almost the same. Vibrations appear in the response from model because of the absent of the damping.

And according to the dynamic model and controller design method, the closed-loop controller is design for the prototype. Decoupling controller and nondecoupling controller are both designed. For the nondecoupling controller shown in Fig. 32, there are two coupling feedback loops. The adjustment of D_2 will also influence V_H in another loop. For the decoupling controller shown in Fig. 33, the decoupling method in Fig. 18is used. With the help of the simplified model, the decoupling stage can be easily calculated in the DSP as (53). The compensator stage $G_C(s)$ adopts PI regulator with $K_{P_1} = 0.1$, $K_{I_1} = 0.05$, $K_{P_2} = 0.25$, and $K_{I_2} = 0.05$. The step response waveforms of two closed-loop controller are shown in Fig. 31. Both two controllers can make the voltage stable. The decoupling controller has better dynamic performance than the nondecoupling controller as lower overshoot and shorter adjustment time. For the proposed SCC with higher voltage gain and M larger than 2, there will be more control variables and more complex coupling relationship. Therefore, the closed-loop controller is able to control the proposed SCC. And the decoupling closed-loop controller design method based on the dynamic model is effective and useful.

VI. Conclusion

Based on the proposed switched-capacitor converter, which can achieve high efficiency and high power density with novel topology and phase shift modulation, this article derives the modeling method of both steady state and dynamic.

1) The steady-state model of the proposed SCC is derived with the steady-state condition of inductors and capacitors. With unified parameter matrix, the output voltage of each stage and the voltage gain of the converter can be solved, which helps voltage regulation of the proposed SCC. And the voltage and current expression of inductors, capacitors and switches can also be obtained, which is helpful for stress design and selection of components.
2) The dynamic model of the proposed SCC is derived with conventional average small signal method. The small signal expressions of inductor current and capacitor voltage are listed. And the small signal model of output voltage of each stage and the whole converter can be solved. And the complexity and order of the conventional small signal

model is derived, which blocks the modeling for high voltage gain SCCs.

3) A simplified small signal modeling method is further proposed. With a unified parameter matrix, the simplified small signal model can be solved with limited order and complexity. The simplified model is based on the small-inductance feature and working mechanism. The accuracy of the simplified model is validated by simulation results.
4) As the proposed SCC is a multi-input and multi-output system, the controller design and decoupling method is proposed. Based on the simplified model, the proposed closed-loop control method can be calculated in real time, which enables the voltage regulation of the proposed SCC under different input voltage and load.

The prototype of the proposed SCC is built with GaN switches. The steady-state experiment validates the steady-state model and the dynamic experiment validates the availability of the closed-loop controller based on the dynamic model. The steady-state model and the dynamic model illustrate the characteristic of the proposed SCC and help the parameter design. With the model and controller, the proposed SCC is able to realize better steady state and dynamic performance and regulate the voltage more accurate and faster, which expands the application in the practical systems.

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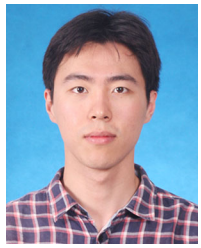

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