Robustness Investigation of Multi-Inverter Paralleled Grid-Connected System With *LCL*-Filter Based on the Grid-Impedance Allocation Mechanism

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***Abstract*—Due to the existence of grid impedance, there is coupling resonance problem which may cause the multi-inverter grid-connected system to become unstable. This article focuses on universal mechanism for multimodule grid-connected system composed of *LCL*-type inverters. By establishing the multi-input multi-output matrix of the multi-inverter system, the system stability is divided into two parts, i.e., the self-stability and the interactive-stability. Then, based on elaborate deduction for the interactive-stability, the equivalent allocation mechanism of grid impedance is raised and a stability criterion for multimodule inverters system is proposed. In addition, on the basis of exploring the effect of the digital-control delay on the stability of the multi-inverter system in the weak grid, the phase-lead compensator combining with the optimal capacitor-current-feedback coefficient is adopted to improve the system robustness against grid impedance variation. Finally, the effectiveness of the theoretical analysis is verified by experimental results.**

***Index Terms*—Digital-control delay, grid-impedance allocation, *LCL*-filter, multi-inverter-paralleled, robustness.**

NOMENCLATURE

$Z_{L1j}(s)$, $Z_{L2j}(s)$, $Z_{Cj}(s)$	Impedance of inverter-side inductor, grid-side inductor and capacitor of inverter j ($Z_{L1j}(s) = sL_{1j}$, $Z_{L2j}(s) = sL_{2j}$ and $Z_{Cj}(s) = 1/sC_j$).
$Z_{\rm g}(s)$ ($Y_{\rm g}(s)$)	Grid impedance (grid admittance).
$V_{{\rm in}j}$, $v_{{\rm inv}j}$, $v_{\rm PCC}$	Input voltage, inverter bridge output voltage of inverter j and voltage at the point of common coupling.
$i_{L1j}(s)$, $v_{Cj}(s)$, $i_{L2j}(s)$	Inverter-side inductor current, capacitor voltage and grid-side inductor current of inverter j.
$v_{\rm g}(s)$, $i_{\rm g}(s)$	Grid voltage and grid current.
H_{i1_j}, H_{i2_j}	Capacitor current feedback coefficient and grid-side inductor current feedback coefficient of inverter j.
$i_{{\rm ref}j}$	Grid-side inductor current reference of inverter j.
$f_{{\rm s}j}$, $T_{{\rm s}j}$	Sampling frequency and sampling period of inverter j.
$K_{{\rm PWM}j}$	Transfer function from modulation wave to $v_{{\rm inv}j}$ of inverter j.
$G_{ij}(s)$, $G_{{\rm d}j}(s)$	Current regulator, and transfer function for digital-control delay of inverter j ($G_{{\rm d}j}(s) = e^{-1.5sTsj}$).
$Z_{{\rm R\_D}j}(s)$ ($Y_{{\rm R\_D}j}(s)$)	Virtual impedance (virtual admittance) paralleled with the filter capacitor of inverter j.
$i_{{\rm cs}j}(s)$, $Y_{{\rm cs}j}(s)$ ($Z_{{\rm cs}j}(s)$)	Equivalent current source and equivalent output admittance (impedance) of inverter j.
$i_{{\rm g}j}(s)$	Net current injected by inverter j into the grid.
$i_{ji}(s)$	Net current injected by inverter j into inverter i.
$Z_{{\rm g}j}(s)(Y_{{\rm g}j}(s))$	Grid impedance (grid admittance) perceived by the jth grid-connected inverter.
PM, $f_{\rm cr}$	Phase margin of the system and intersection frequency of $\sum_{i=1}^{n} Y_{{\rm cs}i}(s)$ and $Y_{\rm g}(s)$.
$K_{{\rm p}j}$	Proportional link of the current regulator $G_{ij}(s)$.
$H_{i1{\rm p}\_j}$	Optimal capacitor-current-feedback coefficient of inverter j.
$R_{{\rm d}j}$	Emulated virtual resistance without considering digital-control delay.
$G_{\rm c}(s)$	Phase-lead compensator.
$Y_{{\rm R\_Dc}j}(s)$	Virtual admittance paralleled with the filter capacitor after introducing the phase-lead link.

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I. Introduction

With the exploitation of the renewable energy to generate electricity, distributed power generation system (DPGS) is built. In DPGS, the grid-connected inverter converts the generated dc power to available ac power, and plays the significant role of regulating electricity [1].

To eliminate the harmonic content of the grid-connected current, *LCL*-filter is usually considered since it has superior harmonic attenuation ability with reduced volume and weight compared with the single-*L* filter [2]. To suppress its inherent resonance peak [3]–[6], the active damping methods are more preferred over the passive damping ones since they would not introduce additional loss [7]–[12]. Among them, capacitor-current-feedback active-damping method has been widely used owing to its simplicity and effectiveness [8]. However, with the digital control adopted, the proportional feedback of the capacitor current becomes a frequency-related impedance instead of a pure resistance, which may bring about the instability of the system [13], [14]. To alleviate and even eliminate the adverse effect from the digital-control delay, scholars have put forward a variety of solutions, such as the minimum delay sampling method [15], [16], the multiple sampling scheme [17], and the predictive control [18]–[20].

With the scale expansion of DPGS, more and more renewable-energy power plants adopt the system structure of multiple inverters connected in parallel. This configuration can realize the optimized allocation for capacity and fault redundant operation of grid-connected system. Nevertheless, in weak grid, all the inverters are coupled through the grid impedance, which causes the inverters to interact with each other, thereby affecting the stability of the entire parallel system. Meanwhile, when digital control is employed, the effect of digital-control delay on the stability of the multi-inverter grid-connected system cannot be ignored either.

Investigations have also been developed for the issue on the multi-inverter grid-connected system. In [21], the coupling resonance mechanism of multiple inverters is revealed by a simplified passive circuit model without considering the inverter controller, thus the resonance mechanism cannot be accurately displayed. In [22], the viewpoint is proposed as that the equivalent grid-impedance for each inverter in parallel system is the actual grid-impedance multiplied by the number of inverters. However, this conclusion is limited by ideal assumption of the current references of parallel inverters being the same. In [23], the Norton circuit of the parallel-inverter system is established. Based on this, the active-damping method is combined with the deadbeat control to solve the resonance problem among multiple inverters. However, the effect of the deadbeat control is greatly dependent on the accuracy of the system modeling, and the parameters of each inverter are selected to be the same to simplify the discussion. In [24], interactive currents and common currents are used to describe the dynamic interaction of multiple grid-connected inverters in the weak grid. This reveals the coupling resonance mechanism to some extent, but the model is established on the premise that the parameters of all the inverters are consistent. Furthermore, the state-space method is another stability analysis approach that evaluates system performance through eigenvalue trace analysis [25]–[27].

Although the above studies have made some impressive conclusions on the issue of coupling resonant, most of them are only for inverters system with the same parameters, and few of them give the insight into the effect of digital-control delay on the stability of the parallel system from the perspective of impedance or admittance. Yet, this article focuses on a general-purpose system. This article is a full extension of our previous work in [28], in which the basic concept of grid-impedance being allocated to each inverter is given out. However, few deductions have been provided to support the idea so that its mechanism is ambiguous. While in this article, logical derivations are offered to naturally achieve the grid-impedance allocation mechanism, whose potential merit is also clarified. Moreover, based on exploring the impact of the digital-control delay on the parallel system by impedance analysis, measures are taken to improve the system robustness.

The article is organized as follows. In Section II, the stability of the multi-input multi-output (MIMO) system is divided into the self-stability and the interactive-stability based on the MIMO matrix. In Section III, the interactive-stability is elaborately analyzed and the current interaction relationship is revealed. Consequently, the grid-impedance allocation mechanism is proposed, and the stability criterion of multi-inverter system is given out. In Section IV, the effect of digital-control delay on the multi-inverter system is intensively studied from the perspective of output admittance and the concept of optimal capacitor-current-feedback coefficient is raised. Also, a phase-lead compensator is introduced to improve the system robustness against grid impedance variation. In Section V, the example illustration and experimental results are provided to validate the theoretical analysis. In Section VI, a discussion is developed on the impact of grid voltage feedforward. Finally, Section VII concludes this article.

II. Establishment of MIMO Matrix and Deconstruction of Control System

The circuit topology of the multi-inverter-paralleled grid-connected system in the weak grid is shown in Fig. 1. Here, we hold the assumption of the grid impedance being inductive-resistive with the general form of $Z_{\rm g}(s) = R + sL_{\rm g}$.

A. Digital-Control Delay Considered Norton Model for Single Grid-Connected Inverter

To initiate the investigation, we take module *j* in Fig. 1 for example to analyze and establish the model for single inverter in the grid-connected system preliminarily. Fig. 2(a) illustrates the control block diagram for the single digitally controlled inverter with the capacitor-current-feedback active-damping, which is equivalent to emulate a virtual impedance $Z_{{\rm R\_D}j}(s)$ in paralleled with the filter capacitor [29]. $Z_{{\rm R\_D}j}(s)$ is written as

$$Z_{{\rm R\_D}j}(s) = \frac{L_{1j}}{H_{i1\_j}K_{{\rm PWM}j}C_j} \cdot \frac{1}{G_{{\rm d}j}(s)}. \tag{1}$$

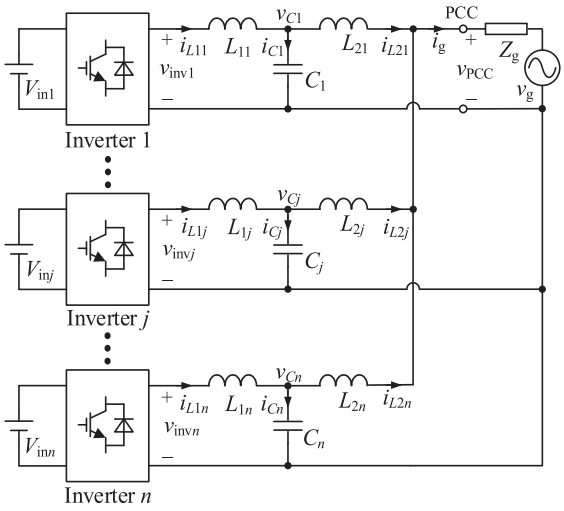

Fig. 1. Topology of the multiparalleled grid-connected inverters system in the weak grid.

Then, Fig. 2(a) can be further equivalent to the simplified control block diagram shown in Fig. 2(b), in which

$$G_{\mathrm{M}j}(s) = G_{ij}(s)G_{\mathrm{d}j}(s)K_{\mathrm{PWM}j}. \tag{2}$$

And the expressions of $Y_{\mathrm{inv}j}(s)$ and $Y_{\mathrm{PCC}j}(s)$ are shown as (3) and (4) shown at the bottom of this page. According to Fig. 2(b), the expression of the grid-side inductor current $i_{L2j}(s)$ can be derived as

$$\begin{aligned} i_{L2j}(s) &= G_{\mathrm{cs}j}(s)\cdot i_{\mathrm{ref}j}(s) - Y_{\mathrm{cs}j}(s)\cdot v_{\mathrm{PCC}}(s) \\ &\triangleq i_{\mathrm{cs}j}(s) - Y_{\mathrm{cs}j}(s)\cdot v_{\mathrm{PCC}}(s) \end{aligned} \tag{5}$$

where

$$G_{\mathrm{cs}j}(s) = \frac{G_{\mathrm{M}j}(s)Y_{\mathrm{inv}j}(s)}{1 + H_{i2\_j}G_{\mathrm{M}j}(s)Y_{\mathrm{inv}j}(s)} \tag{6}$$

$$Y_{\mathrm{cs}j}(s) = \frac{Y_{\mathrm{PCC}j}(s)}{1 + H_{i2\_j}G_{\mathrm{M}j}(s)Y_{\mathrm{inv}j}(s)}. \tag{7}$$

Consequently, from (5), we can acquire the Norton equivalent model for the single inverter (as shown in the dashed box in Fig. 3), which is actually a current source $i_{\mathrm{cs}j}(s)$ paralleled with an output admittance $Y_{\mathrm{cs}j}(s)$ from the PCC point.

B. General MIMO Matrix of Multi-Inverter System and Deconstruction of Control System

Based on the analysis of the last part, we could further obtain the Norton circuit of the whole system, as shown in Fig. 3. According to the circuit in Fig. 3, $v_{\mathrm{PCC}}(s)$ can be derived as

$$v_{\mathrm{PCC}}(s) = \frac{\sum_{i=1}^{n} i_{\mathrm{cs}i}(s) + v_{\mathrm{g}}(s)Y_{\mathrm{g}}(s)}{\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s)}. \tag{8}$$

By substituting (8) into (5), the grid-side inductor current $i_{L2j}(s)$ can be expressed as

$$\begin{aligned} i_{L2j}(s) &= \frac{\sum_{i=1,i\neq j}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s)}{\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s)} \cdot i_{\mathrm{cs}j}(s) \\ &\quad + \sum_{i=1,i\neq j}^{n} \left[\frac{-Y_{\mathrm{cs}j}(s)}{\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s)} \cdot i_{\mathrm{cs}i}(s) \right] \\ &\quad - \frac{Y_{\mathrm{cs}j}(s)Y_{\mathrm{g}}(s)}{\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s)} \cdot v_{\mathrm{g}}(s) \\ &\triangleq M_{jj}(s)\cdot i_{\mathrm{cs}j}(s) + \sum_{i=1,i\neq j}^{n} [M_{ji}(s)\cdot i_{\mathrm{cs}i}(s)] \\ &\quad - N_j(s)\cdot v_{\mathrm{g}}(s) \end{aligned} \tag{9}$$

And $M_{jj}(s)$, $M_{ji}(s)$, and $N_j(s)$ in (9) are shown as follows:

$$M_{jj}(s) = \left(\sum_{i=1,i\neq j}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s) \right) \Bigg/ \left(\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s) \right) \tag{10}$$

$$M_{ji}(s) = (-Y_{\mathrm{cs}j}(s)) \Bigg/ \left(\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s) \right) \tag{11}$$

$$N_j(s) = (Y_{\mathrm{cs}j}(s)Y_{\mathrm{g}}(s)) \Bigg/ \left(\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s) \right). \tag{12}$$

In the light of the former analysis, we can make the following deduction. If we regard the grid-side inductor currents i_{L2j} of all the inverters as the output variables and all the inverter current references $i_{\mathrm{ref}j}$ as the input variables, we can obtain the equivalent control block diagram of multi-inverter grid-connected system, as shown in Fig. 4. It can be seen that the multi-inverter system is actually a MIMO system for now, and furthermore, its equivalent control block diagram can be divided into two subsystems cascaded.

1) The first subsystem is shown in the blue dashed box in Fig. 4. As for this part, the input signals are the current references $i_{\mathrm{ref}j}$ of all the inverters, and the output signals are the equivalent current sources $i_{\mathrm{cs}j}$ of all the inverters. The relationship between them can be described by the transfer function matrix $\boldsymbol{G_{\mathrm{cs},n\times n}}$, which possesses the form as

$$\begin{aligned} \mathbf{G_{cs,n\times n}} &= [\mathbf{I_{n\times n}} + \mathbf{H_{i2,n\times n}}\cdot \mathbf{G_{M,n\times n}}\cdot \mathbf{Y_{inv,n\times n}}]^{-1} \\ &\quad \cdot \mathbf{G_{M,n\times n}}\cdot \mathbf{Y_{inv,n\times n}} \end{aligned} \tag{13}$$

where $\boldsymbol{I_{n\times n}}$ is an identity matrix of $n \times n$ order and $\boldsymbol{G_{\mathrm{M},n\times n}} = \mathrm{diag}\{G_{\mathrm{M1}}(s), G_{\mathrm{M2}}(s), \ldots, G_{\mathrm{M}n}(s)\}$, $\boldsymbol{Y_{\mathbf{inv},n\times n}} = \mathrm{diag}\{Y_{\mathrm{inv1}}(s), Y_{\mathrm{inv2}}(s), \ldots, Y_{\mathrm{inv}n}(s)\}$, and $\boldsymbol{H_{i2,n\times n}} = \mathrm{diag}\{H_{i2\_1}, H_{i2\_2}, \ldots, H_{i2\_n}\}$ are all diagonal matrices. So, the matrix $\boldsymbol{G_{\mathrm{cs},n\times n}}$ is also

$$Y_{\mathrm{inv}j}(s) = \frac{Z_{Cj}(s)Z_{\mathrm{R\_D}j}(s)}{Z_{L1j}(s)Z_{L2j}(s)\cdot(Z_{Cj}(s) + Z_{\mathrm{R\_D}j}(s)) + Z_{Cj}(s)Z_{\mathrm{R\_D}j}(s)\cdot(Z_{L1j}(s) + Z_{L2j}(s))} \tag{3}$$

$$Y_{\mathrm{PCC}j}(s) = \frac{Z_{L1j}(s)\cdot(Z_{Cj}(s) + Z_{\mathrm{R\_D}j}(s)) + Z_{Cj}(s)Z_{\mathrm{R\_D}j}(s)}{Z_{L1j}(s)Z_{L2j}(s)\cdot(Z_{Cj}(s) + Z_{\mathrm{R\_D}j}(s)) + Z_{Cj}(s)Z_{\mathrm{R\_D}j}(s)\cdot(Z_{L1j}(s) + Z_{L2j}(s))} \tag{4}$$

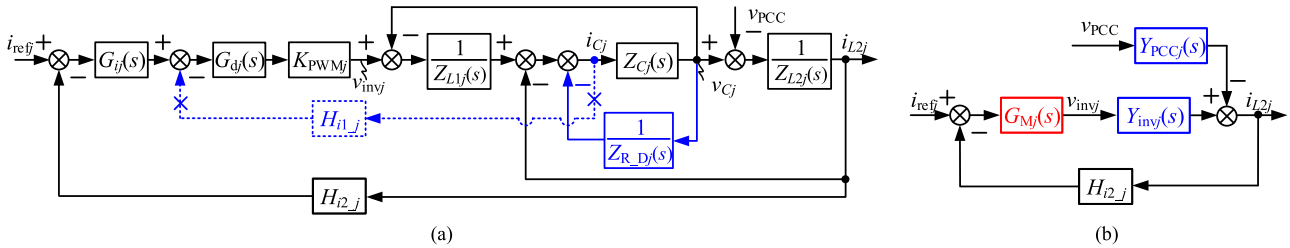

Fig. 2. Control block diagram of inverter *j*. (a) Control block diagram for the *LCL*-type grid-connected inverter with basic capacitor-current feedback active-damping. (b) Equivalent control block diagram.

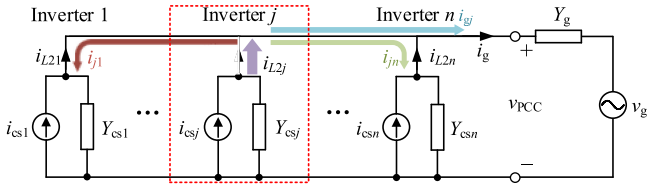

Fig. 3. Norton circuit of multi-inverter grid-connected system in the weak grid.

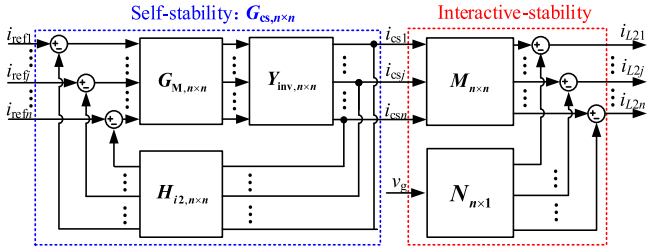

Fig. 4. Equivalent MIMO control block diagram of multi-inverter grid-connected system.

a diagonal matrix. Then, we can get the following matrix:

$$\mathbf{i_{cs,n\times 1}} = \mathbf{G_{cs,n\times n}} \cdot \mathbf{i_{ref,n\times 1}} \Leftrightarrow$$

$$\begin{bmatrix} i_{\mathrm{cs}1}(s) \\ \cdots \\ i_{\mathrm{cs}j}(s) \\ \cdots \\ i_{\mathrm{cs}n}(s) \end{bmatrix} = \begin{bmatrix} G_{\mathrm{cs}1}(s) & \cdots & 0 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & \cdots & G_{\mathrm{cs}j}(s) & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & \cdots & 0 & \cdots & G_{\mathrm{cs}n}(s) \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{ref}1}(s) \\ \cdots \\ i_{\mathrm{ref}j}(s) \\ \cdots \\ i_{\mathrm{ref}n}(s) \end{bmatrix}. \tag{14}$$

It can be seen that, since $\boldsymbol{G_{cs,n\times n}}$ is a diagonal matrix, there is no coupling among all the inverters in terms of this subsystem. Thus, this part could be deemed as *n* single-input single-output (SISO) systems. As a result, the pole distribution of $G_{\mathrm{cs}j}(s)$ will individually determine whether the inverter *j* is stable. As seen, the first subsystem has presented the stability of all the inverters themselves, and consequently the stability of this part can be called self-stability. Since the grid impedance is not involved in this part, the self-stability is actually the stability issue of each inverter in the stiff grid. It can be traced back to Fig. 2(b) that each inverter *j* could be ensured its own stable by reasonably designing $G_{\mathrm{cs}j}(s)$ of no right-half-plane (RHP) poles. Specifically, $G_{\mathrm{cs}j}(s)$ involves $G_{ij(\mathrm{s})}$, H_{i1_j} and etc., which thus should be carefully designed to guarantee the self-stability of each module. Since the design procedure of this part that we could follow has been provided in [30], the detailed designing process is not given here.

2) The second subsystem is shown in the red dashed box in Fig. 4. As for this part, the input signals are the equivalent current sources $i_{\mathrm{cs}j}$ of all the inverters and grid voltage v_{g}, and the output signals are the grid-side inductor currents i_{L2j} of all the inverters. The relationship between them can be described by the MIMO transfer function matrix (15) shown at the bottom of the next page.

In (15), $\boldsymbol{M_{n\times n}}$ is the transfer function matrix from the equivalent current sources of all the inverters to their respective grid-side inductor currents, and the matrix $\boldsymbol{N_{n\times 1}}$ is the transfer function matrix from the grid voltage to the grid-side inductor currents of all the inverters. The expressions of the elements in the matrices $\boldsymbol{M_{n\times n}}$ and $\boldsymbol{N_{n\times 1}}$ are shown in (10), (11), and (12), respectively. It can be seen that, since $\boldsymbol{M_{n\times n}}$ is an nondiagonal matrix, there is the coupling among all the inverters as far as this subsystem is concerned, which manifests that the stability of this part is related to the interaction among the inverters, and thus the stability of this part can be called interactive-stability. In fact, it is the grid impedance dwelling in this part that induces the coupling. For this more intricate part, further investigation would be carried out.

III. Stability Criterion of Multi-Inverter System Based on the Equivalent Allocation of Grid Impedance

A. Elaborate Analysis for the Interactive-Stability

From the analysis in the previous section, we know that there is a coupling phenomenon in multi-inverter-paralleled grid-connected system. Thus, for the sake of exploring the interaction among the inverters, we can decompose (15) as (16), shown at the bottom of this page, where

$$M_{jj,a}(s) = \frac{Y_{\mathrm{g}}(s)}{\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s) + Y_{\mathrm{g}}(s)} \tag{17}$$

$$M_{jj,b}(s)=\frac{\sum_{i=1,i\neq j}^{n}Y_{\mathrm{cs}i}(s)}{\sum_{i=1}^{n}Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}. \tag{18}$$

Accordingly, the control block diagram of the interactive-stability part in Fig. 4 can be equivalent to Fig. 5(a). Here comes the further explanation about Fig. 5(a). Without loss of generality, inverter *j* is taken as an example for illustration. As shown in (16), i_{L2j} could be regarded as consisting of two parts:

$$i_{L2j}(s)=i_{\mathrm{g}j}(s)+\sum_{i=1,i\neq j}^{n}i_{ji}(s) \tag{19}$$

where

$$\begin{aligned}i_{\mathrm{g}j}(s)&=M_{jj,a}(s)\cdot i_{\mathrm{cs}j}(s)-N_j(s)\cdot v_{\mathrm{g}}(s)\\&=\frac{Y_{\mathrm{g}}(s)}{\sum_{i=1}^{n}Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot i_{\mathrm{cs}j}(s)\\&\quad-\frac{Y_{\mathrm{cs}j}(s)Y_{\mathrm{g}}(s)}{\sum_{i=1}^{n}Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot v_{\mathrm{g}}(s)\end{aligned} \tag{20}$$

$$\begin{aligned}\sum_{i=1,i\neq j}^{n}i_{ji}(s)&=M_{jj,b}(s)\cdot i_{\mathrm{cs}j}(s)+M_{ji}(s)\cdot\sum_{i=1,i\neq j}^{n}i_{\mathrm{cs}i}(s)\\&=\frac{\sum_{i=1,i\neq j}^{n}Y_{\mathrm{cs}i}(s)}{\sum_{i=1}^{n}Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot i_{\mathrm{cs}j}(s)\\&\quad-\frac{Y_{\mathrm{cs}j}(s)}{\sum_{i=1}^{n}Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot\sum_{i=1,i\neq j}^{n}i_{\mathrm{cs}i}(s).\end{aligned} \tag{21}$$

On the right side of (19), the first part ($i_{\mathrm{g}j}$) represents the net current injected by inverter *j* into the grid, and the second part represents the sum of the net currents injected by inverter *j* into other ($n-1$) inverters (which are actually the interactive currents). Fig. 3 has just given the illustration of these currents' flowing. Thus, it can be seen that, for the multi-inverter-paralleled grid-connected system in the weak grid, there are not only the currents injected by the inverters into the grid, but also the interactive currents among the inverters.

Besides, from (21) we can further get the expression of single interactive current as

$$\begin{aligned}i_{ji}(s)&=\frac{Y_{\mathrm{cs}i}(s)}{\sum_{i=1}^{n}Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot i_{\mathrm{cs}j}(s)\\&\quad-\frac{Y_{\mathrm{cs}j}(s)}{\sum_{i=1}^{n}Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot i_{\mathrm{cs}i}(s).\end{aligned} \tag{22}$$

As for i_{ji}, it represents the net current injected by inverter *j* into inverter *i*. On the right side of (22), the first part is the response current in the output admittance of inverter *i* excited by inverter *j* as the source, and the second part is the response current in the output admittance of inverter *j* excited by inverter *i* as the source.

Obviously, the total grid current i_{g} is equal to the sum of the grid-side inductor currents i_{L2j} ($j=1, 2, \ldots, n$) of all the inverters, so based on (19) we can further get

$$i_{\mathrm{g}}(s)=\sum_{j=1}^{n}i_{L2j}(s)=\sum_{j=1}^{n}i_{\mathrm{g}j}(s)+\sum_{j=1}^{n}\sum_{i=1,i\neq j}^{n}i_{ji}(s). \tag{23}$$

As for the second part of the right side of (23), we can derive (24), shown at the bottom of next page. Combining with (22), the first term here is taken as an example to be derived as (25), shown at the bottom of next page.

Similarly, we can find that the rest terms, i.e., $i_{13}(s)+i_{31}(s)$, $i_{14}(s)+i_{41}(s), \ldots, i_{23}(s)+i_{32}(s)$, $i_{24}(s)+i_{42}(s), \ldots, i_{(n\text{-}1)n}(s)$

$$\mathbf{i_{L2,n\times 1}}=\mathbf{M_{n\times n}}\cdot\mathbf{i_{cs,n\times 1}}-\mathbf{N_{n\times 1}}\cdot v_{\mathrm{g}}(s)\Leftrightarrow$$

$$\begin{bmatrix}i_{L21}(s)\\\cdots\\i_{L2j}(s)\\\cdots\\i_{L2n}(s)\end{bmatrix}=\begin{bmatrix}M_{11}(s)&\cdots&M_{1j}(s)&\cdots&M_{1n}(s)\\\cdots&\cdots&\cdots&\cdots&\cdots\\M_{j1}(s)&\cdots&M_{jj}(s)&\cdots&M_{jn}(s)\\\cdots&\cdots&\cdots&\cdots&\cdots\\M_{n1}(s)&\cdots&M_{nj}(s)&\cdots&M_{nn}(s)\end{bmatrix}\cdot\begin{bmatrix}i_{\mathrm{cs}1}(s)\\\cdots\\i_{\mathrm{cs}j}(s)\\\cdots\\i_{\mathrm{cs}n}(s)\end{bmatrix}-\begin{bmatrix}N_1(s)\\\cdots\\N_j(s)\\\cdots\\N_n(s)\end{bmatrix}\cdot v_{\mathrm{g}}(s) \tag{15}$$

$$\mathbf{i_{L2,n\times 1}}=\mathbf{M_{a,n\times n}}\cdot\mathbf{i_{cs,n\times 1}}-\mathbf{N_{n\times 1}}\cdot v_{\mathrm{g}}(s)+\mathbf{M_{b,n\times n}}\cdot\mathbf{i_{cs,n\times 1}}\Leftrightarrow$$

$$\begin{bmatrix}i_{L21}(s)\\\cdots\\i_{L2j}(s)\\\cdots\\i_{L2n}(s)\end{bmatrix}=\begin{bmatrix}M_{11,a}(s)&\cdots&0&\cdots&0\\\cdots&\cdots&\cdots&\cdots&\cdots\\0&\cdots&M_{jj,a}(s)&\cdots&0\\\cdots&\cdots&\cdots&\cdots&\cdots\\0&\cdots&0&\cdots&M_{nn,a}(s)\end{bmatrix}\cdot\begin{bmatrix}i_{\mathrm{cs}1}(s)\\\cdots\\i_{\mathrm{cs}j}(s)\\\cdots\\i_{\mathrm{cs}n}(s)\end{bmatrix}-\begin{bmatrix}N_1(s)\\\cdots\\N_j(s)\\\cdots\\N_n(s)\end{bmatrix}\cdot v_{\mathrm{g}}(s)$$

$$+\begin{bmatrix}M_{11,b}(s)&\cdots&M_{1j}(s)&\cdots&M_{1n}(s)\\\cdots&\cdots&\cdots&\cdots&\cdots\\M_{j1}(s)&\cdots&M_{jj,b}(s)&\cdots&M_{jn}(s)\\\cdots&\cdots&\cdots&\cdots&\cdots\\M_{n1}(s)&\cdots&M_{nj}(s)&\cdots&M_{nn,b}(s)\end{bmatrix}\cdot\begin{bmatrix}i_{\mathrm{cs}1}(s)\\\cdots\\i_{\mathrm{cs}j}(s)\\\cdots\\i_{\mathrm{cs}n}(s)\end{bmatrix} \tag{16}$$

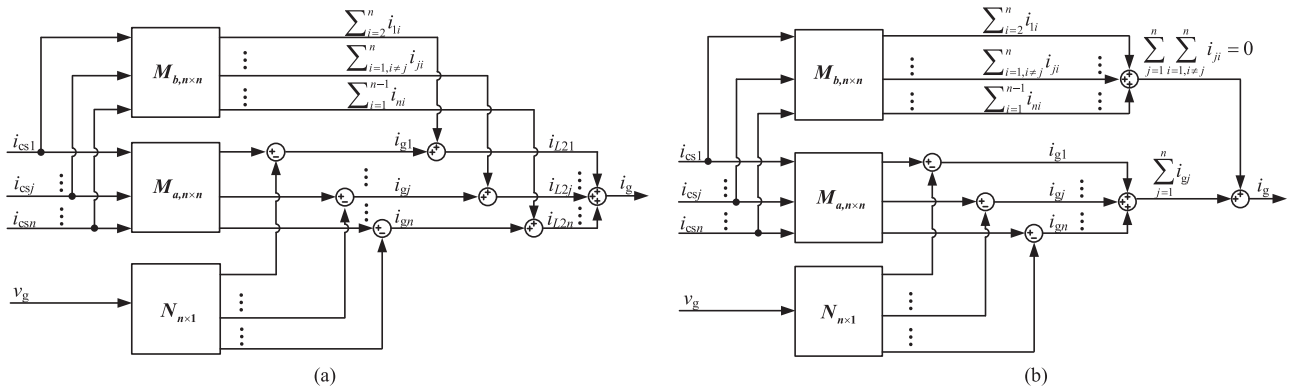

Fig. 5. Equivalent transformation of control block diagram of the interactive-stability of system. (a) Equivalent block diagram of the interactive stability in Fig. 4. (b) Further equivalent block diagram.

$+ i_{n(n\text{-}1)}(s)$ all equal to 0 respectively by obtaining their expressions from (22). Thus, we can get

$$\sum_{j=1}^{n}\sum_{i=1,i\neq j}^{n} i_{ji}(s) = 0. \tag{26}$$

This manifests that the sum of the interaction currents among the inverters is zero, that is, the interaction currents among the inverters are cancelled out by each other. Then, by substituting (26) into (23), we could obtain

$$i_{\mathrm{g}}(s) = \sum_{j=1}^{n} i_{\mathrm{g}j}(s). \tag{27}$$

So, we can conclude that the total grid current i_{g} is actually equal to the sum of the net currents injected into the grid by all the inverters. Accordingly, Fig. 5(a) could be further equivalent to Fig. 5(b).

It is noteworthy that, in all of the above derivation process there is no premise of parameters being the same, which means that the conclusion we get has a good generality for universal parallel system.

B. Grid-Impedance Allocation Mechanism

As for the net current $i_{\mathrm{g}j}(s)$ of each inverter, we can get the following equation according to (20) and make further derivation as

$$\begin{aligned} i_{\mathrm{g}j}(s) &= \frac{Z_{\mathrm{cs}j}(s)\cdot i_{\mathrm{cs}j}(s) - v_{\mathrm{g}}(s)}{Z_{\mathrm{g}}(s)\cdot Z_{\mathrm{cs}j}(s)\cdot\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s) + Z_{\mathrm{cs}j}(s)} \\ &\triangleq \frac{Z_{\mathrm{cs}j}(s)\cdot i_{\mathrm{cs}j}(s) - v_{\mathrm{g}}(s)}{Z_{\mathrm{g}j}(s) + Z_{\mathrm{cs}j}(s)} \end{aligned} \tag{28}$$

where

$$\begin{aligned} Z_{\mathrm{g}j}(s) &= Z_{\mathrm{cs}j}(s)\cdot\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s)\cdot Z_{\mathrm{g}}(s) \\ &= \frac{Z_{\mathrm{cs}j}(s)}{Z_{\mathrm{cs}1}(s)\parallel Z_{\mathrm{cs}2}(s)\parallel\cdots\parallel Z_{\mathrm{cs}n}(s)}\cdot Z_{\mathrm{g}}(s). \end{aligned} \tag{29}$$

The corresponding admittance $Y_{\mathrm{g}j}(s)$ of $Z_{\mathrm{g}j}(s)$ is

$$Y_{\mathrm{g}j}(s) = \frac{Y_{\mathrm{cs}j}(s)}{Y_{\mathrm{cs}1}(s)+Y_{\mathrm{cs}2}(s)+\cdots+Y_{\mathrm{cs}n}(s)}\cdot Y_{\mathrm{g}}(s). \tag{30}$$

$$\begin{aligned} &\sum_{j=1}^{n}\sum_{i=1,i\neq j}^{n} i_{ji}(s) = \sum_{i=2}^{n} i_{1i}(s) + \sum_{i=1,i\neq 2}^{n} i_{2i}(s) + \cdots + \sum_{i=1,i\neq n}^{n} i_{ni}(s) \\ &= [i_{12}(s)+i_{13}(s)+\cdots+i_{1n}(s)] + [i_{21}(s)+i_{23}(s)+\cdots+i_{2n}(s)] + \cdots + [i_{n1}(s)+i_{n2}(s)+\cdots+i_{n(n-1)}(s)] \\ &= \underbrace{\{[i_{12}(s)+i_{21}(s)]+[i_{13}(s)+i_{31}(s)]+\cdots\}}_{(n-1)\text{terms}} + \underbrace{\{[i_{23}(s)+i_{32}(s)]+[i_{24}(s)+i_{42}(s)]+\cdots\}}_{(n-2)\text{terms}} \\ &\quad + \cdots + \underbrace{[i_{(n-1)n}(s)+i_{n(n-1)}(s)]}_{1\text{term}} \end{aligned} \tag{24}$$

$$\begin{aligned} &i_{12}(s)+i_{21}(s) \\ &= \left[\frac{Y_{\mathrm{cs}2}(s)}{\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot i_{\mathrm{cs}1}(s) - \frac{Y_{\mathrm{cs}1}(s)}{\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot i_{\mathrm{cs}2}(s)\right] \\ &\quad + \left[\frac{Y_{\mathrm{cs}1}(s)}{\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot i_{\mathrm{cs}2}(s) - \frac{Y_{\mathrm{cs}2}(s)}{\sum_{i=1}^{n} Y_{\mathrm{cs}i}(s)+Y_{\mathrm{g}}(s)}\cdot i_{\mathrm{cs}1}(s)\right] = 0 \end{aligned} \tag{25}$$

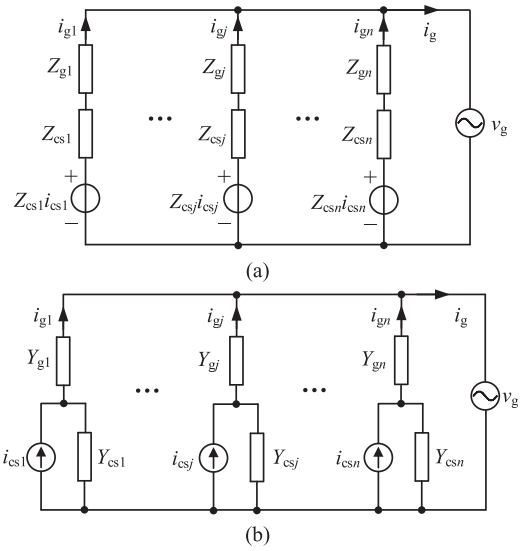

Fig. 6. Grid impedance equivalent allocation circuit of multiparalleled grid-connected inverters system. (a) Equivalent transformation circuit of Fig. 3. (b) Further equivalent transformation circuit.

According to (27) and (28), we can get the equivalent circuit diagram of Fig. 3, as shown in Fig. 6(a). Furthermore, by returning the Thevenin circuit of each inverter in Fig. 6(a) to its Norton circuit, we can obtain the final equivalent circuit diagram of the parallel system, as shown in Fig. 6(b). It can be seen that the grid impedance has been equivalently allocated to each inverter according to (29). In other words, each inverter in parallel operation does not work with the original grid impedance, but works equivalently with the allocated grid impedance affected by the output impedance of other inverters.

As is pointed out in [31] that there is the resonant frequency forbidden region for digital-controlled grid-connected inverter with capacitor-current feedback active-damping, and design considerations are given for the relevant parameters to refrain them out of the forbidden region amid the grid impedance variation, thus ensuring the stability of single inverter. While for parallel system, with the grid impedance allocated to each module, the coupling relationship among inverters induced by grid impedance is decoupled. Moreover, inverters will work with newly allocated grid-impedance instead of the original one, and thus they may touch the restricted area again to cause the instability of the parallel system. This is what the grid-impedance allocation mechanism could reveal and also the merit of it. Then, measures need to be taken to improve the robustness of the whole system.

It can be obtained from Fig. 6 that, after the grid impedance is allocated, the net current $i_{gj}(s)$ of the jth inverter is

$$i_{gj}(s) = \frac{Y_{gj}(s)}{Y_{csj}(s)+Y_{gj}(s)} \cdot i_{csj}(s) - \frac{Y_{csj}(s)Y_{gj}(s)}{Y_{csj}(s)+Y_{gj}(s)} \cdot v_g(s) \triangleq \varepsilon_j(s) \cdot [i_{csj}(s) - Y_{csj}(s)v_g(s)] \quad (31)$$

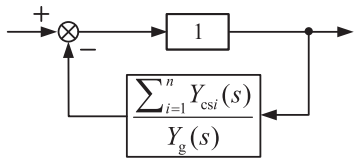

Fig. 7. Block diagram of $\varepsilon(s)$.

where

$$\varepsilon_j(s) = \frac{1}{1+\frac{Y_{csj}(s)}{Y_{gj}(s)}}. \quad (32)$$

Combining the analysis in Section II, we can make further deduction. If the self-stability of each inverter can be guaranteed, the part of $[i_{csj}(s)–Y_{csj}(s)v_g(s)]$ in (31) will have no RHP poles [31]. Then, the stability of i_{gj} after the allocation of the grid impedance will depend on whether $\varepsilon_j(s)$ contains the RHP poles. By substituting (30) into (32), we have

$$\varepsilon_j(s) = \frac{1}{1+\frac{\sum_{i=1}^{n} Y_{csi}(s)}{Y_g(s)}} \triangleq \varepsilon(s). \quad (33)$$

It can be found that the expression of $\varepsilon_j(s)$ for each inverter is the same in spite of all the modules having different parameters, that is, after the equivalent allocation of the grid impedance, each inverter in the parallel system has the same stability.

Summarizing the above discussion, we could obtain the stability criterion applicable to the general multi-inverter-paralleled grid-connected system in the weak grid, which is as follows.

1) Guaranteeing that each inverter itself should be stable without considering the grid impedance, thereby ensuring the self-stability of each inverter.
2) Guaranteeing that $\varepsilon(s)$ should not contain RHP poles, that is, any inverter with equivalently allocated grid impedance could be stable, thereby ensuring the interactive-stability of the system.

IV. Robustness of Multi-Inverter-Paralleled Grid-Connected System Against Grid Impedance

To ensure the interactive-stability of the whole system, $\varepsilon(s)$ should not have RHP poles. In terms of $\varepsilon(s)$, it can be regarded as a negative-feedback closed-loop system, as shown in Fig. 7. Then, we can get that as long as the open-loop function $\sum_{i=1}^{n} Y_{csi}(s)/Y_g(s)$ satisfies the Nyquist stability criterion, the stability of $\varepsilon(s)$ could be guaranteed.

If the self-stability of each inverter has been guaranteed, the output admittance of each inverter does not contain RHP poles. Then, the number of RHP poles of $\sum_{i=1}^{n} Y_{csi}(s)/Y_g(s)$ will be zero. Hence, to ensure the stability of $\varepsilon(s)$, it is required that the amplitude-frequency curve of $\sum_{i=1}^{n} Y_{csi}(s)$ has no intersection with that of $Y_g(s)$, or that the phase margin PM at the intersection frequency f_{cr} is positive when they have intersection [32]. Here, the expression of PM is

$$\mathrm{PM} = 180^\circ - \left(\angle \sum_{i=1}^{n} Y_{csi}(j2\pi f_{cr}) - \angle Y_g(j2\pi f_{cr})\right). \quad (34)$$

Obviously, the phase of $Y_g(s)$ is constant value of $-90°$. So, to ensure the interactive-stability of the system, it is required that the phase of $\sum_{i=1}^{n} Y_{csi}(s)$ at the frequency f_{cr} is less than 90°.

A. Effect of Digital-Control Delay on Output Admittance and Optimal Capacitor-Current-Feedback Coefficient

Still, we begin the analysis with single inverter here. For any single grid-connected inverter j, to ensure the stability of the inverter, the phase of output admittance $Y_{csj}(s)$ is required to be less than 90° at the frequency f_{cr}. The sufficient condition to meet this requirement is that $Y_{csj}(s)$ shows the positive-resistance characteristic at the frequency f_{cr}, which means $\mathrm{Re}\{Y_{csj}(j2\pi f)\} > 0$.

The expression of the output admittance $Y_{csj}(s)$ is shown in (7). Since the current regulator $G_{ij}(s)$ can be approximated as a proportional link K_{pj} at the frequency over the crossover frequency of the current loop [33], $Y_{csj}(s)$ can thus be obtained as (35), shown at the bottom of this page. By substituting $s = j2\pi f$ into (35), the real part of $Y_{csj}(j2\pi f)$ can be obtained as

$$\mathrm{Re}\{Y_{csj}(j2\pi f)\} = \frac{K_{PWMj}\cos(3\pi T_{sj} f)\cdot\gamma_j}{a_j{}^2 + b_j{}^2} \tag{36}$$

where γ_j, a_j, and b_j are shown as

$$\gamma_j = (2\pi f)^2 L_{1j}C_j\cdot(H_{i1\_j} - H_{i2\_j}K_{pj}) + H_{i2\_j}K_{pj}$$

$$a_j = K_{PWMj}\cos(3\pi T_{sj} f)\cdot\left[H_{i2\_j}K_{pj} - (2\pi f)^2 L_{2j}C_j H_{i1\_j}\right]$$

$$\begin{aligned} b_j = & -H_{i2\_j}K_{PWMj}K_{pj}\sin(3\pi T_{sj} f) \\ & + 2\pi f(L_{1j}+L_{2j}) + (2\pi f)^2 L_{2j}C_j H_{i1\_j}K_{PWMj} \\ & \times \sin(3\pi T_{sj} f) - (2\pi f)^3 L_{1j}L_{2j}C_j. \end{aligned} \tag{37}$$

Obviously, the sign of $\mathrm{Re}\{Y_{csj}(j2\pi f)\}$ is mainly affected by two factors: $\cos(3\pi T_{sj} f)$ related to the digital-control delay and γ_j.

Let $\gamma_j = 0$, we can derive the boundary frequencies of γ_j as

$$f_{pj} = \frac{1}{2\pi}\sqrt{\frac{H_{i2\_j}K_{pj}}{L_{1j}C_j\cdot(H_{i2\_j}K_{pj} - H_{i1\_j})}}. \tag{38}$$

Fig. 8 shows the curves of $\cos(3\pi T_{sj} f)$ and γ_j varying with the frequency within the Nyquist frequency range ($f \le f_{sj}/2$). It can be seen that the sign of $\cos(3\pi T_{sj} f)$ changes at $f_{sj}/6$. Meanwhile the sign of γ_j varies with the value of f_{pj}. As a result, the variation of $\cos(3\pi T_{sj} f)$ together with that of γ_j would bring about the change in the sign of $\mathrm{Re}\{Y_{csj}(j2\pi f)\}$. Specifically:

1) when $f_{pj} < f_{sj}/6$, $\mathrm{Re}\{Y_{csj}(j2\pi f)\} \le 0$ during $[f_{pj}, f_{sj}/6]$;
2) when $f_{pj} > f_{sj}/6$, $\mathrm{Re}\{Y_{csj}(j2\pi f)\} \le 0$ during $[f_{sj}/6, f_{pj}]$;
3) when $f_{pj} = f_{sj}/6$, $\mathrm{Re}\{Y_{csj}(j2\pi f)\} = 0$ at frequency $f_{sj}/6$.

From (38), we can find that the variation of f_{pj} could be achieved by adjusting H_{i1_j}. Especially when $f_{pj} = f_{sj}/6$, we

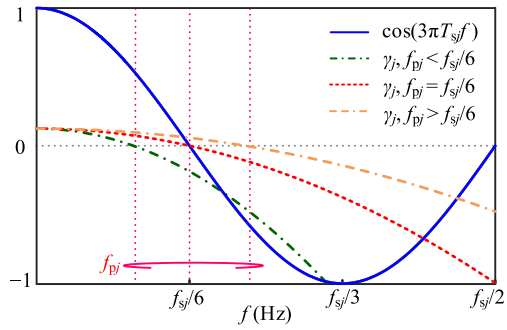

Fig. 8. Curves of $\cos(3\pi T_{sj} f)$ and γ_j vary with frequency.

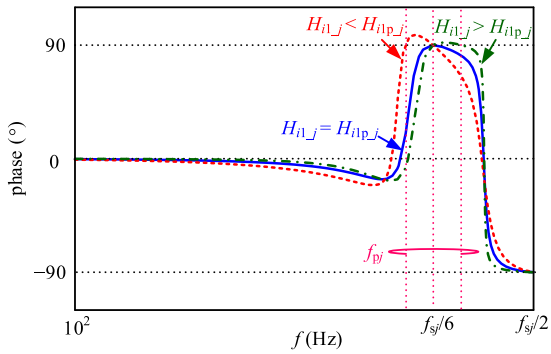

Fig. 9. Phase-frequency plot of $Y_{csj}(s)$ corresponding to different H_{i1_j}.

can acquire the expression of H_{i1_j} as

$$H_{i1\_j} = H_{i2\_j}K_{pj}\cdot\left(1 - \frac{9}{\pi^2 f_{sj}^2 L_{1j}C_j}\right) \triangleq H_{i1p\_j}. \tag{39}$$

Then, we can get the phase-frequency plots of the output admittance Y_{csj} corresponding to the different H_{i1_j}, as shown in Fig. 9. Consequently, we could obtain the non-positive-resistance region with different values of H_{i1_j} as follows:

1) when $H_{i1\_j} < H_{i1p\_j}$, $\mathrm{Re}\{Y_{csj}(j2\pi f)\} \le 0$ during $[f_{pj}, f_{sj}/6]$;
2) when $H_{i1\_j} > H_{i1p\_j}$, $\mathrm{Re}\{Y_{csj}(j2\pi f)\} \le 0$ during $[f_{sj}/6, f_{pj}]$;
3) when $H_{i1\_j} = H_{i1p\_j}$, $\mathrm{Re}\{Y_{csj}(j2\pi f)\} = 0$ at $f_{pj} = f_{sj}/6$.

If the amplitude-frequency curves of Y_{csj} and $Y_g(s)$ intersect in the frequency range of $\mathrm{Re}\{Y_{csj}(j2\pi f)\} \le 0$, the phase margin PM will be negative (or zero), and the system will be unstable (or critically stable). This indicates that H_{i1p_j} is the optimal capacitor-current-feedback coefficient.

B. Effect of Digital-Control Delay on the Robustness of Multi-Inverter System Against Grid Impedance

For the multi-inverter system, to ensure the system stability, the phase of $\sum_{i=1}^{n} Y_{csi}$ at f_{cr} is required to be less than 90°. The

$$Y_{csj}(s) = \frac{s^2 L_{1j}C_j + sC_j H_{i1\_j}K_{PWMj}e^{-1.5sT_{sj}} + 1}{s^3 L_{1j}L_{2j}C_j + s^2 L_{2j}C_j H_{i1\_j}K_{PWMj}e^{-1.5sT_{sj}} + s(L_{1j}+L_{2j}) + H_{i2\_j}K_{PWMj}K_{pj}e^{-1.5sT_{sj}}} \tag{35}$$

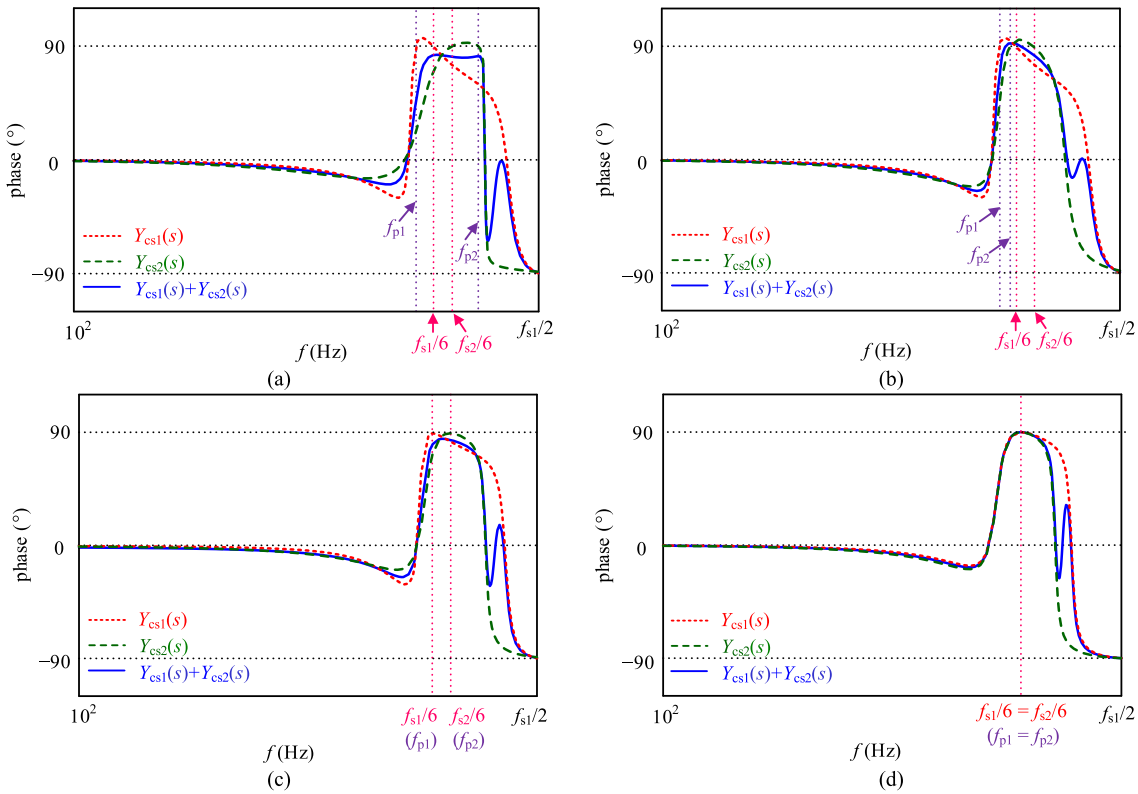

Fig. 10. Phase-frequency plots of $Y_{cs1}(s)$, $Y_{cs2}(s)$, and $Y_{cs1}(s)+Y_{cs2}(s)$ for several typical cases. (a) $f_{p1} \neq f_{s1}/6, f_{p2} \neq f_{s2}/6, f_{s1} \neq f_{s2}$, the negative resistance area of $Y_{cs1}(s) + Y_{cs2}(s)$ is completely cancelled. (b) $f_{p1} \neq f_{s1}/6, f_{p2} \neq f_{s2}/6, f_{s1} \neq f_{s2}$, the negative resistance area of $Y_{cs1}(s) + Y_{cs2}(s)$ still exists. (c) $f_{p1} = f_{s1}/6, f_{p2} = f_{s2}/6, f_{s1} \neq f_{s2}$, the negative resistance area of $Y_{cs1}(s) + Y_{cs2}(s)$ is completely cancelled. (d) $f_{p1} = f_{p2} = f_{s1}/6, f_{s1} = f_{s2}$, the real part of $Y_{cs1}(s) + Y_{cs2}(s)$ is zero at $f_{s1}/6$.

sufficient condition to meet this requirement is that the real part of $\sum_{i=1}^{n} Y_{csi}$ at the intersection frequency f_{cr} is positive. Here, the real part of $\sum_{i=1}^{n} Y_{csi}$ can be expressed as

$$\mathrm{Re}\left\{\sum_{i=1}^{n} Y_{csi}(j2\pi f)\right\} = \sum_{i=1}^{n} \mathrm{Re}\left\{Y_{csi}(j2\pi f)\right\}. \tag{40}$$

Evidently, if the real part of the output admittance Y_{csj} ($j = 1, 2, \ldots, n$) of all the inverters is nonpositive, the real part of $Y_{cs1} + Y_{cs2} + \ldots + Y_{csn}$ would inevitably be non-positive. With reference to Fig. 9 and analysis of the output admittance of the single inverter, we can find that the negative-resistance region of the output admittance of each inverter may probably be different since no matter f_{pj} or $f_{sj}/6$ is different for each inverter, which results from the difference in the *LCL*-filter, current regulator, and sampling frequency of each inverter. In the meanwhile, the negative-resistance region tends to appear near $f_{sj}/6$. In a parallel system of n inverters, there can be at most n different negative-resistance regions, which may be cancelled out or overlapped to generate a new negative-resistance region.

To facilitate analysis, a two-inverter grid-connected system is taken as an example for discussion. The phase-frequency plots of Y_{cs1}, Y_{cs2}, and $Y_{cs1} + Y_{cs2}$ for several typical cases are depicted in Fig. 10. Under the condition of $f_{p1} \neq f_{s1}/6$, $f_{p2} \neq f_{s2}/6$, and $f_{s1} \neq f_{s2}$, the phase-frequency curves of Y_{cs1} and Y_{cs2} will have different negative-resistance regions and the sum of them has two cases primarily. One case is that, the two negative-resistance regions are cancelled out, as shown in Fig. 10(a). It means that the robustness is improved. The other case is, the two negative-resistance regions are overlapped to a certain extent to create a new one, as shown in Fig. 10(b). It means that the poor robustness is maintained. It could be found that when facing the parallel system composed of inverters with different sampling frequencies, the random value of H_{i1_j} may cause completely different operating results to the system. It is expected that the more the number of the paralleled inverters, the more complex and uncontrollable the situation would be.

In order to ensure the controllability of the parallel system, the optimal coefficient H_{i1p_j} is preferred for choice. This way we can at least guarantee the critical stability of each inverter. So we can get the third case, which is $f_{p1} = f_{s1}/6, f_{p2} = f_{s2}/6$, and $f_{s1} \neq f_{s2}$. As for this case, the phase-frequency curves of Y_{cs1} and Y_{cs2} are tangent to 90° at $f_{s1}/6$ and $f_{s2}/6$, respectively. Then, the real part of $Y_{cs1} + Y_{cs2}$ will always be positive, as shown in Fig. 10(c). Therefore, the improvement of robustness for the parallel system could be controllably guaranteed by employing H_{i1p_j}. While, the difference of the sampling frequency resided in each module may be not so much. Thus, it is expected that the phase margin of the system might be not big enough. Especially for the situation when the two inverters having the same sampling frequency (i.e., $f_{s1} = f_{s2}$), it should be noted that, the real part of $Y_{cs1} + Y_{cs2}$ is still be zero at $f_{s1}/6$ ($f_{s2}/6$) even if each inverter adopts its

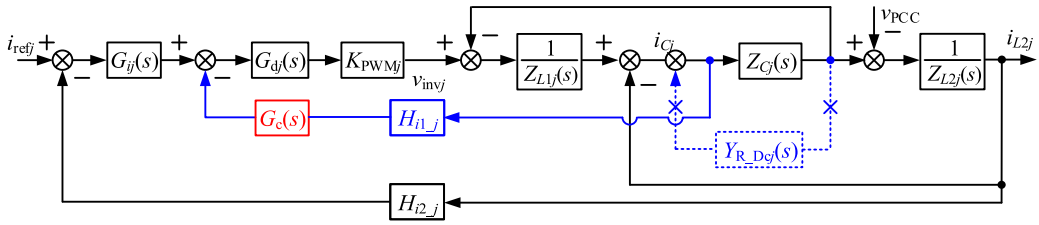

Fig. 11. Control block diagram of the *LCL*-type grid-connect inverter with phase-lead compensator.

optimal coefficient H_{i1p_j}. This is just the fourth case shown in Fig. 10(d). At this time, if the amplitude-frequency curves of $\sum_{i=1}^{n} Y_{csi}(s)$ and $Y_g(s)$ intersect at $f_{s1}/6$ ($f_{s2}/6$), the system will be critically stable. As seen, the parallel system with the same sampling frequency is more likely to be unstable. So, some measures need to be taken to further improve the phase margin of the parallel system so as to make the system be more robust against various disturbances.

C. Introduction of Phase-Lead Compensation to Improve the Robustness of the System

The poor robustness results from the digital-control delay, which makes the capacitor-current feedback active-damping equivalent to a virtual impedance instead of a virtual resistance. From (1), we can get its virtual admittance form as

$$Y_{R\_Dj}(s) = \frac{1}{Z_{R\_Dj}(s)} = \frac{H_{i1\_j} K_{PWMj} C_j}{L_{1j}} \cdot e^{-1.5sT_{sj}} \triangleq \frac{1}{R_{dj}} e^{-1.5sT_{sj}}. \tag{41}$$

To make the compensation of the delay, we could consider introducing a phase-lead link by control theory into the above virtual admittance, deriving

$$Y_{R\_Dcj}(s) = \frac{1}{R_{dj}} \cdot \frac{1+aTs}{1+Ts} \cdot e^{-1.5sT_{sj}} \triangleq \frac{1}{R_{dj}} \cdot G_c(s) \cdot e^{-1.5sT_{sj}} \tag{42}$$

where

$$G_c(s) = \frac{1+aTs}{1+Ts}, \quad a \in (1, \infty). \tag{43}$$

Thus, we can acquire the control block diagram of inverter *j* in Fig. 11. By replacing the capacitor-voltage feedback $v_c(s)$ with the capacitor-current-feedback $i_c(s)$, and relocating the feedback node from the output of $1/sL_{1j}$ to that of $G_{ij}(s)$, we can find that the phase-lead compensator $G_c(s)$ is actually introduced into the capacitive-current feedback path [34]. Note that, the zero of $G_c(s)$ should be properly placed for compensating the phase-lag resulted from the digital-control delay in the vicinity of f_s. To aim this, the zero of $G_c(s)$, i.e., $1/(aT)$, is designed to locate at $2f_s$ in this article. Hence, aT is set to be $0.5T_s$. Furthermore, after using the bilinear transformation [35], the proposed phased-lead compensator $G_c(s)$ in *s*-domain can be rewritten as

$$G_c(s) = \frac{1+b}{1+b \cdot e^{-sT_s}}, \quad b \in (0,1) \tag{44}$$

where

$$b = \frac{a-1}{a+1}, \quad a \in (1, \infty). \tag{45}$$

Substituting $s = j\omega$ into (44), $\angle G_c(j\omega)$ can be acquired as

$$\angle G_c(j\omega) = \arccos \frac{1 + b\cos\omega T_s}{\sqrt{b^2 + 2b\cos\omega T_s + 1}}, b \in (0,1). \tag{46}$$

Rewriting (46), we have

$$\begin{aligned} &\cos \angle G_c(j\omega) \\ &= \frac{1 + b\cos\omega T_s}{\sqrt{b^2 + 2b\cos\omega T_s + 1}} \\ &= \frac{(b^2 + 2b\cos\omega T_s + 1) + 1 - b^2}{2 \cdot \sqrt{b^2 + 2b\cos\omega T_s + 1}} \\ &= \frac{|(\cos\omega T_s + j\sin\omega T_s) - (-b)|^2 + |1|^2 - |-b|^2}{2 \cdot |(\cos\omega T_s + j\sin\omega T_s) - (-b)| \cdot |1|} \\ &= \frac{AB^2 + OA^2 - OB^2}{2 \cdot AB \cdot OA}. \end{aligned} \tag{47}$$

Based on (47), we can draw the plot of $\angle G_c(j\omega)$ in the unit circle in the complex plane, as shown in Fig. 12. As seen, for a given value of *b*, $\angle G_c(j\omega)$ is almost 0 when ωT_s is close to 0 or π, but reaches the maximum when $\omega T_s = \pi/2$. Within the range of *b*, the maximum of $\angle G_c(j\omega)$ becomes larger with increased value of *b*. Hence, the phase-lead compensator can provide more compensation for the phase-lag if *b* is more approaching to 1. According to Fig. 12, we have

$$\angle G_c(j\omega) \in (0, \pi/4). \tag{48}$$

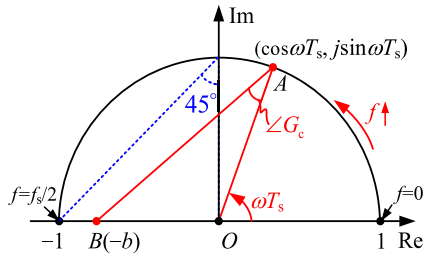

Fig. 12. Plot of $\angle G_c(j\omega)$ with frequency variation.

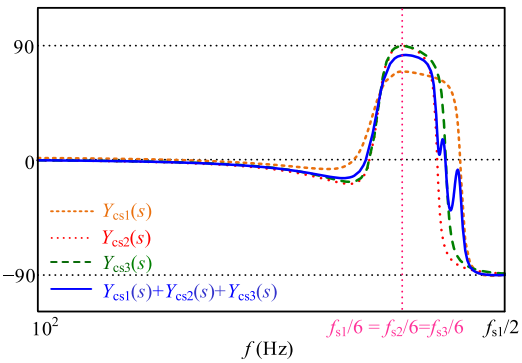

Fig. 13. Phase-frequency plots of $Y_{cs1}(s)$, $Y_{cs2}(s)$, $Y_{cs3}(s)$, and $Y_{cs1}(s) + Y_{cs2}(s) + Y_{cs3}(s)$ with the phase-lead compensator adopted for inverter 1.

As seen, to the maximum, a phase-angle of 45° can be compensated when b approaches to 1, which means a will be infinite. Then, $G_c(s)$ in (43) will reduce to a first-order differential compensator which would amplify the high frequency switching noises. Hence, to tradeoff the compensation performance and the noise immunity, b is set to be 0.8 in this article.

When it comes to inverter clusters with equal sampling frequency, it would be better for each module to employ the phase-lead compensator G_c. While actually, to ensure the stability of the parallel system, the least we could do is to guarantee the adoption of G_c for one of parallel inverters. And simultaneously, the rest of them use their own optimal capacitor-current-feedback coefficient H_{i1p_j}. Here, a three-module system with the same sampling frequency is taken as an example for illustration. G_c is added to inverter 1, and the rest two inverters adopt their H_{i1p_j}. The phase-frequency plots of $Y_{cs1}(s)$, $Y_{cs2}(s)$, $Y_{cs3}(s)$, and $Y_{cs1}(s) + Y_{cs2}(s) + Y_{cs3}(s)$ are shown in Fig. 13. It can be seen that due to the adoption of the phase-lead compensator, the phase of the Y_{cs1} at $f_{s1}/6$ ($f_{s2}/6$, $f_{s3}/6$) is compensated, and the real part of Y_{cs1} is always positive. Meanwhile, since the other two inverters adopts their H_{i1p_j}, the real part of Y_{cs2} and Y_{cs3} is zero only at $f_{s1}/6$ ($f_{s2}/6$, $f_{s3}/6$). Hence, the phase-frequency curve of $Y_{cs1}(s) + Y_{cs2}(s) + Y_{cs3}(s)$ will always be lower than 90°, thereby improving the robustness of the entire parallel system.

V. Example Illustration and Experiment Verification

For better demonstrating the validity of the aforementioned investigation, the grid-connected system consisting of two inverters is taken as an example to analyze the robustness of the inverter system in the weak grid. Since the resistor in the grid impedance helps to stabilize the system, the situation of pure inductor, serving as the worst case of inductive-resistive grid impedance, could be employed to investigate the robustness of the system against the grid impedance [36]. That is, $Z_g(s)$ could be expressed as sL_g here. The main system parameters are given in Table I, in which some parameters are intentionally set to be different to testify the generality of the previous theoretical analysis. With these parameters, a prototype of two-inverter *LCL*-type grid-connected system is also built and tested in the lab, and the prototype photo is shown in Fig. 14. In the experimental setup, an external inductor is connected in series with a programmable ac source (Chroma 6460) for emulating the power grid.

TABLE I
System Parameters

Parameter	Symbol	Value
Inverter-side inductor	L_{11}, L_{12}	550 μH, 550 μH
Filter capacitor	C_1, C_2	5 μF, 5 μF
Grid-side inductor	L_{21}, L_{22}	75 μH, 110 μH
Grid voltage (RMS)	V_g	110 V
Fundamental frequency	f_o	50 Hz
Dc-link voltage	V_{in1}, V_{in2}	180 V, 180 V
Output power	P_{o1}, P_{o2}	0.5 kW,1 kW
Carrier wave amplitude	V_{tri1}, V_{tri2}	3 V, 3 V
Sampling coefficient (i_{L21}, i_{L22})	H_{i2_1},H_{i2_2}	0.15, 0.15
phase-lead compensator	b	0.8

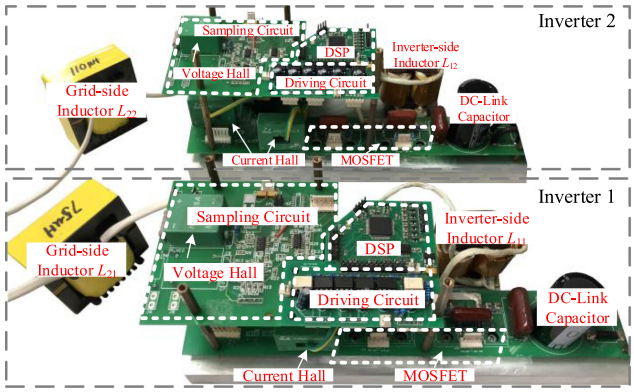

Fig. 14. Prototype photograph of the two-paralleled *LCL*-type grid-connected inverters.

First, example illustration is carried out in correspondence with the aforementioned first three cases in Fig. 10. Here, the two inverters are with different sampling frequency as $f_{s1} =$ 25 kHz and $f_{s2} =$ 30 kHz, respectively. In view of the weak grid, we consider that L_g varying from 0 to 10% per unit (p.u.) of L_{base} (corresponds to 3.85 mH). The bode plots of $Y_{cs1}(s)$ + $Y_{cs2}(s)$ and $Y_g(s)$ when $f_{s1} \neq f_{s2}$ for cases (a), (b), and (c) have been demonstrated in Fig. 15. Here, we suppose following the procedure that module 1 operates alone at first, and then module 2 enters to form the parallel system. Besides, the special parameters involving key information of the inverter system under the three cases are presented in Table II.

As for case (a), the optimal coefficient is not adopted for both H_{i1_1} and H_{i1_2}. As can be seen in Fig. 15(a), there exists a certain unstable frequency band marked in yellow. With the module 2 enters to form the parallel system, PM turns to be greater than 0 all the way, which means that the unstable area has been eliminated. As for case (b), the unstable range of inverter 1 is the same with that in case (a), while the different value of H_{i1_2} affects the stability condition of the parallel system. As a

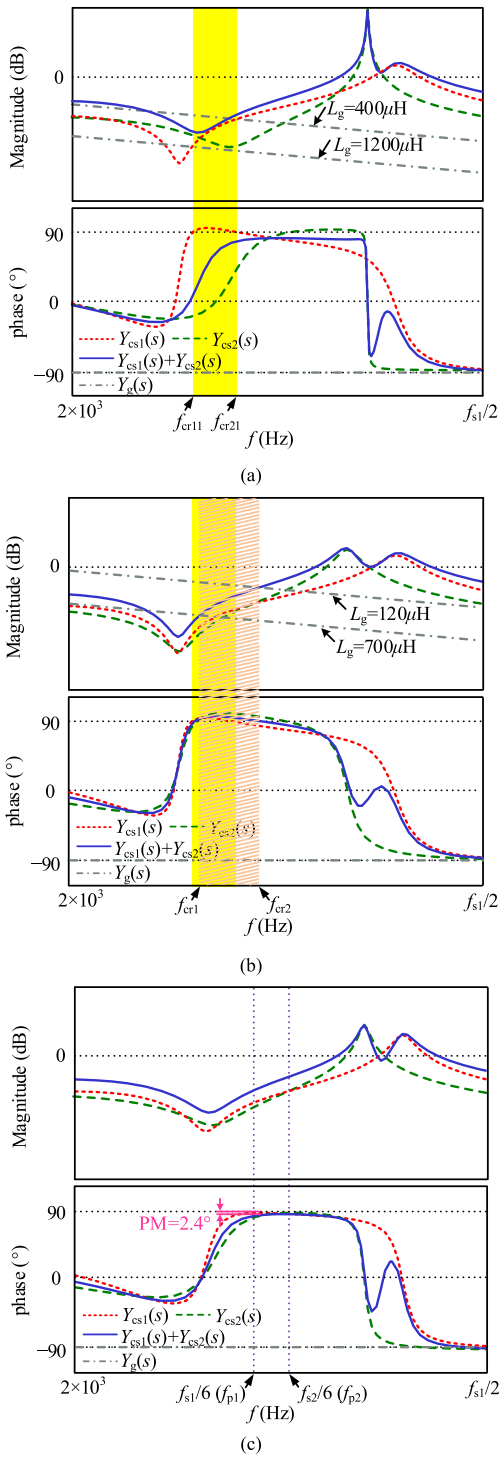

Fig. 15. Bode plots of $Y_{cs1}(s) + Y_{cs2}(s)$ and $Y_g(s)$ in three different cases when $f_{s1} \neq f_{s2}$.

result, there still exists another unstable frequency band for the parallel system, as refers to the orange shaded part in Fig. 15(b). In terms of case (c), optimal coefficient H_{i1p_j} has been selected for each module. It can be seen from Fig. 15(c) that, PM is always a positive value for the parallel system, which means system always stable regardless of $Y_{cs1}(s) + Y_{cs2}(s)$ intercepting

TABLE II
SPECIAL PARAMETERS IN CASES (A), (B), AND (C)

	f_{s1} = 25 kHz, f_{s2} = 30 kHz $G_{i1}(s)$ = 0.9+3000/s, $G_{i2}(s)$ = 0.831+2050/s		
	H_{i1_1},H_{i1_2}	Unstable range of L_g of inverter 1	Unstable range of L_g of the parallel system
Case (a)	0.025, 0.105	400 μH – 1200 μH	/
Case (b)	0.025, 0.03	400 μH – 1200 μH	120 μH – 700 μH
Case (c)	0.063, 0.079	/	/

with $Y_g(s)$ or not. Nevertheless, PM here is found to be only 2.4° at a minimum, which means that the safety margin is still not enough.

The experimental waveforms of the above three cases are given in Fig. 16. As we can see in Fig. 16(a), the inverter 1 is in the resonant state of independent operation in the beginning. Once the inverter 2 is enabled, the original resonance is effectively suppressed and the parallel system resumes stable operation. While, the experimental waveforms in Fig. 16(b) shows another case that the enable of inverter 2 fails to cancel the original negative resistance region, yet resonates with inverter 1 together instead. Then H_{i1p_1} and H_{i1p_2} are adopted for the two inverters respectively, and the waveforms in Fig. 16(c) just demonstrate that the system can be stable when the two inverters are in parallel operation. It can be seen that, the experimental results exactly match the previous analysis.

Hereafter we focus on the situation when two inverters have the same sampling frequency ($f_{s1} = f_{s2} = 30$ kHz). Here, capacitor-current-feedback coefficient is set as $H_{i1\_1} = 0.061$ and $H_{i1\_2} = H_{i1p\_2} = 0.079$, which means that inverter 1 does not select the optimal value while inverter 2 does. And the phase-lead compensator is introduced to inverter 1 in this application.

Fig. 17 depicts the bode plots of $Y_{cs1}(s) + Y_{cs2}(s)$ and $Y_g(s)$ before and after $G_c(s)$ being introduced into the inverter 1 under grid impedance variation. As seen, with the increase of the grid impedance, the amplitude-frequency curves of $Y_{cs1}(s) + Y_{cs2}(s)$ and $Y_g(s)$ without $G_c(s)$ do not intersect until the frequency point f_{cr2} when $L_g = 105$ μH. From this point on till f_{cr1} when $L_g = 267$ μH, the parallel system will be within the unstable frequency range marked in yellow. Then L_g proceeds to ascend, the parallel system will return to a stable state. However, after $G_c(s)$ is added, the unstable region has been eliminated. Moreover, when the grid impedance L_g changes, PM of the amplitude-frequency curve of $(Y_{cs1}(s) + Y_{cs2}(s))/ Y_g(s)$ at the intersection frequency is at least greater than 10.4°, which means that the robustness of the parallel system against the grid impedance has been effectively improved [14].

Fig. 18 show the full-power experimental waveforms of the grid-connected system against different grid-impedance under the condition of inverter 1 operating solely, inverter 2 plugging into the system and G_c being activated for inverter 1. Here, specific values of L_g are carefully selected as 75, 120, 160, and 660 μH, with which the parallel system without G_c are exactly located in the stable or unstable regions in Fig. 17. As shown in

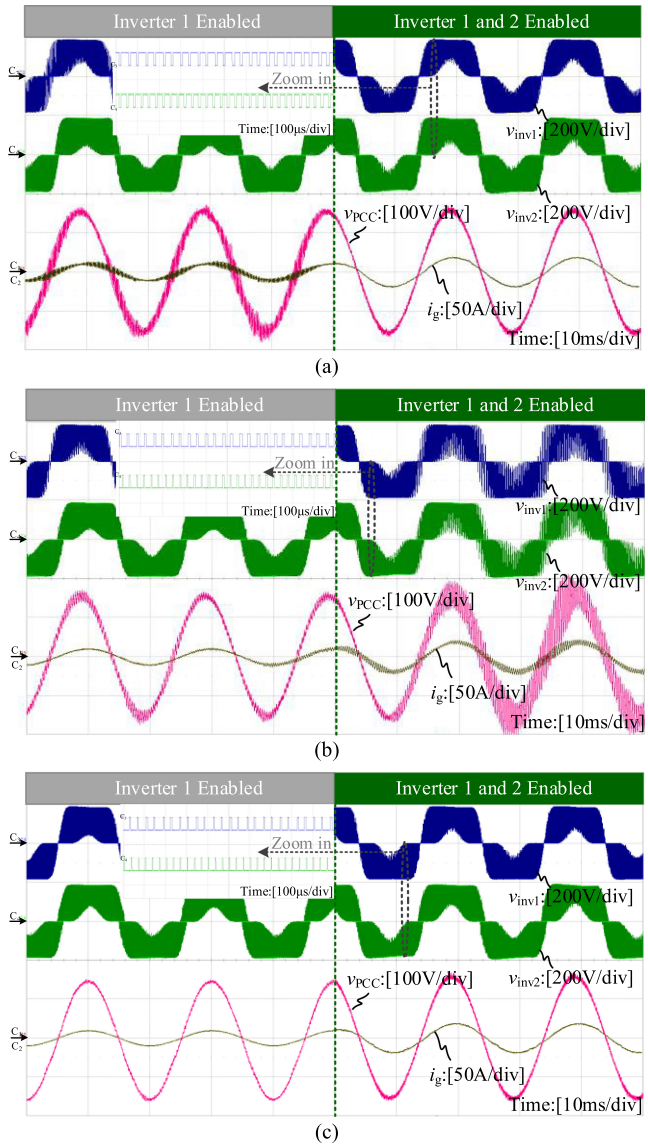

Fig. 16. Full power experimental waveforms of three typical cases when $f_{s1} \neq f_{s2}$ ($f_{s1} = 25$ kHz, $f_{s2} = 30$ kHz). (a) $L_g = 1000$ μH. (b) $L_g = 660$ μH. (c) $L_g = 560$ μH.

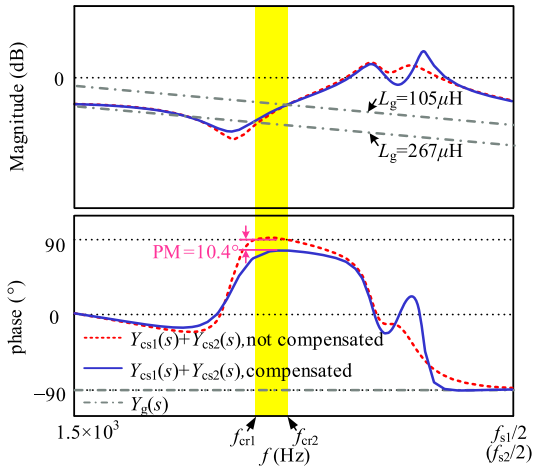

Fig. 17. Bode plots of $Y_{cs1}(s) + Y_{cs2}(s)$ and $Y_g(s)$ with and without the phase-lead compensator adopted for inverter 1 when $f_{s1} = f_{s2}$.

Fig. 18(a) and (d), when $L_g = 75$ μH (and 660 μH), the system is stable whenever inverter 1 works alone or two inverters operate together. Meanwhile, the system is always stable regardless of the activation of G_c for inverter 1. However, things change for the case of $L_g = 120$ μH (or 160 μH). Initially, inverter 1 can works stably alone. However, when inverter 2 plugging into the system, v_{PCC} and i_g oscillate significantly, which means that the system is no longer stable, as shown in Fig. 18(b) [or (c)]. This is because that with inverter 2 entering, the equivalent allocated grid impedance perceived by the inverter 1 has changed, resulting in the alteration in the system stability. Specifically, we can find from Fig. 17 that the PM at the corresponding intersection frequency is negative. Then, after adding G_c to inverter 1, the oscillations of v_{PCC} and i_g disappear, and the system returns to the stable state. Its rationale can turn to Fig. 17, which show that the system steps back into the stable region.

What is more, Fig. 19 also specifically gives the waveforms of i_{L21} and i_{L22} before and after G_c being activated for inverter 1. The experimental condition is the same as that in Fig. 18. It can be seen that with G_c introduced, the current oscillation of i_{L21} and i_{L22} in Fig. 19(b) and (c) can be suppressed promptly, which means that the robustness of the multi-inverter-paralleled system has been improved effectively.

Fig. 20 presents the dynamic experimental waveforms of the grid-connected inverter system after introducing G_c to inverter 1. It can be found that when the grid-side inductor current reference is stepped between half and full of the nominated value, i_{L21}, i_{L22}, i_g, and v_{PCC} have good dynamic performance. This indicates that the employment of the phase-lead compensator makes the system to have a robust adaptation to the grid-impedance variation.

To further study the validity of the proposed solution, we consider the situation of Z_g being inductive-resistive. Here, we let $Z_g = (0.3 + j0.08)$ Ω (i.e., $R = 0.3$ Ω and $L_g = 255$ μH with R/X as 3.75). The LCL parameters are just the same as those of module 1 in Table I. Fig. 21 gives the bode plots of grid admittance as well as inverter admittances with and without the phase-lead compensator. It can be seen that the system is always stable regardless the use of phase-lead compensator, due to the presence of R in grid impedance. Yet, the stability margin is less enough (PM $= 180° - (\angle Y_{cs}(j2\pi f_{cr1}) - \angle Y_g(j2\pi f_{cr1})) = 6.6°$) if the phase-lead compensator is not adopted. However, by incorporating the proposed phase-lead compensator G_c, the stable margin can be increased to 34.1°.

Fig. 22 shows the dynamic responses of inverters with and without phase-lead compensator when the grid-current reference steps down from full load to half load. It can be seen that the measured percentage of overshoot is reduced from 95% to 43% while the settling time is reduced from 1.58 to 0.92 ms by adopting the proposed phase-leading compensator. It is known from [36] that the system with smaller stability margin will suffer

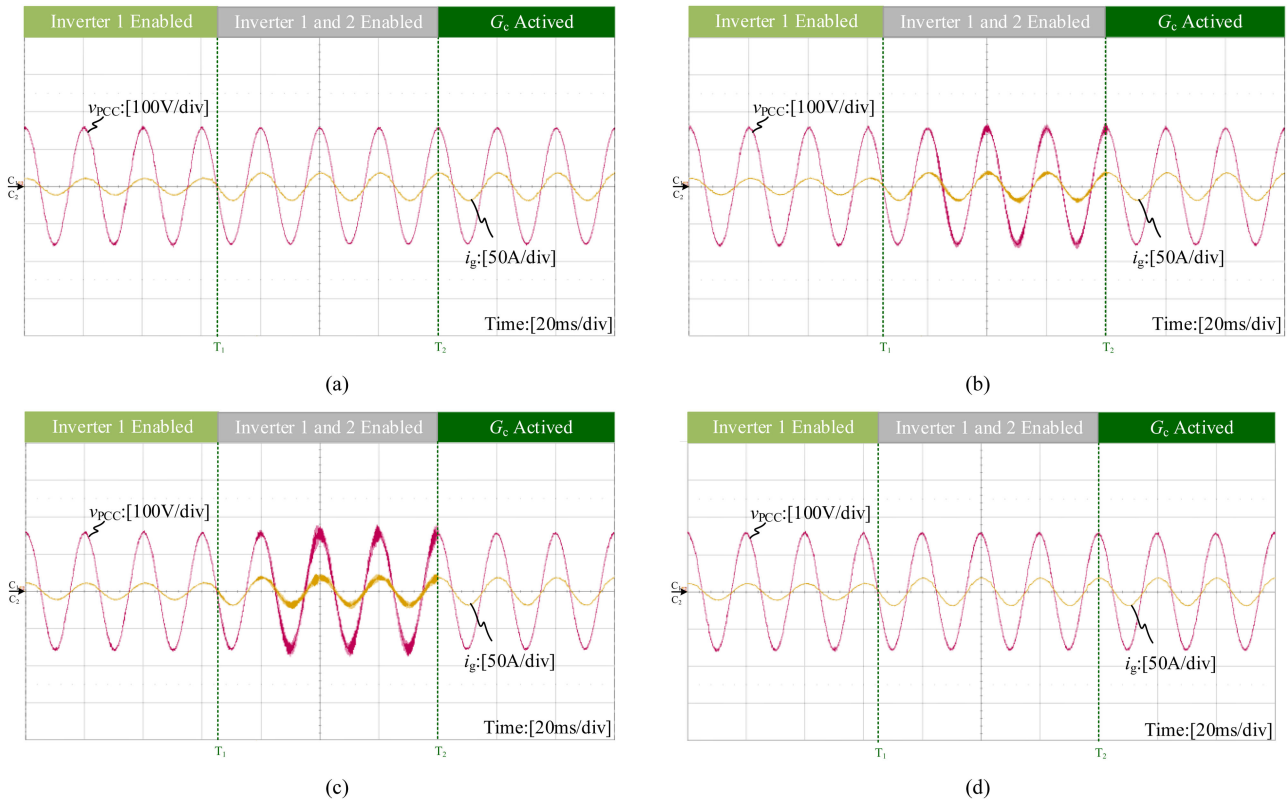

Fig. 18. Full-power experimental waveforms against different grid-impedance before and after inverter 2 plugging into the system, with and without G_c activated for inverter 1 when $f_{s1} = f_{s2} = 30$ kHz. (a) $L_g = 75$ μH. (b) $L_g = 120$ μH. (c) $L_g = 160$ μH. (d) $L_g = 660$ μH.

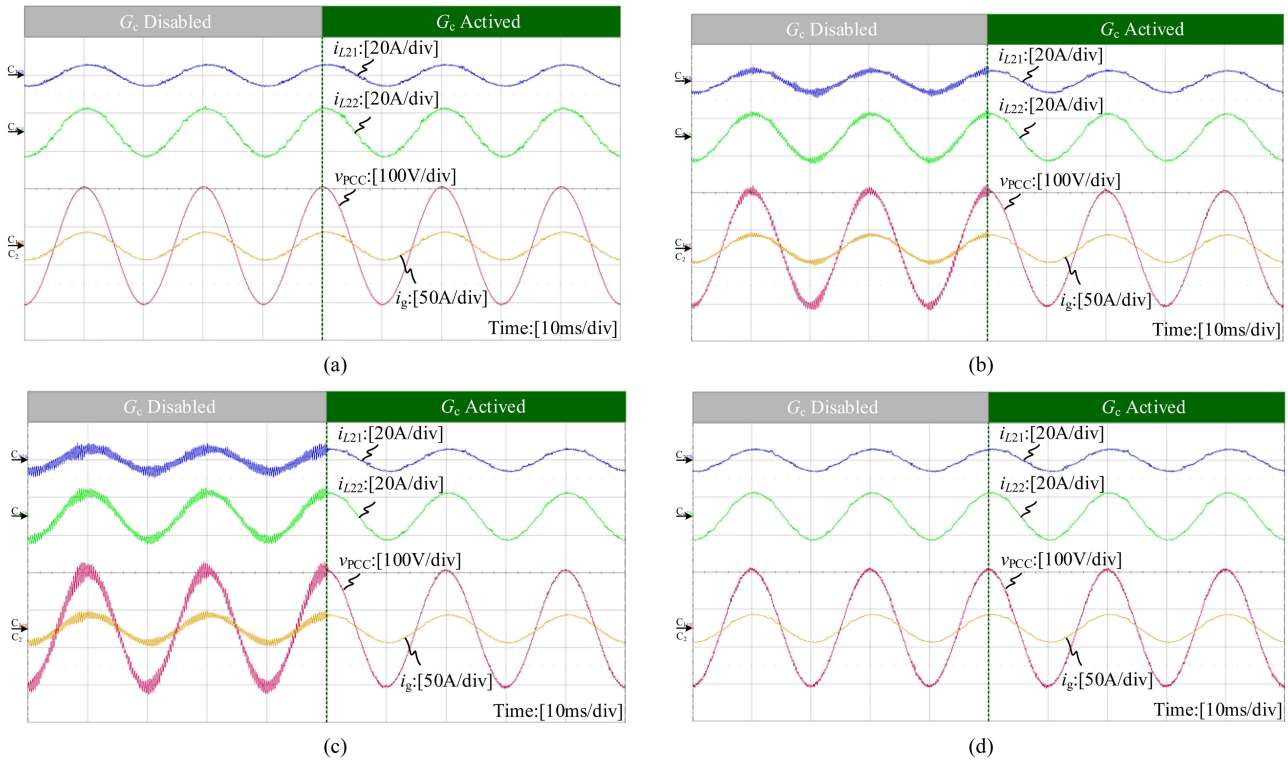

Fig. 19. Full-power experimental waveforms of the grid-connected inverter system with or without the phase-lead compensator when $f_{s1} = f_{s2} = 30$ kHz. (a) $L_g = 75$ μH. (b) $L_g = 120$ μH. (c) $L_g = 160$ μH. (d) $L_g = 660$ μH.

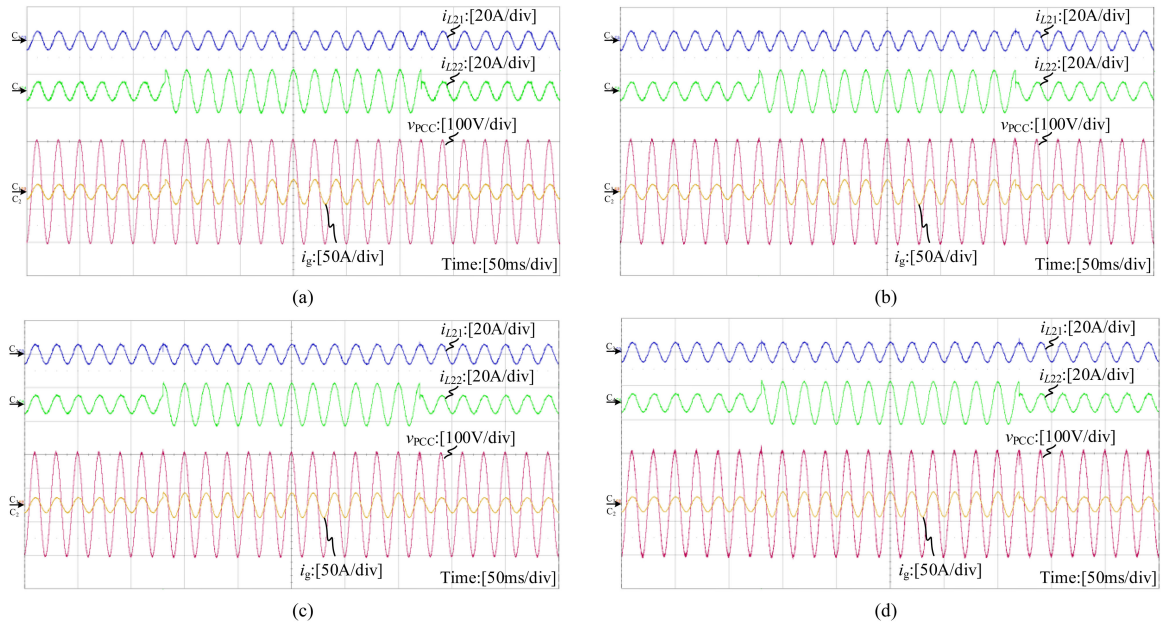

Fig. 20. Dynamic waveforms of the grid-connected inverter system with the phase-lead compensator when $f_{s1} = f_{s2} = 30$ kHz. (a) $L_g = 75$ μH. (b) $L_g = 120$ μH. (c) $L_g = 160$ μH. (d) $L_g = 660$ μH.

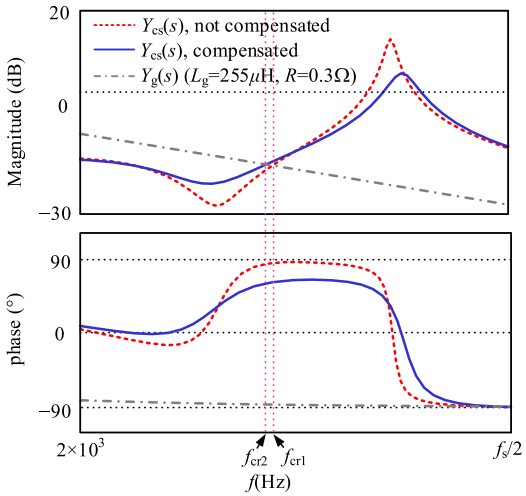

Fig. 21. Bode plots of $Y_{cs}(s)$ and $Y_g(s)$ with and without the phase-lead compensator when $Z_g = (0.3 + j0.08)$ Ω.

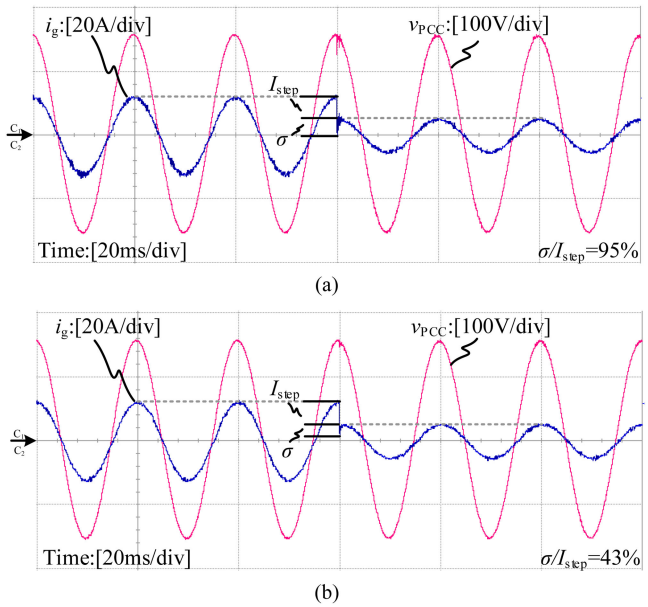

Fig. 22. Dynamic waveforms of the grid-connected inverter system with and without the phase-lead compensator when $Z_g = (0.3+j0.08)$ Ω. (a) Without the compensator. (b) With the compensator.

larger overshoot and longer settling time during the transient. Therefore, the experimental results given in Fig. 22 demonstrates that the proposed solution could effectively increase the stable margin.

VI. Discussion on the Impact of Grid Voltage Feedforward

The grid voltage feedforward is usually employed to make the grid-connected inverter possess harmonic-rejection ability [37]. Here, we take the proportional grid voltage feedforward for example to study its impact. Fig. 23(a) gives the control block diagram of module j with the grid voltage feedforward and Fig. 23(b) is its equivalent version with which we can derive

$$i_{L2j}(s) = i_{csj}(s) - Y'_{csj}(s) \cdot v_{PCC}(s) \tag{49}$$

where

$$Y'_{csj}(s) = Y_{csj}(s) \cdot \left[1 - \frac{1}{K_{PWMj} G_{ij}(s)} \cdot \frac{G_{Mj}(s) Y_{invj}(s)}{Y_{PCCj}(s)}\right] \triangleq Y_{csj}(s) \cdot \Lambda. \tag{50}$$

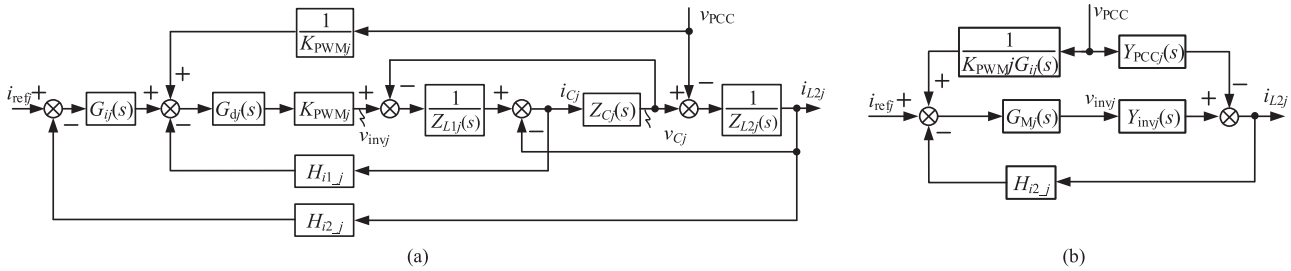

Fig. 23. Control block diagram of inverter j with grid voltage feedforward. (a) Control block diagram for the *LCL*-type grid-connected inverter. (b) Equivalent control block diagram.

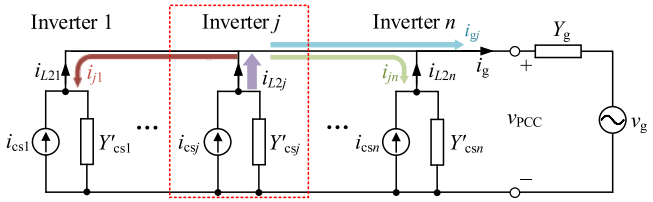

Fig. 24. Norton circuit of multi-inverter grid-connected system in the weak grid with grid voltage feedforward.

Then, we can obtain the Norton equivalent circuit of the multi-inverter system in Fig. 24. Comparing Fig. 24 with Fig. 3, we can find that only the equivalent output admittance of the inverter is changed from $Y_{\mathrm{cs}j}(s)$ to $Y'_{\mathrm{cs}j}(s)$. Likewise, only by replacing $Y_{\mathrm{cs}j}(s)$ with $Y'_{\mathrm{cs}j}(s)$, we can carry on the subsequent formula derivations in the same way as that in Sections II and III. Thus, we can get that the adoption of the grid voltage feedforward would not affect the essential conclusion of the grid-impedance allocation mechanism and the relevant stability criterion. Besides, Λ in (50) will bring about a phase shift during relatively low frequency range to the equivalent output admittance of the inverter, which may degrade the stability in weak grid. Actually, it is a common issue when applying the grid voltage feedforward scheme [37], [38]. Our proposed method focuses on solving the instability issue in the vicinity of $f_s/6$ induced by digital-control delay on the basis of the grid-impedance allocation mechanism. The way to address the instability issue caused by the grid voltage feedforward can refer to [38] and it is also our future work.

VII. Conclusion

This article investigates the stability of multi-inverter grid-connected system in the weak grid. By establishing the MIMO matrix of the multi-inverter system, the self-stability and interactive-stability of the system are discussed. Meanwhile, the interactive current relationship of multimodule system is revealed. Then, on the basis of the grid-impedance allocation mechanism, a stability criterion for a multi-inverter system is obtained. Furthermore, the influence of digital-control delay on the robustness of multi-inverter system in weak grid is explored from the perspective of output admittance. Last, the method of phase-lead compensation combining with the employment of optimal capacitor-current feedback coefficient is applied to improve the robustness of the parallel system against the grid impedance. It is worth noting that the proposed scheme has a good adaptability for general parallel-inverter grid-connected system.

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