Modified VIENNA Rectifier III to Achieve ZVS in All Transitions: Analysis, Design, and Validation

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***Abstract*—In this article, analysis and design of a 3.3-kW isolated single-stage three-phase buck-type rectifier for aircraft applications is presented. The operating principle and modulation method of the proposed rectifier are introduced. The advantageous zero-voltage switching (ZVS) feature in all of the switching transitions is analyzed. A comparison with the VIENNA Rectifier III is done, being different both in the phase-leg implementation and the modulation sequence. A detailed rectifier design guideline is discussed and losses estimations are provided aiming at reaching 93.7% overall efficiency, including the EMI (electromagnetic interference) filter. Simulation waveforms are presented. Finally, experimental results obtained with the designed 3.3-kW hardware demonstrator are provided. The results verify achievement of ZVS in all of the switching transitions from full load down to 50% of nominal load, while exhibiting 1.9% THD_I (total harmonic distortion) and 0.9996 PF (power factor) at nominal power, ultimately showing very good agreement to the simulation results. This article is accompanied by a video demonstrating experimental operation of the proposed rectifier at nominal input voltage, output voltage, and output power.**

***Index Terms*—AC–DC power converters, aircraft application, buck-type rectifier, isolated, power factor, THD, three-phase.**

I. Introduction

IN TRADITIONAL aircrafts, electrical generators are connected to the turbine by a mechanical gearbox. The expensive gearbox system transfers the variable speed of the engine shaft to a constant speed shaft where the three-phase generator is mechanically coupled with the final purpose of producing a three-phase power source with constant mains frequency of 400 Hz and phase voltage of 115 V_{RMS} [1]. The conventional rectifiers employed in nowadays aircraft are relying on the passive solutions. These passive systems consisting of a three-phase diode bridge usually exhibit very poor input current quality, measured by the current total harmonic distortion THD_I, and power factor. The conduction interval can, however, be enlarged if either three inductors are inserted on the ac-side or a single inductor is inserted on the dc-side of the rectifier bridge. This considerably improves the system performance but still the THD_I values above 30% and the power factor below 0.952 characterize the system [2]. The input current quality can be enhanced considerably if two or more phase-shifted rectifier bridges are connected in parallel, which results in passive multi-pulse rectifier systems. In these solutions, transformers are used for phase-shifting and isolation, and such systems are called transformer rectifier units (TRU) [3].

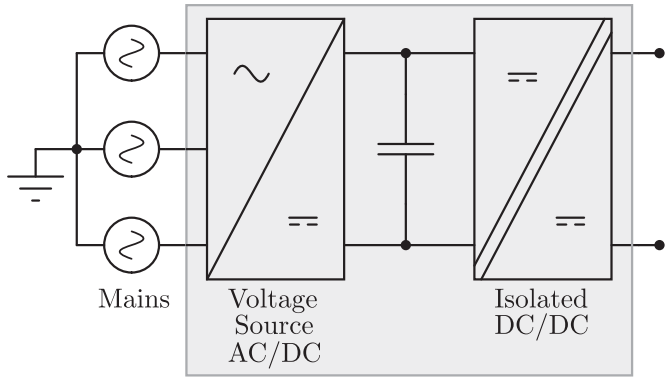

Fig. 1. Block diagram of the two-stage rectifier system with galvanic isolation.

Three-phase ac–dc power supplies with features such as galvanic isolation, low input current THD_I, and high power factor conventionally consist of two cascaded converter stages, as shown in Fig. 1 [4]–[7]. The first ac–dc stage serves as an active-front-end which is in charge of realizing PFC (power factor correction) and low THD_I, meanwhile meeting EMI standards. The second stage is an isolated dc–dc converter which provides tight regulation of the output, and meets the dynamic requirements. In between these two stages, usually there is a dc-link capacitor (or in some cases, a dc-link inductor [8]), which is in general relatively large. Its function is to buffer energy under unbalanced grid condition, thus decoupling the dynamics of the ac–dc and the dc–dc stage. In addition, this allows to

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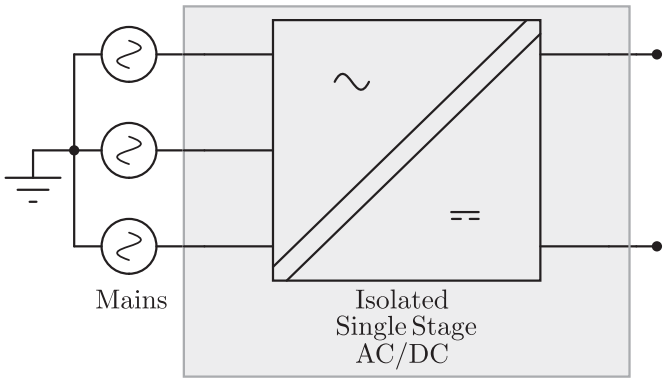


Fig. 2. Block diagram of the single-stage rectifier system with galvanic isolation.

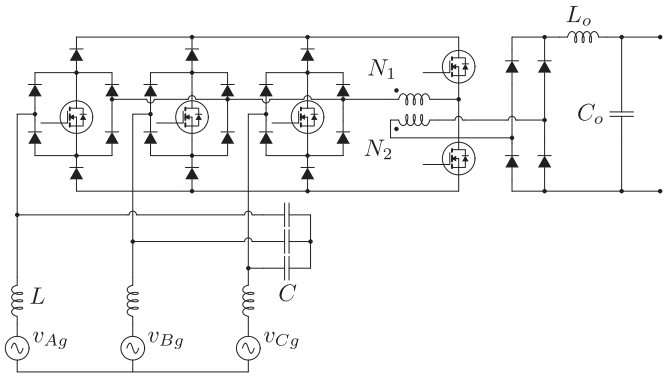


Fig. 3. Circuit topology of VIENNA Rectifier III.

independently design and optimize each of the stages. Moreover, the closed-loop control scheme can be designed for each stage individually.

In applications where the input and output voltage range is wide and energy storage is allowed, the two-stage topologies are of interest due to their flexibility provided by the voltage in the dc-link capacitor [9], [10]. However, this cascaded two-stage solution normally exhibits reduction in overall efficiency, bulky dc-link capacitors, large total component count, and thus increased control complexity. Besides, although zero-voltage switching (ZVS) feature can be realized in certain dc-dc converter topologies, the rectifier topologies seldom implement this feature. Consequently, three-phase rectifier topologies featuring single stage with isolation, aiming at higher efficiency and power density, have emerged since early 90s, depicted as block diagram in Fig. 2 [11]–[16]. In [17], a single-stage ac–dc isolated bidirectional converter is presented with reduced switch count, moderate efficiency, and ability to achieve partial ZVS. Another single-stage buck-type converter with isolation is presented in [18]. There, authors have achieved in six out of eight transitions complete ZVS, while in the other two transitions produce near-zero switching loss. Moreover, the converter is able to achieve high power factor and low THD_I. Recent publication [19] expanded on the work in [18] aiming for ultrahigh efficiency and low THD_I for data center applications. Since very high efficiency was the optimization goal, ZVS feature was optimized along with the use of the third-generation SiC MOSFETs.

The main contribution of this article lies in the modification of the original VIENNA Rectifier III presented in [20] both at the topological level and at the modulation level. Moreover, this article is an expansion of previous published work [21]. As a result of these modifications, ZVS in all MOSFET transitions is achieved, while simultaneously reducing the conduction loss in inactive states. In Section II, the modification process of the original VIENNA Rectifier III is presented, along with a brief comparison of the proposed rectifier with the original one at topological and modulation levels. In Section III, an in-depth analysis of the proposed single-stage rectifier is done. The operating principle and thorough analysis of the modulation for the purpose of achieving ZVS in all transitions is presented. Afterwards, a detailed analysis of all voltage and current stresses of semiconductor devices is carried out in Section IV, along with the dimensioning of passive components as a function of the imposed peak-to-peak ripple criteria. The design is done bearing in mind that the rectifier is used in aircraft applications, and thus avionic standards MIL-STD-704F [22] and DO-160G [23] are addressed. Next, breakdown of all devices power losses is presented, along with the simulation results of the rectifier. An experimental prototype is built, tested, and the results are presented in Section V. Finally, Section VI concludes the article. The measurements obtained on the laboratory demonstrator proved very good agreement with the provided mathematical model, demonstrating low THD_I of the input currents, high input power factor, and compliance with the DO-160G [24] low-frequency current emissions standard.

II. Comparison Between VIENNA Rectifier III and the Modified VIENNA Rectifier III

Under the scope of a single-stage rectifier with galvanic isolation, VIENNA Rectifier III was proposed in [20], [25], [26], and depicted in Fig. 3. This rectifier can shape sinusoidal mains currents in phase with the corresponding phase voltages. Notably, this topology has only five controlled semiconductor devices, which greatly reduce the control complexity. VIENNA Rectifier III is ideally suited for, e.g., realization of welding current sources with low effects on the mains, or for telecom power supply modules with moderately high efficiency and high power density.

During the inactive power transfer state in the VIENNA Rectifier III, no switch on the primary side is in conduction state forcing circulation of the freewheeling current only on the secondary side. As a consequence, there is no primary-side current flow available in this state, making the charging/discharging of MOSFETs output capacitance unviable. As a consequence of this constraint, ZVS feature in the conventional VIENNA III rectifier is not possible.

In recent publication [27], different phase-leg implementations of VIENNA-type rectifier are presented and compared, which lead to different power loss performances. The four phase-leg implementation alternatives for VIENNA-type rectifier from [27] are given in Fig. 4. In the original VIENNA

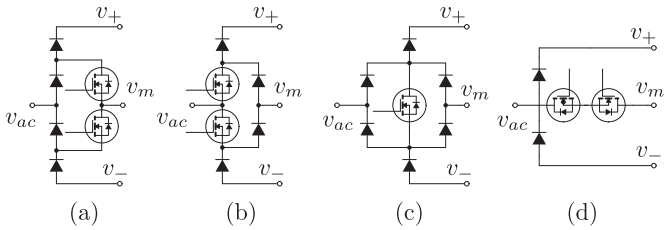


Fig. 4. Alternative phase-leg implementations of VIENNA-type rectifier.

Rectifier III, the implementation of the phase-leg is the one shown in Fig. 4(c). In this article, the phase-leg solution for the proposed modified VIENNA Rectifier III is the one given by Fig. 4(d) due to a significant improvement of overall power devices loss as concluded by [27].

The circuit topology of this modified VIENNA Rectifier III, which is also an isolated single-stage three-phase buck-type rectifier, is shown in Fig. 5. The modification lies in the phase-leg implementation with less conduction losses [from Fig. 4(d)] and addition of one extra leg of MOSFETs $S_{y1} - S_{y2}$. The main benefits of the modified topology are ZVS capability and lower conduction loss, in comparison to the original VIENNA III solution. The following steps describe the improvement process in detail.

i) Since, in [27], it was shown that phase-leg implementation given in Fig. 4(d) shows overall less losses in comparison to (c), which is the case utilized in the original VIENNA Rectifier III, a first variation on the topology can be made while still following the symmetrical modulation method proposed in VIENNA Rectifier III, but utilizing more efficient phase-leg implementation from Fig. 4(d). Based on Fig. 3 in [20], the conduction state sequence and the corresponding current paths inside one switching period of the original VIENNA Rectifier III during mains voltage angle sector 1 (i.e. [0, $\frac{\pi}{6}$]) are depicted in Fig. 6. It can be seen that from state b) to c), ZVS cannnot be achieved, because at this switching transition, two MOSFETs (S_{x2} and S_{yc}) have to be turned OFF at the same time and then the other two (S_{x1} and S_{yb}) have to be turned ON.

ii) In order to facilitate ZVS in all transitions, an asymmetrical modulation method can be implemented by rearranging the operation states shown in Fig. 6. The current paths of different switching states of the proposed asymmetrical modulation sequence are depicted in Fig. 7. After the rearrangement of commutation sequences, not only the freewheeling current is enabled to circulate in the primary side of the rectifier, but also the current direction prior to the X-leg MOSFETs turn-ON is favorable for achieving the ZVS. The ZVS feature greatly improves the switching losses of the rectifier and conducted EMI emissions. Furthermore, only one switch is turned ON or OFF at each switching instant, compared to two turned ON or OFF at the same time in the original VIENNA Rectifier III (see Fig. 9 in [20] S_R, S_S, S_T, S_+, S_- signals).

iii) Continuing with the modifications, an extra Y-leg S_{y1}-S_{y2} can be added between point P and N based on the previous step, which modifies the current paths as depicted in Fig. 8. This finally makes the modified VIENNA Rectifier III. It can be seen

TABLE I
AVAILABLE SWITCHING STATES OF BRIDGE LEG S_x, S_y, RECTIFIER INPUT PHASE CURRENTS $i_{rec,a}$ $i_{rec,b}$ $i_{rec,c}$, RECTIFIER INPUT CURRENT SPACE VECTOR i_r, AND TRANSFORMER PRIMARY VOLTAGE v_{prim} FOR SECTORS 1 AND 2

S_x	S_y	$i_{rec,a}$	$i_{rec,b}$	$i_{rec,c}$	i_r	v_{prim}
1	0	$\frac{N_2}{N_1} I_{out}$	$-\frac{N_2}{N_1} I_{out}$	0	$\frac{2}{\sqrt{3}} \frac{N_2}{N_1} I_{out} e^{-j\frac{\pi}{6}}$	v_{ab}
-1	1	$\frac{N_2}{N_1} I_{out}$	0	$-\frac{N_2}{N_1} I_{out}$	$\frac{2}{\sqrt{3}} \frac{N_2}{N_1} I_{out} e^{j\frac{\pi}{6}}$	$-v_{ac}$
1	-1	$\frac{N_2}{N_1} I_{out}$	0	$-\frac{N_2}{N_1} I_{out}$	$\frac{2}{\sqrt{3}} \frac{N_2}{N_1} I_{out} e^{j\frac{\pi}{6}}$	v_{ac}
-1	0	0	$\frac{N_2}{N_1} I_{out}$	$-\frac{N_2}{N_1} I_{out}$	$\frac{2}{\sqrt{3}} \frac{N_2}{N_1} I_{out} e^{j\frac{\pi}{2}}$	$-v_{bc}$
1	1	0	0	0	0 (Freewheeling)	0
-1	-1	0	0	0	0 (Freewheeling)	0

that by adding this extra leg S_{y1}–S_{y2}, conduction losses can be further reduced in freewheeling states [e.g., in Fig. 8 state (b), current is flowing through S_{y1} instead of bidirectional switches S_{ya} and the diode D_{a+} in Fig. 7 state (b)]. Also, the control complexity is shifted from the switching pair $S_{ya/b/c}$ onto this added leg S_{y1}–S_{y2} [e.g., in in Fig. 8 state (c), connecting phase A voltage to point Y by turning ON only S_{y1} instead of turning ON both switches in S_{ya} as in Fig. 7 state (c)].

As a summary, the difference between the modified VIENNA Rectifier III and the original VIENNA Rectifier III lies both in the phase-leg implementation and the modulation sequence. The comparison is done in the following aspects.

1) *Switching States and Space Vector Modulation (SVM):* The available switching states of the two rectifiers are the same. In Table 1, from [20], the available switching states of the VIENNA Rectifier III are given, together with its input phase currents, input current space vector, and the transformer primary voltage. It can be seen that, in comparison with the proposed rectifier (see Table I), the switching states and formed rectifier current vectors are the same. Explicitly, both rectifiers have four available active switching states, out of which two provide the same current vector but with opposite transformer polarization. The space vector representation of VIENNA Rectifier III can be found in Fig. 4 from [20].
2) *Transformer Volt–Second Balance:* Since both rectifiers can generate the same available current space vectors and the corresponding voltage applied on the transformer is the same under each switching state, the transformer volt–second balance follows the same rule. The only difference is that, as shown in Fig. 10, there are only three active states in the proposed topology, while in VIENNA Rectifier III (see Fig. 9 from [20]), the two active states $+u_{RT}$ and $-u_{RS}$ are divided into a half and placed symmetrically around the active state $-u_{RT}$. The advantage of the asymmetrical sequence for the proposed rectifier is that it facilities the ZVS feature in each switching transition for the merit of its integrated full-bridge structure (stated in Section III-B). On the other hand, the original VIENNA Rectifier III cannot realize ZVS and has one more switching transition than the proposed modification.
3) *Number of Semiconductor Devices:* VIENNA Rectifier III has only five MOSFETs, which shows great simplification

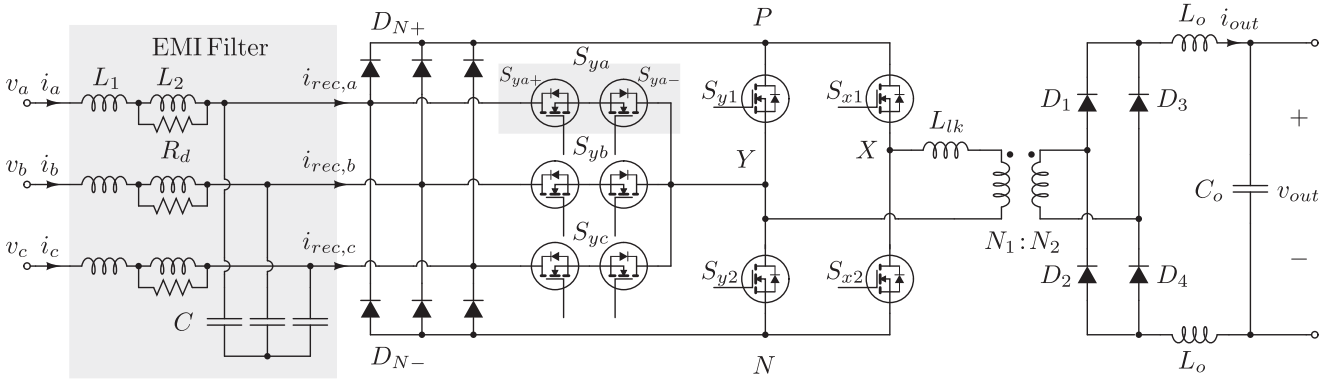


Fig. 5. Topology of the proposed three-phase single-stage isolated buck-type rectifier.

in driving effort, while the proposed rectifier has ten MOSFETs to drive. Nevertheless, from the conduction losses perspective, VIENNA Rectifier III has six semiconductor devices conducting in series on the current path in each active state, while the proposed one has only four. This is further demonstrated in [27], showing that different realizations of phase-leg implementation lead to different power loss performance. The four phase-leg implementation alternatives for VIENNA-type rectifier are given in Fig. 4, where Fig. 4(c) represents the original VIENNA Rectifier III implementation and Fig. 4(d) stands for the proposed rectifier. Moreover, from the losses distribution chart (Fig. 2) provided in [27], Fig. 4(d) clearly shows significant reduction in the diode conduction losses, and slightly lower MOSFET switching losses.

III. Analysis on the Modified VIENNA Rectifier III Topology

In this section, proposed single-stage rectifier topology is introduced with its operating principle analyzed. Next, modulation method for the proposed rectifier and its representation by means of space vectors are discussed. One of the main advantageous features of the proposed rectifier is its ZVS capability, due to its unique bridge-leg structure together with the proposed asymmetrical modulation method. The detailed analysis of ZVS feature is also developed.

A. Operating Principle and Proposed Modulation Method

The proposed circuit topology of this isolated single-stage three-phase buck-type rectifier is presented in Fig. 5. The concept of this circuit combines the demand for PWM sinusoidal input currents with a high-frequency transformer for single-stage isolation purpose. Since the circuit is a buck-derived topology, discontinuous PWM currents are present at the input of the rectifier (i.e. $i_{rec,a}$, $i_{rec,b}$, and $i_{rec,c}$ in Fig. 5). Hence, an EMI filter is necessary to filter out the high-frequency current components. This yields a purely sinusoidal-shaped, line-frequency component that is drawn in phase with the three-phase voltage source. It should be noted that the capacitors C of the EMI filter are not only essential for reaching a certain EMI attenuation, but also fundamental to the rectifier functionality, since they have to be placed very close to the switching stage, in order to provide high-frequency discontinuous currents with minimum inductance paths.

The diode bridges $D_{N\pm}$ are not conventional high-frequency devices since they only conduct PWM current for the 120°-wide interval, where its phase voltage is at the maximum (for D_{N+}, $N \in \{a, b, c\}$) or the minimum (for D_{N-}). To demonstrate the operating principle of the proposed rectifier, the mains three-phase voltages are divided into 12 sectors as shown in Fig. 9. By the functionality of $D_{N\pm}$, upper rail point P always presents the highest voltage among the three phases, while the lowest voltage is always present at lower rail point N. Correspondingly, the voltage v_{PN} exhibits a six-fold waveform in one line cycle, marked with black solid curve in Fig. 9.

Next, in Fig. 5, if MOSFETs S_{x1}, S_{x2}, S_{y1}, and S_{y2} perform conventional phase-shifted full-bridge logic with v_{PN} supplied on the bridge legs, only the highest and the lowest phase will have path to demand current from the source. However, the phase in the middle will have no path to conduct current, which yields failure of complying with the ohmic behavior requirement for each phase. In order to overcome this drawback, a bidirectional switching path is introduced by switching pairs S_{ya}, S_{yb}, and S_{yc}. In Fig. 5, the left switch inside the switching pair is denoted as S_{yN+}, and the right one as S_{yN-}. Consequently, the functionality of the bidirectional switches S_{ya}, S_{yb}, and S_{yc} has to be integrated into the functionality of the full-bridge switches, noting that the below listed two requirements have to be accomplished at the same time:

1) transformer volt–second balance; and
2) ohmic behavior for each phase.

To demonstrate the operating principle of the proposed rectifier, sector 1 in Fig. 9 (where $v_a > 0 > v_b > v_c$) is used as an illustration. The main operating waveforms inside one switching cycle are depicted in Fig. 10, where $v_{\rm prim}$ depicts the voltage applied across the primary of the transformer. In each switching cycle, there are five operation states: three active states (marked as time intervals t_1, t_2, and t_3) and two freewheeling states (each with time interval of $t_4/2$). States 1, 3, and 5 are active states where each phase current, averaged over one switching period, is proportional to its corresponding phase voltage, shown as $i_{rec,a}$, $i_{rec,b}$, and $i_{rec,c}$ in Fig. 10. Moreover, the driven

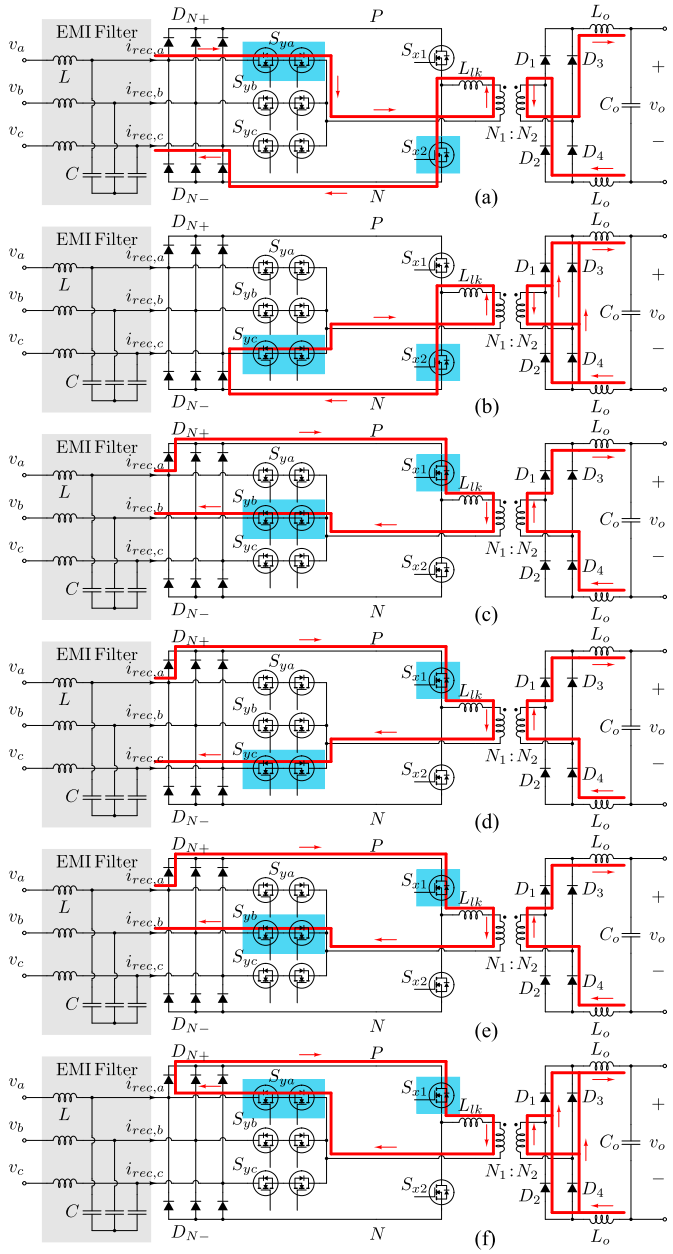


Fig. 6. Conduction state sequence and the corresponding current paths inside one switching period of VIENNA Rectifier III with improved phase-leg implementation, working under its original symmetrical modulation sequence.

signals for the switches S_{x1}, S_{x2}, S_{y1}, S_{y2}, and the bidirectional switch S_{yb} are presented. Driven signals for S_{ya} and S_{yc} are not shown in this example because they are not active in sector 1.

Furthermore, for explicit illustration, the current paths for the abovementioned five operation states are depicted in Fig. 8(a)–(e), respectively.

The modulation method is the essence of the performance for the proposed rectifier topology. Following the operating principle shown in Fig. 10, the key is to calculate the timing of each state, which accordingly defines the duty cycle and switching sequence of all the MOSFETs.

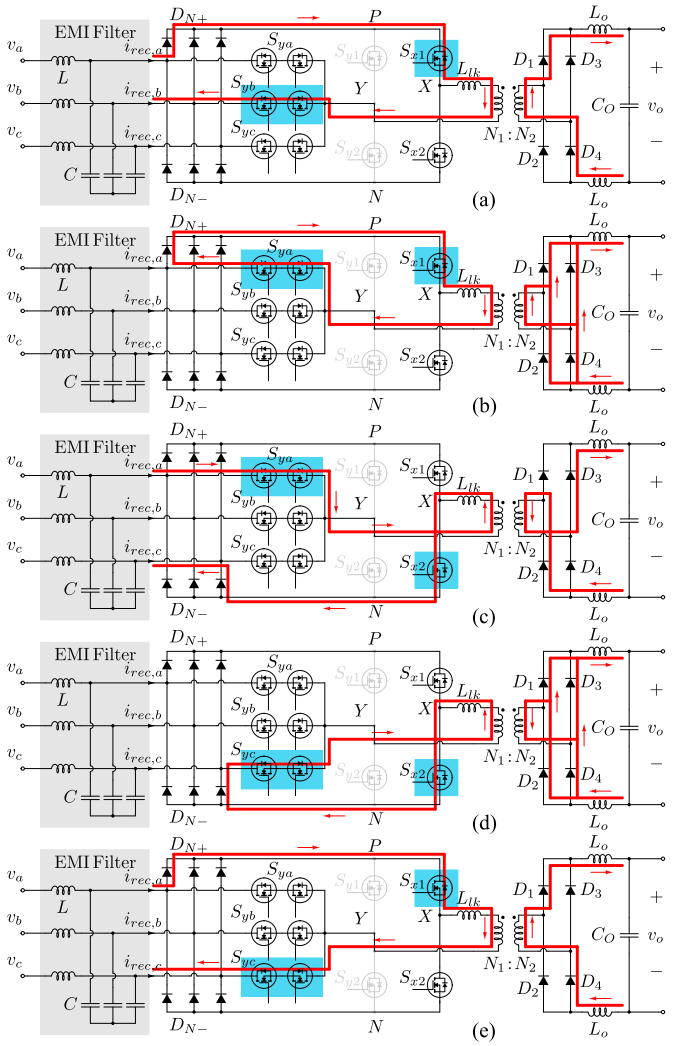


Fig. 7. Conduction state sequence and the corresponding current paths inside one switching period of VIENNA Rectifier III with improved phase-leg implementation, working under the proposed asymmetrical modulation sequence.

Since this topology is also a buck-type rectifier topology, the definition of modulation index M in [28] is still valid for this converter. Thus, there is

$$M = \frac{2}{3}\frac{N_1}{N_2}\frac{V_{\text{out}}}{\hat{V}_N} \tag{1}$$

where V_{out} represents the dc output voltage and $\hat{V}_N$ represents amplitude of the input phase voltages.

First, to ensure the transformer volt–second balance, the magnetizing flux increment and decrement have to be equalized over one switching period. For the case of sector 1, this is mathematically described as

$$(v_a - v_b)t_1 + (v_a - v_c)t_3 = (v_a - v_c)t_2 \tag{2}$$

which yields

$$t_2 - t_3 = \frac{v_a - v_b}{v_a - v_c}t_1. \tag{3}$$

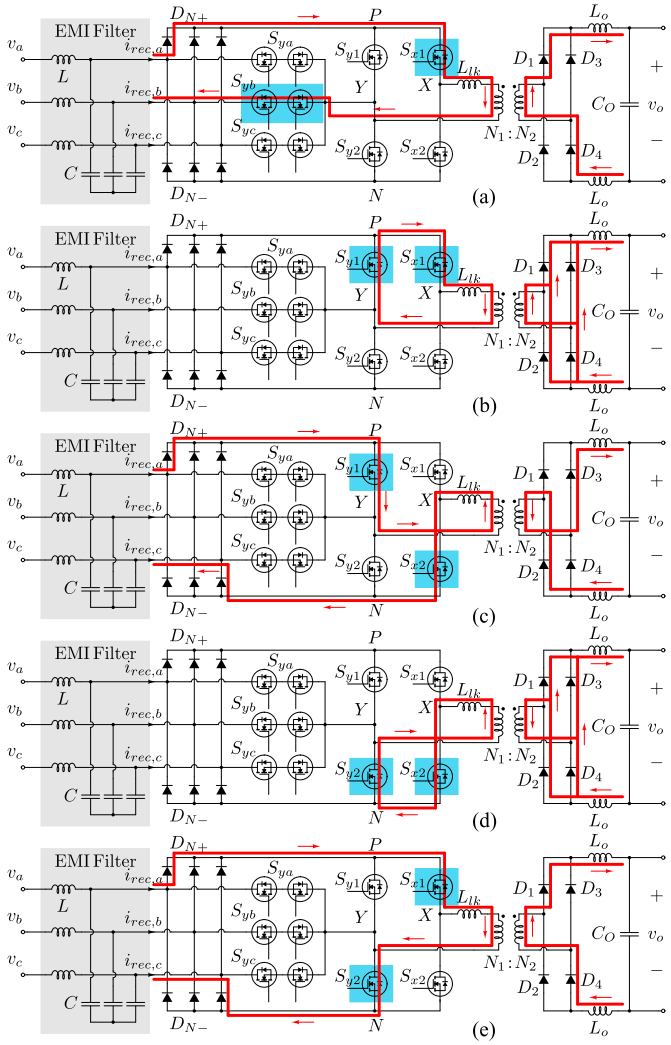


Fig. 8. Conduction state sequence and the corresponding current paths inside one switching period of the final proposed Modified VIENNA Rectifier III.

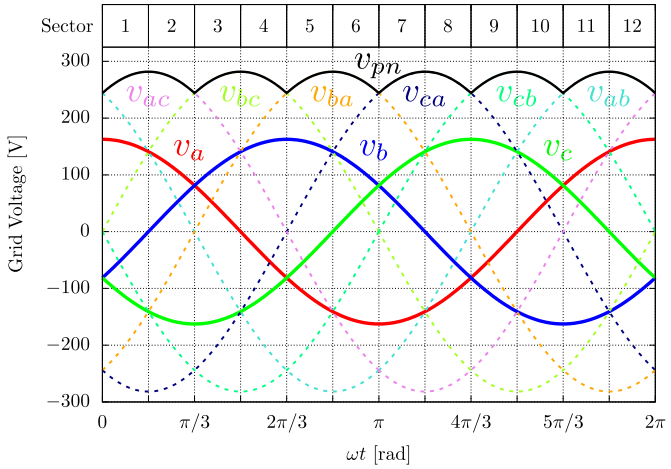


Fig. 9. Sectors 1–12 of the mains phase voltage.

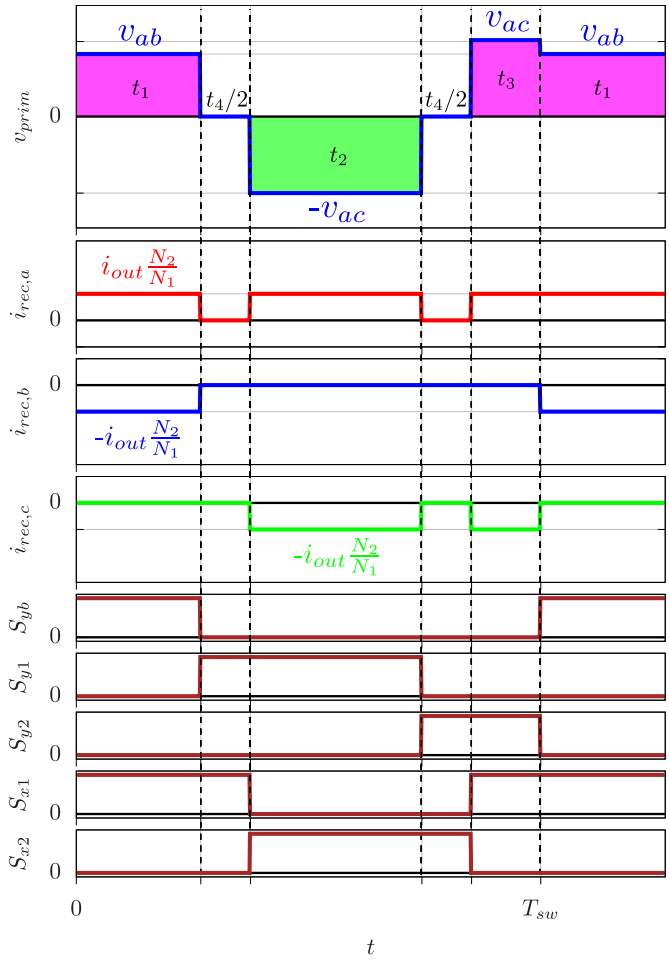


Fig. 10. Operating principle (shown in sector 1) of the proposed rectifier topology.

Moreover, for the lowest phase C in this sector 1, according to the desired purely resistive per-phase behavior, there is

$$t_2 + t_3 = \frac{M}{\hat{V}_N} |v_c| \, T_{\mathrm{sw}}. \tag{4}$$

Also, for the phase in the middle, which is phase B in sector 1, the ohmic requirement translates into

$$t_1 = \frac{M}{\hat{V}_N} |v_b| \, T_{\mathrm{sw}}. \tag{5}$$

Combining (3) and (4), the following active states turn ON times are obtained:

$$t_2 = \frac{1}{2}\left(\frac{M}{\hat{V}_N}|v_c| + \frac{v_a - v_b}{v_a - v_c}\frac{M}{\hat{V}_N}|v_b|\right) T_{\mathrm{sw}} \tag{6}$$

$$t_3 = \frac{1}{2}\left(\frac{M}{\hat{V}_N}|v_c| - \frac{v_a - v_b}{v_a - v_c}\frac{M}{\hat{V}_N}|v_b|\right) T_{\mathrm{sw}}. \tag{7}$$

Finally, the total freewheeling time is calculated as

$$t_4 = T_{\mathrm{sw}} - t_1 - t_2 - t_3 \tag{8}$$

where this state is split into two halves and each $t_4/2$ is placed according to Fig. 10. Thus, duty cycles for all the switches in

sector 1 can finally be obtained as

$$d_{S_{yb}} = t_1/T_{\text{sw}} \tag{9}$$

$$d_{S_{y1}} = \left(t_2 + \frac{1}{2}t_4\right)/T_{\text{sw}} \tag{10}$$

$$d_{S_{y2}} = \left(t_3 + \frac{1}{2}t_4\right)/T_{\text{sw}} \tag{11}$$

$$d_{S_{x1}} = \left(t_1 + t_3 + \frac{1}{2}t_4\right)/T_{\text{sw}} \tag{12}$$

and

$$d_{S_{x2}} = \left(t_2 + \frac{1}{2}t_4\right)/T_{\text{sw}}. \tag{13}$$

The abovementioned modulation method can also be represented in a form of space vectors, modulating the current vector by the composition of different switching states. The three-phase sinusoidal mains voltage can be represented as

$$v_a = \hat{V}_N \cos\theta \tag{14}$$

$$v_b = \hat{V}_N \cos\left(\theta - \frac{2\pi}{3}\right) \tag{15}$$

$$v_c = \hat{V}_N \cos\left(\theta + \frac{2\pi}{3}\right) \tag{16}$$

where $\theta = \omega t$. According to the definition, the rectifier input voltage space vector can be represented as

$$\underline{v}_r = \frac{2}{3}\left(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{-j\frac{2\pi}{3}}\right). \tag{17}$$

Similarly, the rectifier input current space vector can be described as

$$\underline{i}_r = \frac{2}{3}\left(i_{rec,a} + i_{rec,b} e^{j\frac{2\pi}{3}} + i_{rec,c} e^{-j\frac{2\pi}{3}}\right). \tag{18}$$

In order to avoid the short-circuit of input line-to-line voltages, the following conditions must not be violated.

- Out of bridge-leg S_{y1}, S_{y2}, and S_{yn}, only one switch can be turned ON in every instant.
- S_{x1} and S_{x2} cannot be turned ON at the same time.

Noting that the bidirectional switch S_{yn} represents the one in the phase that has line-to-neutral voltage in the middle of all three, which corresponds to switch S_{yb} for sector 1.

Following the abovementioned rule, we name variable S_y to represent the states of bridge-leg S_{y1}, S_{yn}, and S_{y2}. When S_y is in state "1," it means S_{y1} is ON; "0" means that S_{yN} is in conduction state; "-1" corresponds to S_{y2} carrying current. Similarly, variable S_x is defined as "1" representing S_{x1} being turned ON and "-1" meaning that S_{x2} is closed. All available switching states for the sectors 1 and 2 are summarized in Table I. Moreover, the table presents the per-state corresponding current value in each phase, as well as the rectifier current space vector and voltage applied on the transformer primary side.

With the abovementioned available vectors of switching states, the desired rectifier current vector reference in sector 1 can be formed with the sequence illustrated earlier in Fig. 10. In Fig. 11, this vector synthesis forming a rectifier current vector

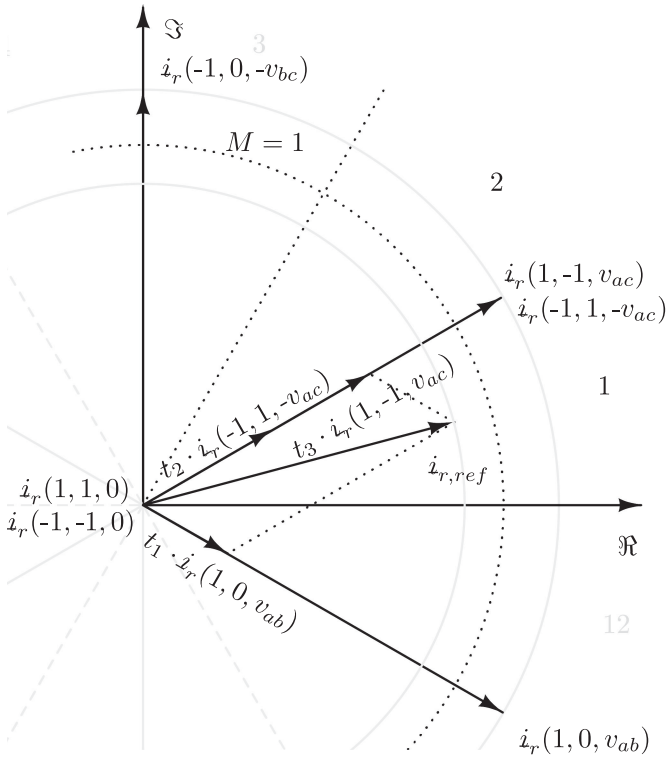


Fig. 11. Space vectors of $\underline{i}_r$ corresponding to the switching states listed in Table I for sectors 1 and 2, including an example of the composed rectifier input current space vector $\underline{i}_{r,ref}$ while in sector 1.

$\underline{i}_{r,ref}$ in sector 1 with the three most nearby current vectors is shown. It can be observed that, even though vectors $(1, -1, v_{ac})$ and $(-1, 1, -v_{ac})$ show the same vector in space, they play opposite roles in balancing the transformer volt–second according to (2).

B. Zero-Voltage Switching (ZVS) Feature

By the merit of the full-bridge architecture, the presence of leakage inductance in the transformer enables ZVS for each switching transition eliminating the turn-ON loss above certain load level [29]. However, in this proposed topology, the functionality of bidirectional path is integrated into the full-bridge operation inside every switching period, thus all the bidirectional switching pairs (S_{ya}, S_{yb}, and S_{yc}) can also realize ZVS.

Similar to a conventional phase-shifted full-bridge, for the leading leg switches S_{y1}, S_{y2}, and S_{yN} at the moment before each turn-ON, the rectifier is always in an active state, where the energy used to charge or discharge the output capacitance of the switches is the energy stored in the leakage inductance L_{lk} plus the energy stored in the output filter inductor L_o. Since the energy in L_o is several orders of magnitude larger in comparison to the energy needed to charge the output capacitance, it can be considered as a constant current source charging the MOSFET C_{oss}. The charging current $I_{p,\max}$ corresponds to the peak value of output inductor current ripple reflected to the primary as

$$I_{p,\max} = \frac{N_2}{N_1} I_{\text{out},\max}. \tag{19}$$

Critical moment to achieve ZVS regarding MOSFET v_{DS} is the moment when the maximum line-to-line voltage reaches its peak:

$$v_{DS,\max} = \sqrt{3}\,\hat{v}_N. \tag{20}$$

For more accurate analysis, the nonlinear behavior of MOSFET C_{oss} must be considered. The total number of C_{oss} capacitances that have to be charged/discharged is equal to five, thus the minimum dead-time applied on leading leg switches $t_{\delta 1}$ can be obtained by (assuming identical MOSFETs):

$$Q_{oss,t,y} = 5\int_0^{v_{DS,\max}} C_{\text{oss}}(v_{DS})\,\mathrm{d}v_{DS} = I_{p,\max} t_{\delta 1}. \tag{21}$$

The left part can be easily achieved by integrating the area below the provided $C_{\text{oss}} - v_{DS}$ curve in MOSFET device datasheet. On the other hand, the turn-ON of the lagging leg switches S_{x1} and S_{x2} happens after a freewheeling state, which means that only the energy stored in the L_{lk} is available for charging or discharging MOSFET capacitance C_{oss}. Then, the energy stored in L_{lk} has to comply

$$\frac{1}{2} L_{lk} I_{p2}^2 > 2\int_0^{v_{DS,\max}} v_{DS} C_{\text{oss}}(v_{DS})\,\mathrm{d}v_{DS} \tag{22}$$

where I_{p2} is the primary current at turn-ON moment of the lagging leg switch given by

$$I_{p2} = \frac{N_2}{N_1}\left(I_{\text{out,max}} - \frac{v_{\text{out}}}{L_o}\frac{t_4}{2}\right). \tag{23}$$

Consequently, the resonance between L_{lk} and C_{oss} provides a near-sinusoidal voltage rise across the switch to be turned ON. The dead-time for the lagging leg switches $t_{\delta 2}$ should be at one-fourth of the resonant period [29]

$$t_{\delta 2} = \frac{T_{res}}{4} = \frac{\pi}{2}\sqrt{L_{lk} C_{\text{oss}}}. \tag{24}$$

However, in practice, the dead-time needs to be adjusted experimentally [30] due to a wide variation of the parasitics in the prototype, and the approximation given by (21) and (24) gives only a fairly good initial estimation.

The simulation result using PLECS [31], showing this ZVS behavior of one switching period in sector 1, is captured in Fig. 12. Proper dead-time has been applied among the driven signals S_{y1}, S_{y2}, S_{x1}, S_{x2}, S_{yb+}, and S_{yb-}. All of the marked five switching instants (ZVS instant 1–5) can realize zero-voltage turn-ON.

For the ZVS 1 time instant, the bidirectional pair is achieving zero-loss turn-ON. It is necessary to turn ON the switch that is not blocking voltage at the same time (or even few tens of ns earlier) as the turn-OFF of the corresponding Y-leg switch. For the case of sector 1, the S_{yb-} must be turned ON when S_{y2} is switched OFF. That allows for the discharge of the S_{yb+} output capacitance, enabling its lossless turn-ON.

Apart from having only the leakage inductance stored energy for ZVS in the transitions 3 and 5, it is necessary to place a small snubbing capacitor between nodes P and N. The reason lies in the fact that there is no closed path for the L_{lk} current flow to the ac capacitors immediately after S_{x1} or S_{x2} turn-OFF due to rectifier diodes $D_{N\pm}$, as it can be observed in Fig. 8 for b)→c) and d)→e)

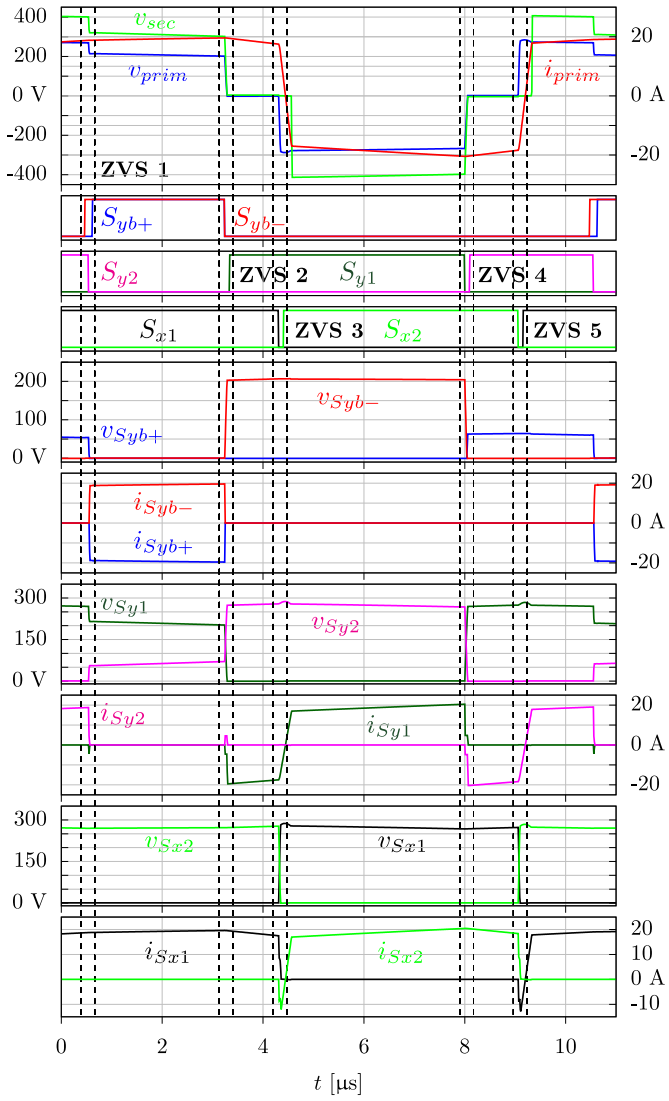


Fig. 12. ZVS details of one switching period $T_{\text{sw}} = 10\,\mu$s in sector 1.

transitions. In order to minimize the overvoltage absorbed by the snubbing capacitor C_{snb}, its value should be chosen so that it stores five to ten times the the energy stored in the L_{lk} as

$$C_{snb} = 5\ldots 10\,\frac{L_{lk}\,I_{p2}^2}{3\,\hat{v}_N^2} \tag{25}$$

assuming the worst case capacitor voltage given by (20). Finally, the ZVS transitions 2 and 4 perform the lossless turn-ON feature similar to the classical phase-shifted full-bridge with the difference that total of five MOSFET output capacitances are charged/discharged as opposed to only two in the conventional dc/dc converter.

IV. Rectifier Design

In this section, analytical expressions of voltage and/or current stresses are provided as a function of the rectifier operating point. This forms a basis for the correct component dimensioning and possible multivariable optimization of the converter.

TABLE II
DESIGN SPECIFICATIONS AND REQUIREMENTS FOR THE HARDWARE DEMONSTRATOR OF THE PROPOSED ISOLATED SINGLE-STAGE THREE-PHASE RECTIFIER

Parameter	Value
Galvanic Isolation	Yes
Input three-phase voltage	115 V_{RMS} nominal (108-118 V_{RMS})
Mains frequency	400 Hz nominal (393-407 Hz)
Power Factor	>0.85 (50% load-nominal load)
THD_I	$\leq 5\%$
Low-frequency harmonics	DO-160G section 16.7.1.2.1
Switching frequency	100 kHz
Output voltage	270 V nominal
Output power rated	3.3 kW
Semiconductor voltage derating	65%
Electrolytic capacitors	Not allowed
Temperature derating	70%

The application of the proposed rectifier topology is rooted in avionic utilities, making military standard MIL-STD-704F [22], as well as DO-160 G section 16 low-frequency current emissions [23] required to be complied. A summary of the key design requirements is shown in Table II.

A. *Transformer Design*

The transformer is one of the most important components in the proposed topology. Besides providing galvanic isolation, the modulation of the rectifier is tightly coupled to the presence of the transformer, as discussed in Section III-A. Moreover, the desired ZVS feature is heavily dependent on the correct value of the transformer leakage inductance L_{lk}, meaning that it has to be determined and taken into account in the design of the transformer.

The waveforms of the transformer primary voltage v_{prim} and primary current i_{prim} inside one switching cycle of sector 1 are shown in Fig. 12. Even though in active state t_1, voltage stress on transformer is smaller compared with active states t_2 and t_3, the maximum flux density $\hat{B}$ is achieved when the primary voltage reaches peak value of the maximum line-to-line voltage, i.e., $\theta = \frac{n\pi}{6}$ $(n = 1, 3, 5, \ldots)$. This can be seen in Fig. 15 that is mentioned in Section IV-G. Moreover, at these time instants, the active state interval t_1 (see Fig. 10) equals to zero since the average current demanded by the phase in the middle is 0. Therefore, active state intervals t_2 and t_3 (also see Fig. 10) are being equal. At these moments, the rectifier operates like a classical phase-shifted full-bridge dc–dc [29] which gives the maximum flux density

$$\hat{B} = \frac{\sqrt{3}\hat{V}_N T_{\text{sw}}/2}{N_1 A_{\text{core}}} \tag{26}$$

where A_{core} represents the cross-sectional area of the chosen core. Based on (1), the turns ratio of the transformer can be represented as

$$N_1/N_2 = \frac{3}{2} M \frac{\hat{V}_N}{v_{\text{out}}}. \tag{27}$$

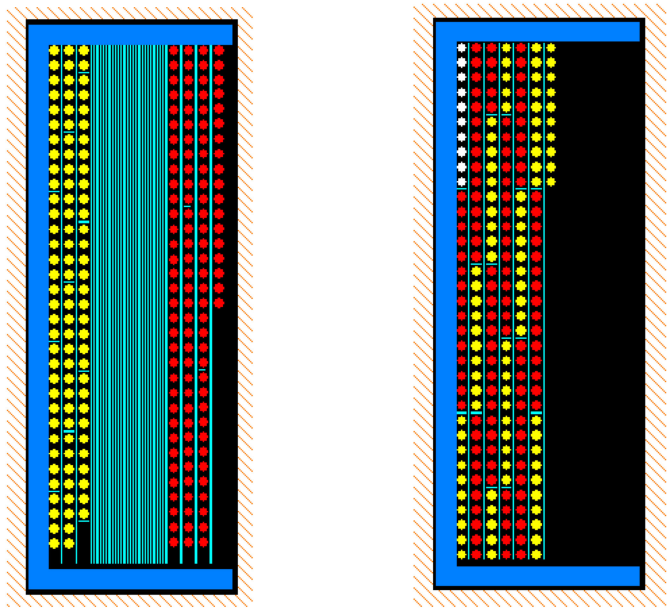


Fig. 13. PEmag winding strategy design of the transformer with EPCOS PM87 N27 core. (a) Separation between primary and secondary windings to achieve desired leakage inductance. (b) Good interleaving between primary and secondary windings.

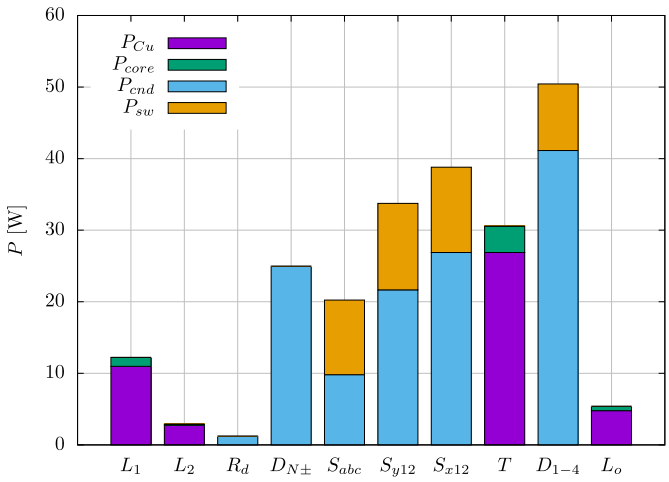


Fig. 14. Distribution of losses estimation for the prototype design at $P_{o,nom} = 3.3$ kW.

Usually, the nominal modulation index for nominal output power is set no greater than 0.9 to leave enough margin under transients [28]. Moreover, the duty cycle loss inherent for the phase-shifted full-bridge topology has to be taken into consideration from applied duty cycle on the primary to the effective duty cycle on the secondary [29]. Finally, the turns ratio is fixed at $N_1 : N_2 = 1 : 1.5$, with the modulation index for nominal condition $M_{\text{nom}} = 0.8$.

Next, ZVS sufficient leakage inductance L_{lk}, as discussed in Section III-B, can be achieved by adding layers of insulator (e.g., kapton tape) between the primary and the secondary windings. However, this worsens the coupling between the primary and the

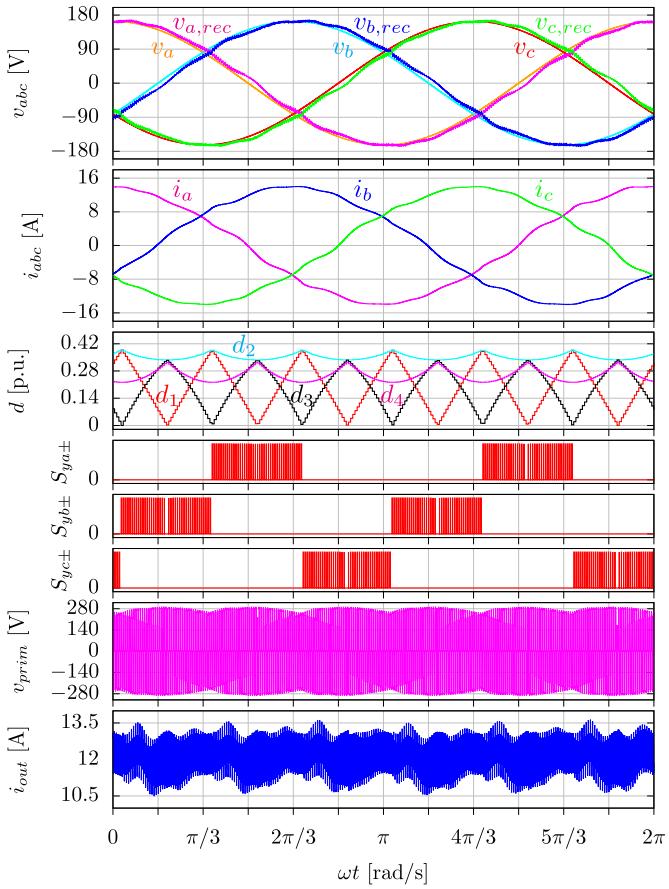


Fig. 15. Simulation result of the rectifier with EMI filter under nominal input and nominal load, showing main waveforms.

secondary, thus compromising the winding ac losses. Alternatively, a transformer with good interleaving between the primary and the secondary that reduces the winding ac loss combined with an external small series inductor could be a viable option. This external inductor in series with the transformer has to be designed apart and presents a high ac flux and a high ac rms (root mean square) current that would penalize the total losses considerably.

A comparison of two different winding strategies is presented below, to elaborate the effect on leakage inductance and ac winding resistance. The focus here is only in the transformer itself, that is to say, the external inductor for good interleaving case is not discussed. A design with separation of primary and secondary to achieve leakage inductance is compared with good interleaving between primary and secondary. The winding strategies are both designed in PEmag/Maxwell 2D finite element analysis software package from Ansys [32] to calculate the leakage inductance and ac winding resistance in all cases. For both winding positioning strategies, the primary winding consists of 10 turns with solid wire of AWG 19 (ϕ0.91 mm), 10 in parallel; and the secondary composes 15 turns with solid wire of AWG 19 also, 8 in parallel. Fig. 13(a) presents the separated winding strategy, where yellow color stands for primary winding and red for the secondary. The blue color represents insulator layer of 6.5 mm horizontal width. On the other hand, Fig. 13(b)

TABLE III
COMPARISON OF THE RESULTS OBTAINED FROM 2D FEA MODELING OF THE TWO DIFFERENT WINDING STRATEGIES IN PEMAG

	Separated windings (Fig. 13a)	**Interleaved windings** (Fig. 13b)
L_{lk} @ 100 kHz	3.6 μH	280 nH
R_{AC} @ 100 kHz	132 mΩ	40 mΩ

TABLE IV
LOSSES ESTIMATION OF THE FINISHED TRANSFORMER

Core losses	3.7 W
AC winding losses	26.9 W
Total	30.6 W

exhibits the winding strategy of good interleaving. After running 2D modeling, the obtained results regarding leakage inductance and ac winding resistance, both reflected on primary side, are concluded in Table III.

It can be seen from Table III that, by separating the primary and the secondary windings, the desired leakage inductance can be easily integrated into the transformer at the cost of a worsening ac winding resistance (132 mΩ vs. 40 mΩ). Meanwhile, dc resistance for both winding strategies are similar, since the number of turns and paralleled windings are exactly the same in both cases.

Thus, the selected option to construct the transformer for the proposed rectifier is to integrate the series inductance in the transformer since the required leakage inductance is small (around 3 μH) having a sensible impact on the transformer performance.

Since this is a high-frequency transformer in which the current through windings exhibits dominantly switching-frequency harmonic content, Litz wire is preferred instead of a solid wire for the sake of minimizing the winding losses from the skin effect and the proximity effect. The constructed transformer winding strategy is thus similar to Fig. 13(a), having a 6.5-mm isolation distance between the primary and the secondary windings. The primary winding consists of 10 turns of Litz wire (200 strands $\times$ ϕ 0.07 mm), 10 in parallel. Afterwards, a 6.5-mm thick layer of kapton isolation tape is wrapped to fix the primary winding in position and also provide separation from secondary. The secondary winding consists of 15 turns of Litz wire (200 strands $\times$ ϕ 0.07 mm), 4 in parallel. It is worth noticing that there is no air gap needed, since the transformer provides direct energy transfer in active states and no energy transfer in freewheeling states.

The final estimated total losses in the transformer based on the FEM analysis consists of the core loss and the winding loss. Since the employed wire type in the actual prototype is Litz wire instead of a solid wire, the winding loss is estimated to have an ac resistance half-way between the two extremes provided in the Table III. This estimation is done due to the fact that currently Litz wire is difficult to model in FEM software analysis tools. The core loss value is taken directly from the FEM software, and the loss breakdown is presented in Table IV. The total winding loss is assumed to be concentrated at 100 kHz with transformer RMS current seen at the primary as

$$I_{prim,RMS} = \frac{N_2}{N_1} I_{\text{out}}. \tag{28}$$

B. Semicondutor Device Selection

The transistors in this topology can be classified into two groups: those switching at high frequency (i.e., switching frequency), and those switching at an equivalently intermediate frequency between mains frequency and switching frequency. The full-bridge switches (S_{y1}, S_{y2}, S_{x1}, and S_{x2}) are always switching at switching frequency, while the bidirectional switching pairs (S_{ya}, S_{yb}, and S_{yc}) are only switching during the sectors where its corresponding phase voltage has the minimum absolute value.

1) MOSFETs S_{y1}, S_{y2}, S_{x1}, and S_{x2}: The voltage stress on the full-bridge switches has an envelope of maximal line-to-line voltage, which gives peak voltage stress as

$$\hat{v}_{S_{y1/y2/x1/x2}} = \sqrt{3}\hat{V}_N. \tag{29}$$

Regarding the current stress, the behavior of the two legs (leg S_{y1}–S_{y2}, leg S_{x1}–S_{x2}) is not exactly the same. The lagging leg switches S_{x1} and S_{x2} are always conducting current in a complementary manner inside each switching cycle, while S_{y1} and S_{y2} are not. The leading leg switches S_{y1}, S_{y2} together with one of the bidirectional switching pairs S_{yN} are conducting current alternatively inside every switching cycle. Moreover, this current stress on the semiconductors depends on modulation index M, output inductor current I_{out}, and the turns-ratio of the transformer N_2/N_1.

The rms current through the switches S_{y1} and S_{y2} is given by

$$I_{S_{y1/y2},RMS} = \sqrt{\frac{1}{2} - \frac{3}{\pi}\left(1 - \frac{\sqrt{3}}{2}\right) M} \frac{N_2}{N_1} I_{\text{out}}. \tag{30}$$

Since S_{x1} and S_{x2} are alternatively sharing the current $N_2/N_1 I_{\text{out}}$ inside every switching cycle and their on-time is symmetrical during every 30°-sector, the rms currents of S_{x1} and S_{x2} is given by

$$I_{S_{x1/x2},RMS} = \frac{\sqrt{2}}{2} \frac{N_2}{N_1} I_{\text{out}}. \tag{31}$$

2) MOSFETs S_{ya}, S_{yb}, and S_{yc}: The highest voltage stress on the bidirectional switching pairs occurs at the moment when one phase voltage reaches its maximum amplitude and the other two are equal to negative half of the maximum amplitude, resulting in

$$\hat{v}_{SyN} = \sqrt{3}\,\hat{V}_N. \tag{32}$$

Regarding the current stress, as discussed in Section IV-B1, S_{yN}, S_{y1}, and S_{y2} are conducting current alternatively inside every switching cycle. The rms current through the bidirectional switching pairs over one mains period is derived as

$$I_{S_{yN},RMS} = \sqrt{\frac{(2-\sqrt{3})M}{\pi}} \frac{N_2}{N_1} I_{\text{out}}. \tag{33}$$

3) Input Diode Bridge $D_{N\pm}$: The three-phase diode bridges D_{N+} and D_{N-} are in principle low-frequency devices, since they conduct at 120-degree line frequency interval. They are experiencing high $\mathrm{d}i/\mathrm{d}t$ transients when corresponding y-branch MOSFET switches; however, they do not block reverse voltage after moving from an ON state to an OFF state, but rather remain forward biased with zero current. Therefore, the devices are required to be fast recovery diodes, while exhibiting no reverse recovery loss mechanism. The voltage stress on the three-phase diode rectifier is equal to the maximal line-to-line input voltage, which leads to the highest voltage stress

$$\hat{V}_{D_{N\pm}} = \sqrt{3}\,\hat{V}_N. \tag{34}$$

Regarding the current stress, the average and rms currents through the three-phase diode bridge diodes are respectively given by

$$I_{D_{N\pm},\text{avg}} = \frac{\sqrt{3}M}{2\pi} \frac{N_2}{N_1} I_{\text{out}} \tag{35}$$

$$I_{D_{N\pm},RMS} = \sqrt{\frac{\sqrt{3}M}{2\pi}} \frac{N_2}{N_1} I_{\text{out}}. \tag{36}$$

4) Output Diodes D_{1-4}: The output diode rectifier is operating at switching frequency, and its voltage stress corresponds to the voltage stress in the low-frequency input diodes multiplied by the turns-ratio of the transformer as

$$\hat{v}_{D_{1-4}} = \frac{N_2}{N_1}\sqrt{3}\,\hat{V}_N. \tag{37}$$

However, in reality, some voltage ringing on the output diode rectifier will be observed due to the interaction of the leakage inductance of the transformer with the parasitic capacitance of the diodes in the output rectifier. This will cause the blocking voltage of the diodes to be higher than the predicted ideal level. Therefore, a certain voltage margin has to be provided in addition to the theoretically predicted voltage level while choosing the devices.

The rectifier diode chosen in this design is CREE 1200 V/43 A C4D30120D SiC Schottky diode. This 1200-V voltage rating is adequate for the ringing case without a snubber. Nevertheless, a passive snubber is also included in order to minimize the ringing in the secondary diode bridge. Finally, the use of SiC diodes removes large portion of the switching losses in the output bridge due to the lack of the reverse recovery mechanism.

The average and rms current stresses of the output diode rectifier are given by

$$I_{D_{1-4},\text{avg}} = \frac{1}{2} I_{\text{out}} \tag{38}$$

$$I_{D_{1-4},RMS} = \frac{\sqrt{2}}{2} I_{\text{out}}. \tag{39}$$

C. Output Inductor L_o Design

Since the proposed topology is derived from the buck-type rectifier, which is also known as the current-source rectifier, an output dc inductor is necessary to suppress and maintain the dc output current. Moreover, this output inductor current also

defines the dc level of the pulsating current that each phase is drawing from the EMI capacitors, denoted by $i_{rec,a/b/c}$ in Fig. 5.

Output filter L_o can be designed based on dc inductor current ripple. The inductor current waveform at nominal load can be seen from Fig. 15 that is presented in Section IV-G. Assuming that the output voltage v_{out} ripple is negligible across C_o, the maximum inductor current ripple happens at moments $\omega t = \frac{n\pi}{6}$ ($n = 1, 3, 5\ldots$). At these time instants, the phase in the middle is crossing zero, and thus no current is demanded from the bidirectional path. Therefore, the maximum inductor current ripple value is given by

$$\begin{aligned}\Delta i_{L,pp,\max} &= \frac{\frac{N_2}{N_1}\sqrt{3}\hat{V}_N - v_{\text{out}}}{L_o} t_{2,\min} \\ &= \frac{3M\hat{V}_N}{4L_o f_{\text{sw}}}\frac{N_2}{N_1}\left(1 - \frac{\sqrt{3}}{2}M\right). \end{aligned} \tag{40}$$

According to empirical data, the dc inductor ripple is usually set to be 20% of the average current value I_{out}. On the other hand, in order to provide an even impedance for the common-mode noise coming from the secondary switching stage to the dc output, the total output inductance L_o is preferred to be split into two inductors and placed on the upper and lower output rail, respectively. The total value of the output inductor is chosen to be 200 μH. The core selected is EPCOS ETD54/28/19 N97 that is appropriate for 100 kHz switching frequency operation. The final design of the two output inductors is included in Table V.

D. Input Capacitor C Design

The input capacitor C can be designed using maximum peak-to-peak ripple voltage $\Delta v_{C,pp,\max}$ that occurs at time instances $\omega t = \frac{n\pi}{3}$ ($n = 1, 3, 5, \ldots$). Assuming that the capacitor value is small enough so that the phase shift introduced by capacitor reactive currents can be neglected, the maximum peak-to-peak ripple voltage at $\omega t = \frac{\pi}{3}$ is given by

$$\begin{aligned}\Delta v_{C,pp,\max} &= \frac{N_2}{N_1} I_{\text{out}} \left(1 - M\cos\omega t\right) \frac{t_{2,\max}}{C} \\ &= \frac{(2-M)M}{4f_{\text{sw}}C}\frac{N_2}{N_1} I_{\text{out}}. \end{aligned} \tag{41}$$

On the other hand, the capacitor C selection should not be chosen too high since it would draw unnecessary high reactive currents impairing the power factor. Based on the empirical data, the value of the peak-to-peak voltage ripple should be contained in the range of 5%–10% of the nominal rms voltage value. The value chosen is 4.5 μF, which gives maximum voltage ripple of 9%, while limiting reactive current draw to 10% of nominal output power.

The RMS current of the capacitor is composed of high-frequency pulsating currents drawn by the rectifier and low-frequency reactive current drawn from the source as

$$I_{C,RMS} = \sqrt{\left(\frac{2M}{\pi} - \frac{M^2}{2}\right)\left(\frac{N_2}{N_1} I_{\text{out}}\right)^2 + \frac{1}{2}\left(\omega C\hat{V}_N\right)^2}. \tag{42}$$

TABLE V
LIST OF THE MAIN COMPONENTS EMPLOYED IN THE PROTOTYPE OF THE PROPOSED ISOLATED SINGLE-STAGE THREE-PHASE BUCK-TYPE RECTIFIER

Component	Description
L_1 = 270 μH	MAGNETICS toroid powder core 58083, N=60, solid copper wire of 1.5 mm diameter
C = 3 x 0.47 μF	EPCOS 0.47μF B32923 (305 Vac) EMI suppression film capacitor
L_2 = 55 μH	MAGNETICS toroid powder core 58548, N=20, solid copper wire of 1.5 mm diameter
R_d = 5 Ω	OHMITE 45F5R0E (5W) silicone-ceramic conformal axial terminal wirewound resistor
Input diodes $D_{N\pm}$	ST Microelectronics 400 V/30 A STTH30R04 ultra-fast recovery diode
Bidirectional switches $S_{ya/b/c}$	Infineon 650 V CoolMOS C6 series (IPW65R037C6)
Switches $S_{x1/x2/y1/y2}$	Infineon 650 V CoolMOS C7 series (IPW65R045C7)
Primary heatsink	Fischer Elektronik LA-6 Cooling aggregates with axial fan
Transformer	EPCOS ferrite core PM87 material N27, N_1/N_2=10/15, primary Litz wire 200 strands x ϕ 0.07 mm, 10 in parallel, insulator material kapton of horizontal width 6.5 mm, secondary Litz wire 200 strands x ϕ 0.07 mm, 4 in parallel
Output diodes D_{1-4}	CREE 1200 V/43 A C4D30120D SiC Schottky diode
Inductor L_o = 2 x 100 μH	EPCOS ferrite core ETD54 material N97, airgap 1.5 mm, 19 turms, solid wire of 0.9 mm diameter 10 in parallel
Capacitor C_o = 4 x 50 μF	WIMA 50 μF DCP4I055007JD2KYSD (600 Vdc) film capacitor

E. Input Inductors L_1, L_2, and Resistor R_d

The input inductor L_1 is normally designed regarding the necessary EMI standard that has to be complied. On the other hand, the filter resonant frequency should be at least one decade higher from the grid frequency in order not to amplify the low-frequency harmonics, namely the fifth and the seventh. The reason for this avoidance is due to the section 16 of DO-160 G imposing stringent requirements on first 40 harmonics drawn by the equipment [23]. Therefore, the resonance frequency is selected to be in the range of 4 kHz, making the L_1 inductor value of 270 μH. In order to limit the resonant peak of the $L_1 - C$ filter, a inductive passive damping scheme with L_2 at 50 μH and R_d of 5 Ω is used, as proposed in [33].

F. Losses Estimation

In order to validate the concept of proposed rectifier topology, the design guideline of a 3.3-kW rectifier including EMI filter has been thoroughly discussed in this chapter. A list of the main components is provided in Table V. The corresponding distribution of losses estimation at 3.3-kW nominal power is listed in Fig. 14. In this power loss estimation, the losses considered are as follows.

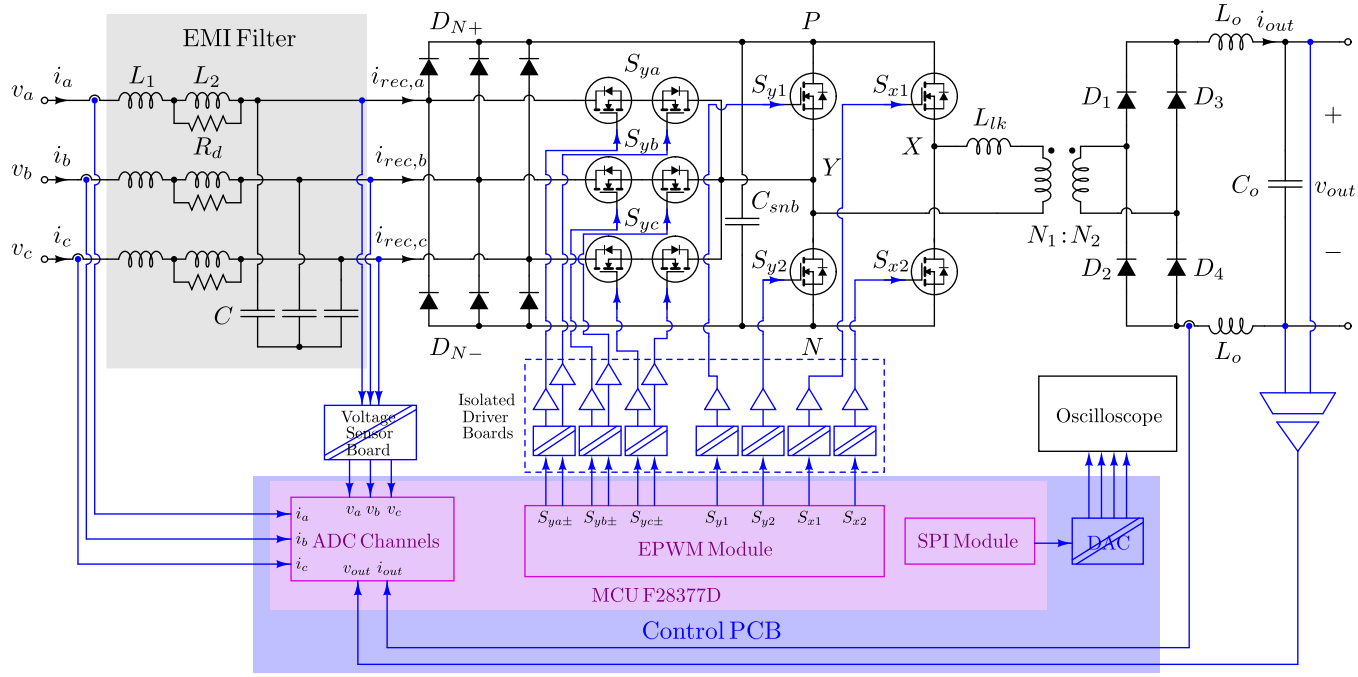


Fig. 16. Block diagram of the hardware demonstrator of the proposed rectifier, including power stage and digital control stage.

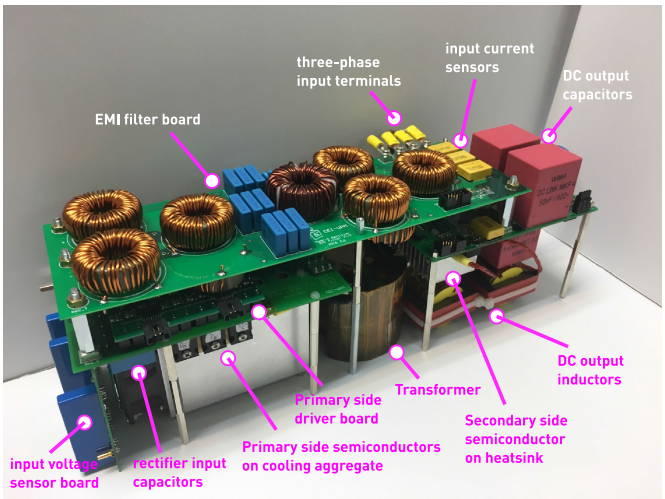


Fig. 17. Photograph of the assembled rectifier hardware (dimension: length 414 mm × width 100 mm × height 140 mm).

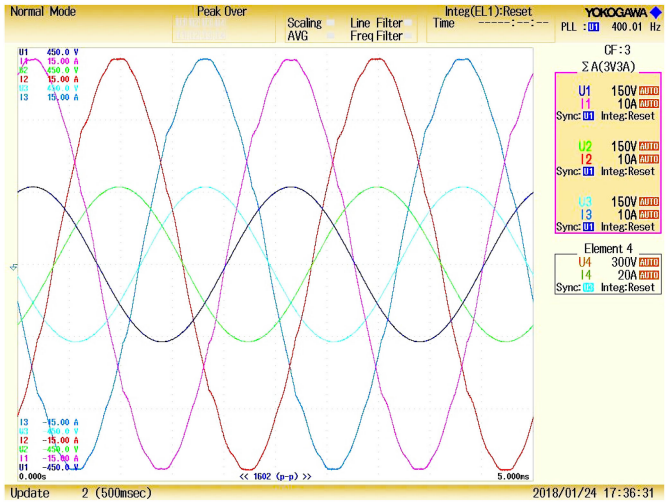


Fig. 18. Experimental waveforms of three-phase input voltages (U1, U2, and U3) and currents (I1, I2, and I3) at nominal input voltage and nominal load.

1) *EMI Filter:* Inductor losses of differential inductors L_1, damping inductors L_2, damping resistor losses of R_d, for all three phases. Capacitor losses are neglected.
2) *Input Diodes:* $D_{N\pm}$ conduction losses only, since these diodes conduct 120 degrees of the grid period. Nevertheless, the chosen devices are ultrafast recovery diodes due to high $\mathrm{d}i/\mathrm{d}t$ transients occurring during the conduction period from carrying full current to carrying near-zero current.
3) *MOSFETs:* Conduction losses of S_{ya}, S_{yb}, S_{yc}, S_{y1}, S_{y2}, S_{x1}, and S_{x2}, respectively. Since all the switches can achieve ZVS, only turn-OFF losses are considered for the switching losses.
4) *Transformer:* Core losses and ac winding losses.
5) *Output Diodes:* D_{1-4} conduction and switching losses. Since the output diodes are all SiC Schottky diodes, reverse recovery losses do not exist. However, switching loss due to charging and discharging of diode capacitance is included.
6) *Output Inductors:* Two dc output inductors core losses and winding losses.

In the end, this estimation shows an overall efficiency of 93.74%, which is moderate compared to the state-of-the-art rectifier topologies with isolation [19], [25], [28], [34], [35]. The efficiency can be improved by utilizing SiC MOSFET semiconductors to further reduce the conduction and turn-OFF loss.

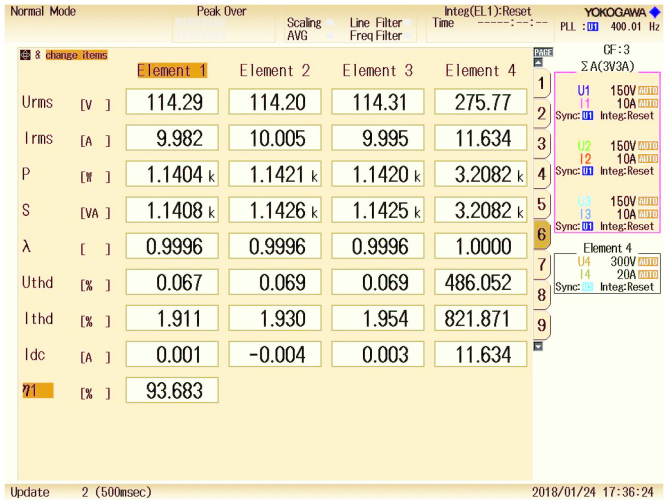


Fig. 19. Power quality overview of three-phase input voltages and currents at nominal input voltage and nominal load.

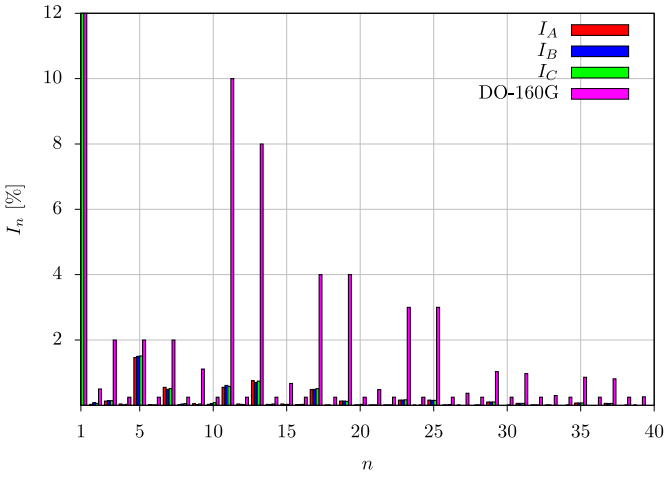


Fig. 20. Experimental results at nominal operating condition of normalized input current spectrum against the DO-160 G limits.

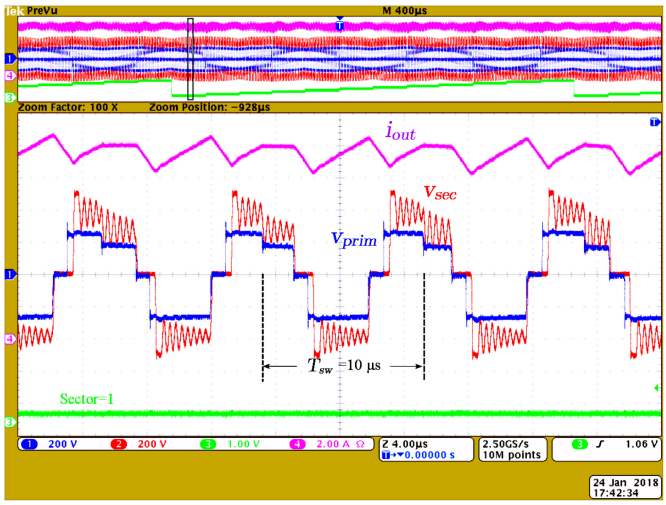


Fig. 21. Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, showing waveforms of v_{prim} (Ch1 in blue, 200 V/div), v_{sec} (Ch2 in red, 200 V/div), sector signal after DAC (Ch3 in green, 1 V/div), dc output inductor current i_{out} (Ch4 in magenta, 2 A/div), at time scale of 4 μs/div.

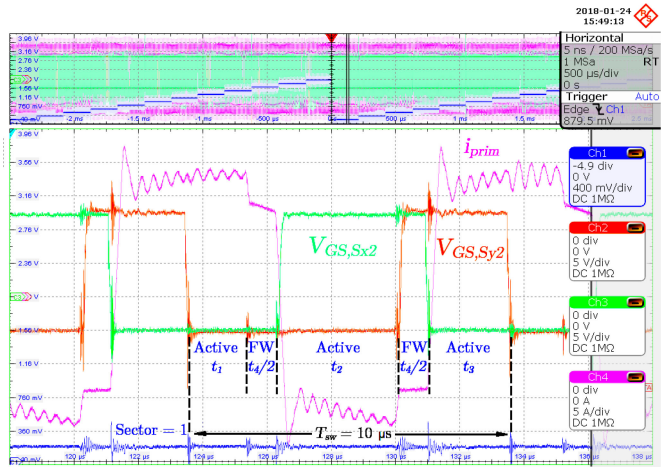


Fig. 22. Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, showing waveforms of sector signal after DAC (Ch1 in blue, 400 mV/div), gate–source signal of S_{y2} (Ch2 in red, 5 V/div), gate–source signal of S_{x2} (Ch3 in green, 5 V/div), and transformer primary current i_{prim} (Ch4 in magenta, 5 A/div), at time scale of 2 μs/div.

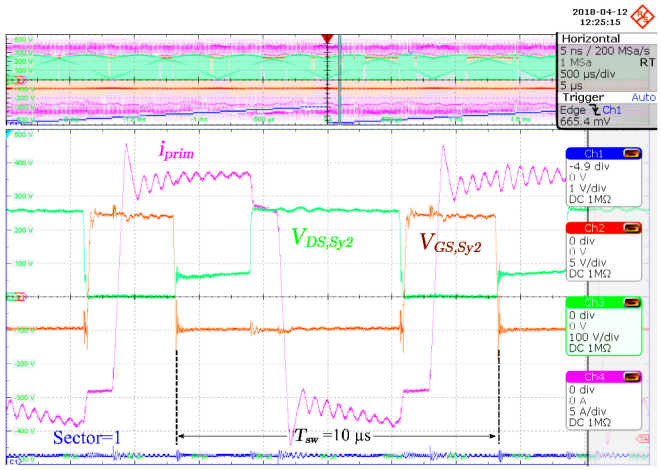


Fig. 23. Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, ZVS details on MOSFET S_{y2}, showing waveforms of sector signal after DAC (Ch1 in blue, 1 V/div), gate–source signal of S_{y2} (Ch2 in red, 5 V/div), drain–source voltage of S_{y2} (Ch3 in green, 100 V/div), transformer primary current i_{prim} (Ch4 in magenta, 5 A/div), at time scale of 2 μs/div.

Also, all diodes could be replaced by SiC MOSFETs as well, which would have a beneficial impact on the conduction loss. Moreover, leakage inductance could be included externally in order to optimize the transformer winding loss. However, this would significantly increment the cost of the rectifier. Finally, the harsh semiconductor voltage and temperature derating applied according to Table II also has negative impact on the efficiency.

G. Simulation Validation

Based on the previous mentioned modulation method, the steady-state operation of the proposed rectifier, including EMI filter working under nominal input and nominal load, is simulated in PLECS [31]. The values of transformer turns ratio, modulation index, EMI filter, and output filter used in this simulation are designed in the previous sections, respectively.

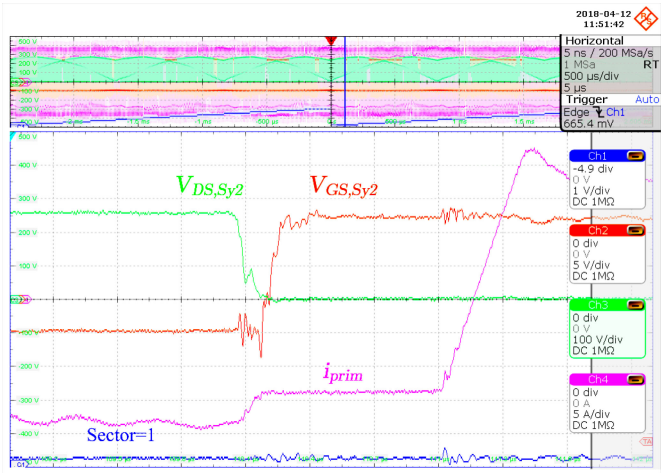


Fig. 24. Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, zoom-in of Fig. 23 at MOSFET S_{y2} turn-ON instant, showing waveforms of sector signal after DAC (Ch1 in blue, 1 V/div), gate–source signal of S_{y2} (Ch2 in red, 5 V/div), drain–source voltage of S_{y2} (Ch3 in green, 100 V/div), and transformer primary current i_{prim} (Ch4 in magenta, 5 A/div).

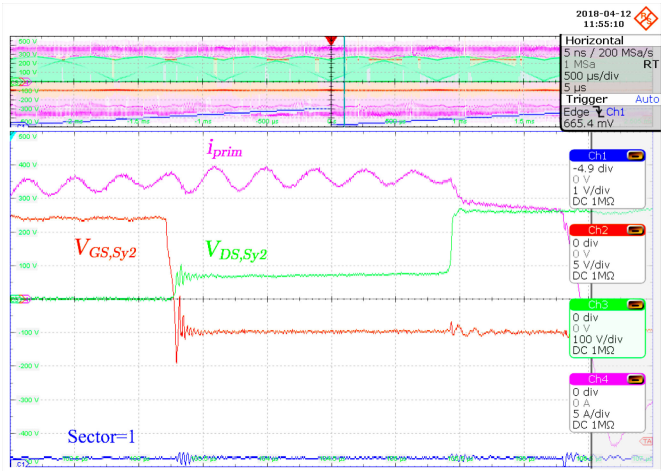


Fig. 25. Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, zoom-in of Fig. 23 at MOSFET S_{y2} turn-OFF instant, showing waveforms of sector signal after DAC (Ch1 in blue, 1 V/div), gate-source signal of S_{y2} (Ch2 in red, 5 V/div), drain-source voltage of S_{y2} (Ch3 in green, 100 V/div), and transformer primary current i_{prim} (Ch4 in magenta, 5 A/div).

The main simulation waveforms are depicted in Fig. 15. Due to the presence of the inductors L_1 and L_2, the rectifier input voltages $v_{\text{rec},a}$, $v_{\text{rec},b}$, and $v_{\text{rec},c}$ exhibit small phase shift with the respect to the three-phase source voltages v_a, v_b, and v_c. The phase currents after filtering by EMI filter are depicted as i_a, i_b, and i_c, which exhibit near-sinusoidal waveform. The relative on-times intervals t_1, t_2, t_3, and t_4 derived in Section III-A are depicted as duty cycle values. It is worth noticing that, the active state interval t_1 is the interval when the phase with minimum absolute value out of the three is allowed to conduct current through the bidirectional switch pair, thus it has exactly the triangular shape at three times line frequency. S_{ya}, S_{yb}, and S_{yc} are the driven signals for the bidirectional switching pairs. It can be seen that, each switching pair only switches when its corresponding phase voltage is in the middle of all three. As discussed in Section IV-A, the transformer primary voltage v_{prim} is discontinuous but shows positive and negative envelopes of a six-fold waveform. The output dc inductor current i_{out} is also presented.

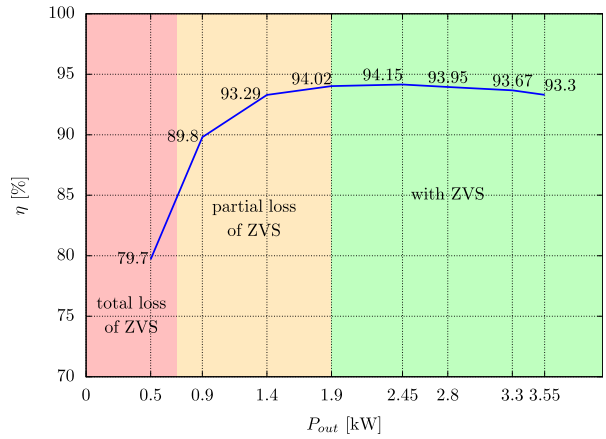


Fig. 26. Efficiency measurement under load sweep of the three-phase rectifier with passive snubber installed.

V. Experimental Validation

In this section, a hardware demonstrator is constructed and tested in order to validate experimentally the concept and the design of the proposed rectifier topology. Experimental results are performed at nominal power, which validates the previous theoretical analysis.

The constructed rectifier system has a block diagram shown in Fig. 16. It can be observed that there are ten driving signals needed to correctly control the rectifier. For each bidirectional switch pair S_{yN}, there is no need to isolate the driver supplies for S_{yN+} and S_{yN-} since the MOSFET pairs are in common-source configuration. This results in the total number of isolated drivers equal to seven. The input voltage sensors are used to determine the sector location and for correct SVM calculation and generation. The input and output current measurement as well as output voltage measurements are all used for rectifier protection purposes. Finally, SPI (serial peripheral interface) module is used in order to send real-time signals from the microcontroller to an external DAC board so that internally measured values can be visualized on an oscilloscope.

The final version of the rectifier hardware demonstrator is shown in Fig. 17, which consists of the primary and secondary PCB of the rectifier, transformer, driver boards for the primary side MOSFETs, three-phase voltages sensor board, and on top of all lies the EMI filter board. Moreover, in order to receive measurements and send modulation signals to the power stage, a control PCB is designed, loaded with a Texas Instruments F28377D controlCARD [36], together with other signal conditioning and protection circuitry.

The experimental results of the proposed three-phase rectifier at nominal input (115 V_{RMS} line-to-neutral, 400 Hz), operating under nominal load (3.3 kW at 270 V) with the passive snubber

TABLE VI
COMPARISON LIST OF THE STATE-OF-THE-ART ISOLATED THREE-PHASE RECTIFIERS

Topology	Semiconductor Technology	Output Power	Input Voltage	Output Voltage	THD_I	PF	Full load Efficiency	Power Density
Phase-Modular SEPIC [11]	Si IGBT Si Diodes	4 kW	3x220 V 50 Hz	400 V	4.0%	99.8%	90%	N/A
Isolated Full-Bridge Boost [13]	Si IGBT Si Diodes	1.7 kW	3x110 V 50 Hz	200 V	N/A	99%	91%	N/A
Swiss-Forward [35]	SiC MOSFET SiC Schottky	3 kW	3x115 V 400 Hz	270 V	2.9%	98.8%	93.5%	0.44 kW/dm^3
IMDAB3R [12]	SiC MOSFET SiC Schottky	1.2 kW	3x115 V 60 Hz	180 V	N/A	N/A	94.4%	N/A
Phase-Modular Ćuk [16]	SiC MOSFET Si Diodes	2 kW	3x115 V 60 Hz	400 V	4.87%	99.9%	94.5%	N/A
Phase-Modular & Scott Transformer [38]	Si IGBT Si Diodes	12 kW	3x220 V 60 Hz	400 V	4.1%	99.2%	95.1%	1.33 kW/dm^3
Phase-Modular PFC & LLC [4]	Si MOSFET SiC Diode	10 kW	3x220 V 60 Hz	300 V	N/A	N/A	95.5%	N/A
IMDAB3R [14]	SiC MOSFET	1 kW	3x115 V 60 Hz	230 V	12.1%	97.0%	96.0%	N/A
Three-phase VIENNA & LLC [5]	SiC MOSFET SiC Schottky	1.16 kW	3x115 V 800 Hz	28 V	5.2%	N/A	97.1%	1.34 kW/dm^3
Isolated Matrix-Type Δ Rectifier [15]	SiC MOSFET SiC Schottky	7.5 kW	3x230 V 50 Hz	400 V	1.45%	99.9%	97.2%	1.03 kW/dm^3
Phase-Modular PFC & LLC [6]	GaN HEMT	22 kW	3x115 V 60 Hz	400 V	6.0%	99.7%	98.0%	3.3 kW/dm^3
IMDAB3R [19]	SiC MOSFET	8 kW	3x230 V 50 Hz	400 V	3.0%	99.0%	99.0%	4.0 kW/dm^3
This work	Si MOSFET SiC Schottky	3.3 kW	3x115 V 400 Hz	270 V	1.95%	99.9%	93.7%	0.57 kW/dm^3

installed, are shown below. The three-phase source used is Pacific Power Source 360AMXT, and the resistive load is realized by a power resistor bank of 22 Ω value. At the input, after the three-phase source and before the EMI filter of the rectifier, Yokogawa WT1800 precision power analyzer [37] is used to measure the waveforms and characteristics of the three-phase input voltages and currents. Fig. 18 demonstrates these three-phase voltages U1, U2, and U3 and currents I1, I2, and I3. It can be seen that, three-phase voltage has a line frequency of 400 Hz and the three-phase currents waveform is very close to a sinusoidal. Numeric values that characterize these waveforms are obtained also by Yokogawa WT1800, as shown in Fig. 19. Elements 1, 2, and 3 correspond to input phases A, B, and C, respectively, while Element 4 represents the dc output. Notably, the constructed rectifier prototype exhibits a very good THD_I of 1.9% per phase. Regarding power factor, Fig. 19 shows an excellent PF of 0.9996. Furthermore, η_1 in the last row stands for the efficiency of the rectifier including the EMI filter, which is 93.7%. Note that the power consumption of the aforementioned control PCB is negligible compared to the total power transfered, thus it is not considered in the efficiency calculation. Summarizing input power quality measurements, the DO-160 G section 16.7.1.2.1 compliance with low-frequency harmonic emissions is given in Fig. 20.

The axial fan in the primary-side heatsink is supplied with 12 V dc from the aforementioned control PCB, and can offer a maximum free-air flow 56 m^3/h. The measured temperature of the primary heatsink is 55 $^\circ$C, with ambient temperature being 25 $^\circ$C. The transformer winding temperature is measured by a preplaced K-type thermocouple (connected to a multimeter) inside the windings, and the transformer windings show a temperature of 45°C.

Fig. 21 represents a detailed waveform measurements within the rectifier. Ch1 measures the transformer primary-side voltage v_{prim}; Ch2 presents the transformer secondary voltage v_{sec}, where the effect of the passive snubber clamping the first ringing peak can be seen; Ch3 is the PLL sector value coming after DAC, the zoom-in shows the area in the middle of sector 1; Ch4 measures the dc output inductor current i_{out}.

In Fig. 22, more waveforms are presented. The zoom-in shows also the area in the middle of sector 1. Ch1 presents the PLL sector information; Ch2 measures the gate–source of MOSFET S_{y2}; Ch3 measures the gate–source of MOSFET S_{x2}; and Ch4 shows the current through the primary of the transformer i_{prim}. Active state time intervals t_1, t_2, and t_3, as well as freewheeling state time interval t_4, are marked in this capture, corresponding to the illustration in Fig. 10. It demonstrates that the turn-ON instant of S_{y2} (Ch2) marks the change from an active state to a freewheeling state, while the turn-ON and turn-OFF of S_{x2} (Ch3) shows the change from a freewheeling state to an active state. When the secondary diode bridge first enters the active state, the first current peak of i_{prim} flows into the secondary snubber capacitor and the snubber clamps its voltage (see v_{sec} in Fig. 21) so that the ringing is mitigated.

In order to show the ZVS details, the drain–source voltage of S_{y2} is measured together with its gate–source signal. Fig. 23 captures the waveforms of Ch1 for PLL sector information, Ch2 for gate–source of MOSFET S_{y2}, Ch3 for drain–source voltage of S_{y2}, and Ch4 for transformer primary current i_{prim}. It is worth noticing that Ch2 in Fig. 23 measures the same signal as Ch2 in Fig. 22, which are both gate–source of S_{y2}. Moreover, drain–source voltage of S_{y2} (Ch3) shows three levels: when it is turned OFF but one MOSFET of the bidirectional switch S_{yn} is on, it blocks an intermediate voltage level; next, when S_{y1} is ON, it

blocks the maximum line-to-line voltage; in the end, when it is turned ON, it shows zero. This measured waveforms exhibit good accordance to the simulated ones (S_{y2} and v_{Sy2}) in Fig. 12.

Furthermore, in order to see the detailed ZVS behaviors, based on Fig. 23, zoom-in captures focused on the turn-ON and turn-OFF instants are presented in Figs. 24 and 25, respectively. It can be seen from Fig. 24, the drain–source of S_{y2} (Ch3) drops to zero before gate–source of S_{y2} (Ch2) is turned ON. Moreover, in Fig. 25, gate–source of S_{y2} (Ch2) is turned OFF and then its drain–source voltage starts to rise to an intermediate value facilitating the ZVS turn-ON of S_{yn}. These measured ZVS instants also coincide with the simulated ones in Fig. 12.

In the end, efficiency measurement under a wide range of load is conducted, and the results are depicted in Fig. 26. The rectifier efficiency peaks at 2.45 kW load, reaching 94.15%. It is also worth mentioning that, one more point over nominal load is also tested, showing efficiency of 93.3% at the load of 3.55 kW. From approximately half load down to 0.75 kW (i.e., 20% of nominal load), partial loss of ZVS is observed, while below 0.75 kW, ZVS is completely lost. Finally, a comparison of the proposed rectifier with the current state-of-the-art three-phase isolated rectifiers is presented in Table VI.

VI. Conclusion

In this article, a modification of the VIENNA Rectifier III is proposed to achieve ZVS in all switching transitions. Corresponding theoretical analysis of the proposed rectifier operating principles is presented. The calculation of timing for each active state and freewheeling state is the essence of the modulation for the rectifier. The proposed current SVM method to compose the input rectifier current space vector is analyzed in detail, based upon a heritage of three-phase buck-type rectifiers. Furthermore, having the high-frequency transformer present, the volt–second balance of the transformer has to be considered and integrated into the calculation of the modulation timing in each switching period. Next, the ZVS capability for every switching transition is an advantageous feature of the proposed rectifier topology offering efficiency benefits. The full-bridge-like structure together with the asymmetrical modulation sequence provides ZVS easily with adequate leakage inductance and sufficient dead-time. Necessary requirements for reaching ZVS above certain load level are derived, and verification in simulation results are provided. Also, complete rectifier design guidelines are given. The analysis shows that the key point in the transformer design is to achieve the desired leakage inductance by separating the primary winding and the secondary winding, although this compromises the winding ac losses in comparison to a well interleaved case. On the other hand, this leakage inductance is essential for achieving ZVS, which can reduce the EMI filtering effort, which provides a good compensation for slightly increased winding losses. Moreover, a passive snubber is used at the secondary of the rectifier, in order to clamp the voltage ringing peak to a lower value, and thus minimize potential EMI issues. In the end, experimental results from a 3.3-kW hardware demonstrator are presented to validate the operating principle of the proposed rectifier. At nominal power, this isolated single-stage three-phase rectifier, including EMI filter, shows an excellent THD_I of 1.9% and a near-unity PF of 0.9996, while complying with DO-160 G low-frequency current emissions requirement. The efficiency at nominal power is 93.7%, which is moderate compared with the state-of-the-art listed in Table VI.

References

[1] P. Wheeler, "The more electric aircraft: Why aerospace needs power electronics?" in *Proc. 13th Eur. Conf. Power Electron. Appl.*, Sep. 2009, pp. 1–30.

[2] J. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems part I,", *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 176–198, Jan. 2013.

[3] J. Chen, Y. Shen, J. Chen, H. Bai, C. Gong, and F. Wang, "Evaluation on the autoconfigured multipulse AC/DC rectifiers and their application in more electric aircrafts," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 4, pp. 1721–1739, Dec. 2020.

[4] H. Kim, J. Baek, M. Ryu, J. Kim, and J. Jung, "The high-efficiency isolated ac–dc converter using the three-phase interleaved LLC resonant converter employing the y-connected rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4017–4028, Aug. 2014.

[5] Q. Wang, X. Zhang, R. Burgos, D. Boroyevich, A. White, and M. Kheraluwala, "Design and optimization of a high performance isolated three phase AC/DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–10.

[6] J. Lu *et al.*, "A modular-designed three-phase high-efficiency high-power-density EV battery charger using dual/triple-phase-shift control," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8091–8100, Sep. 2018.

[7] Y. Jang, M. M. Jovanovic, M. Kumar, Y. Chang, Y. Lin, and C. Liu, "A two-switch, isolated, three-phase ac–dc converter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10 874–10 886, Nov. 2019.

[8] J. M. Molina, P. Alou, J. A. Oliver, M. Silva, and J. A. Cobos, "Three-phase buck type rectifier topology integrated with current fed full-bridge," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 84–91.

[9] T. Nussbaumer, K. Mino, and J. W. Kolar, "Design and comparative evaluation of three-phase buck boost and boost buck unity power factor PWM rectifier systems for supplying variable DC voltage link converters," in *Proc. 10th Eur. Power Qual. Conf. (PCIM 2004)*, vol. 1, May 2004, pp. 126–135.

[10] T. Nussbaumer and J. W. Kolar, "Comparison of 3-phase wide output voltage range PWM rectifiers," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3422–3425, Dec. 2007.

[11] G. Tibola and I. Barbi, "Isolated three-phase high power factor rectifier based on the SEPIC converter operating in discontinuous conduction mode," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4962–4969, Nov. 2013.

[12] N. Hirose, Y. Matsui, and T. Takeshita, "Isolated AC/DC converter using simple PWM strategy," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 3791–3796.

[13] T. Meng, H. Ben, and Y. Song, "Investigation and implementation of a starting and voltage spike suppression scheme for three-phase isolated full-bridge boost PFC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1358–1367, Feb. 2018.

[14] M. A. Sayed, K. Suzuki, T. Takeshita, and W. Kitagawa, "Pwm switching technique for three-phase bidirectional grid-tie dc–ac–ac converter with high-frequency isolation," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 845–858, Jan. 2018.

[15] L. Schrittwieser, P. Cortes, L. Fassler, D. Bortis, and J. W. Kolar, "Modulation and control of a three-phase phase-modular isolated matrix-type PFC rectifier," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4703–4715, Jun. 2018.

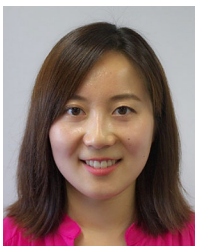
[16] S. Gangavarapu, A. K. Rathore, and D. M. Fulwani, "Three-phase single-stage-isolated cuk-based PFC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1798–1808, Feb. 2019.

[17] R. Baranwal, K. V. Iyer, K. Basu, G. F. Castelino, and N. Mohan, "A reduced switch count single-stage three-phase bidirectional rectifier with high-frequency isolation," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9520–9541, Nov. 2018.

[18] J. Afsharian, D. Xu, B. Wu, B. Gong, and Z. Yang, "The optimal PWM modulation and commutation scheme for a three-phase isolated buck matrix-type rectifier," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 110–124, Jan. 2018.

[19] L. Schrittwieser, M. Leibl, and J. W. Kolar, "99% efficient isolated three-phase matrix-type DAB buck-boost PFC rectifier," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 138–157, Jan. 2020.

[20] J. W. Kolar, U. Drofenik, H. Ertl, and F. C. Zach, "VIENNA rectifier III - A novel three-phase single-stage buck-derived unity power factor AC-to-DC converter system," in *Proc. IEEE Nordic Workshop Power Ind. Electron.*, Aug. 1998, pp. 9–18.
[21] S. Zhao, M. Silva, J. A. Oliver, P. Alou, O. Garcia, and J. A. Cobos, "Analysis and design of an isolated single-stage three-phase full-bridge with current injection path PFC rectifier for aircraft application," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 6777–6784.
[22] Department of Defense Std., MIL-STD-704F, Aircraft Electric Power Characteristics, 2004. [Online]. Available: https://www.ieee.li/pdf/standards-handbooks/MIL-STD-704F.pdf.
[23] RTCA, "Environmental conditions and test procedures for airborne equipment," Radio Tecnical Commission Aeronaut., Washington, DC, USA, 2007. [Online]. Available: Available: https://do160.org/rtca-do-160g/
[24] U. Borovic, S. Zhao, J. A. Oliver, P. Alou, J. A. Cobos, and P. Pejovic, "Design methodology for three-phase buck-type and boost-type rectifiers to comply with the do-160 g current distortion test," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 33–47, Jan. 2020.
[25] F. Stögerer and J. W. Kolar, "Design and experimental analysis of a three-phase single-stage 8.5 kW buck-derived PWM-rectifier system (VIENNA Rectifier III)," in *Proc. 9th Eur. Conf. Power Electron. Appl.*, Aug. 2001.
[26] F. Stögerer, J. W. Kolar, and U. Drofenik, "A novel concept for transformer volt second balancing of a VIENNA rectifier III based on direct magnetizing current measurement," in *Proc. IEEE Nordic Workshop Power Ind. Electron.*, Jun. 2000, pp. 134–140.
[27] Q. Wang, X. Zhang, R. Burgos, D. Boroyevich, A. M. White, and M. Kheraluwala, "Design and implementation of a two-channel interleaved vienna-type rectifier with >99% efficiency," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 226–239, Jan. 2018.
[28] P. Cortes, L. Fassler, D. Bortis, J. W. Kolar, and M. Silva, "Detailed analysis and design of a three-phase phase-modular isolated matrix-type PFC rectifier," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 3864–3871.
[29] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in *Proc. 5th Annu. Proc. Appl. Power Electron. Conf. Expo.*, 1990, pp. 275–284.
[30] V. Vlatkovic, D. Borojevic, and F. C. Lee, "A zero-voltage switched, three-phase isolated PWM buck rectifier," *IEEE Trans. Power Electron.*, vol. 10, no. 2, pp. 148–157, Mar. 1995.
[31] *Plecs Simulation Software*. [Online]. Available: https://www.plexim.com/products/plecs
[32] PEmag tool in Ansys Maxwell software. [Online]. Available: https://www.ansys.com/products/electronics/ansys-maxwell
[33] R. Erickson, "Optimal single resistors damping of input filters," in *Proc. Appl. Power Electron. Conf. Expo.*, 1999, Mar. 1999, pp. 1073–1079.
[34] P. Cortes, D. Bortis, R. Pittini, and J. W. Kolar, "Comparative evaluation of three-phase isolated matrix-type PFC rectifier concepts for high efficiency 380VDC supplies of future telco and data centers," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, Aug. 2014, pp. 1–10.
[35] M. Silva, N. Hensgens, J. A. Oliver, P. Alou, O. Garcia, and J. A. Cobos, "Isolated swiss-forward three-phase rectifier with resonant reset," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4795–4808, Jul. 2016.
[36] Texas Instruments TMS320F28377D microntroller. . [Online]. Available: http://www.ti.com/product/TMS320F28377D
[37] Yokogawa WT1800 power analyzer. [Online]. Available: https://tmi.yokogawa.com/solutions/products/power-analyzers/wt1800e-high-performance-power-analyzer
[38] A. A. Badin and I. Barbi, "Unity power factor isolated three-phase rectifier with two single-phase buck rectifiers based on the scott transformer," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2688–2696, Sep. 2011.



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