Impedance Analysis and Design of IPT System to Improve System Efficiency and Reduce Output Voltage or Current Fluctuations

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***Abstract*—With the increase of load resistance, the impedance angle of the rectifier with passive *C* filter also increases, which may have some negative effects on the characteristics of the inductive power transfer (IPT) system. This article presents an impedance analysis method for *C*-filter rectifiers in continuous conduction mode. The calculation formula of critical load resistance is given and the relevant values are calculated. An improved *C*-filter rectifier circuit is proposed to reduce the phase angle of the IPT system. A very tiny capacitance is connected in parallel at the input end of the rectifier to reduce the impedance angle as load resistance changes, with hardly increased costs. This improved method not only improves the system efficiency, but also reduces the fluctuation of output voltage or current. Simulation and experiment results verify the feasibility of the proposed topology. A 1 kW prototype with primary series, secondary series compensation topology was built. The maximum system efficiency from dc power supply to the load is 94.5%. The efficiency under rated load is as high as 93%. Compared with traditional method, it has increased by 0.6%.**

***Index Terms*—Discontinuous conduction mode (DCM), input impedance angle, paralleled capacitor, passive rectifiers with *C* filter.**

I. Introduction

INDUCTIVE power transfer (IPT) technology has gained wide attention due to its advantages of noncontact, convenience and reliability [1]–[3]. In most applications, electrical energy is transferred from the front stage to the back stage, so diode bridge rectifiers with passive *C*-filters are commonly used. The input impedance of the rectifier is often considered as a resistance approximately in most cases for an IPT system [4]–[6]. As the load resistance after the rectifier increases, the rectifier operates at the discontinuous conduction mode (DCM). In this case, the input impedance can no longer be approximated to a resistor, but a complex impedance because the imaginary part is large. It may result in voltage duty cycle loss, system efficiency reduction, and absence of load-independent output property. The relationship between the input impedance of the rectifier and the load resistance in continuous conduction mode (CCM) and DCM based on the system with capacitor–capacitor–inductor (*LCC*) compensation topology on secondary side was analyzed in [6]–[9]. To address the problem mentioned above, numerous methods are proposed, but they all have their own limitations.

In [10], a primary inductor–capacitor–capacitor, secondary capacitor–capacitor–inductor (*LCC/LCC*) compensation topology and its adjustment method of compensation parameters is given. It is helpful to realize zero voltage switching (ZVS) and reduce the secondary coil current. However, the problem of inductive equivalent load impedance is not solved, and it is only suitable for *LCC/LCC* compensation topologies. Qu *et al*. [11] revels the reason of the increase of the input impedance angle in DCM. An improved primary series, secondary capacitor–inductor–capacitor topology was proposed, which increases the load range but has a narrow scope of application. Mai *et al*. [12] proposed the scheme of active rectifier bridge and auxiliary detection coil, which solves the problem of impedance and can be widely used, but the system becomes much more costly and complex.

The imaginary part of the input impedance of the rectifier increases as the load resistance becomes larger, which has a more tremendous impact on the system with constant current output. In a system of this kind, higher proportion of imaginary part in larger load resistance means higher power and more power loss. Compensation topologies with constant current output, such as primary series, secondary series (S/S) [13], [14], (primary series, secondary series–parallel [15], primary inductor–capacitor, secondary series [16] and *LCC/LCC* [10] are all affected by this problem under heavy load conditions. Especially in the systems introduced in [13] and [15], the inductive equivalent load impedance leads to the increase of the ratio of the input current and the output current of the rectifier. Usually, when the rectifier operates in CCM under small load resistance, the ratio is about $\pi/2$.

In this article, a tiny auxiliary capacitor is paralleled in front of the rectifier with passive C filter, which can significantly reduce the phase angle of the input voltage and current. Fig. 1(a) shows

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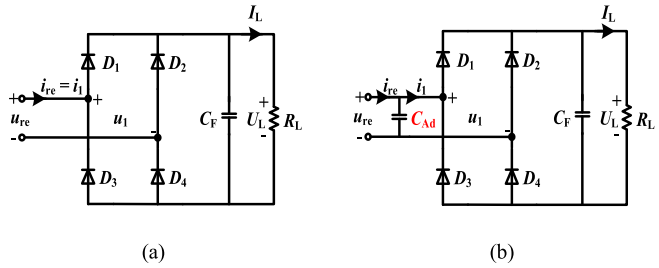

Fig. 1. (a) Traditional rectifier with passive *C* filter. (b) Improved rectifier with passive C filter.

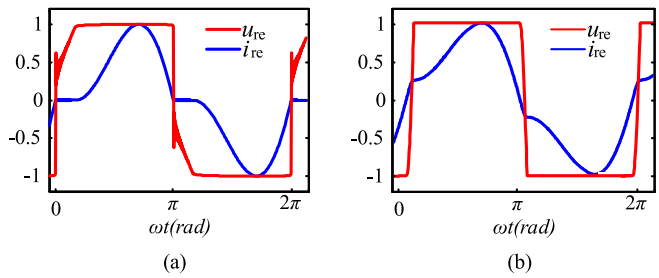

Fig. 2. Waveforms in DCM of the rectifier. (a) Improved. (b) Traditional.

the topology of traditional diode bridge rectifier and Fig. 1(b) shows the circuit of improved rectifier. D_1-D_4 are four rectifier diodes, C_{F} is the filter capacitor, R_{L} is the equivalent resistance of load, and C_{Ad} is the tiny auxiliary capacitor.

Fig. 2 describes the waveforms of voltage and current at DCM, when the load resistance value is large. For the traditional passive rectifier, voltage distortion and duty cycle loss as shown in Fig. 2(a). Severe voltage distortion will result in the loss of duty cycle. At the same time, the input impedance of the traditional rectifier becomes inductive, rather than pure resistive. But, the improved rectifier has overcome these shortcomings.

Then, the calculation method of the equivalent load impedance to fundamental of the traditional and improved rectifier is given. The performance of the improved rectifier in S/S, primary inductor–capacitor–capacitor, secondary series (LCC/S) and *LCC/LCC* compensation topologies are analyzed by simulation. A 1-kW prototype with S/S compensation topology based on the proposed improved rectifier is built. Compared with the traditional method, it not only improves the efficiency, but also reduces the fluctuation of the output current. The value of the added capacitor is very small. And only in the short-term commutation process, there is current flowing through it. So it hardly increases the cost and loss of the system.

II. Analysis of Load Impedance Characteristics of Traditional Rectifiers

As analyzed in [8], the ratio of harmonic current to fundamental current is the main factor affecting the input impedance of the inverter, and the harmonic current is caused by the harmonic voltage generated by the inverter. In order to analyze the input impedance characteristics of the rectifier, the fundamental and harmonic decomposition diagrams of the input current of the rectifier bridge are shown in Fig. 3. In order to simplify the analysis, the parasitic parameters and diode voltage drop are

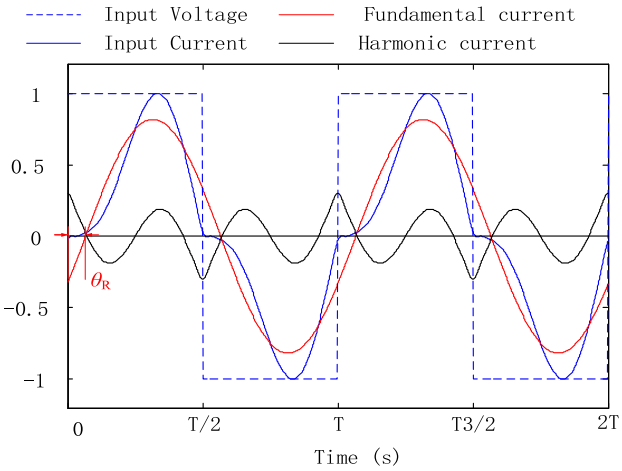

Fig. 3. Fundamental wave and harmonic decomposition diagram of the input current of the traditional rectifier.

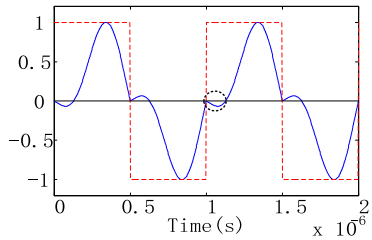

Fig. 4. Waveform of the input current distortion.

ignored. According to the conservation of energy and the fact that commutation point current of the rectifier input current is zero

$$\begin{cases} I_{h0} + I_{\mathrm{o\_top}} \sin(\theta_R) = 0 \\ \frac{2}{\pi} U_o I_{\mathrm{o\_top}} \cos(\theta_R) = \frac{{U_o}^2}{R_L} \end{cases} \tag{1}$$

$$I_h = \sum_{m=1}^{+\infty} \frac{-4U_{\mathrm{o}}}{\pi(2m+1)Z_{2m+1}} \cos((2m+1)\omega_0 t) \tag{2}$$

where $I_{\mathrm{o\_top}}$ is the peak value of the fundamental current, I_h is the harmonic current through the rectifier, I_{h0} is the instantaneous value of the harmonic current when the rectifier diodes are about to turn on, and θ_R is the fundamental impedance angle of the equivalent load impedance of the rectifier The θ_R can be obtained through formula (1) as follows:

$$\theta_R = \arctan \sum_{m=1}^{+\infty} \frac{-8R_L}{\pi^2(2m+1)\,|Z_{2m+1}|} \tag{3}$$

where Z_{2m+1} is the output impedance of the compensation network under the condition of $(2m+1)$ harmonic frequency. It can be found from (3) that the magnitude of the impedance angle is related to the compensation network and the load resistance. The smaller the harmonic impedance of the compensation network, the larger the impedance angle of the rectifier. Besides, there is a positive correlation between the load resistance and the impedance angle. When the load resistance increases to a certain extent, the waveforms of the input current and voltage are shown in Fig. 4. At the moment of the voltage changes from

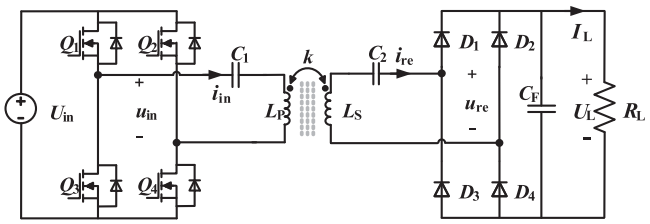

Fig. 5. Typical schematic of S/S compensation topology with traditional rectifier.

negative to positive, the input current is negative. It is impossible for diodes, so the rectifier will enter DCM as shown in Fig. 2(a), and the current will be clamped to zero.

When the rectifier diode is in the critical mode between DCM and CCM, the derivatives of the harmonic current and the fundamental current are equal, shown as follows:

$$\left.\frac{\partial I_{\mathrm{h}}}{\partial_t}\right|_{\mathrm{t=0+}} = -\omega_1 I_{\mathrm{o\_top}}\cos(\theta_R). \tag{4}$$

$\partial h/\partial t$ is shown in (5). When $t = 0$, it can be simplified to (6), where L_{Z} is the inductance corresponding to the high frequency output reactance of the rectifier and the compensation network. Combined (1) and (4), the value of load resistance in critical mode can be given

$$\begin{aligned}\frac{\partial I_{\mathrm{h}}}{\partial_t} &= \sum_{m=1}^{+\infty} -\frac{4U_0 \times (2m+1)\omega_0}{\pi(2m+1)Z_{2m+1}}\sin((2m+1)\omega_0 t)\\ &= \sum_{m=1}^{+\infty} -\frac{4U_0}{\pi(Z_{2m+1}/\omega_0)}\sin((2m+1)\omega_0 t)\end{aligned} \tag{5}$$

$$\begin{aligned}\left.\frac{\partial I_{\mathrm{h}}}{\partial_t}\right|_{\mathrm{t=0+}} &= \left.\sum_{m=1}^{+\infty} -\frac{4U_0}{\pi(2m+1)L_Z}\sin((2m+1)\omega_0 t)\right|_{\mathrm{t=0+}}\\ &= \frac{U_0}{L_{\mathrm{Z}}}\end{aligned} \tag{6}$$

$$R_{LC} = \frac{\pi\omega_1 L_{\mathrm{z}}}{2}. \tag{7}$$

From formula (7), the critical load is only related to the operating frequency and the compensation network.

Take an IPT system based on S/S compensation topology for example, Fig. 5 is the schematic of it. Table I is the circuit parameter, and the compensation parameter C_1 and C_2 satisfies (8). According to (7), the critical resistance of this system is 40.2 Ω. It means when the load resistance is less than 40.2 Ω, the rectifier still operates in CCM. Otherwise, the rectifier will enter DCM. In CCM, the curve of the input impedance angle of the rectifier varying with the load resistance is shown in Fig. 6. It can be seen that the phase angle is proportional to the load. When the load resistance is relatively small, the harmonic components are also very small, which will not cause serious distortion of the rectifier input current. At this time, the rectifier is in CCM mode. When the load resistance is relatively large, the harmonic components are also relatively large, causing serious distortion of the rectifier input current. The current is clamped to 0 at the

TABLE I
PARAMETERS OF SIMULATED CIRCUIT

Parameters	*Value*
U_{in}	56 V
f	85k
L_{P}	58.8 μH
L_{S}	58.5 μH
k	0.43
C_1	59.6 nF
C_2	59.9 nF
C_{Ad}	0 - 4.5 nF
I_{L}	3.4 A
R_{L}	1-40.2 Ω

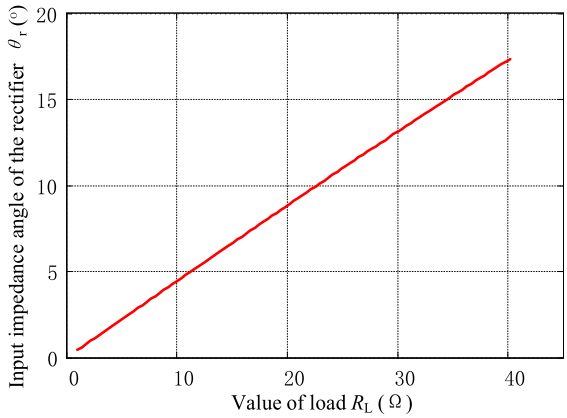

Fig. 6. Curve of the input impedance angle of the rectifier varying with the load obtained by calculation.

moment of voltage commutation. Therefore, the rectifier enters DCM mode

$$\begin{cases} C_1 = \frac{1}{\omega_1 L_{\mathrm{P}}} \\ C_2 = \frac{1}{\omega_1 L_{\mathrm{S}}}. \end{cases} \tag{8}$$

III. ANALYSIS AND DESIGN OF IMPROVED RECTIFIER

As shown in Fig. 2, the working state of the rectifier is changed by adding the tiny capacitor. There are four operation-modes in the proposed rectifier in one cycle T, as shown in Fig. 7. The traditional rectifier has only two modes as shown in Fig. 7(b) and (d). The waveforms of input voltage and different currents in each mode are shown in Fig. 8. There is current flowing through C_{Ad} only when the conduction diode of the rectifier switches. According to symmetry, only half of the modes need to be analyzed.

1) *Mode I:* As shown in Fig. 7(a), it occurs when all of the diodes are OFF and the current $i_1 = 0$, at the time 0-t_1. In this mode, the input current i_{re} continues charging the capacitor C_{Ad} and makes the voltage u_{re} rise. It has the same direction with the positive reference, so $i_{\mathrm{re}} > 0$. After the voltage of C_{Ad} before the rectifier is higher than U_L the diodes return ON. Then the rectifier will enter mode II.
2) *Mode II:* Mode I happens when the rectifier conducts at the positive half cycle. After mode I, u_1 is higher than U_{L},

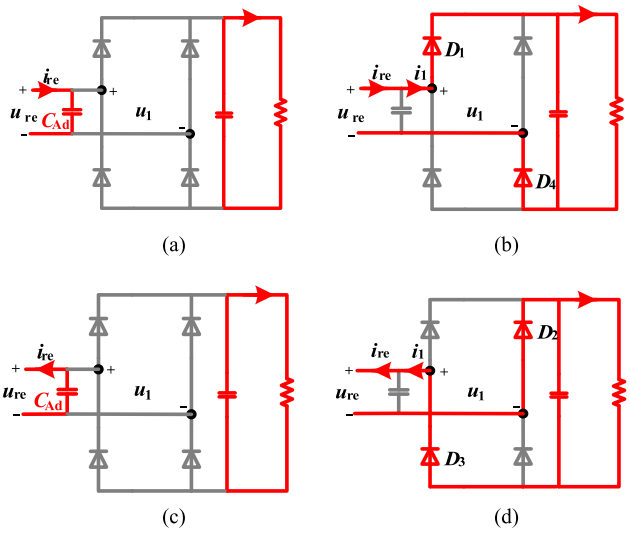

Fig. 7. Equivalent circuit models of the proposed improved rectifier topology over one cycle. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

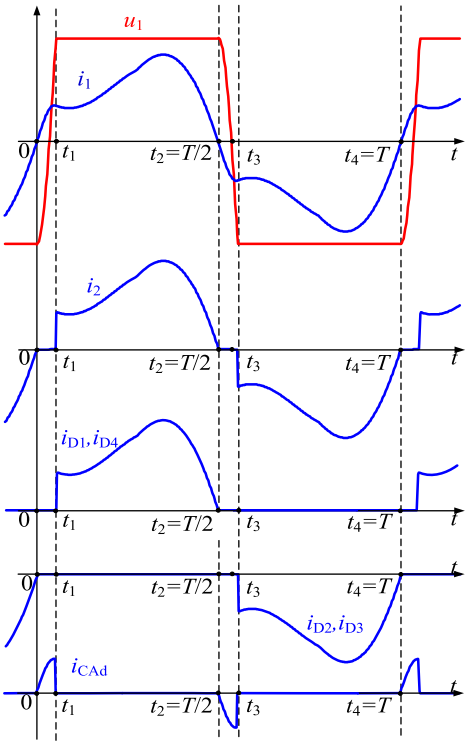

Fig. 8. Waveforms of the input voltage, input current, and diode current of the improved rectifier.

diodes D_1 and D_4 turn ON while D_2 and D_3 turn OFF, so $i_{D1} = i_{D4} > 0$. The equivalent circuit can be represented by Fig. 7(b), and the waveforms are shown in Fig. 8, at the time t_1- t_2. This mode only appears after the charging of C_{Ad} is completed.

3) *Mode III:* The equivalent circuit of mode III is shown in Fig. 7(c), the waveforms are shown in Fig. 8 when $t = t_2 - t_3$. Its process and analysis are similar to mode I, so it is omitted here.

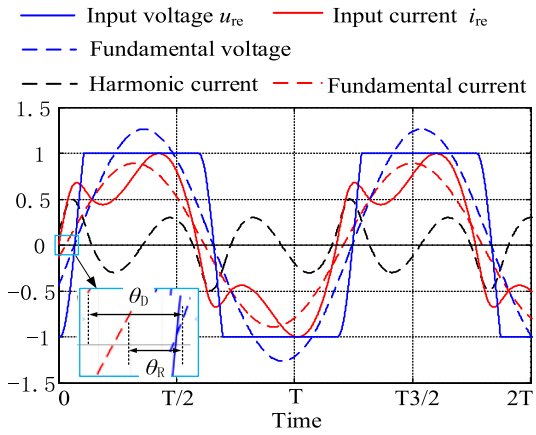

Fig. 9. Fundamental and harmonic wave decomposition diagram of the input current of the improved rectifier.

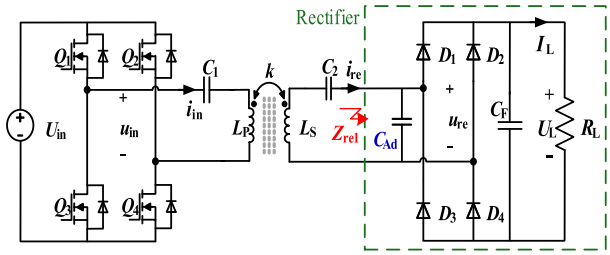

Fig. 10. Typical schematic of S/S compensation topology with improved rectifier.

4) *Mode IV:* In mode IV, the rectifier conducts at the negative half cycle, as shown in Fig. 7(d), at the time of $t_3 - t_4$ in Fig. 8. This mode is symmetrical with mode II.

Fig. 9 is the fundamental and harmonic wave decomposition diagram of the input current of the improved rectifier. When $t = 0$, $I_{\mathrm{re}} = 0$. According to energy conservation and theory of two-port network, formula (9) is obtained. Where, θ_D and θ_R are the phase angle of the input voltage ahead of input current and fundamental current respectively. And u_{in1}, u_{re1} and i_{in1} represent the fundamental wave of the input voltage u_{in}, the output voltage u_{re} and the output current i_{re}, c0 and d0 are the parameters of the transmission matrix shown in (10). In the two modes shown in Fig. 7(a) and (c), the input voltage and current of the rectifier satisfy (11). The values of θ_R and U_o can be obtained by iteratively solving

$$\begin{cases} I_{h0} + I_{\mathrm{o\_top}} \sin(\theta_D - \theta_R) = 0 \\ \frac{2}{\pi} U_o I_{\mathrm{o\_top}} \cos(\theta_R) = \frac{{U_o}^2}{R_L} \\ u_{\mathrm{in1}} = i_{\mathrm{re1}} c_1 + u_{\mathrm{re1}} d_1 \end{cases} \tag{9}$$

$$\begin{bmatrix} i_{\mathrm{in1}} \\ u_{\mathrm{in1}} \end{bmatrix} = \begin{bmatrix} a_1 & b_1 \\ c_1 & d_1 \end{bmatrix} \begin{bmatrix} i_{\mathrm{re1}} \\ u_{\mathrm{re1}} \end{bmatrix} \tag{10}$$

$$u_{\mathrm{re}} = \frac{1}{C_{\mathrm{Ad}}} \int i_{\mathrm{re}}. \tag{11}$$

Fig. 10 is the typical schematic of S/S compensation topology with improved rectifier. The circuit parameters are given in Table I. Formulas according to (9), (10) and (11), the calculations of

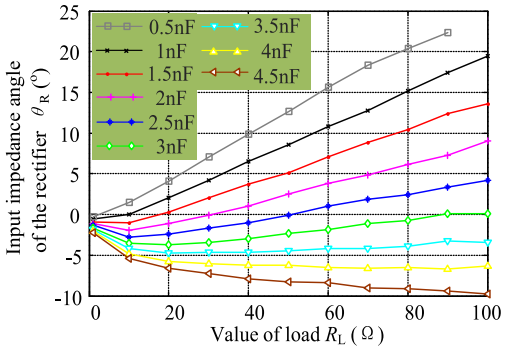

Fig. 11. Curves of the impedance angle of the rectifier varying with the load under different values of C_{Ad}.

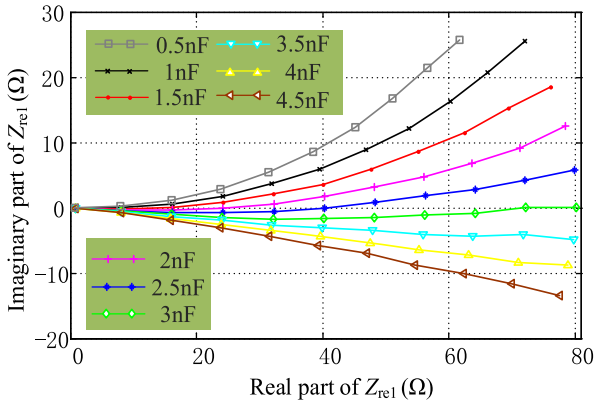

Fig. 12. Complex of the input impedance Z_{re1} of the rectifier varying with the load under different values of inductance C_{Ad}.

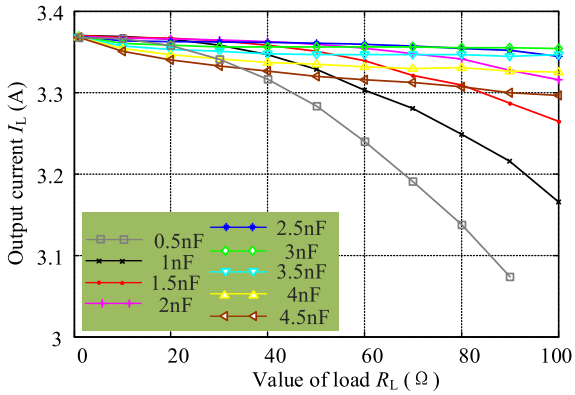

Fig. 13. Output current varying with load under different values of capacitance C_{Ad}.

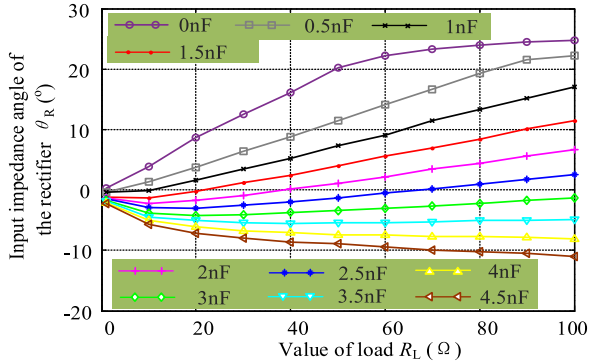

Fig. 14. Simulation of relationship between the impedance angle and value of load when C_{Ad} changes from 0 to 4.5 nF.

the impedance angle of the rectifier varying with the load under different values of capacitance C_{Ad} are shown in Fig. 11. Under the same load condition, the larger the value of C_{Ad}, the smaller the θ_{R}. When $C_{\mathrm{Ad}} = 2.5$ nF, the value of θ_{R} is near 0. When the load resistance is 100 Ω, the impedance angle of the rectifier reaches the largest range. In most studies, the input impedance of the rectifier Z_{re1} is usually approximated as (12). But, it is only satisfied when the load resistance is relatively small. Fig. 12 shows the real part and imaginary part of the input impedance of the rectifier Z_{re1} varying with the load under different values of C_{Ad}. The imaginary part of Z_{re1} does not equal to zero, which is different from (12). When C_{Ad} is between 2.5 and 3.5 nF, Z_{re1} is almost resistive. The output current varying with load under different values of capacitance C_{Ad} by calculated is shown in Fig. 13. With the increase of C_{Ad}, the fluctuation of output current decreases first and then increases

$$Z_{\mathrm{re1}} = \frac{8R_{\mathrm{L}}}{\pi^2}. \tag{12}$$

The compensation parameters are designed through formula (8). The relationship between the input impedance of the system Z_{in} and the input impedance of the rectifier Z_{e1} is shown in (13). If Z_{e1} is inductive, Z_{in} is capacitive. On the contrary, if Z_{e1} is capacitive, Z_{in} is inductive. When C_{Ad} is smaller than 3 nF, the ZVS of the inverter cannot be achieved under 100-Ω load condition. Therefore, the compensation parameters of the system need to be adjusted. According to the design of references, increasing the value of C_1 is a good choice [10]

$$Z_{\mathrm{in}} = \frac{(\omega M)^2}{Z_{\mathrm{re1}}}. \tag{13}$$

IV. Simulated Verification

In this section, two simulation models based on constant current output S/S and *LCC/LCC* compensation topologies are built through EDA software PSIM, then the corresponding parameters are designed. The simulation results strongly verify the validity of the proposed improved rectifier. A typical IPT system based on S/S compensation topology with improved rectifier is shown in Fig. 10, u_{re} and i_{re} represent the input voltage and input current of rectifier, respectively. The simulated circuit parameters are given in Table I.

The simulation result of relationship between the impedance angle of the rectifier θ_R and value of load R_L when C_{Ad} changes from 0 to 4.5 nF is illustrated in Fig. 14. The simulation results are basically consistent with the calculation results in Fig. 11. The slight difference is caused by the voltage fluctuation, voltage drop of the diode and the parasitic parameters of the circuit.

It can be seen clearly that for a traditional rectifier ($C_{\mathrm{Ad}} = 0$), when R_{L} increases, θ_R increases obviously. However, using an auxiliary capacitor C_{Ad} can significantly reduce θ_R, making θ_R close to even lower than zero. What's more, it must be

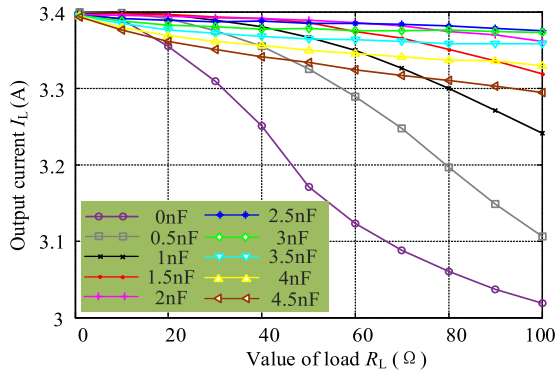

Fig. 15. Output current with value of load increasing when C_{Ad} changes from 0 to 4.5 nF by simulation.

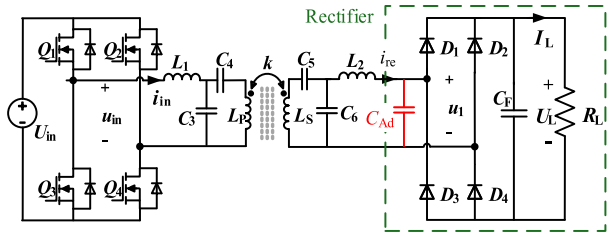

Fig. 16. Typical schematic of LCC/LCC compensation topology with improved rectifier.

noted that the value of C_{Ad} is not the bigger the better, since the input impedance will become capacitive, introducing more reactive power if C_{Ad} is larger than 3.0 nF. The comparison of the constant output current properties when C_{Ad} goes from 0 to 4.5 nF under different load conditions is showed in Fig. 15. The simulation results of the output current are basically consistent with the calculation results.

According to Fig. 15, it is known that output current I_L decreases with the increase of load. However, if the value of C_{Ad} is appropriate, the constant current output property of the rectifier can be kept. When $C_{Ad} = 2.5$ nF, the load-independent output property of the improved rectifier is the best.

The simulation circuit model of a typical *LCC/LCC* compensation topology is shown in Fig. 16. The circuit parameters are given in Table II. According to formula (7), the critical resistance R_{LC} of this *LCC/LCC* compensation topology is smaller. Therefore, although the parameters of the loosely coupled transformers and output current of the two compensation topologies are the same, the rectifier of the system with *LCC/LCC* compensation topology is easier to enter DCM and needs larger value of C_{Ad}.

The simulation result of relationship between the input impedance angle of the rectifier θ_R and value of load R_L when C_{Ad} changes from 0 to 12 nF is illustrated in Fig. 17. When $C_{Ad} = 0$ nF, θ_R first increases with the increase of the load resistance, then it reaches 25° and remains unchanged. When $C_{Ad} = 8$ nF, θ_R is closest to zero. The comparison of the constant output current properties when C_{Ad} goes from 0 to 12 nF under different load conditions is showed in Fig. 18. When $C_{Ad} = 6$ nF, the fluctuation of the output current is the smallest.

TABLE II
PARAMETERS OF SIMULATED CIRCUIT WITH *LCC/LCC* COMPENSATION TOPOLOGY

Parameters	*Value*
U_{in}	56 V
f	85k
L_P	58.8 μH
L_S	58.5 μH
k	0.43
L_1	25.2 μH
C_3	139.0 nF
C_4	104.4 nF
C_5	105.3 nF
C_6	139.0 nF
L_2	25.2 μH
U_L	3.4 A
R_L	1-100 Ω

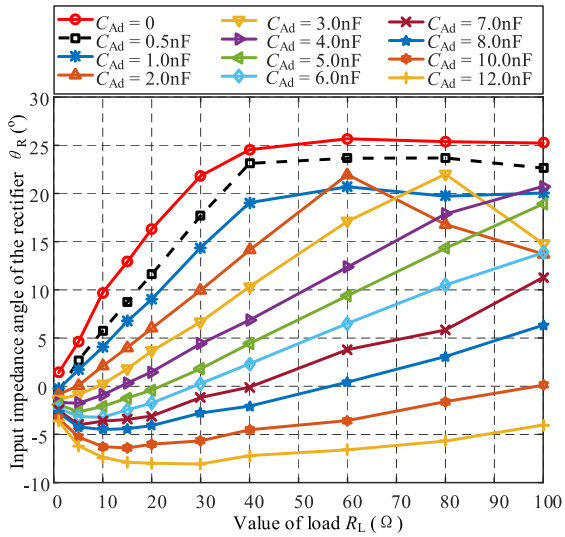

Fig. 17. Relationship between the input impedance angle and value of load when C_{Ad} changes from 0 to 12 nF.

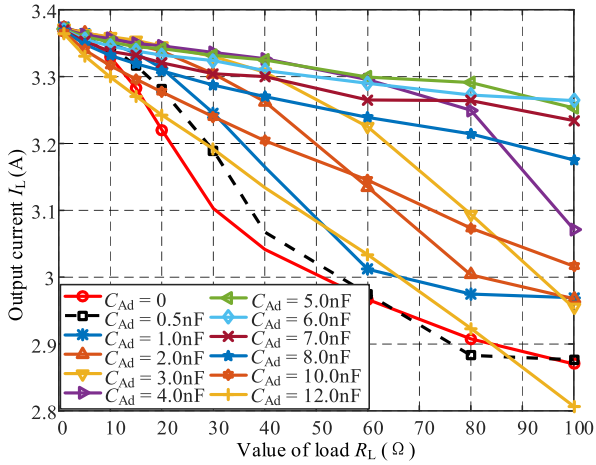

Fig. 18. Output current with value of load increasing when C_{Ad} changes from 0 to 12 nF.

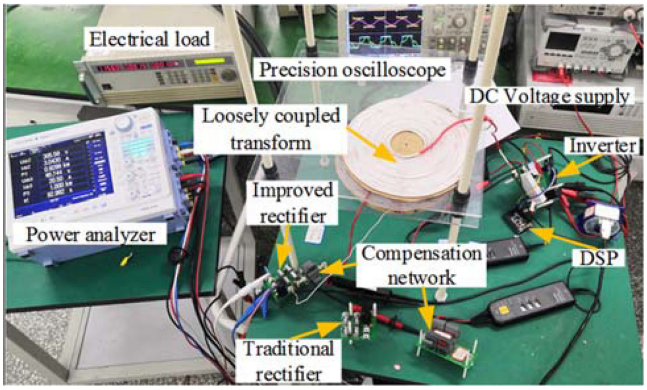

Fig. 19. Experimental prototype of the IPT system.

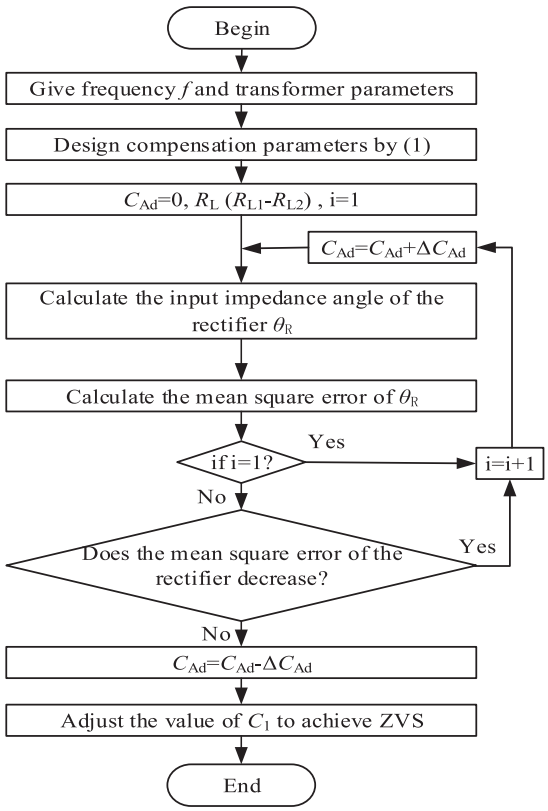

Fig. 20. Parameter design process.

V. Experimental Analysis

The prototype with S/S compensation topology is shown in Fig. 19. The rated power of the improved rectifier is 1000 W, with 56-V dc input voltage and 3.3-A constant dc output current.

Fig. 20 shows the flow chart of parameter design. The compensation parameters and value of C_{Ad} can be calculated from the chart. For the traditional rectifier with C filter, considering the realization of ZVS of power MOSFETs in full load range, the value of C_1 should be larger than calculation by (8). Besides, the fluctuation of output current I_{L} should be minimized when choosing the value of C_1. Through analysis of simulation results and numerical solutions, the value of C_1 is designed to be 62.5 nF. However, for the improved rectifier, C_1 can easily equal to the

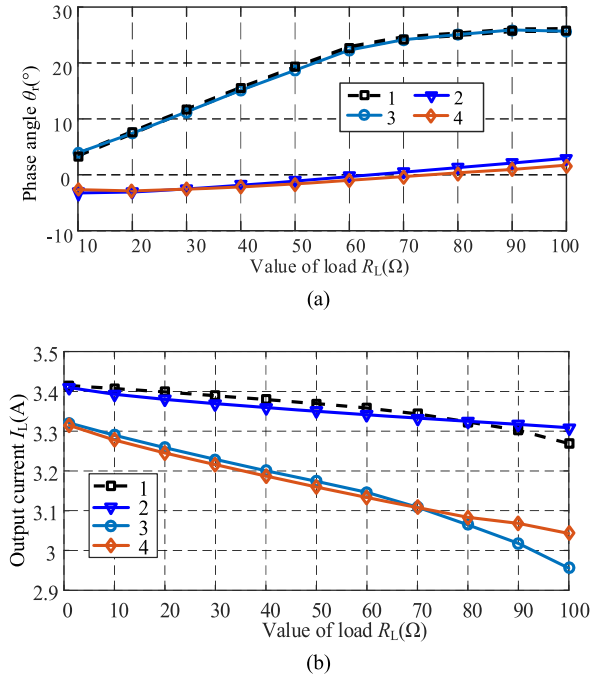

Fig. 21. Experimental and simulation results of the IPT system. (a) Input phase angle. (b) Output current for traditional and proposed improved rectify topologies against RL. 1: Simulation result with $C_{\mathrm{Ad}} = 50$ pF. 2: Simulation result with $C_{\mathrm{Ad}} = 2.5$ nF. 3: Experimental result with $C_{\mathrm{Ad}} = 0.4$: Experimental result with $C_{\mathrm{Ad}} = 2.48$ nF.

calculation, which greatly reduces the complexity of designing. In the improved system, C_1 is equal to 60.34 nF. Considering both the input impedance angle and the output characteristic, the C_{Ad} is 2.5 nF. Due to the tolerance of capacitance, the experimental value is 2.48 nF. Other parameters are the same as in Table I. The parameter design process of other compensation topologies is basically the same as Fig. 20.

Considering the junction capacitance of the chosen diode is about 50 pF, a 50-pF capacitor is paralleled before the rectifier to simulate the actual traditional rectifier. Fig. 21(a) shows the phase angle θ_{R} between the voltage u_{re} and the current i_{re} for both of the two investigated topologies as the load R_L is deliberately varied. The comparative experiment result shows the proposed improved rectifier can effectively reduce the impedance angle. According to Fig. 21(a), the simulation results are consistent with the experimental results. From Fig. 21(b), the output current of improved rectifier is higher than traditional rectifier under heavy load condition, indicating the output properties are significantly enhanced. Since the actual parameters are not completely consistent with the simulation parameters, there are some deviations between the experimental output current and the simulation, but they have the same trend and they can both prove the effectiveness of the proposed improved rectifier.

Fig. 22 shows the real part and imaginary part of the equivalent load impedance of the rectifier Z_{re1} to the fundamental wave. The larger the imaginary part is, the more reactive power transferred. Compared with traditional rectifier, the imaginary part of Z_{re1} of the improved rectifier is much smaller and close to zero, it means the reactive power is also smaller. Fig. 23 shows the peak value of

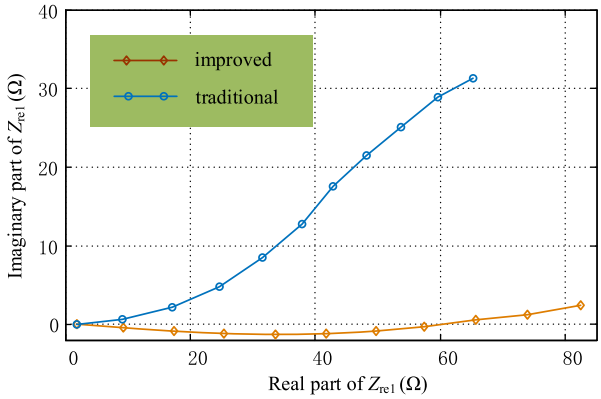

Fig. 22. Composition of complex impedance of the rectifier to fundamental wave.

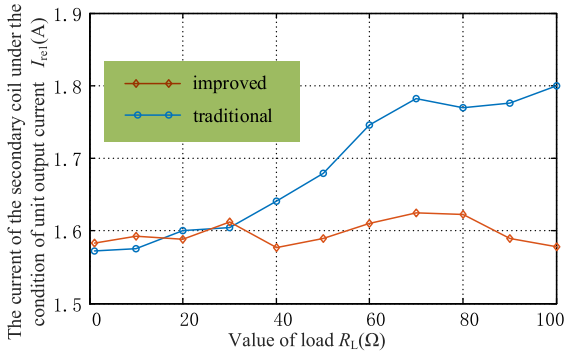

Fig. 23. Current of the secondary coil varying with load under the condition of unit output current.

the fundamental current of the secondary coil I_{re1} varying with load under the condition of unit output current. Under heavy load conditions, current of the secondary coil in the system with traditional rectifier is greater. The larger the load resistance, the greater the current difference. Larger coil current means greater loss and lower efficiency.

Fig. 24 depicts the experimental results of the transfer efficiency. Captures of efficiency from power analyzer at rated power of 1 kW are shown in Fig. 24(a) and Fig. 24(b). The dc–dc efficiency reaches 93% of the improved rectifier which is higher than 92.4% of the traditional rectifier. Fig. 24(c) shows the comparison of the dc–dc efficiency, it can be easily seen the efficiency has been significantly improved during the whole load range.

Fig. 25 describes the waveforms of the output u_{in} and i_{in} of the inverter and the input u_{re} and i_{re} of the different two rectifiers when $R_L = 100\ \Omega$. Positions of the voltages and currents are shown in Fig. 10. According to these figures, the ZVS condition for the MOSFETs is realized. Notably, there are duty loss and voltage distortion in traditional rectifier, resulting in higher harmonic components than improved topology. Therefore, the load range of the proposed topology is wider than traditional rectifier topology. In addition, phase shift happens obviously between the inverter voltage and current when the value of R_L is large. This means the increase of input impedance angle of the overall system and reactive power transferred by the system.

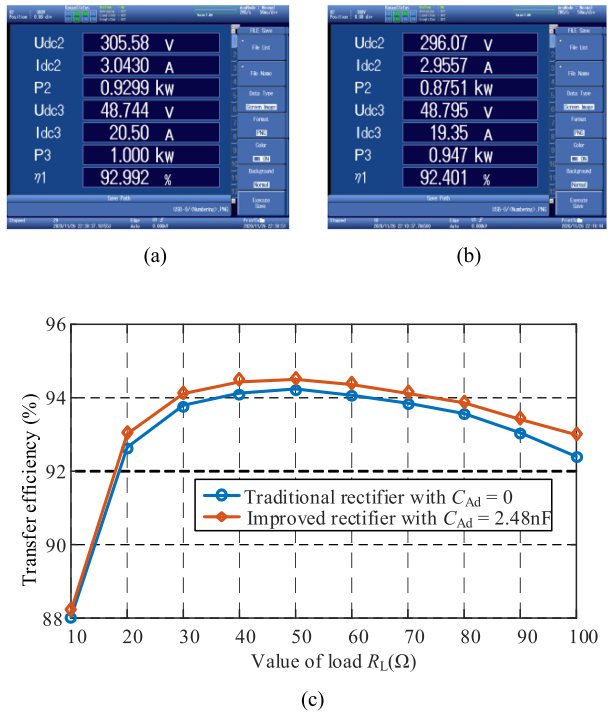

Fig. 24. DC–DC efficiency of the overall system. (a) Improved and (b) traditional rectifier. (c) Comparison in the whole range of load.

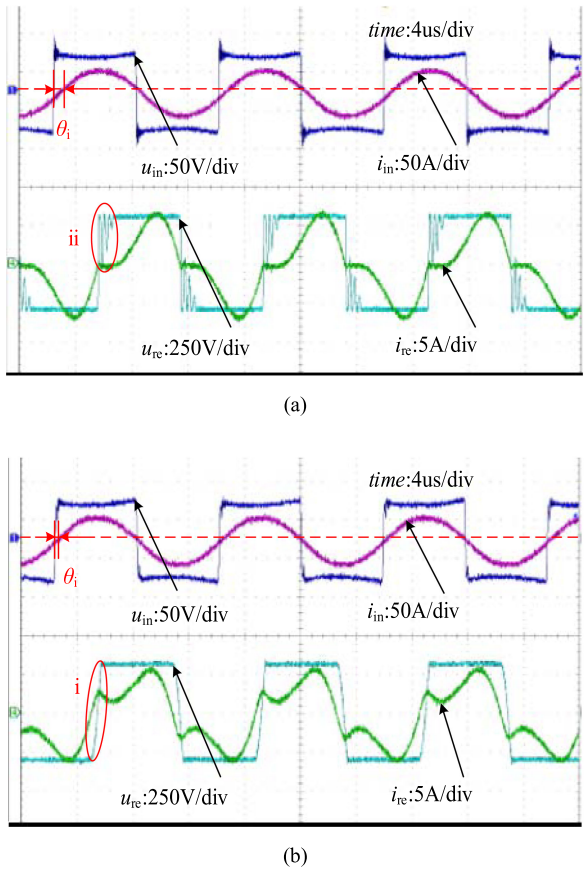

Fig. 25. Waveforms of the inverter and rectifier with two topologies and input phase angle. Waveforms of (a) improved and (b) traditional rectifier. (i) No voltage distortion. (ii) Duty loss and voltage distortion.

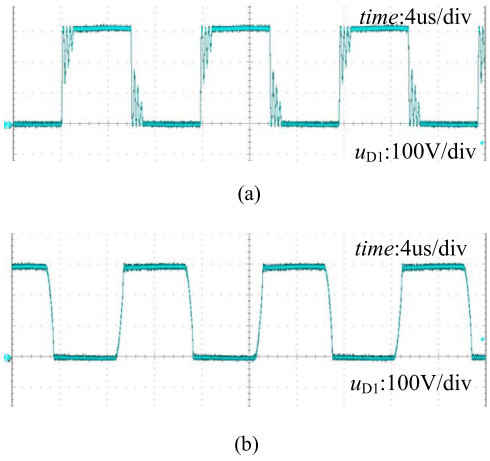

Fig. 26. Waveforms of the voltage on diode D_1 in different rectifiers. (a) Traditional rectifier. (b) Improved rectifier.

The improved rectifier transmits more active power at the same power level. For example, the output power of proposed topology is 0.93 kW while the traditional topology is only 0.875 kW when $R_{\mathrm{L}} = 100\ \Omega$.

The waveforms of the voltage on diode D_1 in the traditional and improved rectifiers is shown in Fig. 26, which is consistent with u_{re} in Fig. 25.

VI. Conclusion

As the load resistance increases, the input impedance angle of the rectifier also increases and finally reaches to 25°. This problem will increase reactive power and output fluctuations of the system. Besides, it will also affect the realization of ZVS. The key reason of the above problem is the increase of the ratio of the harmonic content introduced by the rectifier to the system fundamental wave. This article proposes a solution to the rectifier entering DCM. A very tiny capacitor is connected in parallel on the front side of the rectifier to change its working modes, thereby greatly reducing the variation of the input impedance angle of the rectifier. The analysis and calculation methods of the input impedance of the rectifier are also given. At a small price, it not only improves system efficiency but also reduces output current fluctuations. The excellent performance of the proposed improved rectifier is proved through simulation and experiment. Two 1-kW prototypes based on proposed improved rectifier and traditional rectifier were built respectively. The dc–dc efficiency of the improved topology is 93% at rated load, which is 0.6% higher than the traditional rectifier. The maximum efficiency of the proposed system can reach as high as 94.5%.

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