Enabling Resonant Commutated Pole in Parallel Power FET Bridge Legs

Yanfeng Shen, *Member, IEEE*, Yunlei Jiang, *Student Member, IEEE*, Hui Zhao, *Member, IEEE*, and Teng Long, *Member, IEEE*

***Abstract*—To meet the requirements of higher current ratings and lower thermal impedances, paralleling power field-effect transistor (FET) discretes or modules is often a cost-effective or even an unavoidable solution. While paralleling FETs allows for a significant reduction in conduction loss, the switching loss is increased in hard-switching applications. This article proposes a generic soft-switching modulation scheme for parallel power FET bridge legs. Part of the paralleled FET legs is chosen as an auxiliary leg that is turned ON prior to the remaining main legs. A resonant commutated pole (RCP) mode is then created, which enables the high-side FET of the auxiliary leg to achieve zero-current switching (ZCS) or quasi-ZCS and the remaining FETs to achieve zero-voltage switching. Thus, we can significantly reduce the switching loss that normally dominates the total power loss of high-frequency hard-switching converters particularly at partial and light loads. Experimental results from three parallel GaN high-electron-mobility transistor legs validate the effectiveness of this RCP-enabled solution in reducing switching losses and improving power conversion efficiencies. This article is accompanied by supplementary JIF and PDF files demonstrating the operational details of the RCP mode.**

***Index Terms*—Parallel power field-effect transistors (FETs), zero-voltage switching (ZVS), zero-current switching (ZCS), resonant commutated pole (RCP).**

I. Introduction

PARALLELING power transistor discretes is often a cost-effective or even an unavoidable solution for high-power electronics converters due to current rating availability, thermal restriction, and packaging price [1]–[4]. Bipolar transistors, e.g., insulated-gate bipolar transistor (IGBTs), feature forward voltages. Paralleling IGBTs, even if the current is equally shared, only has a limited influence on the efficiency [5]. By contrast, unipolar field-effect transistors (FETs), e.g., Si/SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) and GaN high-electron-mobility transistors (HEMTs[1]), are characterized by channel resistances. Thus, paralleling FETs can lead to a remarkable reduction in channel resistance and, therefore, to an equal reduction in conduction loss [5]. Also, the parallel operation distributes the thermal stress and lowers the junction temperature. Due to the positive temperature coefficient of FETs [6], the ON-state resistance can be further reduced, bringing more efficiency improvements.

For parallel power FETs, there are many inevitable differences in static and dynamic electrical parameters, e.g., the drain–source ON-state resistance, threshold voltage, gate resistance, and transconductance [7]–[14]. In addition, the layout symmetry may not be always achieved due to space constraint. These differences and asymmetries cause missharing of currents and staggered turn-ON/-OFF between parallel devices. Consequently, the paralleled FETs suffer from different switching/conduction losses and thermal stresses.

To achieve better current sharing among parallel transistors, many approaches have been proposed, including active [11], [15], [16], passive [4], [12]–[14], [17]–[20], and layout symmetrization methods [8], [21], [22]. However, under the premise of absolute layout symmetry guaranteed, current misharing may still occur due to the parameter mismatches of the paralleled transistors. For the active current sharing methods, high-bandwidth current sensing circuits and active gate drivers are necessary, and therefore, the implementation complexity is relatively high. By comparison, the passive current sharing approaches feature simplicity in implementation and high robustness in operation. Particularly, adding small inductors to the ac side of parallel FET bridge legs begins to prevail [12], [17]–[19], [23].

Though better current sharing performance can be achieved with the above solutions, the paralleled FETs still suffer from high switching losses when applied to high-frequency (e.g., above 50 kHz) hard-switching topologies. This issue is particularly pronounced at partial loads, where, typically, the switching loss dominates the total power loss [19], [24], [25]. Therefore, it becomes more prominent to develop a solution, which can reduce the partial-load switching loss as well as improve current sharing at high currents.

The most direct approach of reducing switching losses is to improve the switching speed by using wide-bandgap (WBG)

Manuscript received December 13, 2020; revised April 1, 2021; accepted May 17, 2021. Date of publication June 1, 2021; date of current version August 16, 2021. This work was supported in part by the U.K. Engineering and Physical Sciences Research Council under Grant EP/T02030X and in part by the Shanghai Automotive Industry Corporation. Recommended for publication by Associate Editor J. Wang. *(Corresponding author: Teng Long.)*

Yanfeng Shen was with the Electrical Engineering Division, Department of Engineering, University of Cambridge, CB3 0FA Cambridge, U.K. He is now with Danfoss Silicon Power R&D Munich, 85737 Ismaning, Germany (e-mail: ys523@cantab.ac.uk).

Yunlei Jiang, Hui Zhao, and Teng Long are with the Electrical Engineering Division, Department of Engineering, University of Cambridge, CB3 0FA Cambridge, U.K. (e-mail: yj306@cam.ac.uk; hz352@cam.ac.uk; tl322@cam.ac.uk).

This article has supplementary material provided by the authors and color versions of one or more figures available at https://doi.org/10.1109/TPEL.2021.3085558.

Digital Object Identifier 10.1109/TPEL.2021.3085558

[1]The HEMT is also referred to as a heterostructure FET or modulation-doped FET.

FETs, lowering gate resistances, and enhancing peak gate drive currents. However, faster switching will inevitably increase the turn-OFF drain–source voltage overshoot, the crosstalk, and the electromagnetic interference (EMI) [26]. Therefore, in practice, the switching speed of power FETs has to be limited.

Soft switching enables power FETs to have both reduced switching losses and lower voltage overshoots. There are two main types of soft switching: zero-voltage switching (ZVS) and zero-current switching (ZCS). The ZVS or ZCS of basic half-bridge (HB) legs can be achieved by introducing auxiliary circuits to the dc or ac side [25], [27]–[29]. With the aid of an auxiliary resonant network on the dc link, the modified topologies in [25] and [27], i.e., the resonant dc-link converters with and without active clamping, enable the main and auxiliary switches to achieve ZVS. The main issue with these resonant dc-link topologies is that the voltage stress of main switches is 10–150% higher than the dc-link voltage; thus, the converter loop inductance must be dedicatedly designed in order to suppress the turn-OFF voltage overshoots. By contrast, the auxiliary resonant commutated pole (ARCP) converters [28], [29] enable soft switching by adding auxiliary resonant circuits to the ac side (midpoints) of HB legs. However, the count of auxiliary components, including switches and passive components, is relatively high, particularly for multiphase systems.

In addition, the soft-switching conditions of basic HB legs can also be created by varying the switching frequency and operating in the triangular current mode (TCM) [30]–[32], which enables all power FETs to achieve ZVS without auxiliary switches. However, the switching frequency variation is relatively large, depending on the load and the output voltage; thus, the EMI filter design and the digital control become more complicated [33]. In addition, to support the TCM operation within a reasonable switching frequency range, the output filter inductance is typically on the order of several tens or hundreds of microhenries [30], [34], [35], which is relatively large and is typically not desirable in inductive load applications (e.g., motor drives) due to additional power loss, cost, and volume [23], [36]. Furthermore, as outlined in [37], the required large high-frequency current ripple leads to increased inductor and conduction losses, which reduce the gain of soft switching resulting from the TCM [38]. Therefore, the TCM soft-switching technique may not be superior to the conventional continuous conduction mode (CCM) operation, particularly at high load currents [37]. Though ZVS can be achieved for all parallel power FETs with the quadrilateral conduction mode (QCM) [39], their rms currents are significantly increased. In order to reduce the partial-load switching loss as well as to maintain better current sharing among parallel FETs, a desynchronized modulation scheme is proposed in [19]. However, only part of the paralleled FETs can achieve ZVS, whereas the remaining transistors are still hard switched.

This article proposes a resonant commutated pole (RCP)-enabled modulation scheme that allows parallel power FETs to achieve ZVS and ZCS. Thus, this new scheme can significantly reduce the switching loss that dominates the total power loss of high-frequency hard-switching converters, particularly at partial loads. As the load increases, the conduction loss may outweigh the hard-switching loss; in this case, the power conversion is more efficient by switching the RCP mode back to the conventional hard-switching synchronous CCM. The compatibility of both the RCP mode and the synchronous CCM allows the paralleled power FET legs to maintain high efficiencies over the full load range. It is noted that the number of power FETs in parallel is determined by the synchronous CCM at the full load, where all FETs act as main switches; thus, in order to activate the RCP mode at partial loads, no extra switches are required, but small differential-mode (DM) inductors are added to the midpoints of parallel bridge legs. These DM inductors can be part of the output filter inductor and also enable better current sharing among the paralleled FETs than the conventional direct paralleling.

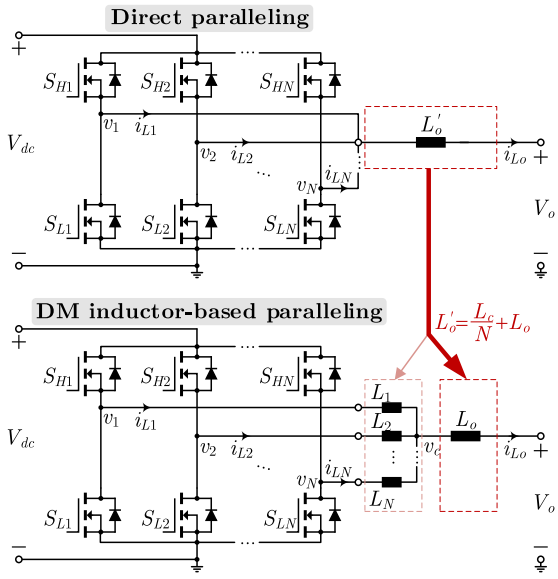

Fig. 1. Structure of DM-inductor-based parallel power FET HB legs. In unidirectional power flow applications, the high-side or low-side FETs can be replaced with diodes to form parallel bridgeless legs. The small DM inductors L_1, L_2,..., L_N can be either uncoupled [17], [19] or inversely coupled [12], [17], [18], [23].

II. Operating Principle in the RCP Mode

A. DM-Inductor-Based Paralleling Structure

The structures of direct paralleling and DM-inductor-based paralleling of power FET bridge legs are shown in Fig. 1. The DM inductors are connected to the midpoints of the paralleled bridge legs, and they are of much lower inductance than the output filter inductance, i.e., $L_1 = L_2 = \cdots = L_N = L_c \ll L_o$. These small DM inductors can be either uncoupled [17], [19] or coupled [12], [17], [18], [23] in implementation.

In contrast with the direct parallel, the addition of the DM inductors brings the following merits:

1) better dynamic current sharing performance among parallel transistors when operating in the synchronous mode [17], [19];
2) reduced dv_c/dt for better electromagnetic compatibility [23];

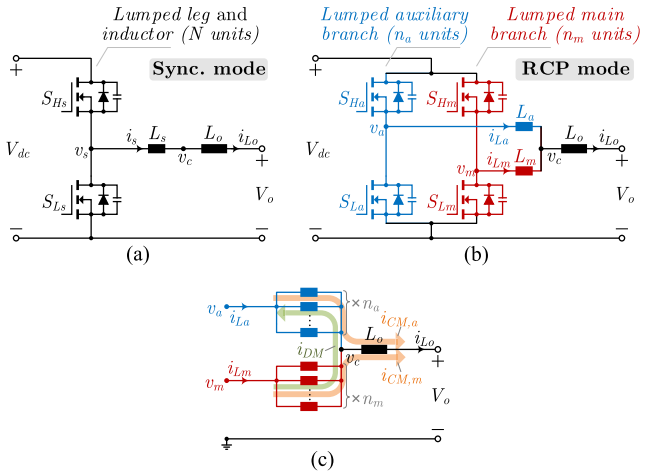

Fig. 2. Equivalent circuits in the conventional synchronous mode and the proposed RCP mode. (a) Equivalent circuit in the synchronous mode with all parallel bridge legs lumped into one. (b) Equivalent circuit in the RCP mode with all auxiliary bridge legs lumped into one and the remaining bridge legs (main legs) combined into another. (c) Definitions of the main CM current $i_{\mathrm{CM},m}$ and the auxiliary CM current $i_{\mathrm{CM},a}$ and the DM current i_{DM}.

3) enabling an inherent RCP mode to significantly lower the switching losses, as proposed and analyzed in this study.

The operating principle and advantages of the DM-inductor-based paralleling structure operating in the synchronous mode have been discussed and experimentally verified in [19]. In this article, a novel RCP operation mode is proposed in order to enable all parallel transistors to achieve soft switching. It should be noted that the proposed RCP mode also applies to parallel bridgeless legs, where either the high-side or low-side power FETs in Fig. 1 are replaced with unidirectional diodes.

B. Switching Pattern in the RCP Mode

1) Lumping HB Legs: To simplify the operation analysis in the RCP mode, the N parallel HB legs are divided into two groups: the auxiliary legs and the main legs. The auxiliary group consists of n_a legs, e.g., S_{H1}-S_{L1}, S_{H2}-S_{L2},..., S_{Hna}-S_{Lna}, and the main group is comprised of the remaining n_m ($n_m = N - n_a$) legs, e.g., S_{Hna+1}-S_{Lna+1}, S_{Hna+2}-S_{Lna+2},..., S_{HN}-S_{LN}. The individual bridge legs inside the auxiliary or main groups are driven synchronously. The switch-node voltages inside the auxiliary or main groups remain the same as each other. Therefore, the synchronously parallel legs in the main group can be lumped into one; the same transformation can be performed to the auxiliary group. Accordingly, the equivalent topology of Fig. 1 can be obtained, as shown in Fig. 2(b).

The subscripts "$_a$" and "$_m$" denote the *auxiliary* group and the *main* group, respectively. Meanwhile, the equivalent DM inductances of the auxiliary and main branches [see Fig. 2(b)] are obtained as

$$\begin{cases} L_a = \frac{L_c}{n_a} \\ L_m = \frac{L_c}{n_m}. \end{cases} \tag{1}$$

2) Switching Pattern: For the parallel HB legs operating in the synchronous CCM [see Figs. 1 and 2(a)], ZVS-ON can be inherently achieved for the low- and high-side switches in the forward and reverse current directions, respectively. For simplicity, this work only considers the forward current direction, where the low-side switches inherently achieve ZVS-ON and the high-side transistors are hard switched in the CCM.

To help the high-side transistors achieve soft switching, a novel RCP-enabled asynchronous modulation scheme is proposed, as shown in Fig. 3. The high- and low-side switches in the main lumped leg S_{Hm}–S_{Lm} are a complementary pair with deadtimes and they are duty cycle modulated. For the auxiliary leg, its high- and low-side FETs, i.e., S_{Ha} and S_{La}, act as a "preswitch" with respect to S_{Hm} and a "postswitch" with respect to S_{Lm}, respectively. Accordingly, the inductor current of the main leg i_{Lm} is forced to fall below 0, creating an RCP, before the main high-side FET S_{Hm} is turned ON; that is a ZVS-ON condition created for S_{Hm} before T_2, as shown in Fig. 3. The auxiliary high-side switch, S_{Ha}, is turned ON under ZCS at T_0 with reduced switching-ON loss. On the other hand, S_{Ha} in the RCP mode turns OFF at a high current (see Fig. 3), and therefore, its switching-OFF loss is increased. Due to the fact that the turn-ON loss dominates the total switching loss for WBG power FETs, normally, the increased turn-OFF loss is not significant. It should also be noted that the gate signal of S_{La} during [t_{2e}, t_{3s}] is optional in theory, but is recommended in practice for conduction loss reduction.

C. Operating Principle

1) Basic Definitions and Assumptions: To facilitate analysis, the lumped inductor currents i_{Lm} and i_{La} are decoupled into a DM current i_{DM} and two common-mode (CM) currents $i_{\mathrm{CM},m}$ and $i_{\mathrm{CM},a}$, as shown in Fig. 2(c). By definition, the two lumped inductor current can be expressed as

$$\begin{cases} i_{Lm}(t) = i_{\mathrm{CM},m}(t) + i_{\mathrm{DM}}(t) \\ i_{La}(t) = i_{\mathrm{CM},a}(t) - i_{\mathrm{DM}}(t). \end{cases} \tag{2}$$

The output current i_{Lo} is the sum of the main and auxiliary CM currents, i.e.,

$$i_{Lo}(t) = i_{\mathrm{CM},m}(t) + i_{\mathrm{CM},a}(t). \tag{3}$$

Based on the superposition theorem, the two CM currents can be expressed as

$$\begin{cases} i_{\mathrm{CM},m}(t) = \frac{n_m}{n_m+n_a} i_{Lo}(t) = \frac{k}{1+k} i_{Lo}(t) \\ i_{\mathrm{CM},a}(t) = \frac{n_a}{n_m+n_a} i_{Lo}(t) = \frac{1}{1+k} i_{Lo}(t) \end{cases} \tag{4}$$

where the numbers ratio of main legs to auxiliary legs is defined as

$$k = \frac{n_m}{n_a} = \frac{L_a}{L_m}. \tag{5}$$

The common output voltage v_c is determined by both v_m and v_a. Applying the superposition theorem yields

$$v_c(t) = \frac{n_a v_a(t) + n_m v_m(t)}{n_m + n_a} = \frac{v_a(t) + k v_m(t)}{1+k}. \tag{6}$$

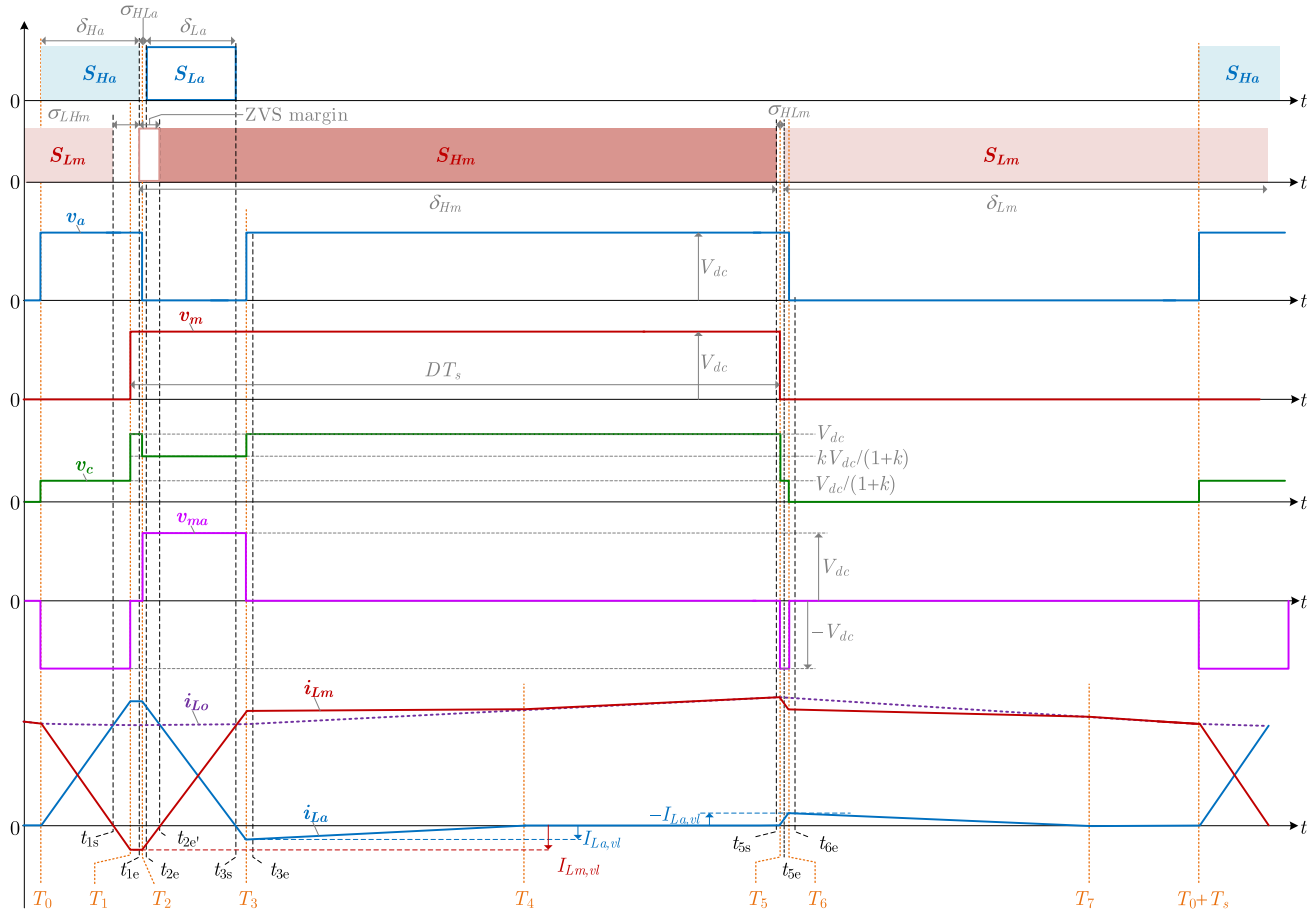

Fig. 3. Simplified operating waveforms of the parallel power FET HB legs [see Fig. 2(a)] in the proposed RCP mode.

The DM and output currents can be always described by the following differential equations:

$$\begin{cases} L_{\rm DM}\frac{{\rm d}i_{\rm DM}(t)}{{\rm d}t} = v_{ma}(t) = v_m(t) - v_a(t) \\ L_o\frac{{\rm d}i_{Lo}(t)}{{\rm d}t} = v_c(t) - V_o \end{cases} \tag{7}$$

where the DM inductance $L_{\rm DM} = L_m + L_a$, and v_{ma} represents the voltage difference between the main and auxiliary switch nodes.

D. Simplified Operation Principle

1) Applying a Linear FET Switching Model: The detailed operation principle and the mathematical model of the RCP mode are shown in the *supplementary material* of this article. The full mathematical model, however, is nonlinear, and there is no closed-form solution for the control variables. Therefore, a linear FET HB model [30], [40] is applied. With the linear model, the switch-node voltage of an HB leg jumps between 0 and $V_{\rm dc}$ with zero rise and fall time; the switch-node voltage remains unchanged until the parasitic output capacitances of the FET HB are injected or ejected charge of Q_{oss}. A comparison between SPICE simulations and the results with the linear FET HB model is shown in Fig. 6. Due to the high nonlinearity of the parasitic output capacitances of FETs with respect to the switch-node voltage, the real inductor currents i_{La} and i_{Lm} during the resonant transitions are close to the case using the linear FET model. The valley values of the main and auxiliary inductor currents are represented by $I_{Lm,vl}$ and $I_{La,vl}$, respectively; the equations for calculating the two valley currents are shown in the *supplementary material*.

Applying the linear FET model, each resonant stage in Fig. S1 (see the *supplementary material*) can be split into two substages that can further be merged with its adjacent nonresonant stages. The simplified waveforms are shown in Fig. 3, where only eight nonresonant stages remain within one switching cycle. The boundaries between these nonresonant stages are the eight time instants T_0, T_1,..., T_7, as illustrated in Fig. 3. The valley values of the main and auxiliary inductor currents are represented by $I_{Lm,vl}$ and $I_{La,vl}$, respectively; the equations for calculating the two valley currents are shown in the *supplementary material*.

Because the transition times during $[T_0, T_3]$ and $[T_5, T_6]$, are relatively short, and $L_o \gg L_c$, it is assumed that the load current i_{Lo} remain as constant as $I_{Lo,T0}$ and $I_{Lo,T5}$ during $[T_0, T_3]$ and $[T_5, T_6]$, respectively.

2) Analysis of Operation in Simplified Stages: The equations describing the switch-node voltages and inductor currents are obtained as follows.

Simplified Stage 1 $[T_0, T_1]$: Neglecting the voltage drops over transistors, the two switch-node voltages are obtained as

$$\begin{cases} v_m(t) = 0 \\ v_a(t) = V_{\rm dc}. \end{cases} \tag{8}$$

Then, the inductor currents can be obtained by solving the differential equations in (7)

$$\begin{cases} i_{Lo}(t) = I_{Lo,T0} \\ i_{Lm}(t) = I_{Lo,T0} - I_{La,T0} - \frac{V_{\rm dc}}{L_{\rm DM}}(t - T_0) \\ i_{La}(t) = I_{La,T0} + \frac{V_{\rm dc}}{L_{\rm DM}}(t - T_0) \end{cases} \tag{9}$$

where $I_{La,T0}$ denotes the initial current of i_{La} at T_0. If i_{La} falls to zero at $T_0 + T_s$ (i.e., $I_{La,T0} = 0$; see Fig. 3), then S_{Ha} achieves ZCS-ON at T_0; otherwise, $0 < I_{La,T0} < |I_{La,vl}|$ and S_{Ha} achieves quasi-ZCS-ON at T_0.

This stage terminates with $i_{Lm}(T_1) = I_{Lm,vl}$, and thus, the auxiliary control variable, i.e., ΔT_{01}, can be obtained as

$$\Delta T_{01} = \frac{L_{\rm DM}}{V_{\rm dc}}(I_{Lo,T0} - I_{Lm,vl} - I_{La,T0}). \tag{10}$$

Simplified Stage 2 $[T_1, T_2]$: The inductor current of main branch i_{Lm} reaches its valley value $I_{Lm,vl}$ at T_1, after which the switch-node voltage of main branch v_m jumps to $V_{\rm dc}$. Thus, both switch-node voltages are equal to $V_{\rm dc}$, keeping the DM current unchanged. Since the load current is assumed constant during this short interval, the main and auxiliary inductor currents also remain unchanged, as follows:

$$\begin{cases} v_m(t) = V_{\rm dc} \\ v_a(t) = V_{\rm dc} \end{cases} \tag{11}$$

$$\begin{cases} i_{Lo}(t) = I_{Lo,T0} \\ i_{Lm}(t) = I_{Lm,vl} \\ i_{La}(t) = I_{Lo,T0} - I_{Lm,vl}. \end{cases} \tag{12}$$

The integrals of i_{Lm} from T_1 to t_{1e} and i_{La} from t_{1e} to T_2 correspond to half of the charges of the main and auxiliary legs, i.e.,

$$\int_{T_1}^{t_{1e}} i_{Lm}(t){\rm d}t + \int_{t_{1e}}^{T_2} i_{La}(t){\rm d}t = n_m Q_{oss} + n_a Q_{oss}. \tag{13}$$

Solving (13) yields the time duration of this interval, ΔT_{12}:

$$\Delta T_{12} = \frac{n_m Q_{oss}}{-I_{Lm,vl}} + \frac{n_a Q_{oss}}{I_{Lo,T0} - I_{Lm,vl}} \approx \frac{n_m Q_{oss}}{-I_{Lm,vl}}. \tag{14}$$

Simplified Stage 3 $[T_2, T_3]$: The auxiliary switch-node voltage v_a jumps to 0 at T_2, whereas v_m remains at $V_{\rm dc}$. Thus, the positive voltage $V_{\rm dc}$ is applied to the DM inductance, causing i_{Lm} and i_{La} to linearly rise and fall, respectively:

$$\begin{cases} v_m(t) = V_{\rm dc} \\ v_a(t) = 0 \end{cases} \tag{15}$$

$$\begin{cases} i_{Lo}(t) = I_{Lo,T0} \\ i_{Lm}(t) = I_{Lm,vl} + \frac{V_{\rm dc}}{L_{\rm DM}}(t - T_2) \\ i_{La}(t) = I_{Lo,T0} - I_{Lm,vl} - \frac{V_{\rm dc}}{L_{\rm DM}}(t - T_2). \end{cases} \tag{16}$$

The time from T_2 to T_3 is denoted as ΔT_{23} and is obtained as

$$\Delta T_{23} = \frac{L_{\rm DM}}{V_{\rm dc}}(I_{Lo,T0} - I_{Lm,vl} - I_{La,vl}). \tag{17}$$

Simplified Stage 4 $[T_3, T_4]$: The auxiliary inductor current i_{La} falls to its valley value $I_{La,vl}$ at T_3, after which the auxiliary switch-node voltage v_a jumps to a high level. Thus, the auxiliary inductor current i_{La} begins increasing to 0, while the main inductor current i_{Lm} starts converging to the load current i_{Lo}. To accurately determine the elapsed time for i_{La} reaching 0 (i.e., i_{Lm} and i_{Lo} converge), the voltage drops over transistors cannot be neglected. Thus, the two switch-node voltages are expressed as

$$\begin{cases} v_m(t) = V_{\rm dc} - i_{La}\frac{R_{\rm on}}{n_m} \\ v_a(t) = V_{\rm dc} + V_f - i_{La}\frac{R_{\rm on}}{n_a} \end{cases} \tag{18}$$

where V_f represents the forward voltage drop of the body diode of a power FET, and R_{on} denotes the ON-state resistance of the transistor. Then, solving the differential equations in (7) yields the expressions for the inductor currents

$$\begin{cases} i_{Lo}(t) = I_{Lo,T0} + \frac{1}{L_o}(V_{\rm dc} - V_o)(t - T_3) \\ i_{Lm}(t) = \frac{kI_{Lo,T0}}{k+1} + \frac{k}{1+k}\frac{V_{\rm dc}-V_o}{L_o}(t - T_3) - \frac{V_f n_m}{R_{\rm on}(1+k)} \\ + \left(\frac{I_{Lo,T0}}{k+1} - I_{La,vl} + \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\exp\left(-\frac{R_{\rm on}(1+k)}{n_m L_{\rm DM}}(t - T_3)\right) \\ i_{La}(t) = \frac{I_{Lo,T0}}{k+1} + \frac{1}{1+k}\frac{V_{\rm dc}-V_o}{L_o}(t - T_3) + \frac{V_f n_m}{R_{\rm on}(1+k)} \\ - \left(\frac{I_{Lo,T0}}{k+1} - I_{La,vl} + \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\exp\left(-\frac{R_{\rm on}(1+k)}{n_m L_{\rm DM}}(t - T_3)\right). \end{cases} \tag{19}$$

It is noted that when the duty cycle is small, i_{La} may have not been reached 0 before v_m jumps to 0 at T_5. In this case, the two instants T_4 and T_5 overlap. For the time from T_3 to T_4, i.e., ΔT_{34}, its maximum can be derived by letting $i_{La} = 0$ in (19) as

$$\begin{aligned} \Delta T_{34,\max} = &-\left(\frac{I_{Lo,T0}}{k+1} + \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\frac{(1+k)L_o}{V_{\rm dc}-V_o} + \frac{n_m L_{\rm DM}}{R_{\rm on}(1+k)} \\ &\times {\rm W}_0\left(\begin{array}{l}\left(\frac{I_{Lo,T0}}{k+1} - I_{La,vl} + \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\frac{R_{\rm on}(1+k)}{n_m L_{\rm DM}}\frac{(1+k)L_o}{V_{\rm dc}-V_o} \\ \times \exp\left(\frac{R_{\rm on}(1+k)}{n_m L_{\rm DM}}\frac{(1+k)L_o}{V_{\rm dc}-V_o}\left(\frac{I_{Lo,T0}}{k+1} + \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\right)\end{array}\right) \end{aligned} \tag{20}$$

where ${\rm W}_0$ is the zeroth branch of the Lambert W function.

Then, the actual ΔT_{34} can be obtained as

$$\Delta T_{34} = \min\{\Delta T_{34,\max},\ \ (DT_s - \Delta T_{12} - \Delta T_{23})\}. \tag{21}$$

Simplified Stage 5 $[T_4, T_5]$: Typically, the negative auxiliary inductor current i_{La} reaches 0 at T_4, and it cannot further increases above 0 due to S_{Ha} is turned OFF. As a result, it is only the main branch (i.e., S_{Hm}) that conducts the load current. The switch-node voltages and inductor currents can be expressed as

$$\begin{cases} v_m(t) = V_{\rm dc} \\ v_a(t) \approx V_{\rm dc} \end{cases} \tag{22}$$

$$\begin{cases} i_{Lo}(t) = I_{Lo,T0} + \frac{1}{L_o}(V_{\rm dc} - V_o)(t - T_3) \\ i_{Lm}(t) = I_{Lo,T0} + \frac{1}{L_o}(V_{\rm dc} - V_o)(t - T_3) \\ i_{La}(t) = 0. \end{cases} \tag{23}$$

It is seen from Fig. 3 that the time ΔT_{45} can be expressed as

$$\Delta T_{45} = DT_s - \Delta T_{12} - \Delta T_{23} - \Delta T_{34}. \tag{24}$$

As mentioned before, i_{La} may have not been reached 0 before v_m jumps to 0 at T_5. In this case, the two instants T_4 and T_5 overlap, i.e., the time duration of *Simplified Stage 5* is 0. Still, ΔT_{45} can be expressed by (24).

Simplified Stage 6 $[T_5, T_6]$: The main switch-node voltage v_m jumps to 0 at T_5, whereas v_a remains at $V_{\rm dc}$. Thus, the negative voltage difference $v_{ma} = -V_{\rm dc}$ causes i_{Lm} and i_{La} to linearly decrease and increase, respectively:

$$\begin{cases} v_m(t) = 0 \\ v_a(t) = V_{\rm dc} \end{cases} \tag{25}$$

$$\begin{cases} i_{Lo}(t) = I_{Lo,T5} \\ i_{Lm}(t) = I_{Lo,T5} - I_{La,T5} - \frac{V_{\rm dc}}{L_{\rm DM}}(t - T_5) \\ i_{La}(t) = I_{La,T5} + \frac{V_{\rm dc}}{L_{\rm DM}}(t - T_5) \end{cases} \tag{26}$$

where $I_{La,T5}$ represents the current of i_{La} at T_5, and it can be obtained by substituting (21) into (19)

$$\begin{aligned} I_{La,T5} = {} & \frac{I_{Lo,T0}}{k+1} + \frac{1}{1+k}\frac{V_{\rm dc} - V_o}{L_o}\Delta T_{34} + \frac{V_f n_m}{R_{\rm on}(1+k)} \\ & - \left(\frac{I_{Lo,T0}}{k+1} - I_{La,vl} + \frac{V_f n_m}{R_{\rm on}(1+k)}\right) \\ & \times \exp\left(-\frac{R_{\rm on}(1+k)}{n_m L_{\rm DM}}\Delta T_{34}\right). \end{aligned} \tag{27}$$

For $I_{Lo,T5}$, it can be obtained from (19) and (23) that

$$I_{Lo,T5} = I_{Lo,T0} + \frac{1}{L_o}\left(V_{\rm dc} - V_o\right)\left(DT_s - \Delta T_{12} - \Delta T_{23}\right). \tag{28}$$

Thus, the main inductor current at T_5 is derived as

$$I_{Lm,T5} = I_{Lo,T5} - I_{La,T5}. \tag{29}$$

The integral of i_{La} from T_5 to T_6 corresponds to half of the charge of the auxiliary leg, i.e.,

$$\int_{T_5}^{T_6} i_{La}(t)\mathrm{d}t = n_a Q_{oss}. \tag{30}$$

Solving (30) yields the time duration of this interval, ΔT_{56}, as

$$\Delta T_{56} = \frac{L_{\rm DM}}{V_{\rm dc}}(-I_{La,vl} - I_{La,T5}). \tag{31}$$

Simplified Stage 7 $[T_6, T_7]$: At T_6, v_a jumps to a low voltage level (close to 0). Thus, the auxiliary inductor current i_{La} begins decreasing to 0, while the main inductor current i_{Lm} starts converging to the load current i_{Lo}. As with the simplified stage 4 $[T_3, T_4]$, the voltage drops over transistors cannot be neglected in order to accurately determine the elapsed time for i_{La} reaching 0 (i.e., i_{Lm} and i_{Lo} converge). Thus, the two switch-node voltages are expressed as

$$\begin{cases} v_m(t) = -i_{La}\frac{R_{\rm on}}{n_m} \\ v_a(t) = -V_f - i_{La}\frac{R_{\rm on}}{n_a}. \end{cases} \tag{32}$$

Combining (7) and (32) yields the time-domain expressions of inductor currents

$$\begin{cases} i_{Lo}(t) = I_{Lo,T5} - \frac{V_o}{L_o}(t - T_6) \\ i_{Lm}(t) = \frac{kI_{Lo,T5}}{k+1} - \frac{k}{1+k}\frac{V_o}{L_o}(t - T_6) + \frac{V_f n_m}{R_{\rm on}(1+k)} \\ \quad + \left(\frac{I_{Lo,T5}}{k+1} + I_{La,vl} - \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\exp\left(-\frac{R_{\rm on}(1+k)}{n_m L_{\rm DM}}(t - T_6)\right) \\ i_{La}(t) = \frac{I_{Lo,T5}}{k+1} - \frac{1}{1+k}\frac{V_o}{L_o}(t - T_6) - \frac{V_f n_m}{R_{\rm on}(1+k)} \\ \quad - \left(\frac{I_{Lo,T5}}{k+1} + I_{La,vl} - \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\exp\left(-\frac{R_{\rm on}(1+k)}{n_m L_{\rm DM}}(t - T_6)\right). \end{cases} \tag{33}$$

Similar with *Simplified Stage 4*, when the duty cycle is large, i_{La} may have not been fallen to 0 before v_a jumps to $V_{\rm dc}$ at $T_0 + T_s$ (i.e., T_0). In this case, the two instants T_7 and $T_0 + T_s$ overlap. For the time from T_6 to T_7, i.e., ΔT_{67}, its maximum can be derived by letting $i_{La} = 0$ in (33) as

$$\begin{aligned} \Delta T_{67,\max} = {} & \left(\frac{I_{Lo,T5}}{k+1} - \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\frac{(1+k)L_o}{V_o} + \frac{n_m L_{\rm DM}}{R_{\rm on}(1+k)} \\ & \times \mathrm{W}_0\left(\begin{matrix} -\left(\frac{I_{Lo,T5}}{k+1} + I_{La,vl} - \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\frac{R_{\rm on}(1+k)}{n_m L_{\rm DM}}\frac{(1+k)L_o}{V_o} \\ \times \exp\left(-\frac{R_{\rm on}(1+k)}{n_m L_{\rm DM}}\frac{(1+k)L_o}{V_o}\left(\frac{I_{Lo,T5}}{k+1} - \frac{V_f n_m}{R_{\rm on}(1+k)}\right)\right) \end{matrix}\right). \end{aligned} \tag{34}$$

The actual ΔT_{67} is obtained as

$$\Delta T_{67} = \min\{\Delta T_{67,\max},\ \ ((1-D)T_s - \Delta T_{56} - \Delta T_{01})\}. \tag{35}$$

Simplified Stage 8 $[T_7, T_0 + T_s)$: At T_7, i_{La} falls to 0, and it cannot further decrease below 0 because S_{La} is kept OFF. Therefore, in this stage, the load current is fully shared by the main branch (i.e., S_{Lm} and L_m). The switch-node voltages and inductor currents are described by

$$\begin{cases} v_m(t) = 0 \\ v_a(t) \approx 0 \end{cases} \tag{36}$$

$$\begin{cases} i_{Lo}(t) = I_{Lo,T5} - \frac{V_o}{L_o}(t - T_6) \\ i_{Lm}(t) = I_{Lo,T5} - \frac{V_o}{L_o}(t - T_6) \\ i_{La}(t) = 0. \end{cases} \tag{37}$$

Clearly, the time duration for *Simplified Stage 8* can be obtained as

$$\Delta T_{78} = (1-D)T_s - \Delta T_{56} - \Delta T_{67} - \Delta T_{01}. \tag{38}$$

As with *Simplified Stage 5*, the time duration of *Simplified Stage 8* will be 0 if i_{La} has not been fallen to 0 before v_a jumps to $V_{\rm dc}$ at $T_0 + T_s$ (i.e., T_0). In this case, (38) is still valid.

E. Determination of Modulation Parameters

Typically, the initial inductor current of auxiliary branch is equal to 0, i.e., $I_{La,T0} = 0$; thus, the auxiliary high-side switch S_{Ha} is able to achieve ZCS-ON. When the duty cycle is large enough, a small positive initial current $I_{La,T0}$ ($0 < I_{La,T0} < |I_{La,vl}|$) may occur. Nevertheless, compared with the load current i_{Lo}, the auxiliary valley current $|I_{La,vl}|$ is small, and even so is $I_{La,T0}$. In this case, the auxiliary high-side switch S_{Ha} achieves quasi-ZCS-ON. It is noted that this small $I_{La,T0}$ has a negligible impact on the characterization of load current i_{Lo}. Hence, in the first step, it is assumed that $I_{La,T0} = 0$. When the

TABLE I
EQUATIONS TO DETERMINE THE TIMING PARAMETERS IN THE RCP MODE

Timing parameters	Equations
Gate pulse width of S_{Ha}	$\delta_{Ha} = \Delta T_{01} + \frac{n_m Q_{oss}}{-I_{Lm,vl}}$
Gate pulse width of S_{La}	$\delta_{La} = \frac{L_{DM}}{V_{dc}} \sqrt{(I_{Lo,T0} - I_{Lm,vl})^2 - \frac{2n_a Q_{oss} V_{dc}}{L_{DM}}} - \epsilon_{HLa}$
Deadtime from S_{Ha} OFF to S_{La} ON	$\sigma_{HLa} = \frac{n_a Q_{oss}}{I_{Lo,T0} - I_{Lm,vl}} + \frac{L_{DM}}{V_{dc}}(I_{Lo,T0} - I_{Lm,vl}) - \delta_{La} + \epsilon_{HLa}$
Deadtime from S_{Hm} OFF to S_{Lm} ON	$\sigma_{HLm} = \frac{n_m Q_{oss}}{I_{Lm,T5}} + \frac{L_{DM}}{V_{dc}} \left(I_{Lm,T5} - \sqrt{I_{Lm,T5}^2 - \frac{2n_m Q_{oss} V_{dc}}{L_{DM}}} \right) + \epsilon_{HLm}$
Deadtime from S_{Lm} OFF to S_{Hm} ON	$\sigma_{LHm} = \frac{3n_m Q_{oss}}{-I_{Lm,vl}} + \epsilon_{LHm}$
Gate pulse width of S_{Hm}	$\delta_{Hm} = DT_s - \frac{n_m Q_{oss}}{-I_{Lm,vl}} - \frac{n_m Q_{oss}}{I_{Lm,T5}} - \epsilon_{LHm}$
Gate pulse width of S_{Lm}	$\delta_{Lm} = T_s - \delta_{Hm} - \sigma_{LHm} - \sigma_{HLm}$

Notes: ϵ_{HLa}, ϵ_{HLm}, and ϵ_{LHm} represent the margins of deadtimes σ_{HLa}, σ_{HLm}, and σ_{LHm}, respectively, in order to satisfy the minimum deadtime requirement. The three deadtime margins can be determined with $\epsilon_i = \max\{(\sigma_{\min} - \sigma_i), 0\}$, where $\sigma_{\min}$ denotes the minimum deadtime and the subscript "$_i$" represents "$_{HLa}$," "$_{HLm}$," and "$_{LHm}$."

steady state is reached, we have

$$I_{Lo,T0} = I_{Lo,Ts} = i_{Lo}(T_0 + T_s). \tag{39}$$

Assume zero loss on the output LC filter (i.e., L_o and C_o), and thus, the average output inductor current is equal to the load current

$$I_{Lo} = \frac{1}{T_s} \int_{T_0}^{T_0+T_s} i_{Lo}(t)\mathrm{d}t. \tag{40}$$

Substituting the above simplified equations for i_{Lo} and the time-interval equations into (39) and (40) yields the initial current $I_{Lo,T0}$ and the output voltage V_o, as follows:

$$I_{Lo,T0} = I_{Lm,vl} + \frac{1}{2I_{Lm,vl}L_{\mathrm{DM}}^2} \times \left(\begin{array}{l} n_m Q_{oss} V_{\mathrm{dc}} L_{\mathrm{DM}} - I_{Lm,vl} T_s V_{\mathrm{dc}} (2L_o - L_{\mathrm{DM}}) \\ - \sqrt{ V_{\mathrm{dc}}^2 \left(\begin{array}{l} [(2D-1) I_{Lm,vl} L_{\mathrm{DM}} T_s + L_{\mathrm{DM}} n_m Q_{oss}]^2 \\ -4 I_{Lm,vl} L_{\mathrm{DM}} L_o T_s (I_{Lm,vl} T_s + n_m Q_{oss}) \\ +(2 I_{Lm,vl} L_o T_s)^2 \end{array} \right) } \\ + 8 V_{\mathrm{dc}} I_{Lm,vl}^2 L_{\mathrm{DM}}^2 L_o T_s (I_{Lo} - I_{Lm,vl}) \end{array} \right) \tag{41}$$

$$V_o = V_{\mathrm{dc}} \times \frac{(D I_{Lm,vl} T_s + n_m Q_{oss}) V_{\mathrm{dc}} - L_{\mathrm{DM}} I_{Lm,vl} (I_{Lo,T0} - I_{Lm,vl} - I_{La,vl})}{(I_{Lm,vl} T_s + n_m Q_{oss}) V_{\mathrm{dc}} - 2 L_{\mathrm{DM}} I_{Lm,vl} (I_{Lo,T0} - I_{Lm,vl} - I_{La,vl})}. \tag{42}$$

With the above initial conditions determined, the initial auxiliary inductor current, $I_{La,T0}$, can be obtained by substituting (35) into (33) as

$$\begin{aligned} I_{La,T0} \approx{}& \frac{I_{Lo,T5}}{k+1} - \frac{1}{1+k}\frac{V_o}{L_o}\Delta T_{67} - \frac{V_f n_m}{R_{\mathrm{on}}(1+k)} \\ & - \left(\frac{I_{Lo,T5}}{k+1} + I_{La,vl} - \frac{V_f n_m}{R_{\mathrm{on}}(1+k)} \right) \\ & \times \exp\left(-\frac{R_{\mathrm{on}}(1+k)}{n_m L_{\mathrm{DM}}} \Delta T_{67} \right). \end{aligned} \tag{43}$$

In order to implement the proposed RCP mode, the modulation timing parameters are required in addition to the duty cycle D, as shown in Fig. 3. Due to the deadtimes, the gate pulsewidth of the main high-side switch, δ_{Hm}, is not exactly equal to the main control variable DT_s. Instead, we have $\delta_{Hm} = DT_s - (T_5 - t_{5s}) - (t_{1e} - T_1)$. In addition, the gate pulsewidth of the auxiliary high-side switch, δ_{Ha}, is not exactly equal to the auxiliary control variable ΔT_{01}, but is expressed as $\delta_{Ha} = \Delta T_{01} + (t_{1e} - T_1)$. Applying the charge-based FET switching model, we can obtain the equations for the key timing parameters in the RCP mode, as listed in Table I.

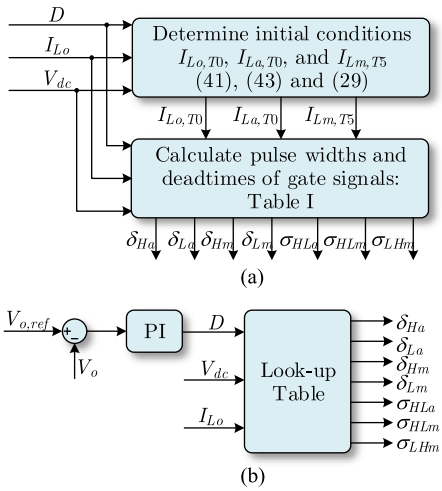

Fig. 4. (a) Block diagram to generate the lookup table for the pulsewidths and deadtimes of gate signals. (b) Control block diagram to regulate the output voltage in the RCP mode.

Fig. 4(a) shows the block diagram to determine the pulsewidths and deadtimes of gate signals.[2] In addition to the duty cycle D, the dc-bus voltage V_{dc} and the average load current I_{Lo} are required in (41), (43), and (29) to determine the initial conditions $I_{Lo,T0}$, $I_{La,T0}$, and $I_{Lm,T5}$. After that, the derived $I_{Lo,T0}$, $I_{La,T0}$, and $I_{Lm,T5}$ are used to calculate the pulsewidths and deadtimes of gate signals with the equations listed in Table I. Since the above calculation is complicated and time consuming, it is more feasible in practice to use lookup tables to obtain the pulsewidths and deadtimes of gates signals, as shown in Fig. 4(b).

With the mathematical model above, the calculated RCP control variable (ΔT_{01}), the gate pulsewidths of S_{Ha} and δ_{Ha}, and the deadtimes at different load currents and duty cycles

[2]The MATLAB code generating the RCP lookup table is available upon request.

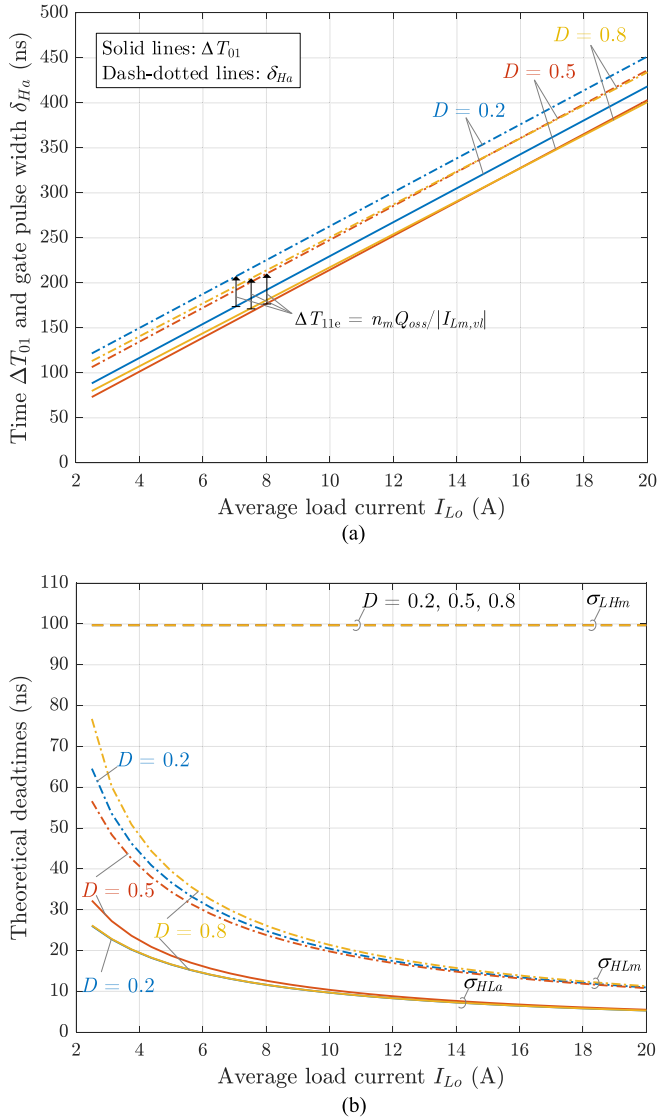

Fig. 5. Calculated timing parameters at different loads and duty cycles. (a) Time ΔT_{01} and gate pulsewidth of S_{Ha}. (b) Theoretical deadtimes. All switches are implemented with GS66508B GaN HEMTs, $V_{\rm dc} = 400$ V, $n_m = 2$, $n_a = 1$, and $L_c = 5\mu$H.

are depicted in Fig. 5. It is seen that the time interval ΔT_{01} is proportional to the average load current I_{Lo}. The RCP control variable ΔT_{01} is directly implemented by adjusting the gate pulsewidth δ_{Ha}, which is obtained by

$$\delta_{Ha} = \Delta T_{01} + \frac{n_m Q_{oss}}{|I_{Lm,vl}|}. \tag{44}$$

It is seen from Fig. 5(b) that as the load current increases, the two deadtimes σ_{HLa} and σ_{HLm} decrease, whereas the deadtime σ_{LHm} remains constant. In practice, however, the turn-ON/OFF time and propagation delay should be taken into account, and therefore, margins (ϵ_{HLa}, ϵ_{HLm}, and ϵ_{LHm}) should be added to the deadtimes, as illustrated in Table I. Thus, the practical deadtimes will be larger than the theoretical values.

F. Simulation Verification of the Mathematical Model

To verify the mathematical model developed in the preceding subsections, SPICE simulations of three parallel GS66808B GaN HEMT HBs (configured as a synchronous buck dc–dc converter operating in the proposed RCP mode) were performed with LTspice, as shown in Fig. 6. In the simulations, the pulsewidths and deadtimes of gate signals are obtained from the equations in Table I. Under the same conditions, the linearized waveforms of the switch-node voltages and inductor currents obtained from the mathematical model developed in Section II-D and II-E are also shown in Fig. 6. It is seen that the linearized inductor currents coincide pretty well with the simulations, which verifies the accuracy of above mathematical model in calculating the gate pulsewidths and predicting the inductor currents.

III. Characteristics, Design Optimization, and Comparison

A. Duty Cycle Range

As seen from Fig. 3, in order to achieve the RCP mode, the duty cycle D should satisfy

$$\frac{\Delta T_{12} + \Delta T_{23}}{T_s} \le D \le 1 - \frac{\Delta T_{01}}{T_s} \tag{45}$$

where ΔT_{01}, ΔT_{12}, and ΔT_{23} are calculated with (10), (14), and (17), respectively. The obtained upper and lower duty cycle boundaries at different load currents and DM inductances are shown in Fig. 7. Overall, the allowed duty cycle range is wide, e.g., [0.048, 0.961] at $L_c = 5$ μH and $I_{Lo} = 20$ A. However, as $L_{\rm DM}$ or I_{Lo} increases, the duty cycle ranges shrinks. When the duty cycle is beyond the range, the parallel HB legs should operate in the synchronous mode.

B. Voltage Gain

With (42), the voltage gain characteristics of the RCP mode at different loads are obtained, as shown in Fig. 8. Different from the synchronous operation, the voltage gain characteristic in the RCP mode is dependent on both the duty cycle and the load. The voltage gain curves in the RCP mode are sharper than the conventional synchronous mode. But the difference is not significant, particularly when the duty cycle is close to 0.5.

C. Double-Pulse RCP to Reduce Conduction Loss

The fixed body diode voltage drops of power FETs vary significantly from 0.7 to 5 V depending on device materials and structures. Typically, enhancement-mode WBG FETs feature higher fixed reverse voltage drops, e.g., V_{sd} =4.5 V at $V_{gs} = -3$ V for the GS66508B GaN HEMT [41] and V_{sd} =3 V at $V_{gs} = -4$ V for the C3M0016120 K SiC MOSFET [42]. As can be seen from Fig. 3, in the single-pulse RCP mode, the auxiliary inductor current i_{La} flows through the body diodes[3] of S_{Ha}

[3]GaN HEMTs do not have intrinsic body diodes, but their reverse conduction characteristics under zero or negative gate–source voltages can be emulated by diodes with fixed voltage drops and ON-state resistances.

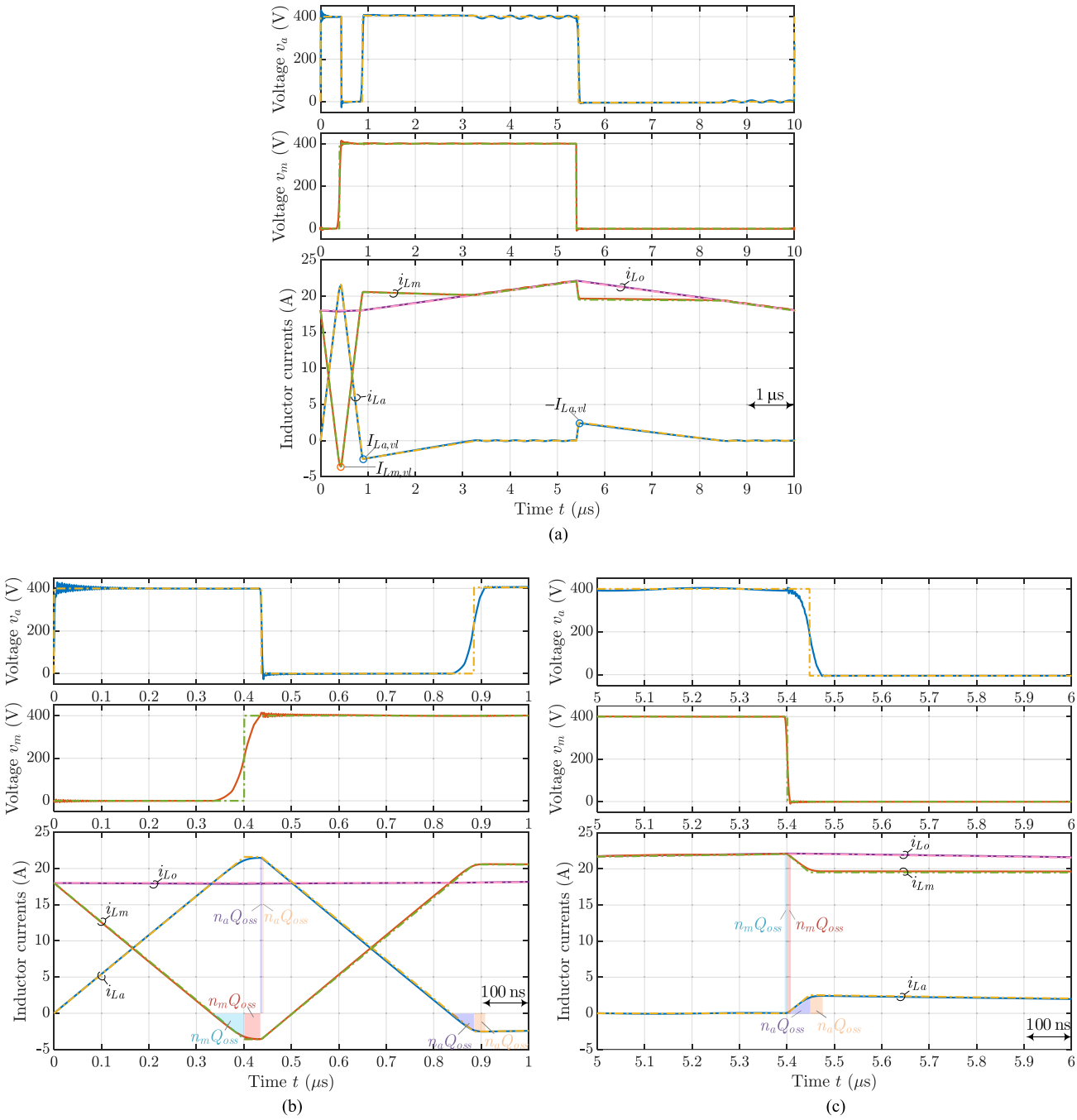

Fig. 6. Waveforms of switch-node voltages and inductor currents with the SPICE simulation (solid lines) and the linear FET model (dashed lines). (a) Over one switching cycle. (b) Zoomed-in waveforms during $t \in [0, 1]$ μs. (c) Zoomed-in waveforms during $t \in [5, 6]$ μs. The switching frequency $f_s = 100$ kHz, $V_{\text{dc}} = 400$ V, $D = 0.5$, $I_{Lo} = 20$ A, $L_c = 5\mu$H, $n_a = 1$, $n_m = 2$, and each of the switches is implemented with one GS66508B GaN HEMT.

and S_{La} during intervals $[T_3, T_4]$ and $[T_6, T_7]$, respectively. If a high gate voltage is applied to S_{Ha} during $[T_3, T_4]$ and to S_{La} during $[T_6, T_7]$, then it is the reverse channel instead of the body diode that conducts i_{La}. As a result, the fixed body diode voltage drop can be eliminated, and the conduction loss can be significantly reduced, particularly for enhancement-mode WBG power FETs. That is, the auxiliary high- and low-side switches are triggered twice during one main switching cycle, and therefore, the improved modulation scheme is termed as the double-pulse RCP.

Applying the single- and double-pulse RCP modulation schemes, the analytical waveforms of inductor currents at different loads are shown in Fig. 9(a) and (b), respectively. With the single-pulse RCP modulation scheme, the inductor current i_{La} converges to zero due to the high voltage drop of body diode, indicating higher conduction losses. By contrast, with

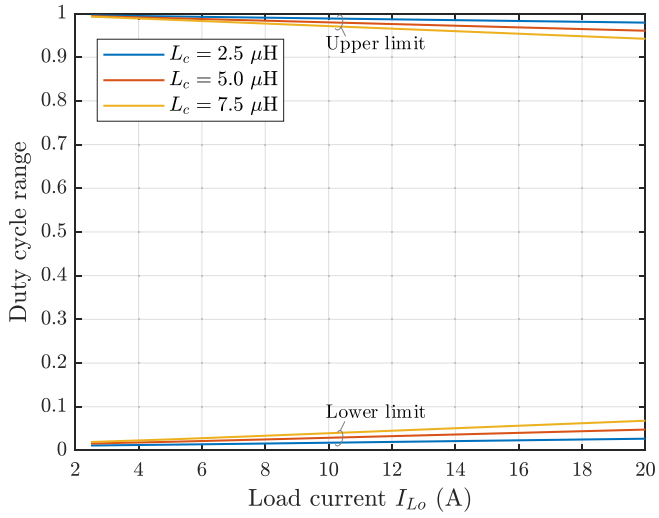

Fig. 7. Allowed duty cycle range when operating in the proposed RCP mode.

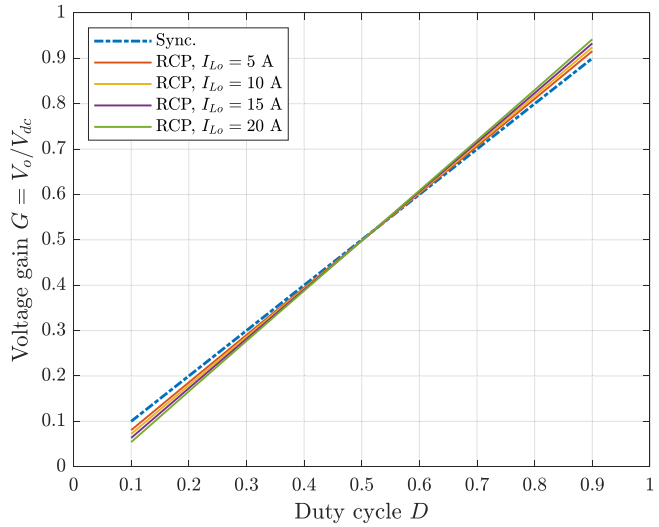

Fig. 8. Voltage gain characteristic in the conventional synchronous CCM and the proposed RCP mode.

the improved double-pulse RCP scheme, the inductor current i_{La} is continuous; neglecting the deadtime, it is always the low-resistance transistor channel instead of the high-voltage-drop body diode that conducts i_{La}. Thus, the conduction loss can be reduced.

On the other hand, in the double-pulse RCP mode, the inductor current i_{La} is quasi-zero at $t = 0$ and therefore the high-side FET of the main leg, S_{Ha}, first achieves quasi-ZCS-ON at $t = 0$. Subsequently, S_{Ha} can achieve ZVS-ON, thanks to the negative valley inductor current $I_{La,vl}$. For the low-side auxiliary transistor, S_{La}, it achieves ZVS-ON twice due to the positive RCP current and the positive valley current $-I_{La,vl}$.

D. Design Optimization of DM Inductors

1) Commutation Inductance L_c: As seen from (S14) and (S17) in the *supplementary material*, the inductor valley currents are inversely proportional to the square root of the commutation

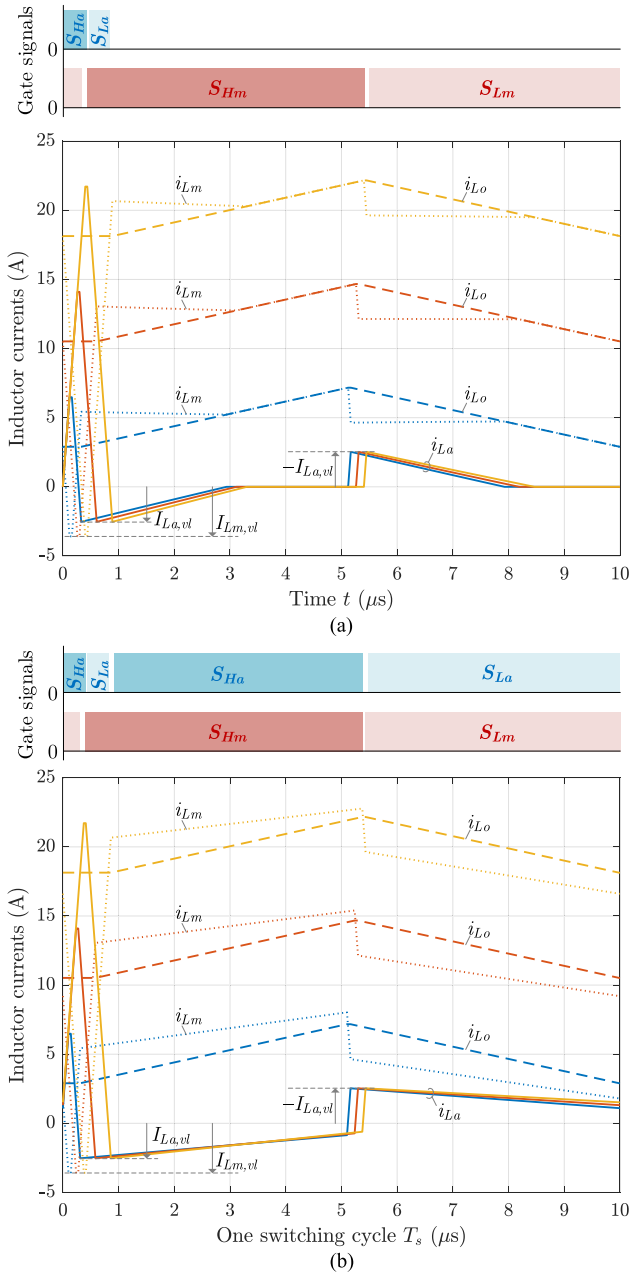

Fig. 9. Analytical waveforms of inductor currents at different loads with (a) single-pulse and (b) double-pulse RCP modulation schemes. The blue, orange, and yellow lines represent the cases of $I_{Lo} = 5$, 12.5, and 20 A, respectively. The gate signals correspond to the case of $I_{Lo} = 20$ A. These inductor current waveforms are generated with the analytical expressions in Section II. The dc-bus voltage $V_{\rm dc} = 400$ V, the duty cycle $D = 0.5$, the switching frequency $f_s = 100$ kHz, the GS66508B GaN HEMT is adopted for each switch, the number of HB legs in parallel $N = 3$, and the number of HB legs chosen as the auxiliary leg $n_a = 1$.

inductance L_c. In order to reduce the valley currents and thereby the rms currents, L_c should be possibly large. On the other hand, however, a larger L_c leads to a smaller duty cycle range, as indicated by Fig. 7. In addition, the inductor volume and power loss are higher with a larger L_c. Therefore, the determination of L_c is a tradeoff among rms currents, duty cycle range, inductor volume, and inductor power loss. In this work, the value of $L_c = 5$ μH is chosen.

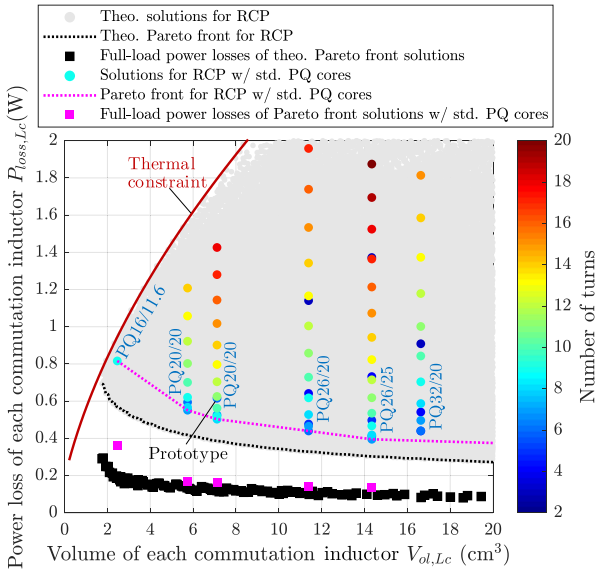

Fig. 10. Power loss–volume Pareto optimal design of DM inductors with theoretical and standard PQ cores at $f_s = 100$ kHz. The design optimization is performed at 75% load ($I_{Lo} = 15$ A) and checked at full load ($I_{Lo} = 20$ A).

2) Power Loss and Volume Pareto Optimization: The magnetic flux density of each commutation inductor is directly related to its current, i.e.,

$$B_j(t) = \frac{L_c i_{Lj}(t)}{N_t A_e} \tag{46}$$

where the subscript "$_j$" represents 1, 2,..., N, $B_j(t)$ denotes the real-time magnetic flux density of inductor L_j, $i_{Lj}(t)$ is the real-time current flowing through inductor L_j, N_t represents the number of turns of each commutation inductor, and A_e denotes the effective cross-sectional area of the used magnetic cores.

It is seen from Figs. 3 and 9 that the commutation inductor currents feature high current ripples, meaning high magnetic flux density swings. Thus, their core losses and volume may be significant without proper design. Hence, a power loss and volume Pareto optimization is necessary for the RCP inductors. The full load current is 20 A, and it is assumed that the RCP mode is enabled when the load is below 75%, i.e., $I_{Lo} = 15$ A. The Pareto optimization is performed at the 75% load, and the design results, including magnetic saturation, power loss, and thermal limit, are checked at the full load, as shown in Fig. 10. It is seen from the Pareto front in Fig. 10 that the power loss of each DM inductor in the RCP mode is relatively low (≤ 0.8 W) compared with the rated converter power 4000 W. When operating in the synchronous mode at the full load (4000 W), the power loss of each DM inductor becomes even more negligible (< 0.4 W). Considering the availability of magnetic core and Litz wire, the design with PQ20/20 and #42 Litz wire (660 strands, six turns) is adopted for the implementation of these DM inductors. The resulting volume and power loss of each DM inductor are 7 cm^3 and 0.61 W (@$P_o = 3$ kW (75% load)), respectively.

E. Comparative Analysis

A comprehensive comparison among various modulation schemes, i.e., the CCM, TCM [30], QCM [39], desynchronized mode [19], and the proposed RCP mode, are shown in Table II. Fig. 11 shows the total rms current squared flowing through the parallel HB legs. The classic CCM features the lowest rms current; however, soft switching cannot be achieved for high-side FETs. The TCM solution enables all power FETs to achieve ZVS-ON at the cost of increased rms current; in addition to the variable switching frequency, the ZVS inductance is large for TCM, which is typically not desirable in inductive load applications (e.g., motor drives) due to additional power loss, cost, and volume [23], [36]. By comparison, the QCM [39], the desynchronized mode [19], and the RCP mode features a fixed switching frequency and requires a much lower ZVS inductance. The QCM enables all FETs to achieve ZVS-ON; however, the rms current is significantly increased compared with the CCM and the TCM, as shown in Fig. 11. The rms current in the desynchronized mode is lower than the QCM; however, only part of the parallel high-side FETs can achieve ZVS-ON. By

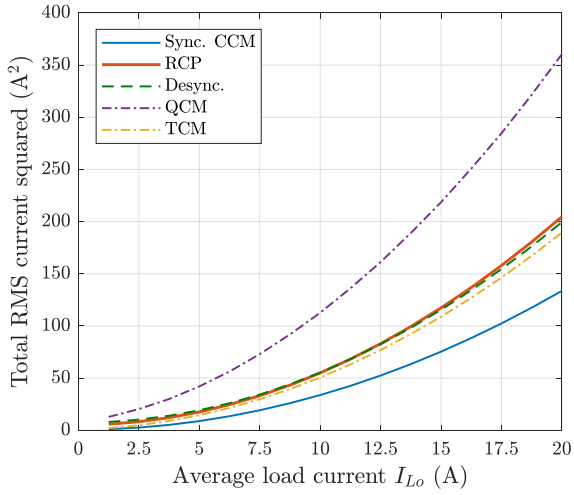

Fig. 11. Comparison of rms currents squared among various modulation schemes: RCP mode, synchronous CCM, desynchronized mode, QCM, and TCM. These operation modes share the same parameters: the dc-link voltage is 400 V, the number of HB legs in parallel is 3, and the duty cycle equals 0.5.

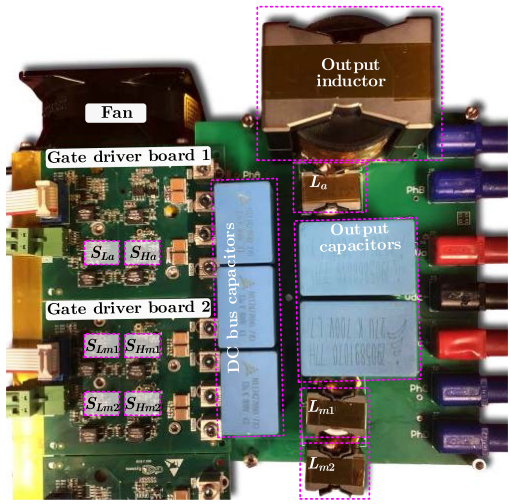

Fig. 12. Prototype of the 4-kW buck dc–dc converter based on three parallel GaN HEMT HB legs and three DM inductors.

TABLE II
COMPARISON AMONG DIFFERENT SCHEMES: CCM, TCM, QCM, DESYNCHRONIZED MODE, AND RCP MODE

Parameters	CCM	TCM [30]	QCM [39]	Desync. Mode [19]	Proposed RCP Mode
Switching frequency	Fixed	Variable	Fixed	Fixed	Fixed
Soft-switching	• *High-side FETs:* Hard-switching • *Low-side FETs:* ZVS-on	• *High-side FETs:* ZVS-on • *Low-side FETs:* ZVS-on	• *High-side FETs:* ZVS-on • *Low-side FETs:* ZVS-on	• *Leading high-side FETs:* Hard-switching • *Lagging high-side FETs:* ZVS-on • *Low-side FETs:* ZVS-on	• *High-side FETs:* ZCS-on or ZVS-on • *Low-side FETs:* ZVS-on
ZVS inductor	N/A	Large	Small	Small	Small
Modulation complexity	Low	Medium	Medium	Medium	High
RMS currents (see Fig. 11)	Low	Medium	High	Medium	Medium
Compatible with CCM	Yes	No	Yes	Yes	Yes

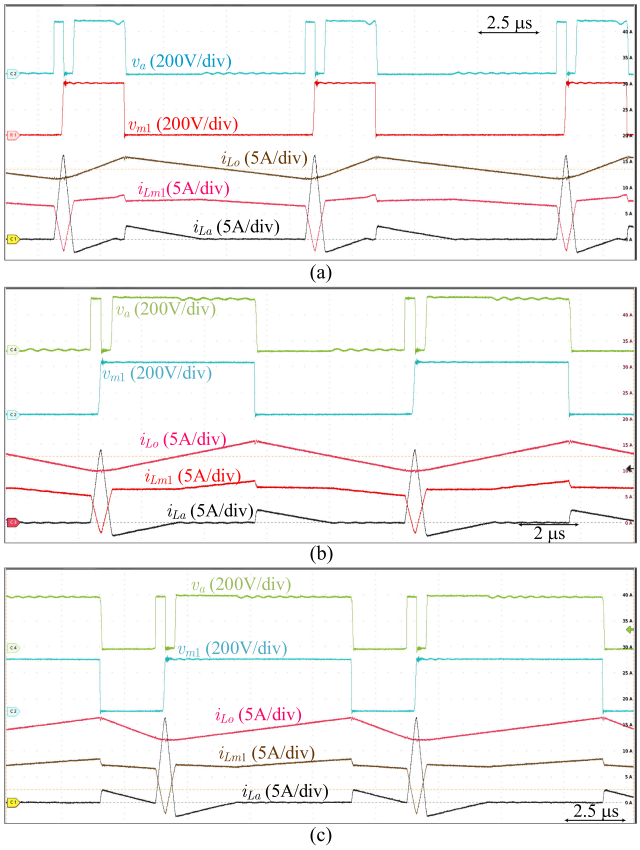

Fig. 13. Steady-state waveforms of the switch-node voltages and inductor currents at $f_s = 100$ kHz with the single-pulse RCP modulation scheme shown in Fig. 3. (a) $D = 0.25$. (b) $D = 0.5$. (c) $D = 0.75$.

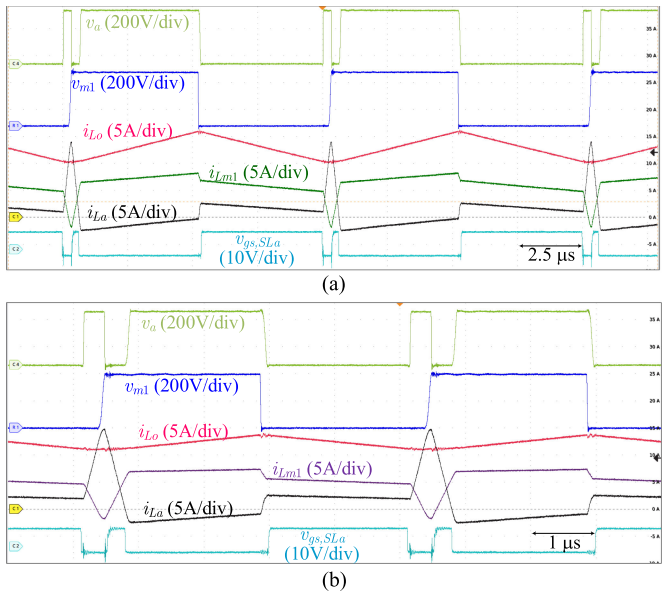

Fig. 14. Steady-state waveforms of the switch-node voltages and inductor currents with the double-pulse RCP modulation scheme shown in Fig. 9(b). The duty cycle $D = 0.5$, and the switching frequency is (a) $f_s = 100$ kHz and (b) $f_s = 200$ kHz.

TABLE III
PARAMETERS OF THE THREE PARALLEL GAN HEMT HB-LEG-BASED BUCK CONVERTER PROTOTYPE

Descriptions	Parameters
Input voltage V_{dc}	400 V
Output voltage V_o	100-300 V
Rated power P_o	4 kW
Number of HB legs in parallel N	3
Power switches $S_{Hm1} - S_{La}$	GS66508B GaN HEMT × 6
DM inductors L_{m1}, L_{m2}, L_a	5 μH × 3 PQ20/20, ferrite PC95 #42 Litz wire, 660strands, 6 turns 165 μH
Output inductor L_o	PQ60/52, ferrite PC95 #38 Litz wire, 500 strands, 24 turns
Output capacitor C_o	27 μF × 2 B32776H8276K000

comparison, the proposed RCP mode enables ZVS/ZCS-ON for all FETs while maintaining relatively low rms currents. The main issue with the RCP solution is that the modulation complexity is high, which should be considered as a tradeoff factor in practice. The implementation details of the RCP modulation in digital signal processor is provided in Section II of the *supplementary material*.

IV. EXPERIMENTAL VERIFICATIONS

A 4-kW synchronous buck dc–dc converter prototype has been developed based on three parallel GS66508B GaN HEMT HBs and three DM inductors (L_{m1}, L_{m2}, L_a), as shown in Fig. 12. When operating in the RCP mode, two HB legs are chosen as main branches, and the remaining HB leg is used as an auxiliary branch; in the synchronous mode, all the three paralleled HBs operate as main legs. The parameters of the converter prototype are listed in Table III.

For the synchronous buck dc–dc converter operating in the CCM, all the low-side switches are inherently able to achieve

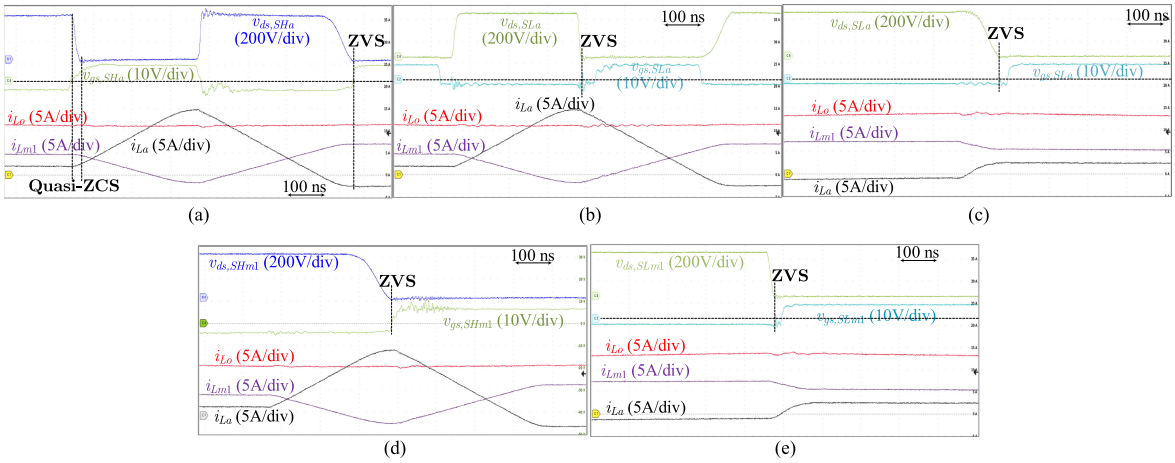

Fig. 15. Soft-switching waveforms of the inductor-based parallel power transistors operating in the proposed RCP mode. Operating conditions: $f_s = 200$ kHz, $V_{\rm dc} = 400$ V, $V_o = 200$ V, and $I_{Lo} = 13$ A. (a) Quasi-ZCS-ON and ZVS-ON of the auxiliary high-side transistor S_{Ha}. (b) First ZVS-ON of the auxiliary low-side transistor S_{La}. (c) Second ZVS-ON of the auxiliary low-side transistor S_{La}. (d) ZVS-ON of the main high-side transistor S_{Hm1}. (e) ZVS-ON of the main low-side transistor S_{Lm1}.

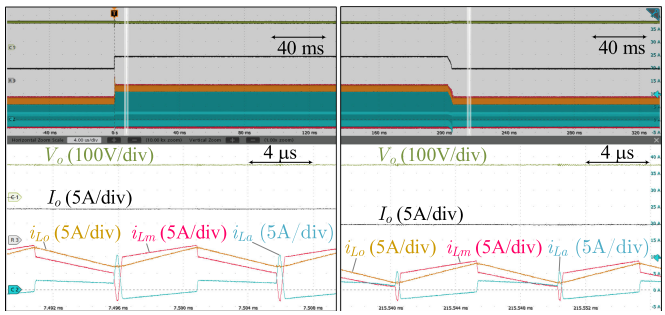

Fig. 16. Measured dynamic waveforms under step load changes with the double-pulse RCP modulation scheme. The input voltage $V_{\rm dc} = 400$ V, the output voltage $V_o = 200$ V, and the switching frequency $f_s = 100$ kHz. (a) Output power increases from 950 to 1900 W. (b) Output power decreases from 1900 to 950 W.

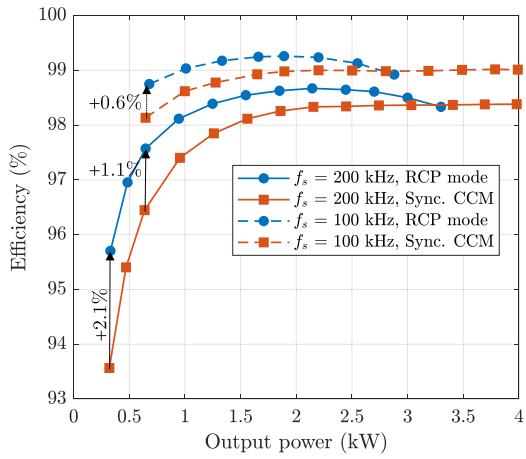

Fig. 17. Measured efficiencies of the parallel GaN HEMT-based buck dc–dc converter operating in different modes and switching frequencies. The input voltage $V_{\rm dc} = 400$ V and the output voltage $V_o = 200$ V.

ZVS-ON due to the positive inductor currents, whereas the high-side switches are hard switched. When the proposed RCP mode is activated, one of the three HB legs, i.e., S_{Ha}–S_{La}, is chosen as an auxiliary branch, whereas the remaining legs (S_{Hm1}–S_{Lm1} and S_{Hm2}–S_{Lm2}) act as main branches. At different duty cycles, the steady-state waveforms of the switch-node voltages (v_{m1} and v_a) and the DM inductor currents (i_{Lm1} and i_{La}) in the RCP mode are shown in Fig. 13. As can be seen, the auxiliary inductor L_a generates a short-time current bump (resonant pole) every switching cycle, causing the main inductor currents i_{Lm1} and i_{Lm2} to fall below 0. Thus, the high-side switches in the main branches, S_{Hm1} and S_{Hm2}, are able to achieve ZVS-ON. The inductor current of the auxiliary branch, i_{La}, is discontinuous, and thus, the auxiliary high-side switch S_{Ha} can achieve ZCS-ON. Meanwhile, the auxiliary low-side switch S_{La} is able to achieve ZVS-ON owing to the positive resonant pole current. The operating waveforms exhibit good coincidence with the theoretical analysis shown in Sections II and III (cf. Fig. 3).

With the double-pulse RCP modulation scheme [see Fig. 9(b)], the steady-state voltage and current waveforms at different switching frequencies are shown in Fig. 14. It is seen that the auxiliary HB leg switches twice during each main switching cycle. The auxiliary inductor current i_{La} becomes continuous; i_{La} falls to quasi-zero and negative before the high-side switch S_{Ha} turns ON; thus, S_{Ha} can achieve quasi-ZCS-ON and ZVS-ON during each switching cycle.

The soft-switching waveforms of these parallel power transistors with the double-pulse RCP modulation scheme are shown in Fig. 15. Different from the switches in the main branches, the auxiliary ones turn ON/OFF twice within each main switching cycle. As seen in Fig. 15(a), during the first turn-ON of the auxiliary high-side switch S_{Ha}, the auxiliary inductor current i_{La} keeps low (2–2.4 A, quasi-zero); thus, S_{Ha} achieves quasi-ZCS-ON at the first switching pulse. After the resonant pole, the drain–source voltage $v_{ds,SHa}$ falls to zero before the gate voltage

of S_{Ha}, i.e., $v_{gs,SHa}$, rises above the gate–source threshold voltage (typically 1.7 V [41]), indicating S_{Ha} achieves ZVS-ON at the second switching pulse. It is seen from Fig. 15(b) and (c) that the drain–source voltage of S_{La} falls to zero before its gate–source voltage rises; thus, the auxiliary low-side FET S_{La} achieves ZVS-ON twice over one main switching cycle. Likewise, the drain–source voltages of HEMTs in the main legs, i.e., $v_{ds,SHm1}$ and $v_{ds,SLm1}$, decrease to zero before the corresponding gate–source voltages $v_{gs,SHm1}$ and $v_{gs,SLm1}$ increase to the threshold voltage, as shown in Fig. 15(d) and (e); hence, the transistors in the main branches achieve ZVS-ON.

Fig. 16 shows the measured dynamic voltage and current waveforms under step load changes with the double-pulse RCP modulation scheme. Despite that the load changes between 950 and 1900 W, the output voltage can be regulated to the reference (200 V); meanwhile, the generated lookup table (see Fig. 4) enables the inductor valley currents to maintain constant and negative such that the high-side FETs can achieve the ZVS-ON.

The efficiencies of this GaN HEMT-based buck dc–dc converter operating in different conditions and modes (synchronous CCM and RCP mode) are measured with a high-precision power analyzer (PPA5530), as shown in Fig. 17. While the synchronous CCM operation enables higher efficiencies at heavy loads, the proposed double-pulse RCP mode exhibits a significant efficiency improvement at partial loads due to the reduced switching losses. The advantages of RCP operation become more remarkable as the switching frequency increases and the load decreases. The maximum efficiency improvement at 320 W (8% load) and 200 kHz is 2.1%. By activating the RCP mode at partial loads and the synchronous CCM at heavy loads, the efficiency performance of the parallel HB legs can be maintained high over the full load range.

V. Conclusion

An RCP-enabled modulation scheme has been proposed for inductor-based parallel power FETs. Compared with the conventional ARCP soft-switching solutions, no auxiliary switches are required in this proposal. The operation principle and timing parameters of the RCP modulation scheme have been investigated in detail. Furthermore, the characteristics, design considerations, and comprehensive experimental validations have been presented. The following conclusions can be drawn.

1) The RCP mode can be enabled by selecting part of the parallel power FET legs as an auxiliary leg without adding extra switches.
2) In the RCP mode, the high-side power FET of the auxiliary leg can achieve the quasi-ZCS-ON/ZCS-ON and ZVS-ON, whereas the remaining FETs achieve ZVS-ON.
3) The RCP mode enables significant partial-load efficiency improvements (up to 2.1%), particularly at high switching frequencies (e.g., 200 kHz).
4) While the switching loss can be significantly reduced in the RCP mode, the conduction loss is higher than the synchronous CCM operation; depending on the switching frequency, the RCP operation may not become as efficient as the synchronous CCM at heavy loads.
5) The inductor-based parallel power FET legs are compatible with both the RCP mode and the synchronous CCM; therefore, the efficiency can be maintained high over the full load range by activating the RCP mode at partial loads and the synchronous mode at heavy loads.

References

[1] Q. Wu, M. Wang, W. Zhou, and X. Wang, "Current balancing of paralleled SiC MOSFETs for a resonant pulsed power converter," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5557–5561, Jun. 2019.

[2] J. Qu, Q. Zhang, X. Yuan, and S. Cui, "Design of a paralleled SiC MOSFET half-bridge unit with distributed arrangement of dc capacitors," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10879–10891, Oct. 2020.

[3] S. G. Kokosis, I. E. Andreadis, G. E. Kampitsis, P. Pachos, and S. Manias, "Forced current balancing of parallel-connected SiC JFETs during forward and reverse conduction mode," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1400–1410, Feb. 2017.

[4] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with aid of a differential mode choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, Feb. 2020.

[5] M. Schulz, "Semiconductor solutions to support high-power battery charging systems in electric mobility scenarios," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion*, Renewable Energy Energy Manage., 2017, pp. 1–4.

[6] M. Du, J. Xin, H. Wang, Z. Ouyang, and K. Wei, "Estimating junction temperature of SiC MOSFET using its drain current during turn-on transient," *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 1911–1918, May 2020.

[7] J. Hu *et al.*, "Robustness and balancing of parallel-connected power devices: SiC versus coolMOS," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2092–2102, Apr. 2016.

[8] J. Lu and R. Hou, "Parasitics optimization for GaN HEMTs in conventional housing-type power modules," in Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage., May 2019, pp. 1–7.

[9] H. Li *et al.*, "Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[10] J. L. Lu and D. Chen, "Paralleling GaN E-HEMTs in 10kW-100 kW systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 3049–3056.

[11] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 1563–1569.

[12] Z. Wang, Y. Wu, J. Honea, and L. Zhou, "Paralleling GaN HEMTs for diode-free bridge power converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2015, pp. 752–758.

[13] Y. Mao, Z. Miao, C. Wang, and K. D. T. Ngo, "Passive balancing of peak currents between paralleled MOSFETs with unequal threshold voltages," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3273–3277, May 2017.

[14] Z. Miao, Y. Mao, G. Lu, and K. Ngo, "Magnetic integration into a silicon carbide (SiC) power module for current balancing," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11 026–11035, Nov. 2019.

[15] D. Bortis, J. Biela, and J. W. Kolar, "Active gate control for current balancing of parallel-connected IGBT modules in solid-state modulators," *IEEE Trans. Plasma Sci.*, vol. 36, no. 5, pp. 2632–2637, Oct. 2008.

[16] J. Ao, Z. Wang, J. Chen, L. Peng, and Y. Chen, "The cost-efficient gating drivers with master-slave current sharing control for parallel SiC MOSFETs," in *Proc. IEEE Transp. Electrific. Conf. Expo*., 2018, pp. 1–5.

[17] R. Schnell, "Paralleling of IGBT modules," *ABB Switzerland Ltd., Zürich Switzerland, Application Note 5SYA 2098-00*, 2013.

[18] S. Lu, X. Deng, S. Li, and E. Rong, "A passive transient current balancing method for multiple paralleled SiC-MOSFET half-bridge modules," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 349–353.

[19] Y. Shen, L. Shillaber, H. Zhao, Y. Jiang, and T. Long, "Desynchronizing paralleled GaN HEMTs to reduce light-load switching loss," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9151–9170, Sep. 2020.

[20] Y. Jiang, Y. Shen, L. Shillaber, C. Jiang, and T. Long, "Split parallel semi-bridge switching cells for full-power-range efficiency improvement," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10889–10905, Sept. 2021.

[21] H. Li, S. Munk-Nielsen, S. Beczkowski, and X. Wang, "A novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8042–8045, Dec. 2016.

[22] C. Zhao, L. Wang, and F. Zhang, "Effect of asymmetric layout and unequal junction temperature on current sharing of paralleled SiC MOSFETs with Kelvin-source connection," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7392–7404, Jul. 2020.
[23] T. Fuchslueger, H. Ertl, and M. A. Vogelsberger, "Reducing dv/dt of motor inverters by staggered-edge switching of multiple parallel SiC half-bridge cells," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, May 2017, pp. 1–8.
[24] R. Hou, Y. Shen, H. Zhao, H. Hu, J. Lu, and T. Long, "Power loss characterization and modeling for GaN-based hard-switching half-bridges considering dynamic on-state resistance," *IEEE Trans. Transp. Electrific.*, vol. 6, no. 2, pp. 540–553, Jun. 2020.
[25] N. He, M. Chen, J. Wu, N. Zhu, and D. Xu, "20-kW zero-voltage-switching SiC-MOSFET grid inverter with 300 kHz switching frequency," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5175–5190, Jun. 2019.
[26] P. Bau, M. Cousineau, B. Cougo, F. Richardeau, and N. Rouger, "CMOS active gate driver for closed-loop dv/dt control of GaN transistors," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13322–13332, Dec. 2020.
[27] G. Venkataramanan, D. M. Divan, and T. M. Jahns, "Discrete pulse modulation strategies for high-frequency inverter systems," *IEEE Trans. Power Electron.*, vol. 8, no. 3, pp. 279–287, Jul. 1993.
[28] R. De Doncker and J. Lyons, "The auxiliary resonant commutated pole converter," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 1990, pp. 1228–1235.
[29] W. Dong, D. Peng, H. Yu, F. C. Lee, and J. Lai, "A simplified control scheme for zero voltage transition (ZVT) inverter using coupled inductors," in *Proc. IEEE 31st Annu. Power Electron. Spec. Conf.*, 2000,vol. 3, pp. 1221–1226.
[30] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.
[31] A. Rodriguez, A. Vazquez, M. R. Rogina, and F. Briz, "Synchronous boost converter with high efficiency at light load using QSW-ZVS and SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 386–393, Jan. 2017.
[32] Q. Huang, R. Yu, Q. Ma, and A. Q. Huang, "Predictive ZVS control with improved ZVS time margin and limited variable frequency range for a 99% efficient, 130-W/in^3 MHz GaN totem-pole PFC rectifier," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 7079–7091, Jul. 2019.
[33] O. Knecht, D. Bortis, and J. W. Kolar, "ZVS modulation scheme for reduced complexity clamp-switch TCM DC-DC boost converter," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4204–4214, May 2018.
[34] W. Konrad, G. Deboy, and A. Muetze, "A power supply achieving titanium level efficiency for a wide range of input voltages," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 117–127, Jan. 2017.
[35] Z. Yao and S. Lu, "A simple approach to enhance the effectiveness of passive currents balancing in an interleaved multiphase bidirectional DC-DC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7242–7255, Aug. 2019.
[36] F. Luo *et al.*, "Analysis of cm volt-second influence on cm inductor saturation and design for input EMI filters in three-phase DC-fed motor drive systems," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1905–1914, Jul. 2010.
[37] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$-Pareto optimization and comparative evaluation of inverter concepts considered for the Google little box challenge," in *Proc. IEEE 17th Workshop Control Model. Power Electron.*, 2016, pp. 1–5.
[38] D. Neumayr, G. C. Knabben, E. Varescon, D. Bortis, and J. W. Kolar, "Comparative evaluation of a full-and partial-power processing active power buffer for ultra-compact single-phase dc/ac converter systems," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1994–2013, Apr. 2021.
[39] Y. Shen, Y. Jiang, H. Zhao, L. Shillaber, C. Jiang, and T. Long, "Quadrilateral current mode paralleling of power MOSFETs for zero-voltage switching," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5997–6014, May 2021.
[40] S. J. Settels, J. L. Duarte, J. van Duivenbode, and E. A. Lomonova, "A 2-kV charge-based ZVS three-level inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3450–3465, Apr. 2020.
[41] *Bottom-Side Cooled 650 V. E-Mode GaN Transistor*, Datasheet GS66508B, GaN Systems, Ottawa, ON, Canada, 2020. [Online]. Available: https://gansystems.com/wp-content/uploads/2020/04/GS66508B-DS-Rev-200402.pdf
[42] C3M0060065K Silicon Carbide Power MOSFET, CREE, Durham, NC, USA, Jul. 2020. [Online]. Available: https://www.wolfspeed.com/media/downloads/1627/C3M0060065K.pdf.

Yanfeng Shen (Member, IEEE) received the B.Eng. degree in electrical engineering and automation and the M.Sc. degree in power electronics from Yanshan University, Qinhuangdao, China, in 2012 and 2015, respectively, and the Ph.D. degree in power electronics from Aalborg University, Aalborg, Denmark, in 2018.

He is currently a Research Engineer in Power Electronic with Danfoss Silicon Power R&D Munich, Ismaning, Germany. From 2019 to 2021, he was a Postdoctoral Research Associate with the University of Cambridge, Cambridge, U.K. He was a Visiting Graduate Research Assistant with Khalifa University, Abu Dhabi, UAE, in 2016. He worked as an Intern with the ABB Corporate Research Center, Beijing, China, in 2015. His current research interests include the thermal management and reliability of power electronics, electric vehicle traction inverters, and SiC power modules.

Dr. Shen is an Industry Editor for *IET Renewable Power Generation*.

Yunlei Jiang (Student Member, IEEE) received the B.Sc. degree from Nanjing Normal University, Nanjing, China, in 2015, and the M.Sc. degree from the School of Electrical Engineering, Southeast University, Nanjing, in 2018. He is currently working toward the Ph.D. degree with the University of Cambridge, Cambridge, U.K., where he is jointly funded by the Jardine Foundation and the Cambridge Trust.

He was a Research Assistant with the Wisconsin Electric Machines and Power Electronics Consortium, University of Wisconsin Madison, WI, USA, from 2018 to 2019. His research interests include high-performance electrical drive and power electronics.

Mr. Jiang is a Jardine Scholar. He was the recipient of the Outstanding Master's Thesis of Jiangsu Province.

Hui Zhao (Member, IEEE) received the bachelor's and master's degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2010 and 2013, respectively, and the Ph.D. degree in power electronics from the University of Florida, Gainesville, FL, USA, in 2018.

He had a Summer Internship with the General Electric Global Research Center, Shanghai, China, in 2013. He was a Postdoctoral Research Associate with the University of Cambridge, Cambridge, U.K., from 2018 to 2021. He is currently a Junior Researcher with Fudan University, Shanghai, China. His research interests include the modeling and driving of power devices, electromagnetic interference, and high-power-density power converters.

Teng Long (Member, IEEE) received the B.Eng. degree from the Huazhong University of Science and Technology, Wuhan, China, the B.Eng. (first class hons.) degree from the University of Birmingham, Birmingham, U.K., both in 2009, and the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 2013.

Until 2016, he was a Power Electronics Engineer with the General Electric Power Conversion, Rugby, U.K. He is currently a Lecturer with the University of Cambridge. His research interests include power electronics, electrical machines, and machine drives.

Dr. Long is a Chartered Engineer registered with the Engineering Council in the U.K.