Design and Implementation of Two Hybrid High Frequency DPWMs Using Delay Blocks on FPGAs

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***Abstract*—The use of very high-resolution digital pulse width modulators (DPWMs) for high frequency dc–dc converters has been steadily increasing in recent years. However, the resolution of the DPWM formed by counters and comparators is limited when the switching frequency rise above MHz range. Given this limitation, new strategies for DPWM architectures are being designed to increase the resolution of the signals. This article proposes two new DPWMs architectures with the aim of increasing the resolution of trigger signals using field programmable gate arrays (FPGAs). The first proposed architecture is a hybrid DPWM, which integrates a clock manager and a delay line. For this architecture, the delay line is configured using FPGA intellectual properties (IP) blocks. This delay stage allows a fine resolution in the picosecond scale. In addition, an alternative solution has been implemented to generate two signals, the main signal and its complementary one, including high resolution for the dead time, which is also configurable. Both architectures have been tested through static and dynamic tests on two FPGAs of different costs, an Artix-7 (low-cost) and a Kintex-UltraScale 7 (high-cost) by Xilinx.**

***Index Terms*—Complementary signal, dc–dc converters, dead time, field programmable gate arrays (FPGA), high resolution, hybrid DPWM, low-cost FPGA.**

I. Introduction

THE development of wide bandgap devices is consolidating as a clear substitute for traditional silicon semiconductors when the switching frequency rises above megahertz [1]. This increase in switching frequency is leading the interest toward new hardware architectures, capable of generating the fast and accurate driving signals needed to operate these devices in an efficient manner [2].

The loss of resolution in the modulator is one of the biggest problems that this increase in frequency generates in semiconductor devices, because the modulator is not able to fix the signals with zero error in the control stage. This effect is called limit cycle [3]. An additional problem to the low time resolution relates to the generation of the dead times, required to drive synchronous switching stages. If the dead time were too small, one switch could still be conducting when the complementary one is switched ON, generating a short-circuit. On the other hand, if the dead time were too high, the efficiency of the converter would be affected.

Traditionally, DPWMs were implemented using a combination of counters and comparators [4], [5]. The counter was responsible for generating the carrier using the device clock as reference, and the comparator produced the pulse modulated signal (pulse control signal for the power converter switches). In these DPWMs, the resolution depended on the ratio between the counter frequency (f_{CLK}) and the converter switching frequency (f_{SW}). Expression (1) shows this relationship, where it can be seen that if the value of the switching frequency is increased, the number of steps of the counter will decrease (n). For example, if a switching frequency of 40 MHz were required using a 400 MHz digital device, the number of counter steps would be only 10. With this number of steps, the duty cycle could only be set in multiples of 10% duty cycle, which would not be sufficient to achieve a satisfactory static regulation of the output voltage.

$$n = \frac{f_{\mathrm{CLK}}}{f_{\mathrm{SW}}}. \tag{1}$$

This problem of low resolution at high switching frequencies generates a need to develop high-resolution DPWMs to operate at these frequencies in the megahertz range.

Currently, there are commercial microcontroller units (MCU) oriented to power electronics applications offering enhanced resolution in the PWM signals, like [6]–[8]. These devices have high-resolution PWM blocks (HRPWM) capable of positioning an edge very finely by subdividing one coarse system clock of a conventional PWM generator, achieving a time step accuracy on the order of 60 ps, although their clock frequencies are up to 300 MHz [9]. However, the duty cycle cannot be controlled in the whole range and the dead time in complementary signals cannot be finely adjusted. On the other hand, FPGAs present

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some advantages compared to MCU, like hardware level protection and the flexibility that the peripherals are implemented by the designer [10]. So, some limitations of the MCU HRPWM can be overcome, like switching frequency range or insufficient resolution. There are also many contributions to design new architectures for implementing high-resolution DPWM on application-specific integrated circuit (ASICs) technologies [2], [11], [12] and FPGAs technologies [4], [5], [13]–[17]. This work focuses on the implementation on FPGAs.

One of the most common strategies in FPGAs is to use digital clock blocks (digital clock manager DCM) to increase the resolution of the basic counter through some subdivisions of the main clock. The operation of this technique consists of setting the PWM signal at high level "1" when the count starts (count = 0) and setting it at low level "0" after a few clock cycles (coarse part) plus a fraction of the clock period (decimal part). This fraction can be achieved using the DCM, which generates several shifted clock signals from the main clock. Then, the proper shifted clock is selected with a multiplexer to adjust the falling edge [14], [17]. The main disadvantage of using this technique is that it is not possible to update instantly the duty cycle, as it requires a few clock periods to do so. Another strategy is to use DCM's own phase shifter to fine-tune [18]. This technique still implies a delay in the PWM signal update. As an alternative, the use of a multiplexer can be omitted at the expense of increasing the update delay by more than one clock period. With this strategy the authors achieved the highest resolution in FPGA technology with 19.5 ps on a 6.25 MHz PWM signal with a Virtex 5 [18].

Another of the most commonly used techniques in DPWM design is to use hybrid architectures, where the use of digital synchronous blocks to make a coarse resolution adjustment is combined with other asynchronous blocks (typically delay lines) that achieve a fine adjustment, allowing a higher resolution without the need to use a high frequency. In [4], the authors propose two designs of their own delay line using logic gates implemented in FPGA logic. These architectures were tested in two different FPGAs. However, both architectures require manual placement and routing to calibrate the delay line. Therefore, the same authors published in [19] an update of their work where, through a delay line placement restriction, it is no longer necessary to adjust the placement of the delay line elements. In [20], the authors proposed a hybrid architecture using carry chain-based delay line and output D flip–flop, achieving a resolution of 41.3 ps. In [21], the authors used a carry-chain path, an AND gate and a set–reset block to adjust the desired delay, achieving a time resolution equal to 40.2 ps. The authors of [22] proposed a new hybrid architecture using IP blocks available in the Virtex-6 FPGA. This IP block (IODELAY) consists of a programmable delay line that allows updating the duty cycle without delays and does not require calibration, but they only achieve a fine tuning of the falling edge of the PWM. In Table I, there is a summary of the state-of-the-art of the most relevant presented architectures.

This article introduces a new hybrid architecture of DPWM, using IP blocks of the FPGA as programmable delay lines. Some preliminary ideas were presented in [24], but one of the main novelties of this proposal is that the architecture is suitable not only to generate a fine duty cycle, but also to produce complementary signals with a fine adjustment of the dead time. The main advantages of this proposal compared to others are: 1) rising and falling edges are finely tuned independently, which means both the dead time and the duty cycle can be finely adjusted; 2) the resolution of the programmable delay lines is in the order of picoseconds; 3) the architecture allows updating the duty cycle in the same CLK period; 4) the proposal does not suffer from limitations like manual routing, specific calibration, etc.; 5) the implementation is easy because IP blocks are easy to handle.

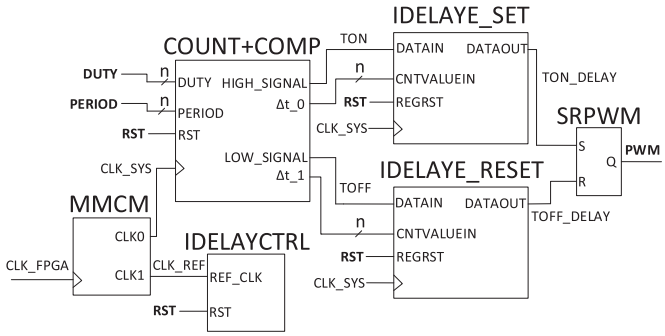

Fig. 1. Hybrid high-resolution DPWM.

Regarding the application related to power electronics, our proposal can be seen as an enabling technology for very high switching frequency power converters, especially those converters with wide band gap devices switching at frequencies close to 10 MHz. At 10 MHz, the MCUs previously described would be able to provide 10.7 b resolution for the duty cycle [9], and it is not possible to have an independent fine tuning of the dead time when producing complementary signals.

The proposed hybrid PWM is validated for two families of FPGAs from the same manufacturer, Xilinx: Artix 7 (low cost) and Kintex-UltraScale 7 (one order of magnitude more expensive and with a better performance). Nevertheless, the proposed architecture could be used for other families adapting the HDL code to their specific implementation of delay lines. And depending on the manufacturer, the proposed architecture could also be used taking into account the specific implementation of programmable delay lines for that device. In this work, we have used Xilinx FPGAs because of the high resolution, which can be achieved thanks to the provided IPs, called IDELAYEs.

This article is organized as follows. In Section II, the proposed hybrid architecture is presented, including measurements of its static and dynamic behavior for two different implementations. In Section III, the architecture for a half bridge dc–dc converter is proposed and the dead time resolution is measured. In Section IV, the architecture is tested in a synchronous buck converter. Finally, the conclusion about this architecture are presented in Section V.

II. Proposed Hybrid DPWM Architecture

A. Description of the Architecture

The proposed hybrid DPWM architecture is shown in Fig. 1, is formed by a synchronous part and an asynchronous delay line.

TABLE I
DPWM ARCHITECTURE COMPARISON

REF	YEAR	FPGA	ARCHITECTURE	CLK FREQ (MHz)	PWM FREQ	RESOLUTION	MAIN CHARACTERISTICS
[17]	2008	Spartan 3	Hybrid DPWM with DLL	128	250 kHz	1.242 ns	- Updating the duty cycle requires more than one CLK period. - Based on DLL (delay-locked loops).
[17]	2008	Virtex 4 LX	Hybrid DPWM with DLL	128	250 kHz	737 ps	- Calibration required: manual place&route or include extra logic. - The linearity depends on the configuration of the place&route.
[17]	2008	Virtex 5 LX	Hybrid DPWM with DLL	128	250 kHz	730 ps	- Generation of complementary signals, fine tuning of the falling edge in the high side and the rising edge in the low side.
[18]	2010	Virtex 5	Fine phase shifting	50	6.25 MHz	19.5 ps	- Updating the duty cycle requires more than one CLK period. - Manual place&route of the asynchronous part. - Duty cycle from 0 to 100%. - Generation of complementary signals, fine tuning of the falling edge in the high side and the rising edge in the low side.
[4]	2012	Cyclone II	Hybrid	-	50 MHz	60 ps	- Manual place&route not required, but constraints required. - Low latency. - Maximum duty cycle 75%. - Fine tuning of the falling edge.
[4]	2012	Virtex 4	Hybrid	-	1 MHz	90 ps	- Manual place&route not required, but constraint required. - Low latency. - With 1 MUX, the DPWM is not monotonic and the resolution is 20 ps. When using 4 MUX, the DPWM is monotonic and the resolution is 90 ps. - Fine tuning of the falling edge.
[22]	2012	Virtex 6	DCM	200	-	625 ps	- Updating the duty cycle requires more than one CLK period. - Manual place&route required for some blocks. - Nonlinearity in the on-time step due to duty-cycle variation. - Fine tuning of the falling edge.
[22]	2012	Virtex 6	Hybrid DPWM with IODELAY	200	-	78 ps	- Autocalibrated programmable delay line based on the use of IODELAY. - Updating the duty cycle requires one CLK period. - Fine tuning of the falling edge.
[15]	2014	Cyclone II	Hybrid DPWM with PLL	250	-	1 ns	- Updating the duty cycle requires more than one CLK period. - Calibration required after automatic place&route. - Duty cycle from 0 to 100% - Fine tuning of the falling edge.
[15]	2014	Cyclone II	Hybrid DPWM with SERDES	200	-	1.256 ns	- Fast updating of the duty cycle. - Automatic place&route. - The resolution is imposed by the maximum data rate tolerated by the FPGA's high speed LVDS output pins. - Duty cycle from 0 to 100%.
[5]	2015	Cyclone IV	Hybrid DPWM with delay line	46.34	90.5 kHz	80 ps	- Additional memory required. - Updating the duty cycle requires more than one CLK period. - No information about the duty cycle range. - Fine tuning of the falling edge.
[23]	2017	Cyclone IV	Hybrid DPWM with PLL	50	10 MHz	12.5 ns	- 8 counters required. - 2 modulators to generate the PWM signal. - Synchronous system.
[20]	2020	Cyclone IV	Hybrid DPWM with chain-based delay line	188	1.47 MHz	41.3 ps	- D flip-flop instead the SET-RESET latch. - Duty cycle from 0.9429% to 99.2%. - Fine tuning of the falling edge.
[21]	2020	Kintex 7	Hybrid DPWM with delay line	250	1 MHz	40.2ps	- Place&route constraints required. - Duty cycle from 0 to 100%. - Fine tuning of the falling edge.

In this work, we have implemented the proposed architecture using two different Xilinx FPGAs, which implement IP blocks called IDELAYE [25]. This IP blocks are the ones used as programmable delay lines in our architecture.

The synchronous part is composed of the following:

1) A MMCM (Mixed Mode Clock Manager, a mixture between DCM and PLL) that allows changing the configuration of the FPGA clock tree in order to increase its speed.
2) The COUNT+COMP block, which generates the signals SET (TON) and RESET (TOFF) for the edges of the PWM signal. Its operation is based on a traditional count/comparator.
3) The IDELAYCTRL block is responsible for doing the reset, which makes the delay line reset synchronous, and can also carry out automatic calibration of the total delay, ensuring that the time value is kept under different voltage or temperature conditions.

The asynchronous part is formed by the following:

1) IDELAYE blocks to finely adjust the duty cycle of the PWM signal. These blocks allow to set the rising or falling edge of a PWM signal between count of the COUNT+COMP block.
2) A SRPWM block that is a SET–RESET latch. When the signal TON_DELAY is "1," its output (the PWM signal) is "1," and when the TOFF_DELAY is "1," the PWM signal is "0." We can configure which pin has priority when both signals are simultaneously at "1," and this will have an impact on the behaviour of the architecture, as will be shown later.

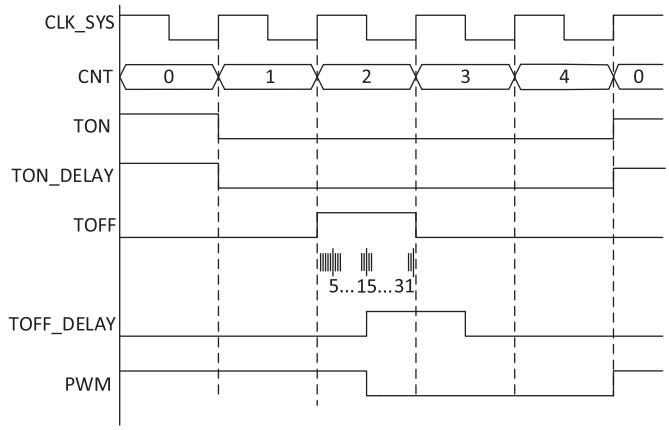

Fig. 2. Example of the architecture DPWM.

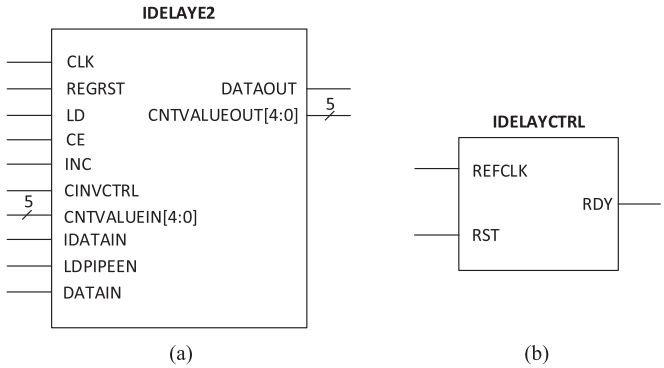

Fig. 3. IDELAYE2 and IDELAYCTRL.

The COUNT+COMP block is responsible for generating the coarse rising and falling edges of the PWM signal. The HIGH_SIGNAL and LOW_SIGNAL outputs correspond to the values generated by the counter and comparators. Additionally, it calculates the required Δt_0 and Δt_1, which correspond to the delays to be applied in the IDELAYE to achieve the fine adjustment of the duty cycle, modifying the rising and falling edges (respectively). The frequency of CLK_SYS (Clock of synchronous COUNT+COMP block) is determined by the total delay time that IDELAYE can achieve.

An example of the basic operation of this architecture is shown in Fig. 2. For this example, the PWM has one duty cycle equal to 2.5 counts of CLK_SYS. To obtain this 0.5 of duty cycle it is necessary to use Δt_0 and Δt_1 to adjust the fine delay. In this example, we use two IDELAYE blocks with 5 b for its CNTVALUEIN signal, which means CNTVALUEIN has 32 taps to configure the fine delay. One tap is the minimum delay variation allowed by the IDELAYE when the CNTVALUEIN changes 1 unit. These 5 b configure the value of the delay depending on the clock references (CLK_REF) value in the IDELAYCTRL block. In this example Δt_0 is zero, so the rising edge of the PWM is synchronized to CLK_SYS. The value of Δt_1 is the half of the total bits, that is, the required delay is 16 taps.

At the beginning, the COUNT+COMP block starts the count and sets to high TON signal for one cycle of CLK_SYS. This signal is connected to IDELAYE_SET and in this case the TON_DELAY signal is delayed with 0 taps (Δt_0 = 0), and consequently TON_DELAY is equal to TON.

When the counter achieves the value of DUTY (2 CLK_SYS counts in this example), the signal TOFF is set to high for one clock cycle. This signal is connected to IDELAYE_RESET and it is delayed for the number of taps indicated by Δt_1, signal calculated by the COUNT+COMP block (in this example, it is equal to half of CLK_SYS period, CNTVALUEIN = 15,). In the instant that TOFF_DELAY changes to "1," the PWM signal changes to "0." Finally, when the counter reaches the PERIOD value, the count will be reset and restart.

There are significant differences comparing our proposal to the one in [22], which also is based on the use of programmable delay lines and implemented on Xilinx FPGA Virtex 6. In our approach, both the rising and falling edges of the PWM can be finely tuned. Additionally, both SET and RESET paths include an IDELAYE block, so the delays of both signals are approximately the same. Therefore, our approach does not require to include additional flip–flops and the duty cycle can be immediately updated. Moreover, it is not required to manually modify the place and route. On the other hand, our proposal requires twice the number of IP blocks. However, this is not an important limitation because of the number of available IDELAYE blocks in the FPGAs.

B. Implementation on an Artix-7

In a first approach, the proposed architecture has been implemented in a Basys3 Artix-7 FPGA Development Board.

1) IDELAYE2 Configuration: The IDELAYE block of the Artix-7 FPGA is called IDELAYE2, and has 5 b for CNTVALUEIN, which means CLK_SYS can be divided into 32 taps. This block is connected to all the HR (High Range) pins, which work at 3.3 V. There are more than 100 HR pins in the Artix 7. Since the proposed architecture requires two IDELAYE blocks per DPWM, a high number of hybrid DPWMs could be implemented on one FPGA. The IDELAYE2, shown in Fig. 3(a), allows generating an output signal (DATAOUT) delayed a certain time with respect to the input signal (IDATAIN). In order to reduce the jitter in this block, the IDELAYE2 has an attribute called HIGH_ PERFORMANCE_MODE.

The IDELAYCTRL IP block, shown in Fig. 3(b), can be used to calibrate IDELAYE2 when using a mode called "TIME." In that case, the delay line is calibrated for the requested time value (defined by CNTVALUEIN), performing voltage/temperature compensation to ensure that this value is kept over time. However, the calibration process requires several clock cycles. As the results show quite stable behavior over working conditions, the mode called "COUNT" has been used instead, in which the CNTVALUEIN value is immediately applied without calibration. In this way, the duty cycle is immediately updated without any delay. Anyhow, a tradeoff between response time and stability over time is possible using these different working modes.

For the proposed design, CLK_REF uses a 200 MHz clock signal, which is the default one. This frequency is used to prevent

an updating time of the duty cycle higher than one clock cycle. Another frequency of CLK_REF increases the update time of the CNTVALUEIN. Also, the IDELAYE2 registers are configured to work in Count Mode and the operation mode is Loadable Variable. Finally, the HIGH_PERFORMANCE _MODE attribute is activated to reduce the IDELAYE2 jitter.

Because of the IDELAYE2 configuration, and by means of Vivado simulations, the tap resolution is expected to be 78 ps. CLK_SYS is determined from the total time applied by the delay line, which is 32 times 78 ps, that is, 2.496 ns (400 MHz).

2) Measurement Set-Up: First of all, it is necessary to determine the appropriate set-up to measure resolutions below 200 ps (5 GHz). Conventional oscilloscopes have sampling frequencies around 5 GSa/s, so they have an insufficient resolution to measure variations of 78 ps (12.8 GHz), as expected. Given the impossibility of making precise measurements using time as a unit, we decided to calculate the average value of the PWM signal, since data acquisition cards have more than 10 b in the vertical scale. Data acquisition cards are slow, but a high-speed acquisition rate is not required to measure a dc signal.

In order to do this, the PWM signal will be passed through a low pass filter, whose cutoff frequency is low enough to minimize the impact of the PWM signal harmonics on the measurement. A first-order *RC* type filter has been chosen, whose cut-off frequency is about four decades below the PWM frequency (80 dB attenuation). Using (2) we can calculate the cutoff frequency of the filter f_{cutoff} and by means of (3) the stabilization time τ. The selected *R* and *C* values are 1 kΩ and 47 nF respectively, so the filter cutoff frequency is 3.38 kHz and the stabilization time is 235 μs.

$$f_{\text{cutoff}} = \frac{1}{2\pi RC} \tag{2}$$

$$\tau = 5 \cdot R \cdot C. \tag{3}$$

In this way, the increase of the value of the duty cycle generated by the fine offset of IDELAYE2 is obtained by measuring the increase of the average value of the PWM signal.

In the case of the proposed design, the average value $\bar{v}$ of the PWM signal depends on its amplitude V_p, its period T_{SW}, the time of the basic counter $T_{\text{on,coarse}}$ and the delay time marked by the number of taps $n_{\text{taps}} \cdot T_{\text{tap}}$, as indicated by the following:

$$\bar{v} = \frac{V_p \cdot T_{\text{on,coarse}}}{T_{\text{SW}}} + \frac{V_p \cdot n_{\text{tap}} \cdot T_{\text{tap}}}{T_{\text{SW}}}. \tag{4}$$

Considering (4), the minimum increase of $\bar{v}$ depends on T_{tap}. The smaller the switching period T_{SW}, the greater the increase in $\bar{v}$ that is added by each tap ($\overline{v_{\text{tap}}}$). In this measurement, the frequency selected for the PWM is 40 MHz ($T_{\text{SW}} = text25ns$). Considering (1), the counter provides only 10 synchronous steps of the duty cycle, while the fine resolution is provided by the 32 taps. Therefore, we achieve a total resolution of 320 taps, approximately 78 ps each, in the duty cycle at 40 MHz. With this frequency value, and knowing that V_p is equal to 3.3 V at the HP pins of the FPGA, it is possible to calculate that the mean value of the PWM signal increases 10.296 mV with a single tap ($\overline{v_{\text{tap}}}$). The number of bits ($n_{\text{bits}}$) required to measure this mean value variation can be calculated using (5), which in this particular case is equal to 9.

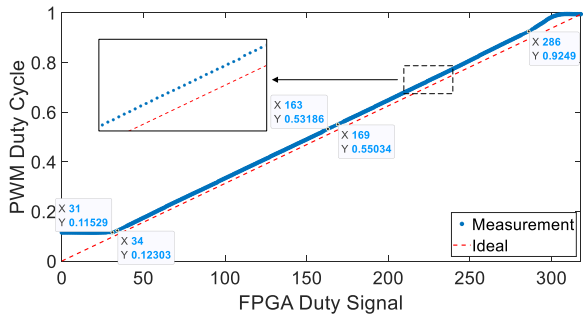

Fig. 4. Measured duty cycle with SET-priority (40 MHz switching frequency).

$$n_{\text{bits}} = \log_2 \left(\frac{V_p}{\overline{v_{\text{tap}}}} \right). \tag{5}$$

For this reason, to carry out the measurements, a data acquisition NI USB-6211 of National Instruments is used, which has a 16-b resolution ADC.

An algorithm is designed to sample automatically the filtered PWM signal with the data acquisition card changing the duty cycle a single tap. Subsequently, the information is post-processed, eliminating the data during the estimated transient time and calculating the average of the remaining data using MATLAB.

3) Experimental Validation With Artix-7: The measurement of the average values of the PWM signal is shows in Fig. 4. For this measurement, we define that the priority of the SRPWM block is given by the SET pin.

It can be observed that, to generate a 40 MHz signal, the width of the signal can be varied in a total of 320 points compared to the 10 that are obtained with a traditional DPWM based on a counter. The architecture has a linear and monotone behaviour. It should be noted that up to 11.6% of the PWM signal (34 taps), the DPWM does not update the duty cycle. The reason is that, for this configuration with SET priority, the SRPWM block needs a minimum time of 2.5 ns between the TON_DELAY and TOFF_DELAY to be able to change between high and low.

In the figure, the measurements are compared to the ideal duty cycle, represented in dotted line. Both lines are parallel, but the measured duty cycle is a little shifted upward, that is, it is a little higher than expected. For instance, for a theoretical duty cycle equal to 10% (32 taps), the effective duty cycle of the PWM is 11.547%. In a converter working close-loop, this fact would not be important because the duty cycle would be determined to get zero error. On the other hand, this offset can be adjusted by modifying the delay of the SET signal in the IDELAYE_SET block.

Finally, from Fig. 4, it is possible to estimate the achieved resolution, by means of the following:

$$T_{\text{tap}} = \frac{|y_2 - y_1|}{|x_2 - x_1|} \cdot \frac{1}{f_{\text{SW}}}. \tag{6}$$

Using the values in Fig. 4, the calculated resolution is 76.9 ps. However, if we divide 400 MHz (CLK_SYS) into 32 parts we get that each division should be 78.125 ps. The difference between 78.125 and 76.9 ps is due to a larger step between the tap 31 and

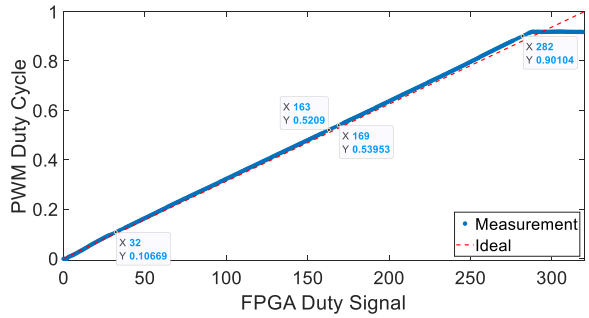

Fig. 5. Measured duty cycle with priority in RESET (40 MHz switching frequency).

the next tap 0. This step can be quantified in 1.225 ps, so the total time for 32 taps is 39.2 ps. Using the extreme values of the linear zone (from 34 to 286) the measured average resolution achieved with this architecture is 79.6 ps.

The same experiment, but giving priority to the RESET in the SRPWM block, is presented in Fig. 5. As it can be seen in the figure, in this case duty cycles below 10% are available. However, with this change in priority, it is no longer possible to generate a duty cycle greater than 90%. Another point to note is that there is a slight change in the slope in the range from 0 to 10% of the duty cycle, but the system continues being monotonic. Setting the priority of the SRPWM block can cover all possible values of the duty cycle according to the design specifications

After the analysis of the DPWM static behavior, a dynamic test was made to observe the time needed by the architecture to update the duty cycle. For this test, a 4 MHz PWM signal was generated and forced to change its duty cycle in the last CLK_SYS count before the period was restarted, that is, on the last step of the counter before the PWM signal starts from 0. The duty cycle changed among 700 (21 counts and 28 taps, 21.87% duty cycle), 1500 (46 counts and 28 taps, 46.87% duty cycle) and 2000 (62 counts and 16 taps, 62.5% duty cycle).

The waveforms measured with the Rohde&Schwarz RTE 1104 1.5 GHz 5 GSa/s oscilloscope are shown in Fig. 6. The upper signal is generated by the FPGA to indicate the instant in which the duty cycle value is updated. Its duration is different to identify which duty cycle value is applied: for the 21.87% signal it is 1 cycle of CLK_SYS (smaller pulse), for the 46.87% signal it is two cycles of CLK_SYS and for the 62.5% signal it is three cycles of CLK_SYS (larger pulse). The lower signal is the PWM signal measured directly at the FPGA pins. As can be seen in the figure, the architecture is able to modify the duty cycle in the next switching cycle of the PWM signal when the new value of duty cycle is updated in the last count before the restart.

C. Implementation on a Kintex-UltraScale 7

In a second approach, the proposed architecture was implemented on a Xilinx Kintex-UltraScale XCKU035-1SFVA784I of series 7, which has a higher cost but better performance than the previous one.

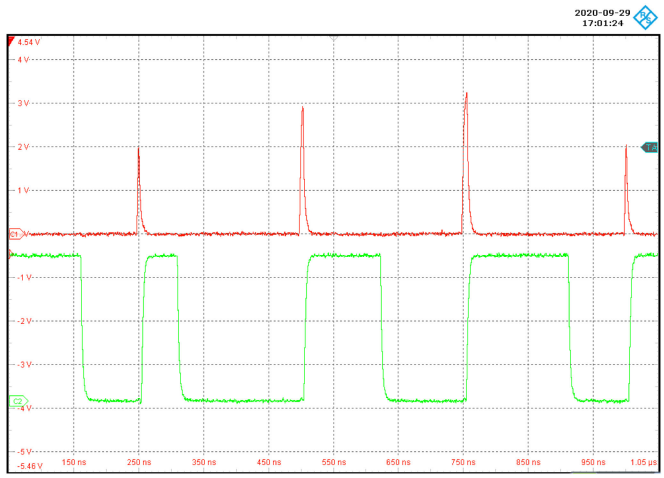

Fig. 6. Dynamic response of Artix-7 architecture to sudden changes of the duty cycle (SET-priority).

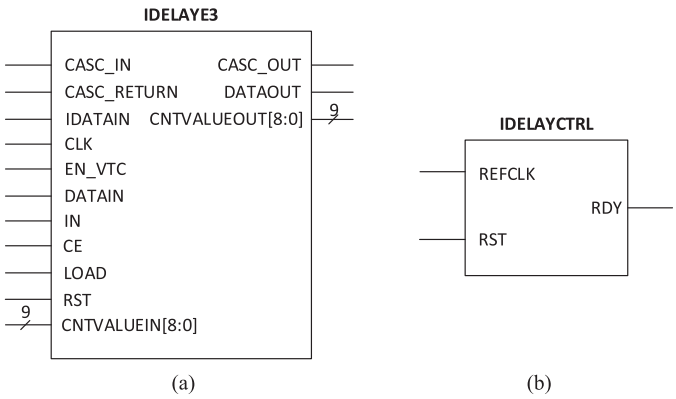

Fig. 7. IDELAYE3 and IDELAYCTRL.

1) IDELAYE3 Configuration: The Kintex-UltraScale uses the IDELAYE3 with 9 b for the resolution. This block is connected to all the HP (High Precision) pins, which work at 1.8 V. There are many more than 100 HP pins in the Kintex-Ultrascale 7. Since the proposed architecture requires two IDELAYE blocks per DPWM, a very high number of hybrid DPWMs could be implemented on one FPGA.

Xilinx Kintex-UltraScale 7 implements the IP blocks by means of IDELAYE3 [26] (see Fig. 7). This IP block is similar to the IDELAYE2 block. The principal differences are:

1) The fine resolution is determined by a 9-b CNTVALUEIN, 4 b more than IDELAYE2. In total it has 512 taps that allow adjusting the delay of the DATAIN signal.
2) The IDELAYE3 block has a pin called EN_VTC that allows activating a voltage and temperature compensation function. However, we deactivated this pin because it requires several cycles of the clock to self-adjust the delay value when changing the value of CNTVALUEIN, opting for faster response time instead of increased time stability.
3) In the IDELAY3, the method of updating the value of the delay line can be asynchronous, synchronous and manual. Asynchronous mode allows changing the delay

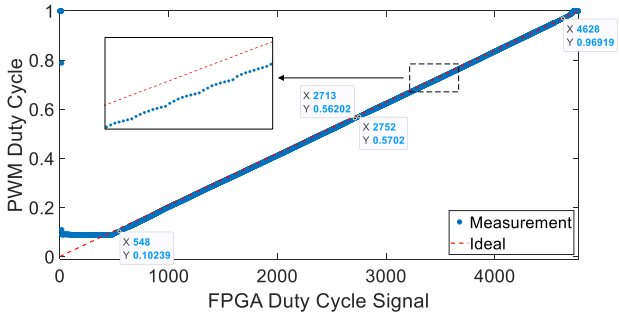

Fig. 8. Measured Kintex-UltraScale 7 duty cycle with priority in SET (45 MHz switching frequency).

value without needing the CLK and this setting was chosen for the sake of faster updates.

The IDELAYCTRL can be configure by the reference clock (REFCLK) with one value between 200-800 MHz, this frequency selects the value of the delay introduced by each tap. By default, the used frequency of REFCLK is 300 MHz.

For our design, we configured IDELAYE3 with 300 MHz of CLK and REFCLK. The design was simulated using the Vivado tool to find out the resolution obtained with the IDELAYE3, being 5 ps the delay of a single tap. Thus, with this configuration it is possible to delay 2.55 ns using 512 taps for each step of the counter, which would be equivalent to a frequency of 390 MHz. To increase the maximum frequency that could be generated for the PWM signal, we decided to increase the CLK_SYS clock frequency to 450 MHz instead of 390 MHz. Therefore, to adjust the delay line to the period value of CLK_SYS, only the first 477 taps of the 512 available are used. This value was adjusted after implementing the architecture and measuring the necessary taps for that frequency.

2) Experimental Validation With the Kintex-UltraScale 7: The measured average values of the 45 MHz PWM signal are plotted from 0 to 1 of the duty cycle in Fig. 8. For these measurements, the SRPWM has a configuration with SET priority. According to the parameters mentioned before, there is a total of 4770 points to determine the duty cycle of the PWM signal. From the figure, it can be appreciated a linear and monotone behaviour. However, from the zoom shown in the figure it can be observed that there are slight differences in the duration of the taps, though the system remains increasing monotonously.

Using the values shown in Fig. 8 for a switching frequency of 45 MHz, the measured resolution of IDELAYE3 is approximately to 4.661 ps. However, due to the higher steps every 477 taps, the effective resolution is around of 4.72 ps.

If we compare both zooms for IDELAYE2 and IDELAYE3, for IDELAYE3 the increase between taps is less linear than for IDELAYE2. Knowing that each tap must be 4.658 ps (for 477 taps in total) using a 450 MHz CLK_SYS, the duty cycle error due to each tap between the comparator divisions has a deviation approximate of 1.431 ps.

To perform the dynamic test, a frequency of 4.5 MHz is used and, as done before, three different values of the duty cycle are swept to check the time it takes the system to change this value. The considered duty cycle values are: 10 000 (20 counts and 460 taps, 20.964%), 23 000 (48 counts and 104 taps, 48.218%), 35 770 (74 counts and 472 taps, 74.989%). As it was done for the Artix-7, the value of the duty cycle is updated in the last period before the counter is restarted.

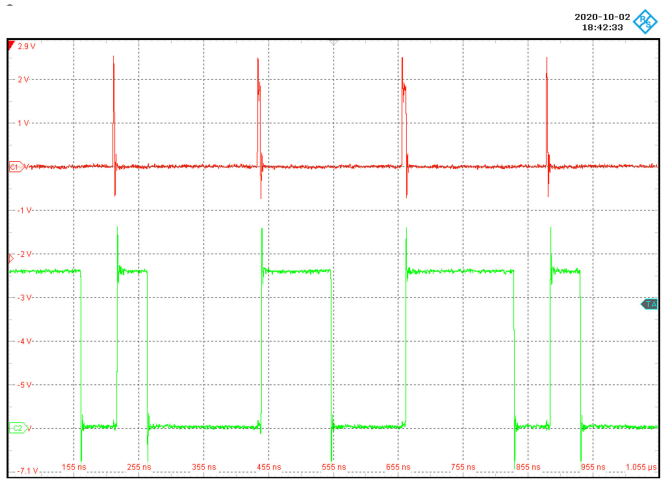

Fig. 9. Dynamic respond of Kintex-Ultrascale 7 architecture (SET-priority).

The waveforms measured for the Kintex-UltraScale 7 are shown in Fig. 9. The pulse width duration of the upper signal indicates, as before, which duty cycle value it corresponds to. For the 20.946% duty cycle, this signal lasts 1 cycle of CLK_SYS (smaller signal), for the 48.218% value the signal lasts 2 cycles of CLK_SYS and for the 74.989% signal it corresponds to three cycles duration of CLK_SYS. As can be seen in the figure, there is one clock of CLK_SYS since the value of the duty cycle is updated in the PWM signal before restart the count. It is interesting for digital control because these FPGAs can load and update the new duty cycle value in the last count of the period.

III. Complementary PWM Architecture

A. Proposed Architecture

Given the results obtained by the proposed architecture with the use of IDELAYE as programmable delay lines, we decided to implement another architecture with the objective of controlling complementary signals, for example for half- bridge topologies. One of the main advantages of a high resolution is the ability to precisely adjust the dead times of architectures that use structures of this kind.

In this section, we present an architecture for a half-bridge where the main generated signal is the PWM_0 signal and the complementary signal is PWM_1 (see Fig. 10).

Comparing this architecture with the one shown in Fig. 1, the synchronous and the asynchronous parts have the same blocks. However, in the COUNT+COMP block a modification has been made: the new input of this block is DEAD_TIME, which allows controlling the specified dead time between the trigger signals PWM_0 and PWM_1. As shown in Fig. 11, in this implementation, Δt_0 is equal to zero, Δt_1 is used to finely tune the duty cycle of PWM_0, Δt_2 and Δt_3 are used to fix

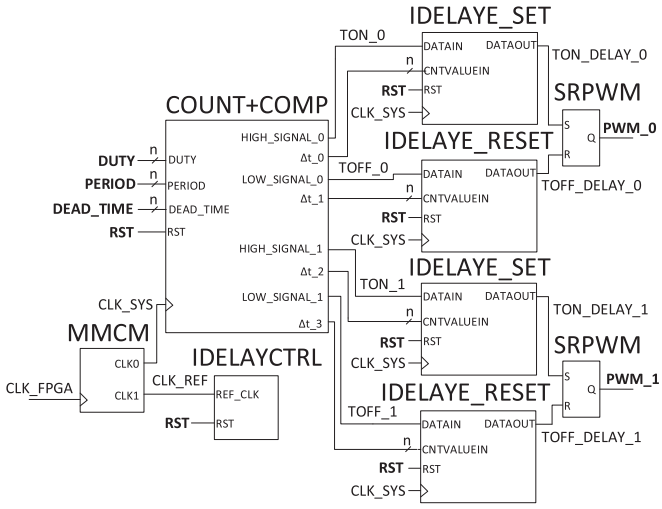

Fig. 10. Hybrid high-resolution DPWM with complementary signal.

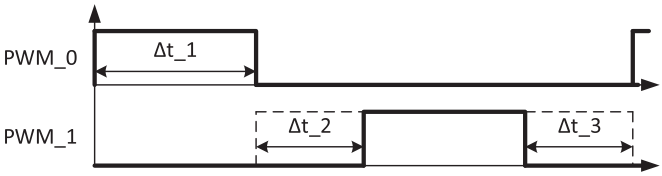

Fig. 11. Generated complementary signals.

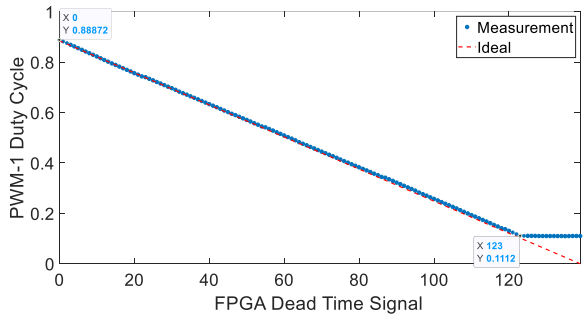

Fig. 12. Measured PWM_1 duty cycle (Artix-7 with SET-priority).

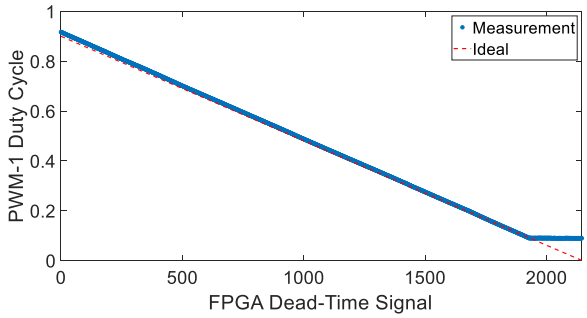

Fig. 13. Measured PWM_1 duty cycle (Kintex-UltraScale 7 with SET-priority).

the dead time. The rising edge of the PWM_1 signal is delayed and the falling edge is advanced according to Δt_2 and Δt_3 respectively, to set the proper dead time.

B. Artix-7 Measurement

Two 40 MHz signals (PWM_0 and PWM_1) are generated for this measurement, and the configuration of the IDELAY is the same as in the previous section. The complementary signal PWM_1 is passed through the previously calculated low-pass filter and its average value is measured. Increasing the dead time with a constant duty cycle of PWM_0, means that the effective duty cycle of PWM_1 is reduced. So, in order to make a complete sweep of the dead time, the PWM_0 signal is set to its minimum value (11.6% according to Fig. 4). Then, the dead time value of PWM_1 signal will be increased so that the effective duty cycle of that signal goes from less than 90% to 0% (0 to 144 taps of the FPGA).

It is important to highlight that, due to the high working frequencies and the high resolution, slight differences in the routing could have an impact on the operation. For example, slight differences in the routing of the SET and RESET for the PWM_0 and the PWM_1 yield an effective duty cycle higher than expected, which means that both signals are not perfectly complementary. This issue can be easily compensated by measuring the duty cycle of both signals and including the required dead time, which should be only few taps.

The results of the dead time sweep are shown in Fig. 12. The blue line represents the duty cycle obtained by measuring the mean value of the PWM_1 signal. The dotted line corresponds to the ideal value of the duty cycle. As the dead time increases, the effective duty cycle decreases and the measurements match well the ideal values. In the points closest to 10% of the duty cycle (nonrealistic high dead time), the value of the PWM_1 signal is above the ideal value and cannot be lower than 10% because of the SET-priority, as explained before.

C. Kintex-Ultrascale 7 Measurement

The same experiment has been performed using the Kintex-UltraScale 7 with a PWM switching frequency of 45 MHz. One more time, the complementary signal PWM_1 is passed through the designed filter to measure the average voltage of the signal. As the PWM_0 signal has 10% of duty cycle, values for the IDELAYE3 dead time signal will be swept from 0 to 2147, equivalent to a dead time of 0 (90% duty cycle) and 10% duty cycle (because of the limitations associated to the SET-priority).

The results of the dead time value sweeps for this FPGA are presented in Fig. 13. The line corresponds to the measured average duty cycle and the dotted line is the ideal effective duty cycle for each dead time value. It can be seen that both lines are very close, giving this architecture a very good linearity to generate these dead times.

IV. Experimental Measurements on a DC/DC Converter Using Complementary PWM Implemented on the Artix-7 FPGA

In this section, we will test the complementary PWM architecture controlling an actual power converter. This experiment is interesting because the FPGA output signal is affected by other

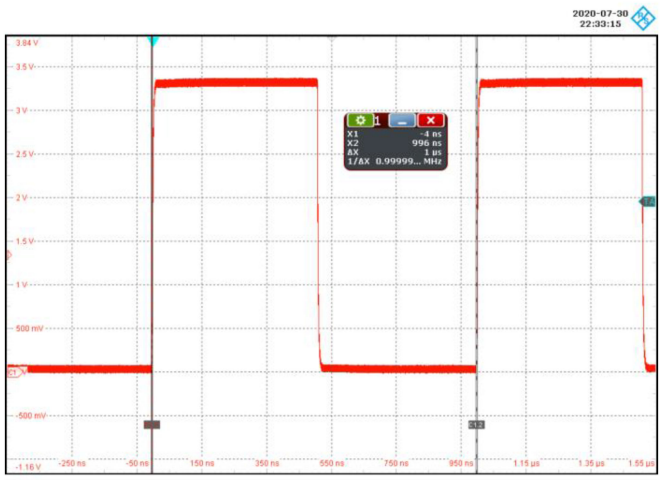

Fig. 14. PWM signal at the output pin of the Artix-7 FPGA.

elements of the circuit. For instance, for high frequencies, the routing and the driver play an important role in the performance of the power converters.

We have designed a synchronous buck converter using the LMG5200 Half Bridge power stage, because of two reasons: 1) it incorporates integrated drivers along with the half bridge; 2) the Artix-7 HR pins at 3.3 V can be directly connected to the LMG5200 control inputs (the typical driver voltage threshold is around 2 V). The frequency of the generated PWM signal is 1 MHz and the converter input voltage is 5 V. A 50% duty cycle is used, with a dead time of 5 taps affecting both sides of the complementary signal, which should be approximately 380 ps.

A. Artix-7 Output Signals

In this first test, the output of the PWM signal was measured directly at the pins of the FPGA. The waveform of the 1 MHz PWM_0 signal is depicted in Fig. 14.

To measure the time per tap in the voltage waveforms, a PWM_0 signal of 50% was generated and, after several periods, the duty cycle was increased by 100 taps. The increase of each tap in the Artix-7, calculated from the measurements of the mean duty cycle, was 76.9 ps. So, the time increase due to 100 taps should be 7.69 ns. However, it is important to take into account the additional 39.2 ps due to the adjustment of the 32 taps in each subdivision of the clock. The measured waveforms from this test are depicted in Fig. 15. It can be seen that the increase of the signal is 7.8 ns, which validates the calculations.

This measurement also allows to obtain an estimation of the signal jitter. The measurement was performed using a persistence mode, which superimposes multiple waveforms on the same view. The points that are repeated most frequently are represented with warm colors, while the less repeated measured values are in blue tones. Measuring the time variation between the most extreme values of this persistence measurement, the maximum variation of the signal is approximately 250 ps. Note that the oscilloscope has 5 Gsa/s, that is, 200 ps resolution.

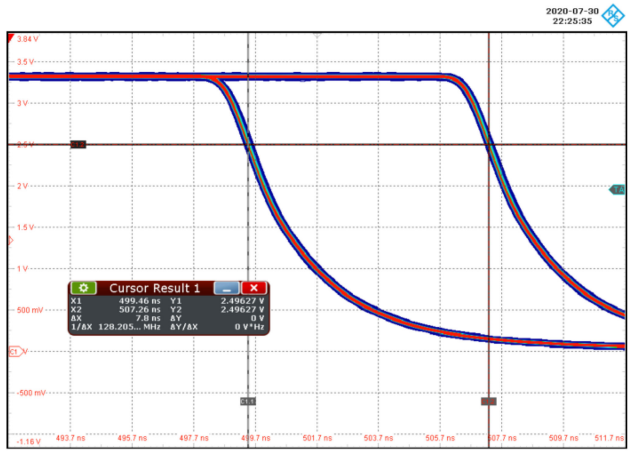

Fig. 15. Measurement of 100-tap increase in the duty cycle.

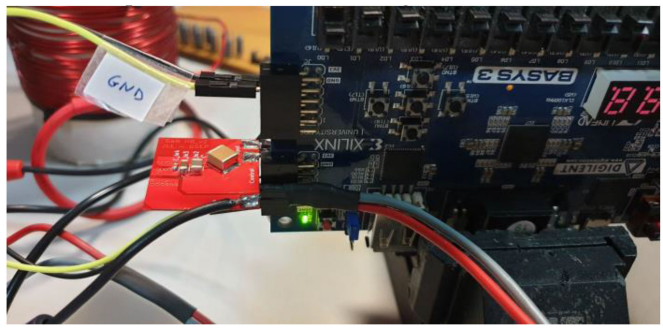

Fig. 16. Connection of the Basys3 with the drivers board.

Fig. 17. Measured voltage at the output of LMG5200 half bridge.

Fig. 16 shows the connection of the LMG5200 half bridge power stage and the Basys3 board without the output filter. Since the LMG5200 incorporates integrated drivers, the effects that can be produced due to the routing are reduced.

The voltage waveform on the central node of the half bridge is displayed in Fig. 17, where the measurement was taken in persistence mode. The figure also shows the measured persistence results, where the average frequency is 1 MHz and the duty cycle is 50.3%.

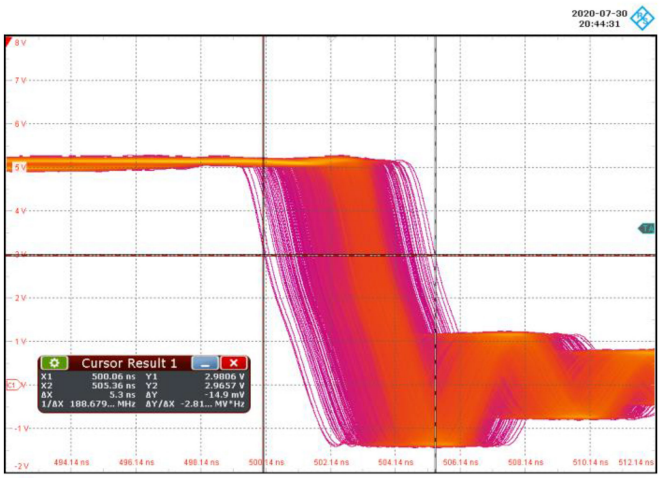

Fig. 18. Persistence measurement of the PWM falling edge, measured at the output of the LMG 5200.

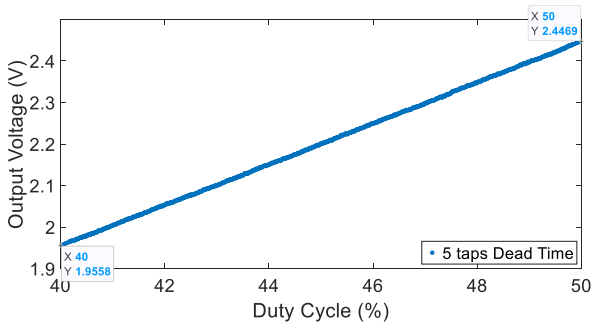

Fig. 19 Measured output voltage with 1 MHz switching frequency and 380 ps dead time.

A zoom of the trailing edge in Fig. 17 is shown in Fig. 18. If we compare this signal with the one obtained at the FPGA pins (see Fig. 14), the variation for the same value of the duty cycle increases. In this case the variation measured with the cursors is 5.2 ns. The LMG5200 datasheet defines a variability between 2 and 8 ns in the edges of the generated signals. Compared to the variation generated by the FPGA, the driver has a much more important variation effect for the generated signal.

Finally, a synchronous buck converter was built with the same conditions described above (5 V at the input, 1 MHz switching frequency and 380 ps dead time). A duty cycle sweeps similar to the one shown in Fig. 4 was done, to measure the output voltage of the converter, as depicted in Fig. 19. In this case, it was obtained by sweeping from 40% to 50% duty cycle. Since the frequency is 1 MHz, there are 1280 possible values of duty cycle points within this range.

As shown in Fig. 19, the output voltage of the converter increases linearly with increasing duty cycle. This output voltage varies from 1.9558 V with a 40% duty cycle to the value of 2.4469 V with a 50% duty cycle. Considering that in this interval there are 1280 duty cycle values, the output voltage increases 0.384 mV per tap. This value is equivalent to increase the duty cycle 76.8 ps per tap, which matches the 76.9 ps measured at 40 MHz (see Fig. 4). This is in good agreement with the expected

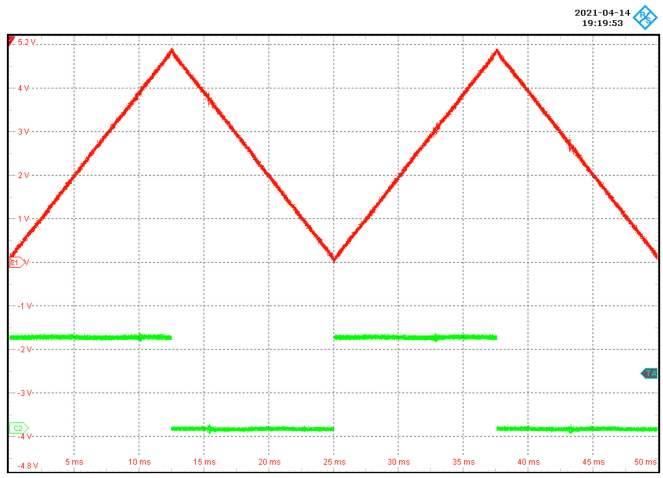

Fig. 20. Measured output voltage following a triangular reference, when duty cycle is varying tap by tap.

voltage resolution, which is 0.39 mV/tap (input voltage 5 V divided by the total number of taps 12 800).

An additional test has been performed to the converter driven by the proposed DPWM, modifying the duty cycle according to a triangular waveform changing tap by tap. The measured waveforms are depicted in Fig. 20: red line is the measured output voltage and green line is the reference trigger signal (1 when the duty cycle starts to increase, 0 when it starts decreasing). From these measurements, we can obtain the following conclusions.

1) The total available number of taps for a 1 MHz switching frequency is 12 800 and the duty cycle sweep goes from 130 to 12670 taps. Consequently, the period of the resulting triangular waveform should be 25.08 ms, which is in good agreement with the measurement.
2) The evolution of the output voltage is perfectly synchronized with the evolution of the duty cycle. Moreover, there is no delay, since the output voltage begins to increase from its lowest value at the same time as the duty cycle begins to increase.

V. Conclusion

In this work, we present a hybrid DPWM architecture of high resolution that can be scalable to other FPGAs either low or high end, according to the required specifications. For the proposed DPWM architecture, FPGA IP blocks are used as programmable delay lines, with the advantage that they do not require manual placement nor calibration. The experimentally measured resolutions of the IPs for two different FPGAs are 76.9 ps for the IDELAYE2 block of the Xilinx Artix-7 and 4.658 ps for the IDELAYE3 block of the Xilinx Kintex-UltraScale 7.

Additionally, a new DPWM architecture that allows the generation of high-resolution dead times has been presented and tested for the two mentioned FPGAs. The measured time resolution for the Artix-7 is 79.6 ps, while for the Kintex-UltraScale 7 the average resolution is 4.72 ps. This resolution of 4.72 ps is much higher than the minimum registered in the state of the art of 19.5 ps. In both architectures a great linearity and a monotonic

behaviour is appreciated and the duty cycle does not require several clocks to be updated.

Finally, more experimental tests were carried out driving a synchronous buck converter with the Artix-7, switching at 1 MHz and with 5 V input voltage. The duty cycle was swept from 40% to 50%. The measured output voltage is linear, the output voltage increases 0.384 mV and the measured time resolution is 76.8 ps.

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