Averaged Modeling and SRF-Based Closed-Loop Control of Single-Phase ANPC Inverter

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***Abstract*—This article presents a dynamic averaged model of active neutral point clamped inverter (ANPCI). The proposed model helps in significant reduction of computational resources required for system-level studies in various applications which employ ANPCI as main power conversion stage. The average model derived in this article can consider the effect of various nonidealities in ANPCI, and also its capacitor voltage-balancing issues. The model is also modular in nature, i.e., it can be extended for an N-level ANPCI. PSCAD/EMTDC simulations and experiments are performed for steady-state and transient conditions to show that the averaged model developed in this article accurately predicts the steady-state and dynamic waveforms of ANPCI in both open-loop and closed-loop operations, even for large simulation time-steps. For the closed-loop operation, synchronous reference frame *dq*-based controller is developed and implemented in a digital signal processor. In addition, the strength of the model is demonstrated by comparing the simulation waveforms and computational times required for simulating an ANPCI-based solar PV system using switching circuit model and the proposed averaged model.**

***Index Terms*—5L-ANPC converter, ANPCI-based PV system, average circuit model, capacitor voltage balancing, SRF-dq control.**

I. Introduction

MODELING and computer-based simulations are the essential steps for design and analysis of power-electronic-based systems such as microgrids, industrial drives, and solar and wind energy conversion systems, etc [1]–[8]. For these system-level studies, the power electronic converters can be modeled and simulated by using either detailed switching circuit or averaged model. The switching circuit model (SCM)-based approach simulates every switching instant of the power semiconductor devices and it is used for capturing the switching frequency components in the converter waveforms. Here, the simulation time-step should be much less than the switching time period of the converter. Hence, the SCM-based simulations require extensive computational resources while performing system-level studies, involving large number of power electronic converters. On the other hand, the averaged models of power electronic converters are developed by approximating the converter waveforms after omitting the switching-frequency components. Using the averaged model based approach, the averaged steady-state and dynamic waveforms of the converters can be accurately predicted with fairly large simulation time-steps. For system-level studies, the average model-based approach will significantly reduce the time and computational resources required for the study. Although the converter switching frequency components cannot be evaluated using averaged models, they are generally of less interest while analyzing large-scale electrical systems.

In the literature, various average modeling approaches are presented for power electronic converters. Early works on average modeling are mainly focused on dc–dc converters and diode/thyristor-based rectifiers. The synthesis of equivalent averaged circuit models for different dc–dc converters using state-space averaging and in-place or direct-circuit averaging has been described in [4], [9]. In [5], [6], [10], dynamic average value models are presented for line commutated converter-synchronous machine system using analytical average value modeling (AAVM) approach. Here, the ac-side variables of the system in each subinterval of a particular switching interval are transformed into *dq*-reference frame and then their averaged values are determined analytically. These averaged values in each subinterval are carefully integrated to obtain the averaged value model for a given operating mode. In [7], [8], parametric average value models (PAVM) are developed for the machine-rectifier systems. In this approach, the average-value relationship among the variables is established using different parametric functions, which are generally determined by simulating the detailed system model. Unlike AAVM, the PAVM is easier to develop and it can be used to simulate the converter in a wide range of operating conditions.

The averaged models of pulsewidth-modulated (PWM) two-level and multilevel inverters (MLIs) are presented in [11]–[16]. In [11], state-space averaging approach is used to obtain two separate models for positive and negative half-cycle of the filter inductor current, resulting in a discontinuous converter model. In [12], a comprehensive dynamic model of three-phase four-level diode clamped inverter is derived based on the generalized state-space averaging method. The authors have used line-cycle averaging to remove the discontinuity in the converter model. However, line-cycle averaging limits the validity of the model to half the fundamental frequency. In [13], differential equations-based modeling is used based on state-space form.

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The switches are considered as ideal and unity power factor operation is assumed. Averaged model of a three-level neutral-point clamped (NPC) multilevel inverter (MLI) using switching-cycle averaging is presented in [14], which is valid up to half the switching frequency. In [15], two-stage inverter is modeled by splitting the inverter into two buck converters and then dc–dc averaged modeling approach is applied for the averaged circuit model. In [16], generalized average models for PWM inverters are proposed based on a quasi-Fourier series representation of the switching functions that includes fundamental and switching frequency components as well as sideband components of the switching frequency. These generalized average models are suitable for simulation applications in which both fundamental and switching behavior have to be predicted accurately with fast run times. These models run faster than the detailed model and slower than the state-space averaged model in simulation.

In this article, dynamic average circuit model (DACM) has been developed for a single-phase five-level active neutral point clamped inverter (ANPCI). The key contributions of this article are listed as follows.

1) The circuit diagram, switching states, and steady-state operation of single-phase five-level ANPCI are explained in detail. In each switching state of the converter, the relation between charging/discharging conditions of the capacitors and the inductor current is determined.
2) The phase disposition and shifting (PDS) PWM technique is applied for gate signal generation of ANPCI, because it generates lower total harmonic distortion (THD) compared to conventional PWM techniques of MLIs.
3) Based on the charging/discharging conditions of the capacitors in each switching state of ANPCI, a capacitor voltage balancing algorithm is developed and explained in detail. The algorithm is successful in regulating the capacitor voltages of ANPCI to their respective reference values.
4) DACM with capacitor voltage balancing has been developed for ANPCI without nonidealities using step-by-step procedure. Further, the model is developed by considering nonidealities also. Unlike AAVM and PAVM, the model does not have complex mathematical equations. Also, the model can be directly simulated using any standard circuit simulation software. The model is also modular in nature and valid for all the operating conditions of the converter. The model significantly reduces the computational resources and execution times while analyzing or designing power electronic systems involving ANPCI.
5) A closed-loop synchronous reference frame (SRF)-dq controller is developed for the single-phase ANPCI. The controller is also implemented in a stand-alone PV system using ANPCI.
6) Extensive experimental and simulation results are presented to validate the operation, capacitor voltage-balancing algorithm, and DACM of the ANPCI. The results demonstrate the advantages and the strength of the average model developed for ANPCI.

The organization of the article is as follows. Section II describes the advantages of ANPCI, its circuit diagram, and detailed operation. The PWM technique and capacitor voltage-balancing algorithm implemented in this article are also given in Section II. Section III presents the step-by-step procedure to develop the average circuit model of ANPCI. The SRF-dq closed-loop controller of single-phase ANPCI is given in Section IV. Section V presents the experimental results to validate the PDS-PWM technique, capacitor voltage-balancing algorithm, and SRF-dq controller for ANPCI. Further, this section also presents results for validation of the DACM in open-loop and closed-loop operations of ANPCI. Section VI describes the operation of a standalone PV system with SRF-dq-controlled ANPCI as power converter interface. Section VI also presents the results to demonstrate strength of the DACM developed in this article. Finally, Section VII concludes the article.

II. ANPCI: Circuit Diagram and Operation

The concept of multilevel power conversion using five-level ANPCI is introduced in [17]. The ANPCI can be seen as a combination of two popular MLIs, viz., NPC MLI and flying capacitor (FC) MLI, and hence it combines the features of both these MLI topologies [18]. Unlike NPC MLI, the ANPCI has redundant switching states to balance the capacitor voltages. Due to the increased number of switching states in ANPCI, a loss-balancing control can be implemented for equal distribution of power losses and junction temperature among its switches [19]. Therefore, the power-handling capability of ANPCI can be increased further compared with the NPC MLI. Owing to its advantages, the ANPCI has been proposed as an alternative to the NPC MLI in medium voltage drives and renewable energy applications [20]–[23]. In [24], [25], the authors have mentioned that five-level active-neutral-point-clamped converter is the only commercially available five-level multilevel converter, which does not require multiple isolated dc sources. Due to the advantages and increasing applications of ANPCI, in this article, an average circuit model has been developed for this topology. The model significantly reduces the computational resources and execution times while analyzing or designing power electronic systems involving ANPCI.

This section describes the operation, PWM control, and capacitor voltage balancing of ANPCI. The average modeling is developed in Section III.

A. Circuit Diagram and Steady-State Operation

Fig. 1 shows the circuit diagram of single-phase five-level ANPCI consisting of two dc-link capacitors C_1 and C_2, one flying capacitor FC, and eight switches S_1 to S_8, each with an antiparallel diode. The average voltage across each of the capacitors C_1 and C_2 is maintained at 50% of the input voltage, V_{DC}, while the average voltage across FC is maintained at 25% of V_{DC}. At any instant of time, the PWM output voltage v_{an} can be equal to any one of the five voltage levels: $+\frac{V_{DC}}{2}$, $+\frac{V_{DC}}{4}$, 0, $-\frac{V_{DC}}{4}$, and $-\frac{V_{DC}}{2}$. The LC filter, consisting of L_f and C_f, filters out the switching frequency components in five-level PWM voltage v_{an} so that the load voltage v_o is pure sinusoidal waveform.

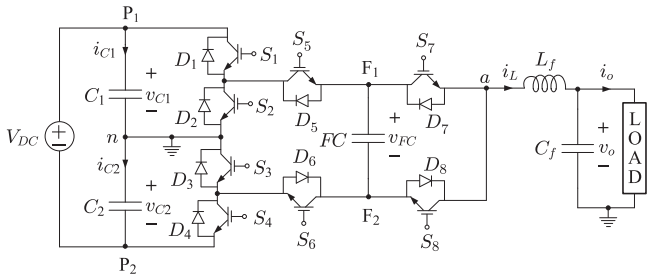

Fig. 1. Circuit diagram of single-phase five-level ANPCI.

TABLE I
POSSIBLE SWITCHING STATES FOR THE ANPCI OF Fig. 1

State	v_{an}	Switch positions*			$i_L > 0$			$i_L < 0$		
		S_1	S_5	S_7	v_{C1}	v_{C2}	v_{FC}	v_{C1}	v_{C2}	v_{FC}
I	$+\frac{V_{DC}}{2}$	1	1	1	↓	↑	—	↑	↓	—
II	$+\frac{V_{DC}}{4}$	1	1	0	↓	↑	↑	↑	↓	↓
III	$+\frac{V_{DC}}{4}$	1	0	1	—	—	↓	—	—	↑
IV	0	1	0	0	—	—	—	—	—	—
V	0	0	1	1	—	—	—	—	—	—
VI	$-\frac{V_{DC}}{4}$	0	1	0	—	—	↑	—	—	↓
VII	$-\frac{V_{DC}}{4}$	0	0	1	↓	↑	↓	↑	↓	↑
VIII	$-\frac{V_{DC}}{2}$	0	0	0	↓	↑	—	↑	↓	—

* $S_2 = S_4 = S_1'$, $S_3 = S_1$, $S_6 = S_5'$ and $S_8 = S_7'$; S_1', S_5', and S_7' are the logical complements of S_1, S_5, and S_7, respectively.

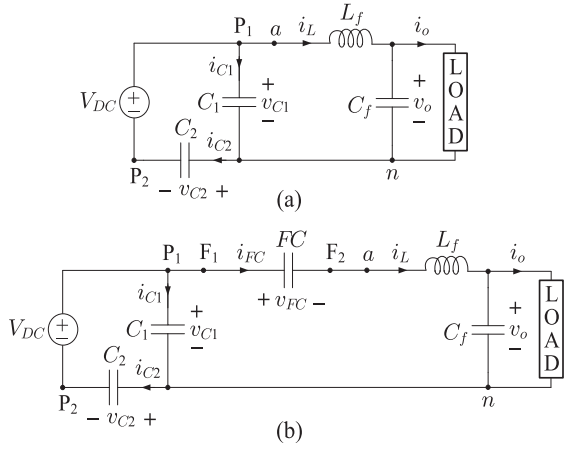

Fig. 2. Equivalent circuits for ANPCI in (a) State-I and (b) State-II.

Table I lists eight possible switching states of ANPCI and the corresponding voltage level, v_{an}. Although ANPCI has eight switches, there are only three independent switching signals: S_1, S_5, and S_7. Other five switching signals can be obtained as $S_2 = S_4 = S_1'$, $S_3 = S_1$, $S_6 = S_5'$, and $S_8 = S_7'$. In Table I, redundant switching states are available for voltage levels: $+\frac{V_{DC}}{4}$, 0, and $-\frac{V_{DC}}{4}$. Fig. 2(a) shows the equivalent circuit of ANPCI in State I, in which the switches S_1, S_3, S_5, S_7 are ON and S_2, S_4, S_6, S_8 are OFF. The PWM voltage v_{an} is equal to v_{C1} as capacitor C_1 is directly connected between nodes a and n.

To determine the effect of i_L on capacitor voltages v_{C1} and v_{C2}, one can write from Fig. 2(a)

$$i_L = -i_{C1} + i_{C2} \tag{1}$$

$$V_{DC} = v_{C1} + v_{C2}. \tag{2}$$

Differentiating (2) on both sides and noting that V_{DC} is constant

$$\frac{dv_{C1}}{dt} = -\frac{dv_{C2}}{dt}. \tag{3}$$

Also, the capacitor currents, i_{C1} and i_{C2}, can be expressed as

$$i_{C1} = C_1\frac{dv_{C1}}{dt} \quad \text{and} \quad i_{C2} = C_2\frac{dv_{C2}}{dt}. \tag{4}$$

Assuming $C_1 = C_2$, and using (1), (3), and (4), it can be shown that

$$i_{C1} = -i_{C2} = -\frac{i_L}{2}. \tag{5}$$

From (4) and (5), it can be concluded that if i_L is positive, v_{C1} decreases and v_{C2} increases as mentioned in Table I. Similarly if i_L is negative, v_{C1} increases and v_{C2} decreases. Note that in State I, FC is not connected in the circuit and hence v_{FC} is unaffected in this state.

Fig. 2(b) shows the equivalent circuit of ANPCI in State II, in which switches S_1, S_3, S_5, and S_8 are ON and S_2, S_4, S_6, and S_7 are OFF. The PWM voltage v_{an} is equal to $(v_{C1} - v_{FC})$ in this state. Here FC is connected in series with L_f and, hence,

$$i_{FC} = (FC)\frac{dv_{FC}}{dt} = i_L. \tag{6}$$

Therefore, if i_L is positive, v_{FC} increases and if i_L is negative, v_{FC} decreases. Note that (1)−(5) are valid in this state also as $i_{FC} = i_L$. Thus, the effect of i_L on v_{C1} and v_{C2} is the same as that determined in State I. Using similar analysis, the effect of i_L on v_{C1}, v_{C2}, and v_{FC} is determined in other switching states and listed in Table I.

B. PWM Technique

Phase disposition (PD), phase opposition disposition, and alternative phase opposition disposition techniques are widely known PWM techniques for generating switching signals for NPC MLI [26], [27]. These methods can be easily extended for generating switching signals of ANPCI. However, in this article, the PDS-PWM technique is chosen as it produces lowest THD output voltage for single-phase ANPCI [28]–[30]. Because in PDS-PWM technique, the effective switching frequency of ANPCI is two times the carrier frequency due to which the dominant harmonics in v_{an} will appear at twice the carrier frequency.

Fig. 3 shows the PDS-PWM technique which involves comparison of a sinusoidal modulation signal, $m_a = M \cdot \sin(\omega_o t)$, with four triangular carrier signals: v_{t1}, v_{t2}, v_{t3}, and v_{t4}. The carrier signals, v_{t1} and v_{t2} vary from 0 to 1, while v_{t3} and v_{t4} vary from 0 to -1. Also, the signals v_{t2} and v_{t4} are 180° phase shifted from v_{t1} and v_{t3}, respectively. The peak of m_a is called the

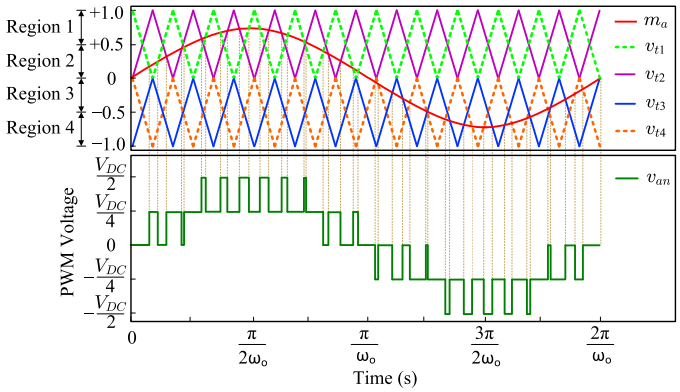

Fig. 3. Generation of PWM voltage (v_{an}) using PDS-PWM technique by comparison of modulation (m_a) and carrier signals (v_{t1}, v_{t2}, v_{t3}, and v_{t4}).

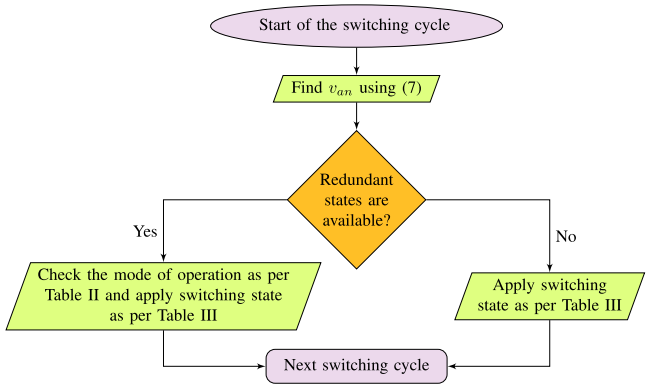

Fig. 4. Flowchart for implementation of capacitor voltage balancing algorithm.

modulation index, M. Based on the instantaneous value of m_a, four different regions are defined in Fig. 3. The PWM voltage level, v_{an}, in each of these four regions is determined depending on the relative values of modulation and carrier signals, as given in (7a)−(7d).

$$\text{Region 1: } v_{an} = \begin{cases} +\frac{V_{DC}}{2} & \text{if } m_a > v_{t1} \text{ and } m_a > v_{t2} \\ +\frac{V_{DC}}{4} & \text{if } m_a < v_{t1} \text{ or } m_a < v_{t2} \end{cases} \quad (7a)$$

$$\text{Region 2: } v_{an} = \begin{cases} +\frac{V_{DC}}{4} & \text{if } m_a > v_{t1} \text{ or } m_a > v_{t2} \\ 0 & \text{if } m_a < v_{t1} \text{ and } m_a < v_{t2} \end{cases} \quad (7b)$$

$$\text{Region 3: } v_{an} = \begin{cases} 0 & \text{if } m_a > v_{t3} \text{ and } m_a > v_{t4} \\ -\frac{V_{DC}}{4} & \text{if } m_a < v_{t3} \text{ or } m_a < v_{t4} \end{cases} \quad (7c)$$

$$\text{Region 4: } v_{an} = \begin{cases} -\frac{V_{DC}}{4} & \text{if } m_a > v_{t3} \text{ or } m_a > v_{t4} \\ -\frac{V_{DC}}{2} & \text{if } m_a < v_{t3} \text{ and } m_a < v_{t4}. \end{cases} \quad (7d)$$

Once the desired value of v_{an} is determined using (7), the switching state to be applied can be found from Table I. Note that if $v_{an} = +\frac{V_{DC}}{2}$ or $-\frac{V_{DC}}{2}$, there is only one possible switching state that can be applied. However, if $v_{an} = \pm\frac{V_{DC}}{4}$ or 0, redundant switching combinations are available in Table I. The choice between these redundant switching states is made by the capacitor voltage balancing algorithm, which will be explained in the next subsection. The main objective here is to maintain the FC voltage to be within the range $\frac{V_{DC}}{4} \pm \epsilon$ and dc-link capacitor voltages to be within the range $\frac{V_{DC}}{2} \pm \epsilon$. Here ϵ is a predefined tolerance for the capacitor voltages based on their allowable deviations from the respective nominal values.

C. Capacitor Voltage Balancing Algorithm

To achieve dc-link capacitor voltage balancing and FC voltage regulation in ANPCI, many modulation strategies have been presented [31], such as phase-shifted PWM (PS-PWM) [30], selective-harmonic-elimination (SHE) PWM [32], and zero-sequence voltage injection [33]. However, these methods are suitable for three-phase applications only. In single-phase applications, the dc-link of the ANPCI may also experience voltage variation and it is important to keep the dc-link neutral point voltage balanced using a suitable method. In [34], optimized

TABLE II
OPERATING MODES OF ANPCI DEFINED BASED ON THE DEVIATION OF THE CAPACITOR VOLTAGES

Condition for capacitor voltages		Mode of operation
v_{FC}	v_{C1}	
$v_{FC} < v_{FC}^* - \epsilon$	—	M1
$v_{FC} > v_{FC}^* + \epsilon$	—	M2
$v_{FC}^* - \epsilon < v_{FC} < v_{FC}^* + \epsilon$	$v_{C1} < v_{C1}^* - \epsilon$	M3
	$v_{C1} > v_{C1}^* + \epsilon$	M4
	$v_{C1}^* - \epsilon < v_{C1} < v_{C1}^* + \epsilon$	M5

switching pulse patterns for single-phase five-level ANPCI are obtained based on SHE and iterative method. The basic objective is to maintain THD and individual harmonic magnitudes below the acceptable range. If there are multiple pulse patterns meeting these objectives, then the solution with minimum FC voltage deviation is chosen which helps in FC voltage regulation. But no information is given in [34] about dc-link capacitor voltage balancing. In [35], the authors have designed a modulation method of controlling FC voltage to follow the dc-link capacitor voltage. However, because in each half-cycle only one dc-link capacitor is providing the energy, it will have a line-frequency voltage disturbance, resulting in the line frequency voltage ripple in FC. Additionally, after each zero-crossing point of output current, the FC voltage will change suddenly because its reference voltage is changed. So, the complexity of modulation is increased to reduce THD in the output current. In [36], a simplified single-carrier PWM method for single-phase five-level ANPCI with capacitor voltage self-balancing is presented. By employing the proposed sensor-less switching method, the FC is equally charged and discharged in each PWM period, which causes sensorless voltage balancing of FC.

The capacitor voltage-balancing algorithm proposed in this article can be explained using the flowchart given in Fig. 4 and Tables II and III. As shown in the flowchart, in each switching cycle, the voltage level v_{an} is found using (7). Then, the algorithm checks whether the redundant switching states are available in Table I or not. Since redundant states are not available for voltage level $+\frac{V_{DC}}{2}$, switching state I is directly applied without checking any other conditions, as given in Table III. In

TABLE III
SELECTION OF SWITCHING STATES FOR THE ANPCI BASED ON CAPACITOR VOLTAGE BALANCING ALGORITHM

v_{an}	Redundant states are available?	Mode as per Table II	State to be applied	
			$i_L > 0$	$i_L < 0$
$+\frac{V_{DC}}{2}$	No	Not checked	I	I
$+\frac{V_{DC}}{4}$	Yes	M1 or M4	II	III
		M2 or M3	III	II
		M5	III	III
0	Yes	Not checked	IV	V
$-\frac{V_{DC}}{4}$	Yes	M1 or M3	VI	VII
		M2 or M4	VII	VI
		M5	VI	VI
$-\frac{V_{DC}}{2}$	No	Not checked	VIII	VIII

case the redundant switching states are available, the algorithm checks for the deviations of v_{FC}, v_{C1} and polarity of i_L before determining the switching state to be applied. For example, if the desired voltage level is $+\frac{V_{DC}}{4}$, there are two possible switching states. So, as shown in Tables II and III, the algorithm checks whether the v_{FC} is within allowable range or not. If the value of v_{FC} is less than the tolerance range (Mode M1 in Table II), the FC needs to be charged. Now if the inductor current i_L is positive, switching state II will be applied to the ANPCI, and if i_L is negative, switching state III will be applied. If v_{FC} is already within the acceptable range, then the algorithm checks the value of v_{C1}. If v_{C1} is below the tolerance range (Mode M3), then it has to be charged. Now if i_L is negative, State II is applied so that v_{C1} is increased. However, if i_L is positive, there is no switching state to charge C_1. In this case, State III will be chosen to avoid further decrease in v_{C1}. If the algorithm detects that both v_{FC} and v_{C1} are within allowable range (Mode M5), then State III will be applied, irrespective of the polarity of i_L. Similarly, the algorithm chooses between other redundant switching states as given in Fig. 4 and Tables II and III. Note that, if v_{C1} is maintained within the acceptable range, then the value of v_{C2} will be regulated automatically, so that (2) is satisfied.

III. AVERAGE MODELING

A. Single-Phase Five-Level ANPCI

The average circuit model of ANPCI is obtained such that the average capacitor voltages and inductor current of the converter during steady-state and transients are accurately predicted with less computational time and resources. To achieve this, the switch network of ANPCI is replaced with a network of dependent voltage and current sources, whose control variables are chosen such that the following conditions are satisfied. First, the voltage v_{an} of the average circuit model is equal to the fundamental component of PWM voltage expressed as a function of m_a, v_{C1}, v_{C2}, and v_{FC}. Second, the average capacitor currents are obtained as a function of m_a and i_L. Third, the instantaneous power balance is maintained in the average circuit. Fourth, the capacitor voltages are maintained within the acceptable tolerance range around their respective nominal values.

To develop the average model of ANPCI as mentioned above, one fundamental cycle of m_a is divided into four different regions as shown in Fig. 3. Then, the average circuit model in each of these four regions and the control variables of dependent sources are determined. As the switching states used by the ANPCI are different in each of these four regions, the average circuit model has to be obtained separately for each region. However, it is important to note that the averaging in each region is actually performed over one switching (or PWM) cycle only. Once the average circuit models are developed in each of the four regions, all these individual circuits are carefully combined to obtain the average circuit model which is valid for entire fundamental cycle. The detailed description of these steps is given below.

Region 1: $0.5 < m_a < 1$**:** In this region, the PWM voltage, v_{an}, of switching circuit can be either v_{C1} or $(v_{C1} - v_{FC})$ or v_{FC}. Thus, the average value of v_{an} is a function of v_{C1}, v_{FC}, and m_a. However, for simplification in the average circuit model, it is assumed that the v_{FC} is constant in this region and C_1 is responsible for supplying power to the load due to the following reasons. First, in this region, average value of v_{an} is always greater than $+\frac{V_{DC}}{4}$, and hence most of the time, the voltage level v_{C1} has to be applied. Second, the tolerance level of v_{FC} is much smaller compared to that of v_{C1}. Third, even if there is an energy exchange between FC and output terminals, the energy supplied by FC primarily comes from C_1 and C_2. With this approximation, the average model of ANPCI in "Region 1" can be obtained as shown in Fig. 5(a). The control variable, v_{aD}, for the dependent voltage source in Fig. 5(a) is given by

$$v_{aD} = m_a \overline{v}_{C1} \text{ for } 0.5 < m_a < 1$$

or

$$v_{aD} = d_P \overline{v}_{C1} \tag{8}$$

where d_P is a multiplying factor defined such that

$$d_P = \begin{cases} m_a \text{ if } 0.5 < m_a < 1 \\ 0 \quad \text{otherwise.} \end{cases}$$

The expression for d_P and other multiplying factors used in the average modeling are given in Table IV. Similarly, i_{D1} and i_{D5} are given by

$$i_{D1} = i_{D5} = d_P \bar{i}_L. \tag{9}$$

Region 2: $0 < m_a < 0.5$**:** In this region, the voltage v_{an} of switching circuit can be either $(v_{C1} - v_{FC})$ or v_{FC} or 0. Thus, the average value of v_{an} is a function of v_{C1}, v_{FC} and m_a. Unlike "Region 1," here FC is connected to the output terminals for most of the time, and hence v_{FC} cannot be considered as constant. In the switching circuit, the choice between the states $(v_{C1} - v_{FC})$ and v_{FC} is made based on the capacitor voltage balancing algorithm. Hence, there are two possible average circuit models as shown in Fig. 5(b) and (c). The choice between these two circuits is made based on the sign of $\bar{i}_L$ and deviation of $\bar{v}_{C1}$, $\bar{v}_{FC}$ from their respective nominal values. The average circuit of ANPCI becomes Fig. 5(b), if v_{an} depends on both

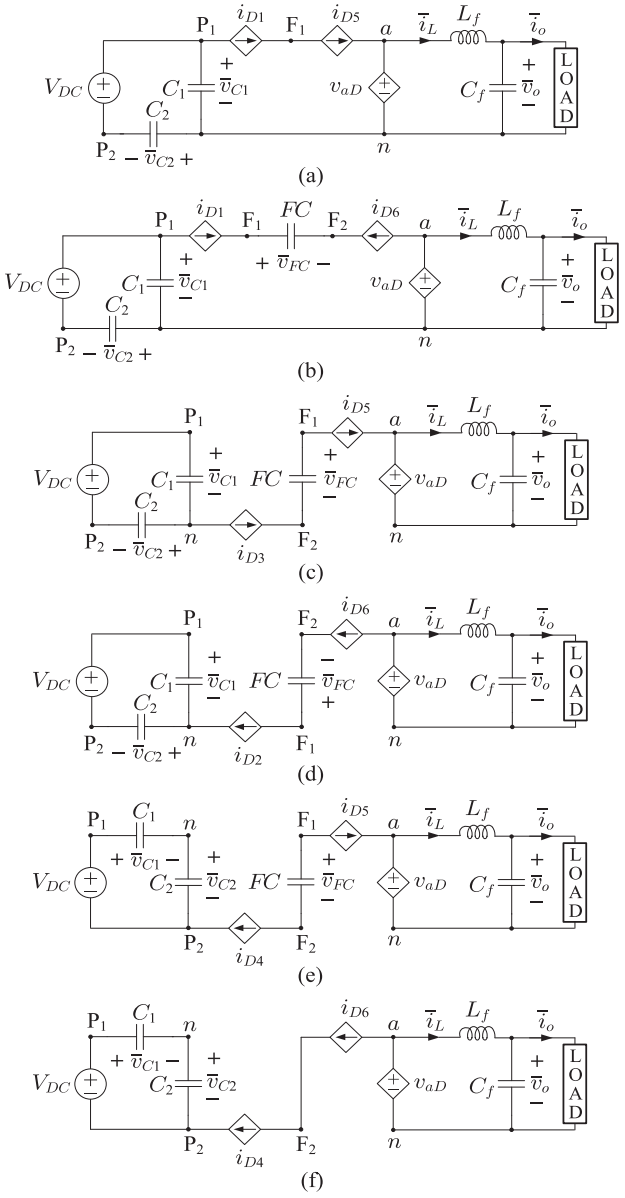

Fig. 5. Average models of ANPCI in (a) Region 1, (b) Region 2, Modes M1 and M4, (c) Region 2, Modes M2 and M3, (d) Region 3, Modes M1 and M3, (e) Region 3, Modes M2 and M4, and (f) Region 4.

v_{C1} and v_{FC}, e.g., when $i_L > 0$ and FC has to be charged. The control variables of sources in Fig. 5(b) can be written as

$$\begin{aligned} v_{aD} &= (\alpha_1 + \alpha_3 + \alpha_5 + \alpha_8)\, d_{PH}\, (\overline{v}_{C1} - \overline{v}_{FC}) \\ &= \beta_1 d_{PH}\, (\overline{v}_{C1} - \overline{v}_{FC}) \end{aligned} \tag{10}$$

$$i_{D1} = -\, i_{D6} = \beta_1 d_{PH} \bar{i}_L \tag{11}$$

where α_i $(i = 1, 2, \ldots, 9)$ and β_j $(j = 1, 2, 3, 4)$ are the multiplying factors defined in Table IV. Similarly, the average circuit of ANPCI becomes Fig. 5(c), if v_{an} depends only on v_{FC}, e.g., when $i_L < 0$ and FC has to be charged. The control variables of sources in Fig. 5(c) can be written as

$$v_{aD} = \beta_4 d_{PH} \overline{v}_{FC} \tag{12}$$

TABLE IV
MULTIPLYING FACTORS USED IN THE AVERAGE MODEL OF ANPCI

Variable	Expression	Variable	Expression
d_P	$0.5 \cdot (1 + sgn(m_a - 0.5))\, m_a$	α_1	$\gamma_1\gamma_9$
d_{PH}	$[1 + (sgn(m_a)\ sgn(0.5 - m_a))]\, m_a$	α_2	$\gamma_2\gamma_9$
d_{NH}	$[(sgn(m_a)\ sgn(0.5 + m_a)) - 1]\, m_a$	α_3	$\gamma_2\gamma_{10}$
d_N	$0.5 \cdot (sgn(m_a + 0.5) - 1)\, m_a$	α_4	$\gamma_1\gamma_{10}$
γ_1	$0.5 \cdot (1 + sgn(v^*_{FC} - \epsilon - \overline{v}_{FC}))$	α_5	$\gamma_3\gamma_4\gamma_6\gamma_9$
γ_2	$0.5 \cdot (1 - sgn(v^*_{FC} + \epsilon - \overline{v}_{FC}))$	α_6	$\gamma_3\gamma_4\gamma_6\gamma_{10}$
γ_3	$0.5 \cdot (1 + sgn(v^*_{FC} + \epsilon - \overline{v}_{FC}))$	α_7	$\gamma_3\gamma_4\gamma_5\gamma_9$
γ_4	$0.5 \cdot (1 - sgn(v^*_{FC} - \epsilon - \overline{v}_{FC}))$	α_8	$\gamma_3\gamma_4\gamma_5\gamma_{10}$
γ_5	$0.5 \cdot (1 + sgn(v^*_{C1} - \epsilon - \overline{v}_{C1}))$	α_9	$\gamma_3\gamma_4\gamma_7\gamma_8$
γ_6	$0.5 \cdot (1 - sgn(v^*_{C1} + \epsilon - \overline{v}_{C1}))$		
γ_7	$0.5 \cdot (1 + sgn(v^*_{C1} + \epsilon - \overline{v}_{C1}))$	β_1	$\sum_{i=1,3,5,8} \alpha_i$
γ_8	$0.5 \cdot (1 - sgn(v^*_{C1} - \epsilon - \overline{v}_{C1}))$	β_2	$\sum_{i=2,4,5,8} \alpha_i$
γ_9	$0.5 \cdot \left(1 + sgn(\bar{i}_L)\right)$	β_3	$\sum_{i=1,3,6,7,9} \alpha_i$
γ_{10}	$0.5 \cdot \left(1 - sgn(\bar{i}_L)\right)$	β_4	$\sum_{i=2,4,6,7,9} \alpha_i$

$$i_{D3} = i_{D5} = \beta_4 d_{PH} \bar{i}_L. \tag{13}$$

Region 3: $-0.5 < m_a < 0$**:** In this region, the voltage v_{an} of switching circuit can be either $-v_{FC}$ or $(v_{FC} - v_{C2})$ or 0. Thus, the average v_{an} is a function of v_{C2}, v_{FC} and m_a. Similar to "Region 2," here FC is connected to the output terminals for most of the time. In the switching circuit, the choice between the states $-v_{FC}$ and $(v_{FC} - v_{C2})$ is made based on the capacitor voltage balancing algorithm. Hence, there are two possible average circuit models as shown in Fig. 5(d) and (e). The choice between these two circuits is made based on the sign of $\bar{i}_L$ and deviation of $\overline{v}_{C2}$, $\overline{v}_{FC}$ from their respective nominal values. The average circuit of ANPCI becomes Fig. 5(d), if v_{an} depends only on v_{FC}, e.g., when $i_L > 0$ and FC has to be charged. The control variables of sources in Fig. 5(d) can be written as

$$v_{aD} = -\, \beta_3 d_{NH} \overline{v}_{FC} \tag{14}$$

$$i_{D2} = i_{D6} = -\beta_3 d_{NH} \bar{i}_L. \tag{15}$$

Similarly, the average circuit of ANPCI becomes Fig. 5(e), if v_{an} depends on both v_{C2} and v_{FC}, e.g., when $i_L < 0$ and FC has to be charged. The control variables of sources in Fig. 5(e) can be written as

$$v_{aD} = \beta_2 d_{NH}\, (\overline{v}_{FC} - \overline{v}_{C2}) \tag{16}$$

$$i_{D4} = -\, i_{D5} = -\beta_2 d_{NH} \bar{i}_L. \tag{17}$$

Region 4: $-1 < m_a < -0.5$**:** In this region, the voltage v_{an} of switching circuit can be either $-v_{C2}$ or $(v_{FC} - v_{C2})$ or $-v_{FC}$. Thus, the average v_{an} is a function of v_{C2}, v_{FC}, and m_a. However, similar to "Region 1," for simplification in the average circuit model, it is assumed that the v_{FC} is constant in this region and only C_2 is responsible for supplying power to the load. With this approximation, the average model of ANPCI in this region can be obtained as shown in Fig. 5(f). The control variables for the dependent sources in Fig. 5(f) are given by

$$v_{aD} = -\, d_N \overline{v}_{C2} \tag{18}$$

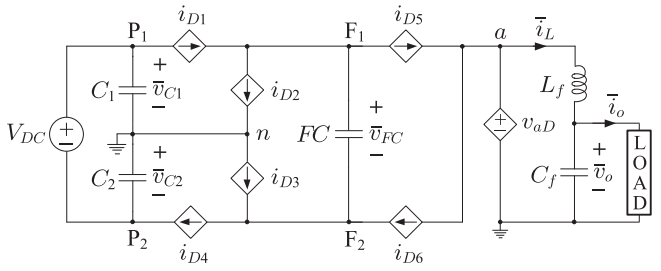

Fig. 6. Combined dynamic average circuit model of the ANPCI.

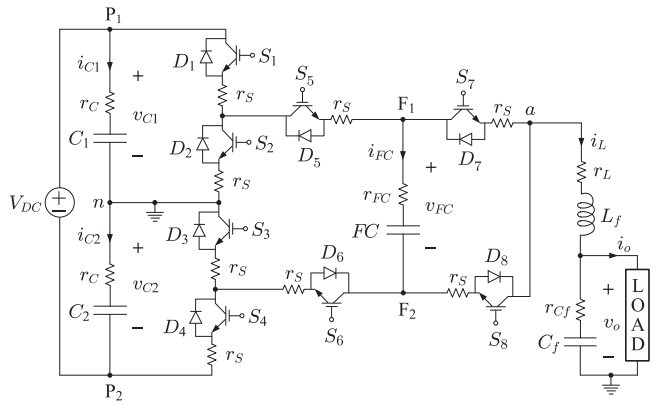

Fig. 7. SCM of the ANPCI with nonidealities: switch ON-state resistance (r_S) shown separately for each switch.

$$i_{D4} = i_{D6} = -d_N \overline{i}_L. \tag{19}$$

By carefully combining the circuits given in Fig. 5(a)−(f) and (8)−(19), the final DACM of ANPCI is obtained as shown in Fig. 6. The control variables of dependent sources in Fig. 6 are given by

$$\begin{aligned} v_{aD} &= d_P \overline{v}_{C1} - d_N \overline{v}_{C2} + \beta_1 d_{PH}(\overline{v}_{C1} - \overline{v}_{FC}) \\ &\quad + \beta_2 d_{NH}(\overline{v}_{FC} - \overline{v}_{C2}) - (\beta_3 d_{NH} - \beta_4 d_{PH})\,\overline{v}_{FC} \end{aligned} \tag{20}$$

$$= \left(\frac{V_{DC}}{2}\right) m_a$$

$$i_{D1} = (d_P + \beta_1 d_{PH})\,\overline{i}_L \tag{21}$$

$$i_{D2} = -\beta_3 d_{NH} \overline{i}_L \tag{22}$$

$$i_{D3} = \beta_4 d_{PH} \overline{i}_L \tag{23}$$

$$i_{D4} = -(d_N + \beta_2 d_{NH})\,\overline{i}_L \tag{24}$$

$$i_{D5} = (d_P + \beta_2 d_{NH} + \beta_4 d_{PH})\,\overline{i}_L \tag{25}$$

$$i_{D6} = -(d_N + \beta_1 d_{PH} + \beta_3 d_{NH})\,\overline{i}_L. \tag{26}$$

B. Inclusion of Nonidealities in the DACM

Fig. 7 shows the circuit diagram of ANPCI considering nonidealities such as 1) ON-state resistance of each switch, r_S; 2) equivalent series resistance (ESR) of each dc-link capacitor, r_C; 3) ESR of the FC, r_{FC}; 4) ESR of the filter capacitor, r_{Cf}; and 5) ESR of the filter inductor, r_L.

TABLE V
SWITCHES IN THE ON-STATE, AND SWITCHES IN THE CONDUCTION MODE CARRYING THE INDUCTOR CURRENT (i_L) FOR EACH SWITCHING STATE OF THE ANPCI OF Fig. 1

State	Switches in ON-state	Switches in the conduction mode carrying the inductor current, $(i_L)^\sharp$
I	S_1, S_3, S_5, S_7	S_1, S_5, S_7
II	S_1, S_3, S_5, S_8	S_1, S_5, S_8
III	S_1, S_3, S_6, S_7	S_3, S_6, S_7
IV	S_1, S_3, S_6, S_8	S_3, S_6, S_8
V	S_2, S_4, S_5, S_7	S_2, S_5, S_7
VI	S_2, S_4, S_5, S_8	S_2, S_5, S_8
VII	S_2, S_4, S_6, S_7	S_4, S_6, S_7
VIII	S_2, S_4, S_6, S_8	S_4, S_6, S_8

$^\sharp$ When a switch is said to be in conducting mode, the conducting device can be either the IGBT or its antiparallel diode, depending on the polarity of i_L.

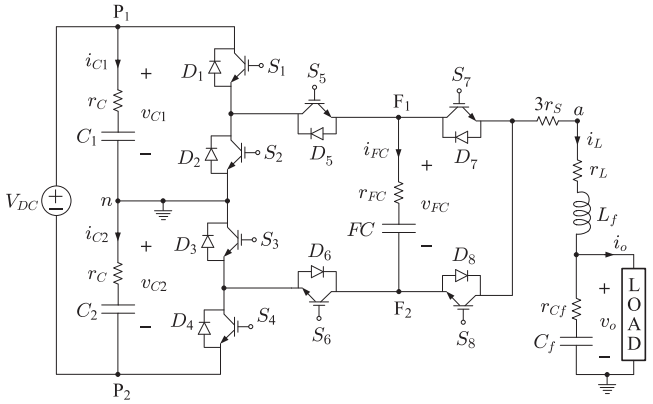

Fig. 8. SCM of the ANPCI with nonidealities: ON-state resistance of three conducting switches is combined and placed in series ($3{\cdot}r_S$) with the filter inductor L_f.

From Table V, it can be seen that only four switches are turned ON in each switching state, out of which only three switches are conducting at any time. Also these three switches will be connected in series with the filter inductor L_f and hence all of them carry the current i_L. For instance, in State I, the switches S_1, S_3, S_5, and S_7 are turned ON; however, the conducting switches are only S_1, S_5, and S_7. Switch S_3 does not conduct in this state and it is turned ON only to balance the voltage stress among the switches. Note that when a switch is said to be in conducting mode, the conducting device can be either the IGBT or its antiparallel diode, depending on the polarity of i_L.

Therefore, the combined effect of the switch ON-state resistance on the ANPCI output voltage can be represented as a single resistance, $3{\cdot}r_S$, connected in series with the filter inductor L_f, as shown in Fig. 8. Fig. 9 shows the DACM of ANPCI considering the nonidealities listed above. Note that, as the position of all the passive components is not changed in the average circuit model, there is no need to rederive the equations

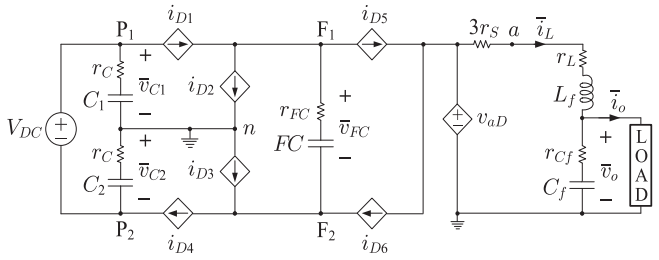

Fig. 9. DACM of the ANPCI with nonidealities, i.e., for the SCM shown in Fig. 8.

for the dependent sources in the average model. This is the main advantage of the DACM presented in this article.

C. Single-Phase N-Level ANPCI

The circuit diagram of ANPCI is modular, i.e., for increment of every two levels of PWM voltage, two switches and one flying capacitor have to be integrated to the five-level ANPCI shown in Fig. 1 [21]. Fig. 10 shows the circuit diagram of N-level ANPCI, where $N \geq 5$ is an odd integer. It can be observed that for N-level output voltage waveform, the required number of switches and flying capacitors are $(N+3)$ and $(\frac{N-3}{2})$, respectively. Note that the nonidealities are not shown here for simplicity. The averaged modeling concept presented in this article can also be extended for the N-level ANPCI by adding two dependent current sources and one flying capacitor to the circuit of Fig. 6 for increment of every two output voltage levels. The average circuit model obtained for an N-level ANPCI is shown in Fig. 11. The number of dependent current sources required in the average circuit model of N-level ANPCI is $(N+1)$. However, only one dependent voltage source is required irrespective of the number of output voltage levels.

IV. Closed-Loop SRF-dq Control of ANPCI

The operation and average model of single-phase five-level ANPCI presented in Sections II and III have been verified in both open-loop and closed-loop modes of the converter. For closed-loop operation, an SRF-dq controller [37] has been developed for the ANPCI to regulate its load voltage v_o to a reference v_o^*. The block diagram of the closed-loop controller is shown in Fig. 12, which uses a second-order generalized integrator [38] to generate a set of orthogonal signals, $\begin{bmatrix} i_\alpha & i_\beta \end{bmatrix}^T$ and $\begin{bmatrix} v_\alpha & v_\beta \end{bmatrix}^T$ from the sensed inductor current, i_L, and output voltage, v_o. These $\alpha\beta$-domain signals are then transformed into dq-domain using the transformation given by

$$T_{\alpha\beta\rightarrow dq} = \begin{bmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{bmatrix}. \tag{27}$$

The SRF-dq controller block takes the dq-domain quantities $\begin{bmatrix} i_d & i_q \end{bmatrix}^T$, $\begin{bmatrix} v_d & v_q \end{bmatrix}^T$ and the reference voltage $\begin{bmatrix} V_d^* & V_q^* \end{bmatrix}^T$ as inputs. The SRF-dq controller has a cascaded control structure with an inner current controller and an outer voltage controller, which are depicted in the block diagram of Fig. 13. It can be seen that PI controllers are used to regulate both d-axis and q-axis currents and voltages. To design these PI controllers, the circuit diagram of ANPCI is modeled as

$$\frac{dv_o}{dt} = \left(\frac{i_L}{C_f}\right) - \left(\frac{v_o}{R_L C_f}\right) \tag{28}$$

$$\frac{di_L}{dt} = \frac{(v_{an} - v_o - i_L r_L)}{L_f} \tag{29}$$

where R_L is the load resistance and r_L is the ESR of L_f. This model is then transformed to dq-domain using the transformation given in (27). The mathematical model of ANPCI in dq-domain is given by

$$\frac{d}{dt}\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_L C_f} & \omega \\ -\omega & -\frac{1}{R_L C_f} \end{bmatrix} \cdot \begin{bmatrix} v_d \\ v_q \end{bmatrix} + \frac{1}{C_f} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{30}$$

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L_f} & \omega \\ -\omega & -\frac{r_L}{L_f} \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_f} \cdot \begin{bmatrix} v_{and} - v_d \\ v_{anq} - v_q \end{bmatrix}. \tag{31}$$

The time domain model is then transformed into s-domain, which is given by the transfer functions

$$\frac{v_d(s)}{i_d(s) + \omega C_f v_q(s)} = \frac{R_L}{1 + sR_L C_f} \tag{32}$$

$$\frac{v_q(s)}{i_q(s) - \omega C_f v_d(s)} = \frac{R_L}{1 + sR_L C_f} \tag{33}$$

$$\frac{i_d(s)}{v_{and}(s) - v_d(s) + \omega L_f i_q(s)} = \frac{1}{sL_f + r_L} \tag{34}$$

$$\frac{i_q(s)}{v_{anq}(s) - v_q(s) - \omega L_f i_d(s)} = \frac{1}{sL_f + r_L}. \tag{35}$$

These transfer functions are used to determine the PI controller parameters. The outer voltage controller generates the dq-domain reference currents, $\begin{bmatrix} I_d^* & I_q^* \end{bmatrix}^T$, which are given as inputs to the inner current controller. The current controller block generates the modulation signal $\begin{bmatrix} m_d & m_q \end{bmatrix}^T$ in SRF, which is transformed back into stationary reference frame and used to generate the gate signals for ANPCI as shown in Fig. 12.

V. Results and Discussion

The experimental setup of single-phase ANPCI is developed to validate the analysis and average circuit model developed in this article. Table VI gives the parameters used for validation and Fig. 14 shows the photograph of experimental setup. The switching signals for the ANPCI are generated using PDS-PWM technique implemented in TMS320F28335 digital signal processor (DSP). The capacitor voltage-balancing algorithm and SRF-dq controller are also implemented using the same DSP. The source voltage, V_{DC}, capacitor voltages, v_{C1}, v_{FC}, and the load voltage, v_o, are measured using the LEM voltage sensors LV-25P, and the inductor current, i_L, is measured using the LEM current sensor LA-55P.

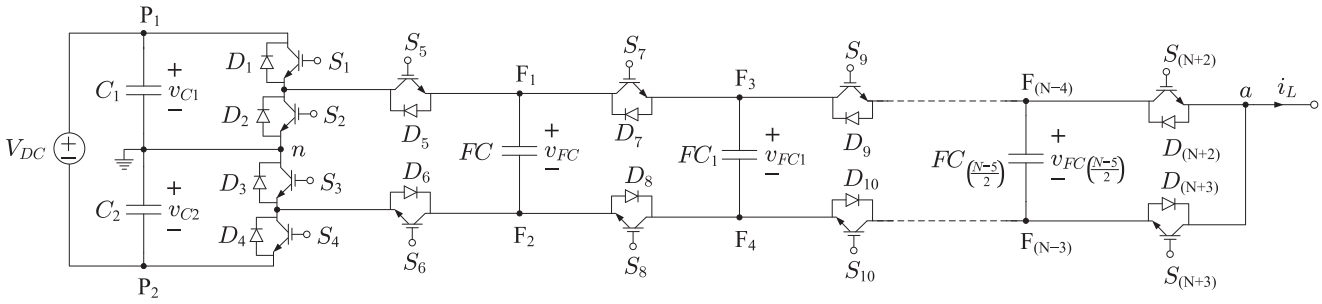

Fig. 10. Circuit diagram of single-phase N-level ANPCI.

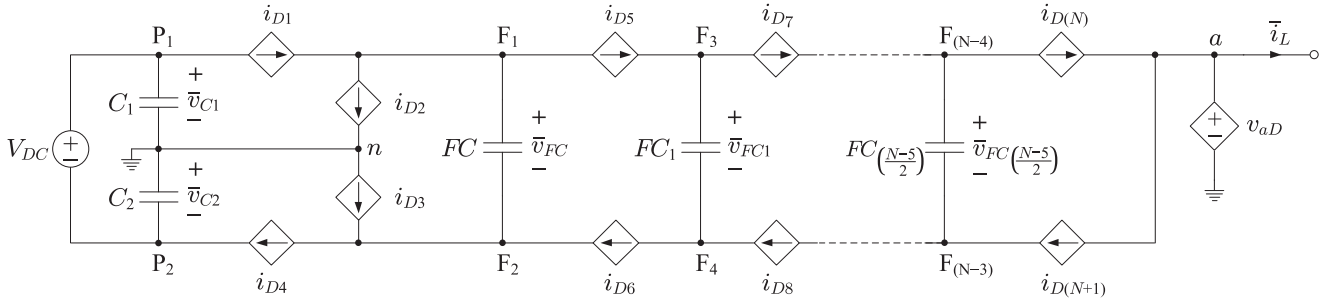

Fig. 11. Dynamic average circuit model of the single-phase N-level ANPCI.

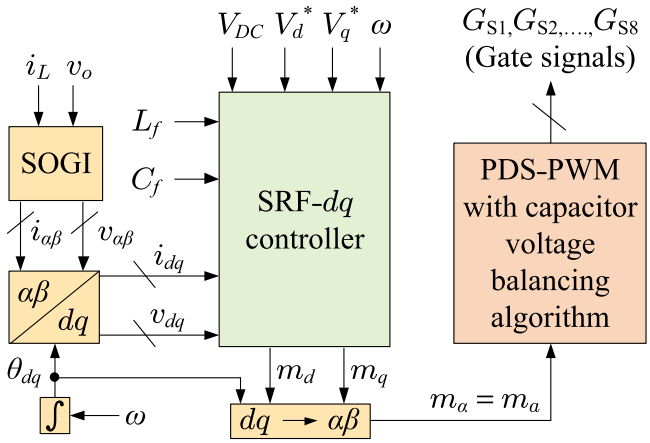

Fig. 12. Block diagram of closed-loop controller for ANPCI.

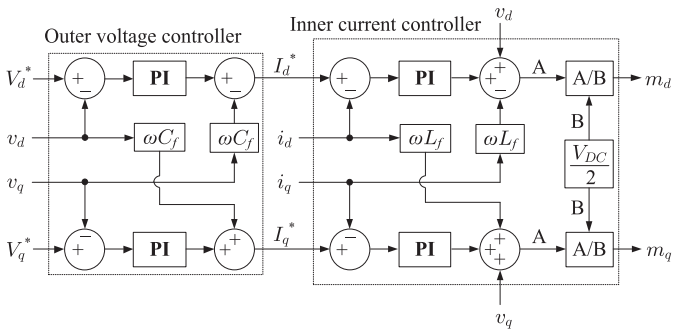

Fig. 13. Detailed diagram of SRF-dq controller for ANPCI.

TABLE VI
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Attributes
C_1 and C_2	3.3 mF
FC	2 mF
L_f	2 mH
C_f	20 μF
Fundamental frequency $\left(f_o = \frac{\omega_o}{2\pi}\right)$	50 Hz
Switching frequency (f_s)	10 kHz
V_{DC}	128 V
Output power	300 W

In this section, the results are presented for open-loop and closed-loop operation of the ANPCI. Results to validate the average circuit model are also presented in this section. The results for strength demonstration of the average circuit model are given in Section VI. Note that all the simulation results presented in Sections V and VI are obtained using PSCAD/EMTDC software on a desktop computer with Intel Core$^{\text{TM}}$ i5-3470 CPU @ 3.2 GHz processor, 8 GB RAM, and Windows 10 64-bit operating system.

A. Validation of PWM and Capacitor Voltage-Balancing Algorithm

Fig. 15 shows the experimental results of ANPCI during open-loop operation. Fig. 15(a) shows the steady-state waveforms of dc-link capacitor voltage (v_{C1}), FC voltage (v_{FC}), load voltage (v_o), and the load current (i_o) with the modulation index, $M = 0.9$. It is observed that the mean value of v_{C1} is half the dc-link voltage, i.e., 64 V, with a peak-to-peak (P-P) ripple of 8 V and

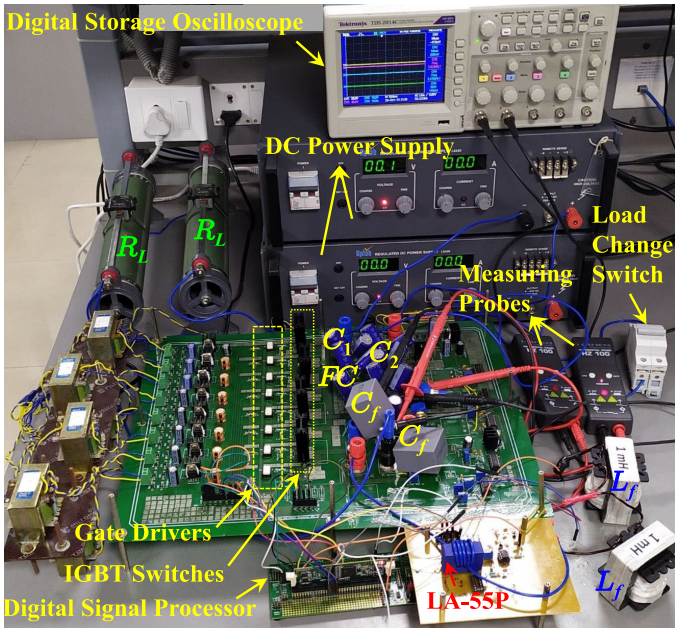

Fig. 14. Photograph of the experimental setup.

the mean FC voltage is 31.9 V with a P-P ripple of 0.8 V. Load voltage and current are sinusoidal and their rms values are observed as 33.85 V and 6.44 A, respectively. The THD in v_o and i_o are 4.53% and 4.6%, respectively. Fig. 15(b) shows the results when modulation index is suddenly changed from 0.9 to 0.4, while the load resistance, R_L, is 5 Ω. It can be observed that, when M becomes below 0.5, a three-level PWM voltage waveform is obtained with a P-P value of 64 V and the rms value of i_o is reduced to 3.11 A from 6.5 A. Note that the average values of the v_{C1} and v_{FC} are obtained as 62.8 and 32 V, respectively. Further, the P-P ripple in v_{C1} is reduced to 2.5 V due to reduction in the load current. Fig. 15(c) shows the results when the load step change is given from 5 Ω to 10 Ω with $M = 0.9$. The reduction in rms load current from 6.5 to 3.39 A can be observed from Fig. 15(c). Moreover, the v_{C1} and v_{FC} are maintained at their respective reference values.

B. Validation of SRF-dq-Based Closed-Loop Controller

Fig. 16 shows the experimental results of ANPCI during closed-loop operation. Fig. 16(a) shows the steady-state waveforms using SRF-dq controller for the v_{C1}, v_{FC}, v_o, and i_o. The reference load voltages in the dq frame, V_d^* and V_q^*, are set to 46 and 0 V, respectively, which corresponds to 32.6 and 0 V rms, respectively. In Fig. 16(a), the rms values of the sinusoidal waveforms, v_o and i_o, are obtained as 32.6 and 6.37 A, respectively, with 5 Ω load resistance. The calculated THD in v_o and i_o are 3.86% and 3.04%, respectively. Also, the mean of v_{C1} and v_{FC} are observed as 63.3 and 32.1 V, respectively. Fig. 16(b) shows the results when the load is suddenly changed from 10 Ω to 5 Ω, with 46 V constant peak reference load voltage. It is observed that the ripple in v_{C1} is increased due to the rise of rms load current from 3.39 to 6.36 A. In spite of increase in the rms load current, the positive peak of v_o tracks its reference value, V_d^*, because of the closed-loop controller. Fig. 16(c) shows the results when step change in the V_d^* is given from 36 to 46 V with $R_L = 5\,\Omega$. The rms load current is 5 A before the step change and 6.53 A after the step change. Note that the load voltage is tracking its reference with in two fundamental cycles.

The closed-loop results shown in Fig. 16 confirm the effectiveness of SRF-dq controller in maintaining the load voltage at its reference value during steady-state and transient operations. The results in Figs. 15 and 16 also confirm the effectiveness of capacitor voltage-balancing algorithm in both open-loop and closed-loop operation of ANPCI. As small variation in the v_{FC} causes significant distortion in the v_o, high priority is set to maintain low ripple in the FC voltage rather than the dc-link capacitor voltages in the capacitor voltage-balancing algorithm. Thus, the FC voltage in Figs. 15 and 16 is flat with negligible P-P ripple.

C. Validation of the Dynamic Average Circuit Model

To validate the DACM of the ANPCI developed in this article, the waveforms obtained from DACM simulation are compared with the SCM simulation waveforms and the experimental waveforms for various test cases. These simulations also consider the nonidealities present in the switches and passive components used in hardware prototype. However, the EMI and the dead band effects are ignored. The time instants of step changes given in the simulation waveforms of the SCM and DACM are the same as given in the experimental waveforms for each test case. The simulation time-step (T_{st}) considered is 1μs and the simulation plot step (T_p) is 40μs for the SCM. In Figs. 17 and 18, $Avg40$ and $Avg160$ represent the DACM waveforms obtained with the simulation time-steps of 40 and 160 μs, respectively.

Fig. 17 shows the comparison of open-loop waveforms obtained from simulation of DACM and SCM, and experiment. The steady-state waveforms of v_{C1}, v_{FC}, v_o, and i_o are shown in Fig. 17(a). The modulation index step change is given from 0.9 to 0.4 at $t = 50.92$ ms with the constant load resistance of 5 Ω, and the corresponding waveforms are shown in Fig. 17(b). In Fig. 17(c), the load resistance is suddenly increased from 5 Ω to 10 Ω at $t = 37.6$ ms. Fig. 18 shows the comparison of closed-loop waveforms obtained from simulation of DACM and SCM, and experiment. Fig. 18(a) shows the steady-state waveforms for the reference peak load voltage (V_d^*) of 46 V and 5 Ω load. Fig. 18(b) and (c) shows the waveforms with step change in load resistance given at $t = 38.01$ ms and step change in the reference load voltage given at $t = 25.55$ ms, respectively. From Figs. 17 and 18, it is confirmed that the average circuit model accurately predicts the waveforms of ANPCI in both steady-state and transient conditions. Note that the average model requires very less computational time compared to the switching circuit simulation. The results to support this are presented in Section VI.

In addition to comparison of waveforms, the effectiveness of DACM is also validated using root mean square error (RMSE) for various test cases listed in Table VII. The rms error for all these test cases with three different simulation time-steps (T_{st}),

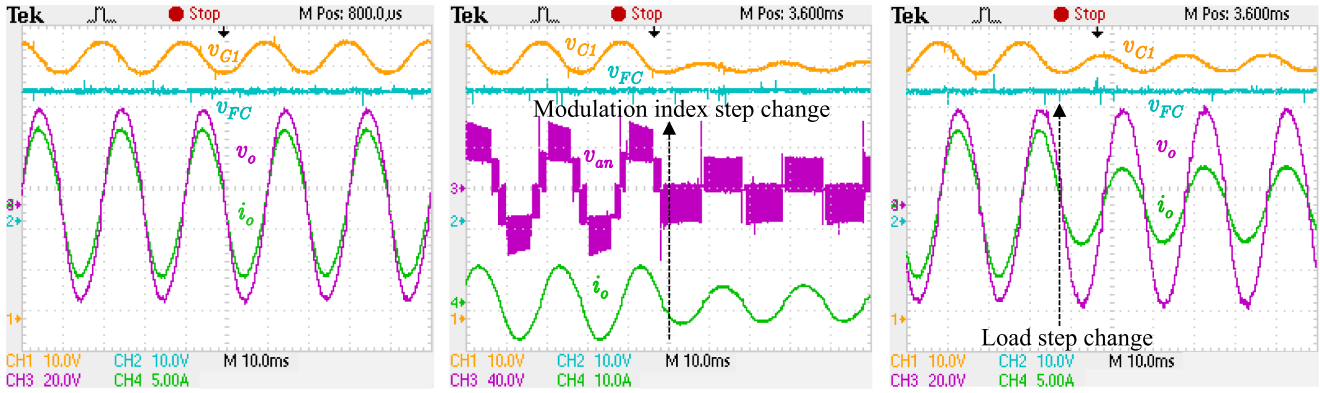

Fig. 15. Experimental results in open-loop for (a) steady-state operation, (b) step change in the modulation index from 0.9 to 0.4, and (c) step change in the load from 5 Ω to 10 Ω.

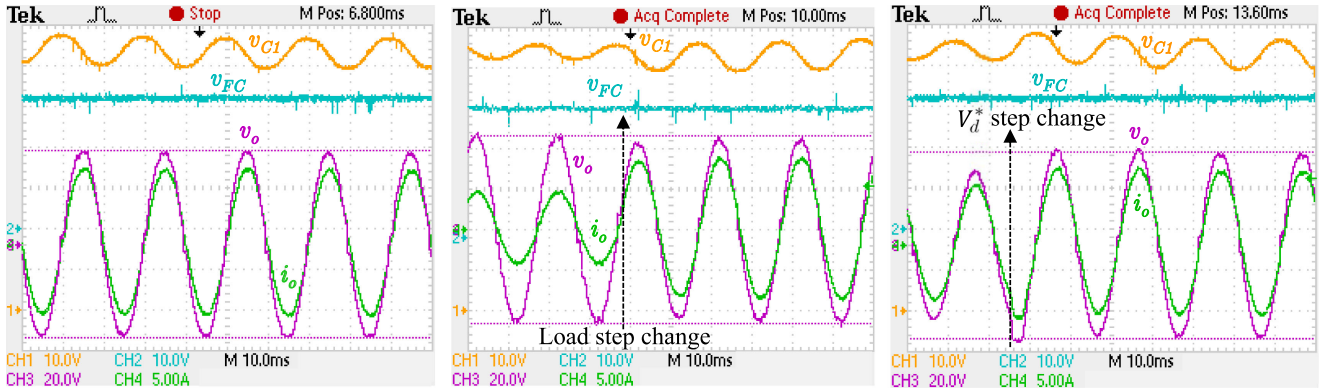

Fig. 16. Experimental results in closed-loop for (a) steady-state operation, (b) step change in the load from 10 Ω to 5 Ω, and (c) step change in the reference peak voltage from 36 V to 46 V.

TABLE VII
PARAMETERS FOR VARIOUS CASES CONSIDERED FOR VALIDATION OF AVERAGE MODEL

Variables	Open-loop cases			Variables	Closed-loop cases			
	C-1	C-2	C-3		C-4	C-5	C-6	C-7
M	0.9	0.4	0.9	V_d^*	46 V	46 V	46 V	36 V
R_L	5 Ω	5 Ω	10 Ω	R_L	5 Ω	8.4 Ω	10 Ω	5 Ω

viz., 40, 80, and 160 μs are listed in Table VIII. It can be seen that the rms errors for all the test cases considered are in acceptable range for both simulation and experiment. Note that, in all the results presented in this article, the units of rms errors are the same as the units of the signals under consideration.

VI. STRENGTH DEMONSTRATION OF THE DYNAMIC AVERAGE CIRCUIT MODEL

To demonstrate the strength of the DACM of the ANPCI and to compare the computational time required for switching circuit-based simulation and average model-based simulation, SRF-dq-controlled ANPCI-based standalone PV system is considered as shown in Fig. 19. The PV array in Fig. 19 consists of four series-connected KC200GT PV panels, each with open-circuit voltage, $V_{OC} = 32.9$ V, and short-circuit current, $I_{sc} = 8.21$ A [39]. In Fig. 19, C_{PV} is 6 mF and the parameters of the ANPCI are the same as given in Table VI. However, the $V_{DC}(= V_{PV})$ will depend on the connected load and the operating point on the PV curve. The characteristics of the combined PV array are shown in Fig. 20 for various irradiation (G) and temperature (T) conditions. Also, Table IX gives the maximum power point and V_{OC} values of these curves.

To simulate the system shown in Fig. 19, the PV array model given in [39] is utilized. The load voltage in Fig. 19 is maintained to be constant in all the operating conditions, whereas the terminal voltage of the PV array, V_{PV}, depends on the operating point. The proposed test system is run for 100 s with step changes in solar irradiation, temperature, and the load. Fig. 21 shows the comparison of waveforms obtained from switching circuit-based simulation and average model-based simulation. In this figure, $Avg40$ and $Avg160$ represent the DACM waveforms obtained with the simulation time-steps of 40 and 160 μs, respectively. Fig. 21(a) shows the results with the initial parameters, $G = 350\frac{W}{m^2}$, $T = 30°$C, $V_d^* = 46$ V, and $Z_L = (5+j3.14)\Omega$, so that the system operates at point A on the PV curve shown in Fig. 20. At $t = 20$ s, the temperature is changed to 25°C and the operating point has changed to B. Later, in Fig. 21(b), a step change is given in the irradiation at $t = 40$ s, from $350\frac{W}{m^2}$ to $250\frac{W}{m^2}$, due

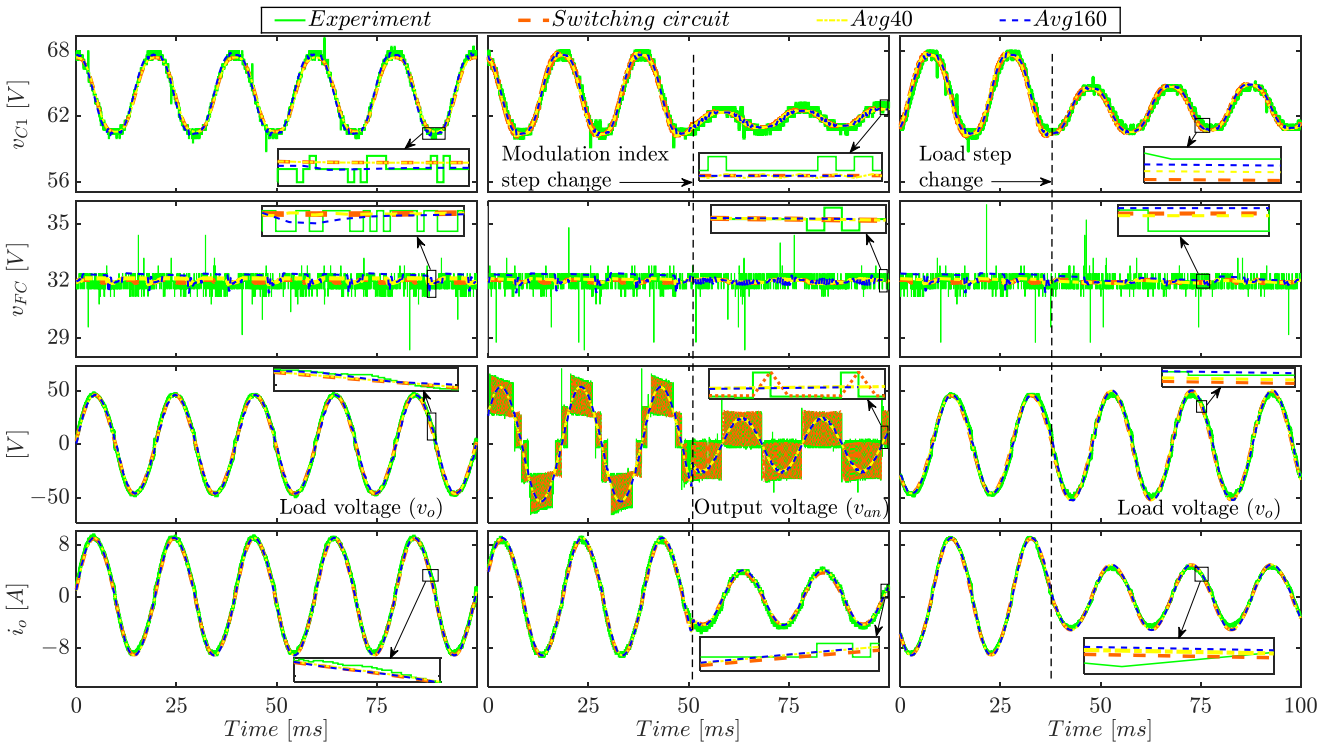

Fig. 17. Comparison of waveforms obtained from simulation of DACM, simulation of SCM, and experimental prototype of ANPCI in open-loop for (a) steady state, (b) step-down change in modulation index (M), and (c) step-down change in load.

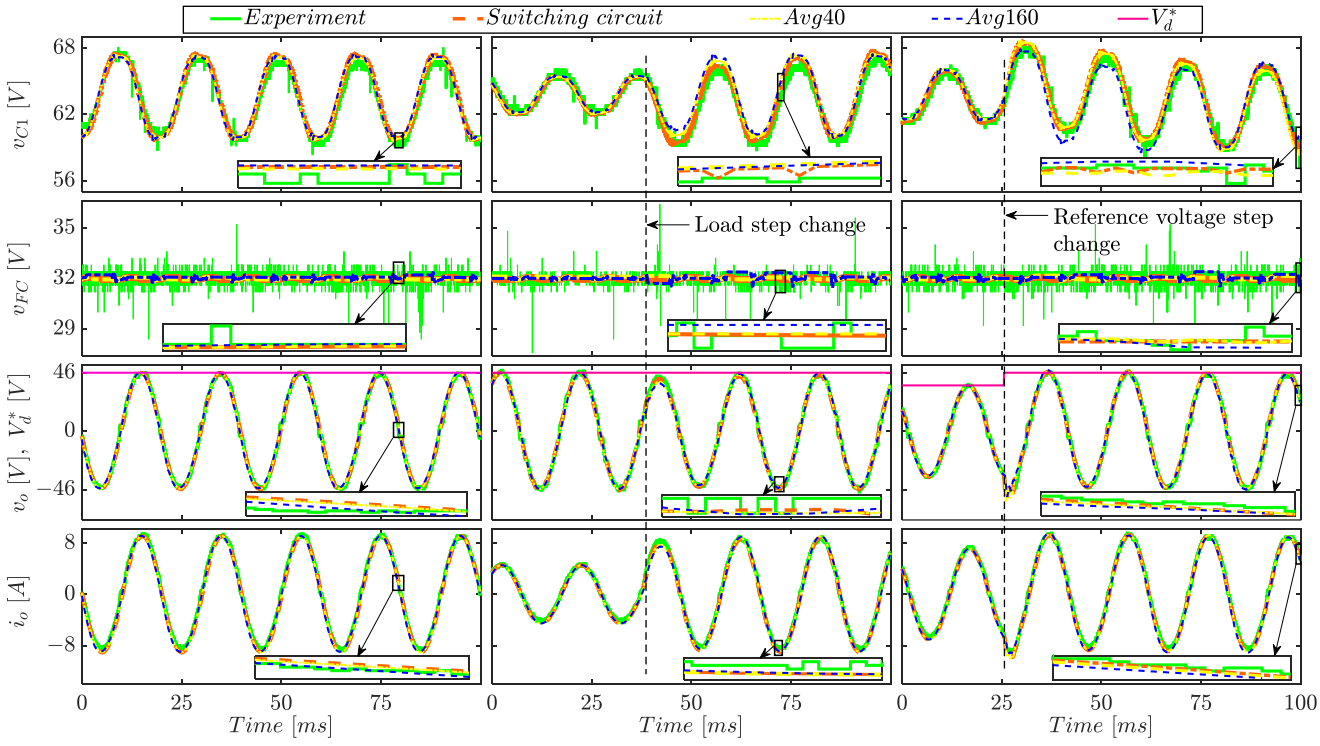

Fig. 18. Comparison of waveforms obtained from simulation of DACM, simulation of SCM, and experimental prototype of ANPCI in closed-loop for (a) steady-state, (b) step-up change in load, and (c) step-up change in reference load voltage (V_d^*).

TABLE VIII
RMS ERRORS FOR THE CASES LISTED IN TABLE VII WITH DIFFERENT SIMULATION TIME-STEPS OF THE AVERAGE MODEL (DACM)

Case	T_{st}	RMS Errors							
		DACM Simulation and SCM Simulation				DACM Simulation and Experiment			
		v_{C1}	v_{FC}	v_o	i_o	v_{C1}	v_{FC}	v_o	i_o
C-1	40 μs	0.28	0.10	0.49	0.09	0.38	0.35	2.41	0.36
	80 μs	0.27	0.07	0.53	0.1	0.38	0.34	2.36	0.36
	160 μs	0.31	0.32	1.49	0.26	0.38	0.46	2.82	0.36
C-2	40 μs	0.17	0.03	—	0.22	0.34	0.25	—	0.37
	80 μs	0.17	0.06	—	0.26	0.33	0.25	—	0.4
	160 μs	0.17	0.11	—	0.24	0.33	0.26	—	0.36
C-3	40 μs	0.15	0.03	0.53	0.05	0.33	0.27	2.71	0.4
	80 μs	0.15	0.04	0.54	0.05	0.33	0.29	2.75	0.4
	160 μs	0.2	0.15	2.35	0.23	0.27	0.36	2.47	0.41
C-4	40 μs	0.26	0.07	0.53	0.1	0.56	0.47	1.74	0.52
	80 μs	0.28	0.08	1.1	0.14	0.61	0.48	1.99	0.55
	160 μs	0.28	0.16	2.18	0.35	0.61	0.46	2.7	0.61
C-5	40 μs	0.17	0.07	0.59	0.06	0.35	0.37	2.59	0.27
	80 μs	0.22	0.08	0.68	0.08	0.37	0.4	2.52	0.26
	160 μs	0.19	0.17	1.69	0.2	0.36	0.44	1.92	0.19
C-6	40 μs	0.16	0.11	0.68	0.06	0.34	0.37	1.91	0.27
	80 μs	0.18	0.08	0.78	0.06	0.33	0.41	1.94	0.27
	160 μs	0.21	0.06	1.08	0.09	0.28	0.51	1.94	0.29
C-7	40 μs	0.29	0.05	0.43	0.08	0.43	0.42	1.55	0.36
	80 μs	0.27	0.08	0.52	0.05	0.44	0.37	1.61	0.37
	160 μs	0.31	0.12	0.74	0.09	0.44	0.38	1.76	0.39

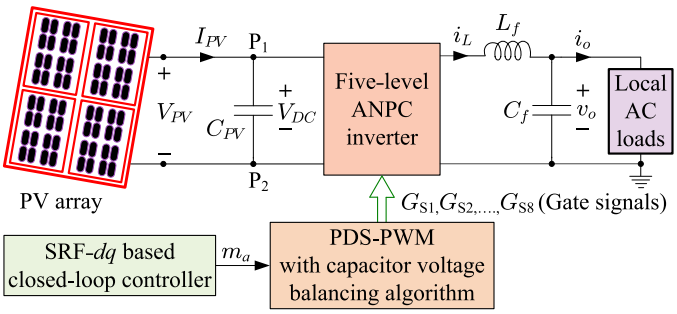

Fig. 19. Block diagram of ANPCI-based standalone PV system.

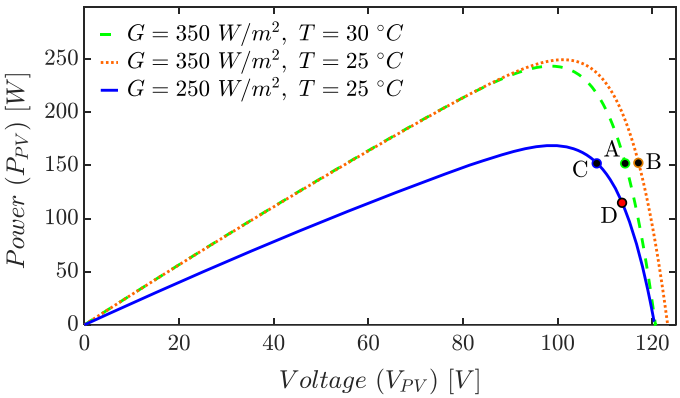

Fig. 20. Power vs. voltage characteristics of the PV array.

TABLE IX
V_{OC} AND MAXIMUM POWER POINT (MPP) OF THE PV-CURVES SHOWN IN Fig. 20

Parameters	Maximum power point		V_{OC}
	V_{MPP}	P_{MPP}	
$G = 350\ \frac{W}{m^2}$ and $T = 30\ ^\circ$C	98.53 V	243.51 W	120.66 V
$G = 350\ \frac{W}{m^2}$ and $T = 25\ ^\circ$C	101.13 V	249.54 W	123.24 V
$G = 250\ \frac{W}{m^2}$ and $T = 25\ ^\circ$C	98.88 V	168.70 W	120.38 V

TABLE X
STEADY-STATE OPERATING POINTS ON PV- CURVES FOR CLOSED-LOOP OPERATION OF ANPCI-BASED PV SYSTEM

Point	SCM	DACM		
	$T_{st} = 1\ \mu$s	$T_{st} = 40\ \mu$s	$T_{st} = 80\ \mu$s	$T_{st} = 160\ \mu$s
A	(114.3,151.75)	(114.35,150.3)	(114.45,148.75)	(114.7,145.7)
B	(117.1,152.3)	(117.2,150.3)	(117.32,148.7)	(117.5,145.7)
C	(108.3,151.8)	(108.75,150.3)	(109.1,148.7)	(109.65,145.7)
D	(113.65,114.7)	(113.75,113.9)	(113.77,113.3)	(113.9,111.85)

TABLE XI
RMS ERRORS FOR SIMULATION OF ANPCI-INTEGRATED PV ARRAY USING AVERAGE MODEL (DACM) AND SWITCHING CIRCUIT (SCM)

Parameters	T_{st}	RMS Errors				
		DACM and SCM				
		V_{PV}	v_{C1}	v_{FC}	v_o	i_o
$G = 350\ \frac{W}{m^2}$,	40 μs	0.01	0.03	0.11	0.92	0.09
$T = 30\ ^\circ$C, $V_d^* = 46$ V,	80 μs	0.17	0.09	0.12	0.98	0.11
and $Z_L = 5 + j3.14\ \Omega$	160 μs	0.38	0.37	0.17	1.51	0.17
$G = 350\ \frac{W}{m^2}$,	40 μs	0.1	0.1	0.11	1.0	0.09
$T = 25\ ^\circ$C, $V_d^* = 46$ V,	80 μs	0.19	0.2	0.13	0.86	0.1
and $Z_L = 5 + j3.14\ \Omega$	160 μs	0.36	0.32	0.16	2.83	0.43
$G = 250\ \frac{W}{m^2}$,	40 μs	0.36	0.25	0.16	0.65	0.08
$T = 25\ ^\circ$C, $V_d^* = 46$ V,	80 μs	0.7	0.49	0.23	0.69	0.04
and $Z_L = 5 + j3.14\ \Omega$	160 μs	1.27	0.17	0.36	2.4	0.36
$G = 250\ \frac{W}{m^2}$,	40 μs	0.07	0.12	0.08	0.56	0.06
$T = 25\ ^\circ$C, $V_d^* = 46$ V,	80 μs	0.14	0.22	0.1	1.06	0.12
and $Z_L = 8 + j3.14\ \Omega$	160 μs	0.28	0.45	0.15	2.23	0.25

to which the operating point becomes C. Fig. 21(c) shows the results with step change in the ac load (Z_L) from $(5+j3.14)\Omega$ to $(8+j3.14)\Omega$ at $t = 80$ s and the system operates at point D on the PV curve. Table X lists the steady-state operating points of the ANPCI-based PV system obtained from SCM and DACM for various time-steps. From the results of Fig. 21 and Table X, it can be observed that waveforms obtained from average model-based simulation are closely following the waveforms obtained from switching circuit based simulation during both steady-state and transients. Table XI gives the rms errors of the average circuit model with respect to the SCM for various system parameters and simulation time-steps. It can be observed that the RMS errors for the PV system simulation are also in acceptable range.

Further, note that the execution time required for simulating the ANPCI-based PV system will significantly reduce if DACM

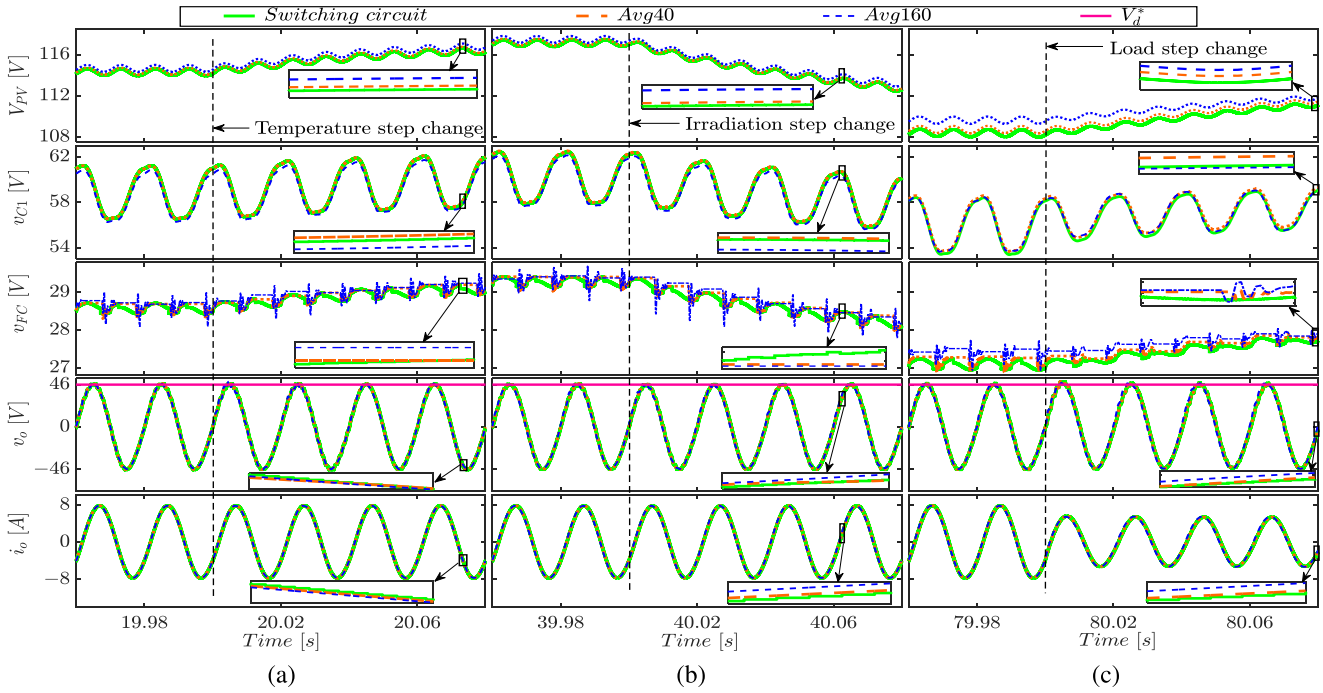

Fig. 21. Comparison of waveforms obtained from DACM and SCM simulations of ANPCI integrated PV array in closed-loop for step-down change in (a) temperature, (b) irradiation, and (c) load.

TABLE XII
EXECUTION TIMES (T_e) FOR 100 S RUN TIME OF PV ARRAY-INTEGRATED ANPCI USING SWITCHING CIRCUIT (SCM) AND AVERAGE MODEL (DACM)

Case	Simulation parameters*					Execution time	
	SCM			DACM		SCM	DACM
	T_{st}	T_p	f_s	T_{st}	T_p	T_e	T_e
I	1 μs	40 μs	10 kHz	1 μs	40 μs	4688 s	1732 s
II	1 μs	80 μs	10 kHz	1 μs	80 μs	4588 s	1692 s
III	1 μs	160 μs	10 kHz	1 μs	160 μs	4555 s	1680 s
IV	1 μs	50 μs	10 kHz	40 μs	40 μs	4622 s	96 s
V	2 μs	50 μs	5 kHz	80 μs	80 μs	2367 s	48 s
VI	5 μs	50 μs	2 kHz	160 μs	160 μs	991 s	24 s

*All other system parameters are the same as those considered for Fig. 21.

of the ANPCI is used for simulation. This is because the DACM-based simulations can use larger simulation time-steps (T_{st}) compared to those used for SCM-based simulations. To verify this, the execution times (T_e) required to simulate the PV system of Fig. 19 for 100 s runtime are compared in Table XII for six different cases: Case-I to Case-VI. In each case, different values of simulation time-step (T_{st}), plot step (T_p) are considered for SCM and DACM, as listed in Table XII. The simulation is run for a duration of 100 s while keeping all other system parameters the same as those considered for Fig. 21. Note that, as mentioned in Section V, these execution times are obtained by simulating the system using PSCAD/EMTDC software on a desktop computer with Intel Core$^{\text{TM}}$ i5-3470 CPU @ 3.2 GHz processor, 8 GB RAM, and Windows 10 64-bit operating system.

As listed in Table XII, for Case-I to III, the simulation time-step (T_{st}) is considered as 1 μs for both SCM- and DACM-based simulations, whereas the plot step (T_p) is varied from 40 to 160 μs. It can be seen that for the same simulation time-step, the DACM-based simulation runs approximately three times faster than the SCM-based simulation. Further, it is also observed that the value of plot step has negligible or no effect on the total execution time. In Case-IV, the simulation time-steps for the DACM-based simulations is considered as 40 μs, which is 40 times higher than that considered for SCM-based simulation. It can be seen that the execution time of DACM-based simulation is very less (approximately 50 times) compared to the SCM-based simulation. This clearly demonstrates the strength of DACM in reducing the simulation times required for system-level studies.

Further, in Case-V and Case-VI, the switching frequency of the SCM is changed to 5 and 2 kHz, respectively, which helps to increase the simulation time-step for SCM-based simulations. Even for these two cases, the DACM-based simulation has significantly smaller execution times compared with the SCM-based simulations.

VII. CONCLUSION

This article has presented the detailed operation and capacitor voltage-balancing algorithm of single-phase five-level ANPCI. The article has also developed a DACM of ANPCI. The DACM can include the nonidealities in the converter components and the capacitor voltage balancing. The model is also modular in nature and hence it can be extended for an N-level ANPCI. The article has also presented an SRF-dq controller for the single-phase ANPCI. The waveforms obtained from PSCAD/EMTDC simulations of switching circuit, experiments, and average model, and the corresponding RMS errors confirm that the averaged model presented can accurately predict the steady-state and dynamic waveforms of ANPCI in both open-loop and closed-loop operation. In addition, the effectiveness of the model is also demonstrated using a simple standalone PV system with ANPCI as the

power conversion stage. From the results presented, it is confirmed that the DACM requires significantly less computation time compared with the detailed SCM. Thus, the average model can be recommended for system-level studies with ANPCI as power converter interface to save the computational time and resources required.

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