An Input-Series Output-Parallel Modular Three-Phase AC–AC Capacitive-Link Power Converter

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***Abstract*—Modular converters with stackable cells are widely used in high-power applications, where the voltages and/or currents are beyond the ratings of the commercially available switches. Majority of existing modular converter topologies are based on dc-link converters that require several electrolytic capacitors with large capacitances, which reduce the lifetime of the power converter and increase size and volume. This article proposes an input-series output-parallel modular three-phase ac–ac universal power converter, which is formed by three identical and stackable capacitive-link modules that do not require electrolytic capacitors for power conversion. Exclusion of the electrolytic capacitors is achieved by operating the modules in discontinuous capacitor voltage mode. Each module requires two film capacitors with very small capacitances for transferring the power and provides galvanic isolation through high-frequency transformers. Utilization of film capacitors with small capacitances enhances the reliability. Furthermore, the proposed stackable capacitive-link modules enable a scalable and modular design. In this article, power cells are connected in series at the input and in parallel at the output to form a modular universal power converter that can share voltage/current among the power cells in an ac–ac power conversion system. Frequency transformation and voltage step-up/-down are among the other features of the proposed converter. The details of the operation principles along with design considerations are discussed in this article. Moreover, the proposed modular power converter with two power cells is evaluated through simulations and experiments.**

***Index Terms*—AC–AC converter, capacitive-link, high-frequency isolation, modular converter, stackable modules, universal converter.**

I. Introduction

CONVERTERS used in high-power applications typically need to handle voltages and/or currents beyond the ratings of the commercially available switches and need to offer high power density, high efficiency, high reliability, and low cost. Since the technology of the semiconductor devices is still limited, modular converters formed by stackable power cell topologies, in which the voltage and current can be shared among the power cells to reduce *dv/dt* and/or *di/dt* are preferable. This enables employing the commercially available wide-bandgap semiconductor devices for high-power conversion systems.

Majority of well-known ac–ac converters are based on two/multistage dc-link converters, in which two or more decoupled power conversion stages are cascaded. In these converters, several capacitors should be placed in series and parallel to from a dc-link, decouple conversion stages, and maintain a high dc voltage with small ripples. Multilevel dc-link-based converters with stackable cells are widely used in high-voltage high-power systems [1]. Among the several existing dc-link-based multilevel converters are neutral point clamped (NPC) [2], flying capacitor [3], [4], and cascaded H-bridge (CHB) [5], [6]. NPC is the most widely used multilevel topology in high-power industrial applications [7]. One challenge associated with NPCs is the voltage imbalance of the dc-link capacitors. Unequal loss distribution and unsymmetrical temperature distribution of the semiconductor junction are the other drawbacks of the NPCs [7], which have been the focus of many research efforts [8], [9]. CHBs offer very modularized layout and packaging by series connection of H-bridges; however, its major disadvantage is that each H-bridge requires an isolated dc source, which is typically provided by series/parallel connection of several capacitors [10]. Furthermore, modular multilevel converters (MMCs) have been proposed in [11], [12] for high-power applications with medium-/high-voltage levels, which offer flexible and modular design for any voltage level requirement. The main drawbacks of the MMCs are voltage imbalance of floating capacitors, acute voltage fluctuations at low frequency, and circulating currents [13], [14].

Clearly, presence of multiple large capacitors with high capacitances is inevitable in high-power multilevel converters, although the power processed by each power cell is a fraction of the total power; this increases initial cost as well as maintenance and replacement expenses [15]. Furthermore, typically, electrolytic capacitors, which have short lifetime, low reliability, and extreme sensitivity to temperature, are employed for this purpose [16].

Recently, an extensive amount of research has been conducted on universal power converters as an alternative solution for ac–ac conversion systems. They are known as a class of single-stage power converters, which perform the power conversion through small energy transferring elements, and offer high reliability,

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small size, light weight, and low cost. Universal converters do not have the challenges associated with electrolytic capacitors, and can be categorized as inductive-link and capacitive-link [17]–[30]. These converters extend the principles of the operation of indirect dc–dc converters to multiphase systems. For instance, in [17], the principles of the operation of a dc–dc buck–boost converter was extended to a three-phase ac–ac converter, in which an inductive link transfers the power from input phases to output phases, and the switches have hard switching.

In [31], the Dyna-C topology is proposed for solid state transformer (SST) applications. This converter consists of two three-phase bridges interconnected through a high-frequency transformer (HFT); the magnetizing inductance of this transformer acts as the energy transferring component. However, the reported efficiencies of this converter were poor mainly because of the high conduction losses [29]. In [30], an auxiliary circuit is added to the Dyna-C converter to enable the soft switching transition of the switches and improve the efficiency. In [32], [33], two families of soft-switching inductive-link universal power converters with reduced peak link current are proposed that can be applied in applications, where buck/boost/buck–boost functions and bidirectional power flow are required. However, no modular structure has been discussed for the proposed universal power converter. Capacitive-link universal power converters were proposed and studied in [26], [28], [34], [35]. Being universal, these converters can transfer power from any type of electrical source to any type of electrical load. The dc–ac and ac–ac power conversions are thoroughly investigated in [34], [35] that offer reduced number of switches with two-quadrant link.

Although universal power converters promise numerous advantages, modular and scalable structures of these power converters for ac–ac conversion systems have been rarely investigated, especially in hardware prototypes. Although the three-phase terminals of these power converters can be placed in parallel to share current, it is not feasible to connect the three-phase terminals in series for voltage sharing. Series/parallel connection of three-phase terminals to form a modular layout has never been discussed/evaluated for these power converters. For example, [30] has discussed a potential application of an inductive-link universal converter in a modular configuration, but no further discussions or results are provided in the article. In [36], a modular structure of Dyna-C is proposed for instantaneous reactive power compensation; however, the applications/results of the proposed power converter in a three-phase ac–ac conversion system are not discussed. In addition, in [37], another Dyna-C derived modular converter is proposed that can interface low-voltage dc or low-voltage ac, while providing bidirectional power flow and high-frequency galvanic isolation. However, the operation principles and results are solely presented for modular dc–dc and dc–ac conversions, and three-phase ac–ac conversion has not been discussed. Two other isolated ac–ac converters with HFT were presented in [38], [39], but the operating principles and scopes are totally different from the universal converters.

The authors of this article have studied and proposed modified stackable topologies of capacitive-link universal power converters in [40], [41], where a number of power cells can be stacked to share the voltage and current among the power cells. This article introduces a new modular ac–ac universal power converter topology, which is formed by three stackable capacitive-link modules. The stackable module is derived from the capacitive-link universal power converter proposed in [26], and operates in discontinuous capacitor voltage mode (DCVM). The proposed power cell topology does not require decoupling electrolytic capacitors; instead, film capacitors with very small capacitances can transfer the power, owing to the DCVM operation. This is a major advantage over the dc-link power converters, in terms of reliability. This is achieved by utilization of film capacitors with very small capacitances, which significantly lowers the failure rate of the proposed power converter. Another advantage of the proposed converter is that each module offers galvanic isolation through a compact HFT. This eliminates the need for a low-frequency transformer, which is very bulky. In the proposed topology, two or more power cells form a modular universal power converter, in which input three-phase terminals are connected in series and output three-phase terminals are connected in parallel such that voltage/current is shared among the power cells. Frequency transformation and voltage step-up/-down are among the other features of the proposed converter.

This modular converter topology was originally proposed in [42], in which basics of operation principles and preliminary low-power experimental results with one power cell were presented. In this article, the operation of the converter is discussed in more details and full-power experimental results with two power cells, verifying its scalability feature in input-series output-parallel (ISOP) configuration, are provided. Furthermore, in this article, in-depth discussions on the power loss and efficiency analysis, transformer design, inductive filter design, and clamping circuit design are provided. Additionally, the reliability of the proposed modular converter is discussed and compared with the commonly used MMC.

The article is structured as follows. Section II presents the configuration of the proposed stackable capacitive-link ac–ac converter. In Section III, the operation principles of the proposed capacitive-link converter are explained. Section IV presents the proposed control strategy and design consideration. The performance of the converter is verified through simulations and experiments in Sections V and VI, respectively. Section VII discusses the reliability improvement. Finally, Section VIII concludes the article and summarizes the features of the proposed converter.

II. Proposed Converter

Fig. 1 shows the configuration of module *X*, which has a single-phase ac port at the input side and a three-phase ac port at the output side. Here, "*X*" is a generic representation of the input phases, *A*, *B*, and *C*. In module X [Fig. 1(a)], an H-bridge diode rectifier is employed at the input side in parallel with an active switch, S_{inx} to control the input currents and voltages. The topology shown in Fig. 1(a) offers unidirectional power flow. The bidirectional power flow can be guaranteed by removing S_{inx} and replacing the input side diode bridge with an H-bridge that consists of four active switches, as shown in Fig. 1(b). Module *X* uses small film capacitors for power transferring,

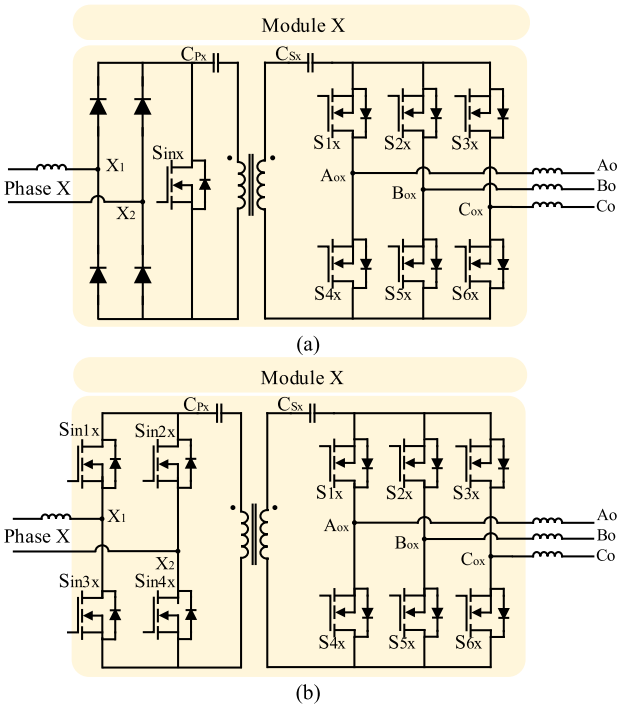

Fig. 1. (a) Unidirectional module and (b) bidirectional module.

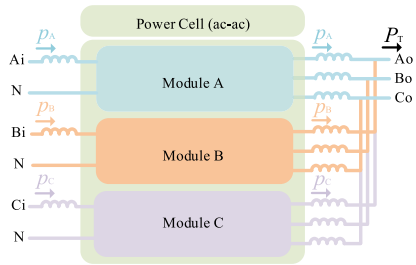

Fig. 2. Three-phase ac–ac power cell formed by modules *A*, *B*, and *C*.

instead of large electrolytic capacitors, owing to the DCVM control. Fig. 2 demonstrates the three-phase ac–ac power cell that is formed by stackable modules *A*, *B*, and *C*. Considering a lossless circuit (power flow from left to right), the output power that will be delivered to the load, is equal to summation of the power that modules of phases *A*, *B*, and *C* (p_A, p_B, p_C) are handling, as illustrated in Fig. 2. The proposed modular converter was originally proposed in [42], and in this article, more detailed analysis with full-power experimental results are provided.

Fig. 3 depicts the proposed modular ISOP configuration that is formed by *n* power cells for a high-power system, in which the input side deals with a three-phase high-voltage source and the output side handles high levels of current. The proposed converter offers a modularized layout. An ISOP configuration is developed and investigated in this article, which shares the voltage by series connection of the input three-phase terminals of the modules and shares the current at the output side by parallel connection of the output terminals.

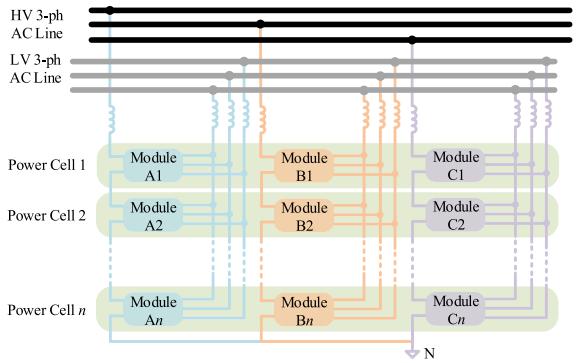

Fig. 3. Modular ISOP configuration formed by *n* power cells.

III. Principles of Operation

The principles of the operation are explained for the generic unidirectional module *X*, which can be extended to modules *A*, *B*, and *C*, as they follow the same guidelines. These guidelines were briefly presented in [42], and in this article, more details are discussed. Each module has three modes of operation: one mode for charging the link capacitors by the input side phase *X* current and two modes for discharging the link capacitors by the output side module currents. The charging mode duration is the same in modules *A*, *B*, and *C*; however, the duration of the discharging modes can be different in these modules. Despite having different durations for discharging modes, the link cycles in these three modules start and finish synchronously.

In order to control and operate the proposed modular converter, two key concepts are defined as "zone" and "mode." These two definitions help to determine the proper switching commands and implementation of the pulsewidth modulation. Mode can be either charging or discharging; a charging mode implies that the input current is energizing the link capacitors; and a discharging mode implies that an output current is de-energizing the link capacitors and energy is transferred to the output load. Zone depends on instantaneous value and polarity of three-phase voltage/current references.

The switching of the input side bridge in module *X* is straightforward and depends on the operation mode; if the converter is operating in the charging mode (mode 1*X*), S_{inxm} should be turned OFF; if the converter is operating in discharging modes (modes 2*X* and 3*X*), S_{inxm} should be turned ON [42]. However, the switching status of the output side bridges depends on both the operation mode and the zone, which can be obtained according to zone and mode. In order to determine switch selection, the two key concepts, i.e., mode and zone, need to be processed first. Once mode and zone values are known to the controller, the proper switches can be selected to operate the converter.

First, zone factor needs to be determined by using Fig. 4(a). The references for the output line–line voltages across the output terminals of the converter are denoted by $v_{abo}{}^*$, $v_{bco}{}^*$, and $v_{cao}{}^*$ and the output side current references are denoted by $i_{Ao}{}^*$, $i_{Bo}{}^*$, and $i_{Co}{}^*$. Fig. 4(a) demonstrates the zone determination with respect to the absolute maximum line–line voltage and current references. In Fig. 4(a), the $+/-$ sign next to the absolute term

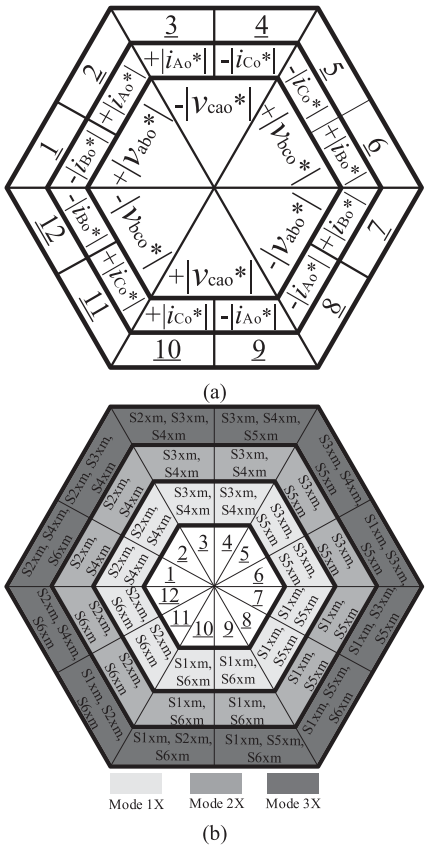

Fig. 4. (a) Output zone determination with respect to the output voltage/current references. (b) Switch selection for output bridges with respect to mode and zone.

TABLE I
ASSUMPTIONS FOR DESCRIPTION OF THE OPERATION PRINCIPLES

Line-Line Voltage References	Actual Currents
$abs(-v_{abo}^*)>abs(+v_{bco}^*)>abs(+v_{cao}^*)$	$abs(-i_{Aoxm})>abs(+i_{Boxm})>abs(+i_{Coxm})$

shows the actual polarity. For example, in zone 3, $v_{cao}{}^*$ has the largest absolute value with negative polarity and $i_{Ao}{}^*$ has the largest absolute value with a positive polarity.

Second, mode factor needs to be determined. Once the zone is determined, the switches that need to be turned ON during each mode can be obtained from Fig. 4(b). For example, if zone is determined as 8, and mode is 2*X*, S_{1xm}, and S_{5xm} from the output side bridge of module *X* need to be turned ON. The following explanations are given for zone 8, as shown in Table I. It should be noted that *abs*(*a*) in Table I denotes the absolute value of (*a*) and the positive (+) or negative (−) signs next to the voltages and currents show their polarities.

Fig. 5 shows the behavior of the module *X* during each mode of operation. In Fig. 5, X_{1m} and X_{2m} are the converter side terminals and X_{i1m} and X_{i2m} are the grid side terminals of the *m*th module connected to the phase *X* of the input ac source. It should be noted that $X\in\{A, B, C\}$ and $m\in\{1, 2, \ldots, n\}$, where *n* is the number of power cells. Furthermore, i_{xim} is the input side phase *X* current, and i_{Aoxm}, i_{Boxm}, and i_{Coxm} are the output currents of each module. i_{Aoxm}, i_{Boxm}, and i_{Coxm} can be determined with respect to i_{Ao}, i_{Bo}, and i_{Co}, which are the total

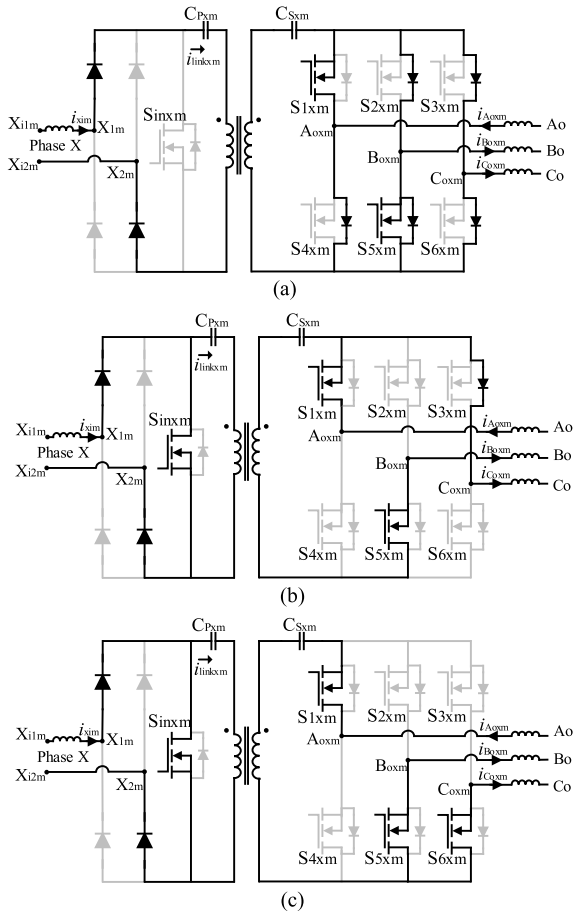

Fig. 5. Behavior of the module *X* in (a) mode 1*X*, (b) mode 2*X*, and (c) mode 3*X*. $X\in\{A, B, C\}$ and $m\in\{1, 2, \ldots, n\}$, where *n* is the number of power cells.

output load currents. The relationship between the output side module currents and the total output load currents is discussed in Section IV. The following subsections provide the details of operation for each mode.

A. Mode 1X

Fig. 5(a) demonstrates the behavior of the module *X* in mode 1*X* during which the current of phase *X* charges the link capacitors, C_{Pxm} and C_{Sxm}. At this moment, it is assumed that the phase *X* current is positive (flowing from left to right). If the current is negative, the complementary diodes will be forward-biased. During this mode, S_{inxm} is kept OFF, so that i_{xim} flows through the link capacitors and the link capacitors voltages ramp up. The output side anti-parallel diodes provide the path for the link current to flow back toward the input side bridge. Also, two switches at the output side (according to Fig. 4, S_{1xm} and S_{5xm} for the given time interval) are turned ON to let the three-phase output currents freely flow, as shown in Fig. 5(a). The selection of these two switches depends on the output line–line voltage/current references. For the condition of Table I, switch S_{1xm} needs to be turned ON to let i_{Aoxm} flow. Also, since i_{Boxm} is positive (flowing from left to right), switch S_{5xm} needs to be turned ON and the anti-parallel diodes of S_{2xm},

S_{4xm}, S_{3xm}, S_{5xm}, and S_{6xm} will handle i_{Boxm} and i_{Coxm} and the link current that comes from the input side. Depending on the value of the input and output currents, the conduction of the switches/diodes for the output side bridge may be different in charging modes. However, the switching algorithm does not change. Once the duration of this mode meets its reference, the discharging modes begin. Desired duration of each mode can be calculated using the current and voltage references, which is discussed in Section IV of the article.

B. Mode 2X

Thus far, the link capacitors are energized, and the link voltage has ramped up to a certain value. In discharging modes, the output currents need to de-energize the link capacitors so that the stored energy in the capacitors is transferred to the load. A negative current (flowing from right to left) has to flow through the link capacitors until their voltages reach zero volts and DCVM operation is ensured. During mode 2*X*, which is the second operation mode and the first discharging mode for module *X*, the second largest output current (i_{Boxm} in Fig. 5) discharges the link capacitors. This is accomplished by turning ON S_{inxm} and providing a path for the negative link current to discharge the capacitors. Turning ON S_{inxm} also allows phase *X* current to freely flow. There is no switch transition at the output side bridge from mode 1*X* to 2*X* and the output switches follow the gate commands of mode 1*X* as it is depicted in Fig. 4(b). However, all the anti-parallel diodes at the output-side stop conducting except for the anti-parallel diode of switch S_{3xm}, which provides a path for current of phase C_o. Once the duration of this mode is met, the next operation mode begins.

C. Mode 3X

During mode 3*X*, the largest output current (i_{Aoxm} in Fig. 5) fully discharges the link capacitors. To do so, S_{inxm} is kept ON and switch S_{6xm} is turned ON (according to Fig. 4), so that i_{Coxm} flows through this switch and the anti-parallel diode of S_{3xm} stops conducting (this diode was conducting in the previous mode). Therefore, i_{Aoxm} flows through the link capacitors and i_{Boxm} and i_{Coxm} flow through S_{5xm} and S_{6xm}. Module *X* remains in this mode until the link capacitors are fully discharged. When T_S (period of the linkcycle) is met, the next link cycle in all modules starts synchronously. It should be noted that if the link capacitors of module *X* are fully discharged before the end of the link cycle (T_S), the link capacitors current and voltage remain zero, and no power is transferred from input side of module *X* to the output side until the end of cycle.

D. Power Cell Operation

Fig. 6 illustrates the main waveforms of the converter with one power cell ($n = 1$). The link capacitors voltages are shown in this figure along with the current that flows through the link capacitors of each module. The depicted link capacitors voltage for each module is the summation of the voltages across the primary and secondary sides' capacitors of that module. Also,

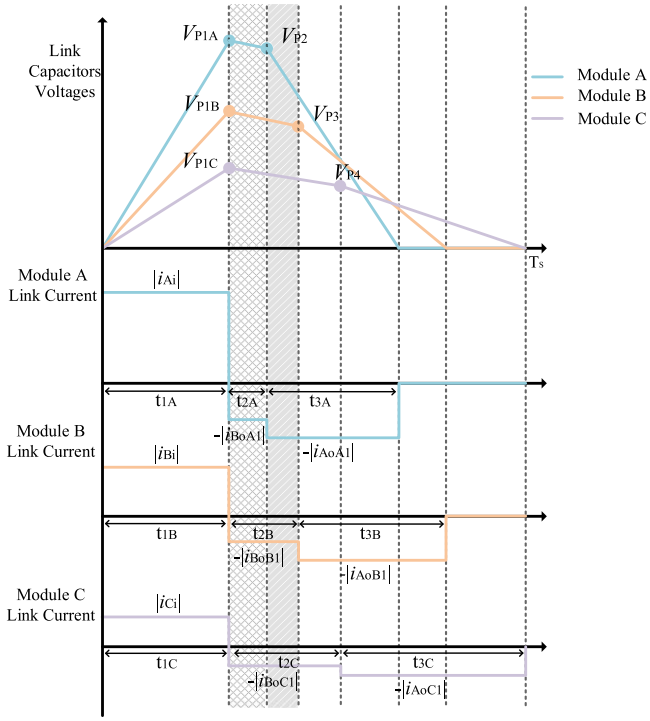

Fig. 6. Key operating waveforms of the proposed converter topology.

duration of each mode is denoted by t_{1X}, t_{2X}, and t_{3X}, where $X \in \{A, B, C\}$.

The behavior of the modules *A*, *B*, and *C* during the charging mode is shown in Fig. 7(a), assuming that phase *A* current is positive and phase *B* and *C* currents are negative. This time interval is $0<t<t_{1A}$. It should be noted that duration of the charging mode for modules *A*, *B*, and *C* is equal, $t_{1A}=t_{1B}=t_{1C}$, and the behavior and switch selection of these three modules are identical during the charging mode. Fig. 7(b) demonstrates the operation of the power cell when all the modules are operating in their first discharging mode ($t_{1A}<t<t_{1A}+t_{2A}$with the gray pattern of outlined diamond). The assumed conditions for the output side voltage/current references follow Table I. Hence, the behavior of modules *A*, *B*, and *C* should be according to mode 2*X* of module *X* in Fig. 5(b).

Fig. 7(c) illustrates the behavior of the power cell for the time interval $t_{1A}+t_{2A}<t<t_{1B}+t_{2B}$ (specified with the gray pattern of upward diagonal) of Fig. 6, during which the operation modes of the three modules are not the same. In this time interval, module *A* is operating in the second discharging mode (mode 3*A*, $t>t_{1A}+t_{2A}$) and modules *B* and *C* are operating in their first discharging mode (modes 2*B* and 2*C*, respectively). The behavior of the three modules during the rest of the time intervals can be simply analyzed by using the proper mode of operation of module X (Fig. 5). One can realize that the operation modes of modules *A*, *B*, and *C* during discharging modes are not necessarily the same. However, in a modular configuration with *n* power cells, as shown in Fig. 3, the modules of the same input phase, e.g. , modules *A*1, *A*2, …, *An*, would have the same operating modes, mode durations, and behavior.

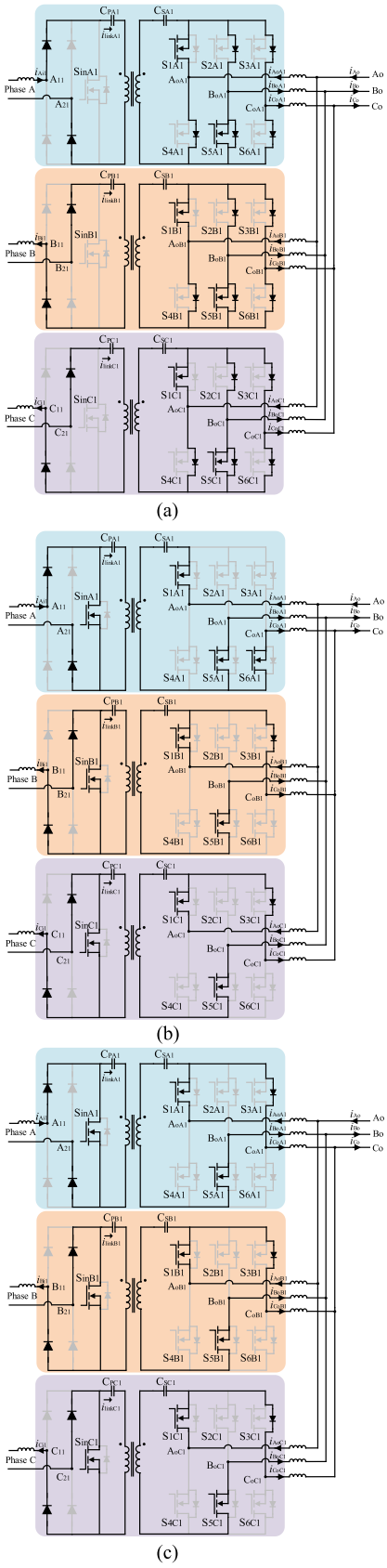

Fig. 7. (a) Behavior of modules *A*, *B*, and *C* during the charging mode. (b) Behavior of the modules *A*, *B*, and *C* when they are in the first discharging mode. (c) Behavior of the modules *A*, *B*, and *C*, when module *A* is in the second discharging mode and modules *B* and *C* are in the first discharging mode ($n = 1$).

IV. Analysis, Design, and Control

This section establishes the design and control implementation guidelines for the proposed converter. Duration of each operation mode for each module is denoted by t_{1X}, t_{2X}, t_{3X}, where the generic letter $X \in \{A, B, C\}$.

A. Mathematical Analysis

${v_{Ai}}^*$, ${v_{Bi}}^*$, ${v_{Ci}}^*$, ${v_{Ao}}^*$, ${v_{Bo}}^*$, and ${v_{Co}}^*$ are the input and output phase voltage references, respectively. ${i_{Ai}}^*$, ${i_{Bi}}^*$, ${i_{Ci}}^*$, ${i_{Ao}}^*$, ${i_{Bo}}^*$, and ${i_{Co}}^*$ are the input and output current references, respectively. Given that in an ISOP configuration with n power cells, the input terminals are connected in series, the input voltage references (${v_{Ai}}^*$, ${v_{Bi}}^*$, and ${v_{Ci}}^*$) should be divided by n; and, since the output terminals are connected in parallel, the output current references (${i_{Ao}}^*$, ${i_{Bo}}^*$, and ${i_{Co}}^*$) should be divided by n. The output current references for each module can be obtained as [42]

$$ {i_{Ao,\,A}}^* = {i_{Ao}}^* \times p_a/n \tag{1} $$

$$ {i_{Bo,A}}^* = {i_{Bo}}^* \times p_a/n \tag{2} $$

$$ {i_{Co,A}}^* = {i_{Co}}^* \times p_a/n \tag{3} $$

$$ {i_{Ao,B}}^* = {i_{Ao}}^* \times p_b/n \tag{4} $$

$$ {i_{Bo,B}}^* = {i_{Bo}}^* \times p_b/n \tag{5} $$

$$ {i_{Co,B}}^* = {i_{Co}}^* \times p_b/n \tag{6} $$

$$ {i_{Ao,C}}^* = {i_{Ao}}^* \times p_c/n \tag{7} $$

$$ {i_{Bo,C}}^* = {i_{Bo}}^* \times p_c/n \tag{8} $$

$$ {i_{Co,C}}^* = {i_{Co}}^* \times p_c/n \tag{9} $$

where ${i_{Ao,A}}^*$, ${i_{Bo,A}}^*$, ${i_{Co,A}}^*$, ${i_{Ao,B}}^*$, ${i_{Bo,B}}^*$, ${i_{Co,B}}^*$, ${i_{Ao,C}}^*$, ${i_{Bo,C}}^*$, and ${i_{Co,C}}^*$ are, respectively, the output current references for modules *A*, *B*, and *C*. p_a, p_b, and p_c are the per-unit values of power for each phase, which are equal to p_A/P_T, p_B/P_T, and p_C/P_T, respectively, where p_A, p_B, and p_C are the total instantaneous power values that modules of phases *A*, *B*, and *C* handle, respectively, and P_T is the rated power, which is equal to $p_A+p_B+p_C$.

In Fig. 6, V_{P1A} and V_{P2} are the values of the link capacitors voltage in module A at the end of modes 1*A* and 2*A*, respectively. Mode 1*A* represents mode 1 for module *A* and is similar to mode 1*X* for module *X* of Fig. 5. The same concept can be extended to modules *B* and *C*, as well. V_{P1B} and V_{P3} are the values of the link capacitors voltage in module *B* at the end of modes 1*B* and 2*B*, respectively; V_{P1C} and V_{P4} are the values of the link capacitors voltage in module *C* at the end of modes 1*C* and 2*C*, respectively.

V_{CM1A}, V_{CM1B}, and V_{CM1C} are the averages of the unfiltered voltage seen across input converter-side terminals $A_{11}A_{21}$, $B_{11}B_{21}$, and $C_{11}C_{21}$, respectively, during the charging mode of the given link cycle. The purpose of the controller algorithm is to equalize these averages with the input side reference voltages (${v_{Ai}}^*/n$, ${v_{Bi}}^*/n$, and ${v_{Ci}}^*/n$). In Fig. 6, these voltage references are assumed to be sorted as $|{v_{Ai}}^*| > |{v_{Bi}}^*| > |{v_{Ci}}^*|$ for the given cycle.

Also, V_{DM1A},V_{DM1B},V_{DM1C}, V_{DM2A},V_{DM2B}, and V_{DM2C} are the averages of the unfiltered line–line voltage seen at the output terminals of modules *A*, *B*, and *C*, during the first and second discharging modes, respectively. V_{DM1A},V_{DM1B}, and V_{DM1C} are associated with the phase pairs that have the second largest output line–line voltage reference and V_{DM2A},V_{DM2B}, and V_{DM2C} are associated with the phase pairs that have the minimum output line–line voltage reference. The references for the voltage across these phase pairs can be calculated with respect to ${v_{Ao}}^*$, ${v_{Bo}}^*$, and ${v_{Co}}^*$. The relation between the average voltages and the link capacitors voltages are as follows [42]:

$$V_{CM1A} = \frac{1}{2} V_{P1A} t_{1A} f \tag{10}$$

$$V_{CM1B} = \frac{1}{2} V_{P1B} t_{1B} f \tag{11}$$

$$V_{CM1C} = \frac{1}{2} V_{P1C} t_{1C} f \tag{12}$$

$$V_{DM1A} = \frac{1}{2} \left(V_{P1A} + V_{P2}\right) t_{2A} f \tag{13}$$

$$V_{DM1B} = \frac{1}{2} \left(V_{P1B} + V_{P3}\right) t_{2B} f \tag{14}$$

$$V_{DM1C} = \frac{1}{2} \left(V_{P1C} + V_{P4}\right) t_{2C} f \tag{15}$$

$$V_{DM2A} = \frac{1}{2} V_{P2} t_{3A} f \tag{16}$$

$$V_{DM2B} = \frac{1}{2} V_{P3} t_{3B} f \tag{17}$$

$$V_{DM2C} = \frac{1}{2} V_{P4} t_{3C} f. \tag{18}$$

Because of the parallel connection of the modules *A*, *B*, and *C* terminals at the output side, the following condition exists for V_{DM1A}, V_{DM1B},V_{DM1C},V_{DM2A},V_{DM2B} ,and V_{DM2C} [42]:

$$V_{DM1A} = V_{DM1B} = V_{DM1C} \tag{19}$$

$$V_{DM2A} = V_{DM2B} = V_{DM2C}\,. \tag{20}$$

For simplicity, in the following, V_{DM1A},V_{DM1B}, andV_{DM1C} are replaced with V_{DM1}, andV_{DM2A},V_{DM2B}, and V_{DM2C} are replaced with V_{DM2}.

The current that flows through the link capacitors of each module during charging mode is equal to the absolute value of the current of input phase that is connected to the module; i.e., I_{CM1A}, I_{CM1B}, and I_{CM1C} are the link capacitor currents in modules *A*, *B*, and *C*, respectively, and are equal to absolute values of i_{Ai1}, i_{Bi1}, and i_{Ci1}, respectively, as shown in Fig. 7. I_{DM1A},I_{DM1B}, andI_{DM1C} are the second largest module output current discharging the link capacitors of modules *A*, *B*, and *C*, respectively, in the first discharging mode; and I_{DM2A}, I_{DM2B}, and I_{DM2C} are the largest module output current discharging the link capacitors of modules *A*, *B*, and *C*, respectively, in the second discharging mode. The relation between the link currents, link voltages, and the equivalent link capacitance of each module is shown as follows [42]:

$$I_{CM1A} = C_{\text{eq}} \frac{V_{P1A}}{t_{1A}} \tag{21}$$

$$I_{CM1B} = C_{\text{eq}} \frac{V_{P1B}}{t_{1B}} \tag{22}$$

$$I_{CM1C} = C_{\text{eq}} \frac{V_{P1C}}{t_{1C}} \tag{23}$$

$$I_{DM1A} = C_{\text{eq}} \frac{V_{P1A} - V_{P2}}{t_{2A}} \tag{24}$$

$$I_{DM1B} = C_{\text{eq}} \frac{V_{P1B} - V_{P3}}{t_{2B}} \tag{25}$$

$$I_{DM1C} = C_{\text{eq}} \frac{V_{P1C} - V_{P4}}{t_{2C}} \tag{26}$$

$$I_{DM2A} = C_{\text{eq}} \frac{V_{P2}}{t_{3A}} \tag{27}$$

$$I_{DM2B} = C_{\text{eq}} \frac{V_{P3}}{t_{3B}} \tag{28}$$

$$I_{DM2C} = C_{\text{eq}} \frac{V_{P4}}{t_{3C}} \tag{29}$$

Where C_{eq} is the equivalent link capacitance in each module ($C_{\text{eq}} = \frac{C_{PA}}{2} = \frac{C_{SA}}{2} = \frac{C_{PB}}{2} = \frac{C_{SB}}{2} = \frac{C_{PC}}{2} = \frac{C_{SC}}{2}$), and *f* is the link frequency. Using (1)–(29), the transferred power during each mode of modules *A*, *B*, and *C* can be calculated as [42]

$$P_{CM1A} = V_{CM1A} \times I_{CM1A} \tag{30}$$

$$P_{CM1B} = V_{CM1B} \times I_{CM1B} \tag{31}$$

$$P_{CM1C} = V_{CM1C} \times I_{CM1C} \tag{32}$$

$$P_{DM1A} = V_{DM1} \times I_{DM1A} \tag{33}$$

$$P_{DM1B} = V_{DM1} \times I_{DM1B} \tag{34}$$

$$P_{DM1C} = V_{DM1} \times I_{DM1C} \tag{35}$$

$$P_{DM2A} = V_{DM2} \times I_{DM2A} \tag{36}$$

$$P_{DM2B} = V_{DM2} \times I_{DM2B} \tag{37}$$

$$P_{DM2C} = V_{DM2} \times I_{DM2C}. \tag{38}$$

Then, the duration of each mode can be obtained as [42]

$$t_{1A} = \frac{2V_{CM1A}}{\sqrt{\frac{2fP_{CM1A}}{C_{\text{eq}}}}} \tag{39}$$

$$t_{1B} = \frac{2V_{CM1B}}{\sqrt{\frac{2fP_{CM1B}}{C_{\text{eq}}}}} \tag{40}$$

$$t_{1C} = \frac{2V_{CM1C}}{\sqrt{\frac{2fP_{CM1C}}{C_{\text{eq}}}}} \tag{41}$$

$$t_{2A} = \frac{2V_{DM1}}{\sqrt{\frac{2fP_{CM1A}}{C_{\text{eq}}}} + \sqrt{\frac{2f(P_{CM1A} - P_{DM1A})}{C_{\text{eq}}}}} \tag{42}$$

$$t_{2B} = \frac{2V_{DM1}}{\sqrt{\frac{2fP_{CM1B}}{C_{\rm eq}}} + \sqrt{\frac{2f(P_{CM1B}-P_{DM1B})}{C_{\rm eq}}}} \tag{43}$$

$$t_{2C} = \frac{2V_{DM1}}{\sqrt{\frac{2fP_{CM1C}}{C_{\rm eq}}} + \sqrt{\frac{2f(P_{CM1C}-P_{DM1C})}{C_{\rm eq}}}} \tag{44}$$

$$t_{3A} = \frac{2V_{DM2}}{\sqrt{\frac{2f(P_{CM1A}-P_{DM1A})}{C_{\rm eq}}}} \tag{45}$$

$$t_{3B} = \frac{2V_{DM2}}{\sqrt{\frac{2f(P_{CM1B}-P_{DM1B})}{C_{\rm eq}}}} \tag{46}$$

$$t_{3C} = \frac{2V_{DM2}}{\sqrt{\frac{2f(P_{CM1C}-P_{DM1C})}{C_{\rm eq}}}}. \tag{47}$$

B. Link Capacitors Design

In order to keep the link capacitors voltages to operate in DCVM, the following condition should be met for module *X*, where *X* can be *A*, *B*, or *C*:

$$t_{1X} + t_{2X} + t_{3X} \le \frac{1}{f}. \tag{48}$$

Using (39), (42), and (45) to replace t_{1X}, t_{2X}, and t_{3X}, the maximum value for the equivalent link capacitance is obtained. The link capacitance has its maximum value when $P_{DM1A} = P_{DM2A}$ and $V_{DM1} = V_{DM2}$, and it can be determined based on the selected link frequency at this point:

$$C_{\rm eq} \le \frac{P_T/n}{f\left(V_i/n + 3\sqrt{2}V_o\right)^2}. \tag{49}$$

To calculate the link peak voltage, the power of module *A* can be calculated using (10) and (21):

$$P_{CM1A} = \frac{1}{2}\left(V_{P1A}\right)^2 C_{\rm eq} f. \tag{50}$$

The link voltage has its maximum value when power of module *A* is at its peak, which is $2P_T/3n$. Therefore, the link peak voltage is equal to

$$V_{C\text{link,max}} = \sqrt{\frac{4P_T/n}{3fC_{\rm eq}}} \tag{51}$$

where V_i and V_o are the peak values of the line–line input and output voltages, respectively, *n* is the number of power cells, and $V_{C\text{link,max}}$is the peak value of the link voltage in each module, which determines the voltage stress of the switches.

C. Selecting the Number of Power Cells in the Proposed Modular Converter

Once the power level (P_T), input/output voltages V_i and V_o, and switching frequency (f) are known, the design procedure can begin with an assumed number of power cells (for example, $n = 1$). Then, $C_{\rm eq}$ and $V_{C\text{link,max}}$ can be calculated using (49) and (51). If the link peak voltage exceeds the blocking voltage capability of the commercially available switching devices, the number of power cells can be incremented by one unit, and this process continues until the link voltage, which is equal to the voltage stress of the switches, becomes sufficiently lower than the blocking voltage of the selected switching devices. By the end of this part, $C_{\rm eq}$ is known and the design procedure can proceed to the design of inductive filters, which is discussed in part E of this section. Eventually, the design of the transformer, which is discussed Section VI-A, can be performed. To minimize the effect of leakage inductance of the transformer on the performance of the converter a clamping circuit is used, the details of which will be discussed in Section VI-B. Once the design is complete, the control algorithm, which will be discussed in the next part using (1)–(47), is implemented.

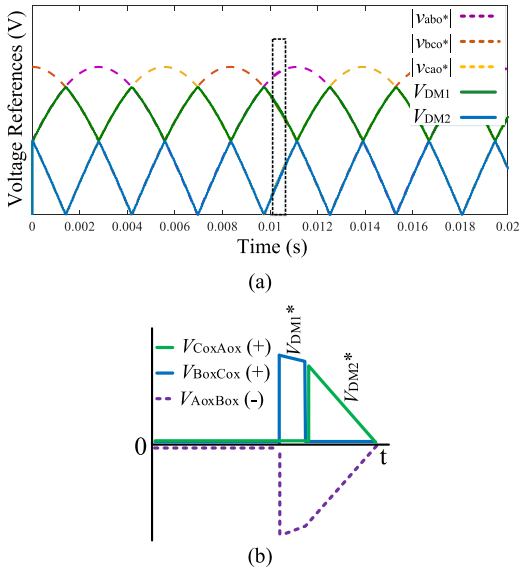

Fig. 8. (a) Absolute values of line–line voltage references. (b) Unfiltered line–line voltages of module *X* for the given condition of Table I.

D. Control Algorithm Implementation

In order to calculate the desired duration of each mode according to (39)–(47), the following steps should be taken:

$I_{CM1A}, I_{CM1B}, I_{CM1C}, V_{CM1A}, V_{CM1B}$, and V_{CM1C} should be replaced with the proper values calculated by absolute value of current/voltage references of input phases *A*, *B*, and *C*, respectively. It should be noted that t_{1A}, t_{1B}, and t_{1C} are fixed and equal for a given set of voltage and current references. Hence, for the control purpose, only one of them is calculated and used to regulate the duration of the charging mode in all the modules.

V_{DM1} and V_{DM2} should be replaced with the second largest and minimum absolute line–line voltage references, respectively, which can be obtained from the output side voltage references ($v_{Ao}{}^*$, $v_{Bo}{}^*$, and $v_{Co}{}^*$), as shown in Fig. 8. For example, for the given conditions of Table I (the black-dashed frame in Fig. 8), $V_{DM1}{}^*$ and $V_{DM2}{}^*$should be replaced with instantaneous values of $|v_{bco}{}^*|$ and $|v_{cao}{}^*|$, respectively.

$I_{DM1A}, I_{DM1B}, I_{DM1C}, I_{DM2A}, I_{DM2B}$, and I_{DM2C} should be replaced with the desired largest and second largest absolute current references for each module.

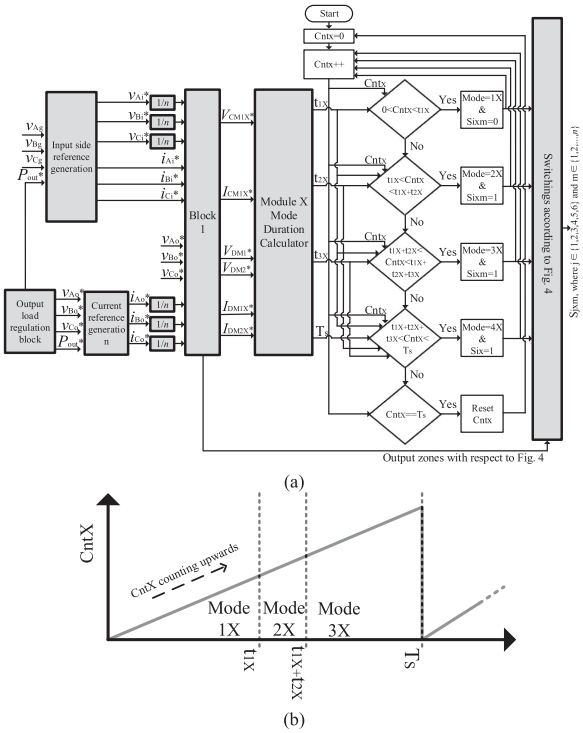

Fig. 9. (a) Control block diagram of module *X*, where $X \in \{A, B, C\}$. (b) *CntX* that counts upwards and determines the mode.

These mode durations must ensure that during each link cycle, averages of unfiltered line–line voltages across terminals, for example, terminals $B_{ox}C_{ox}$ (V_{BoxCox}) and $C_{ox}A_{ox}$ (V_{CoxAox}) as shown in Fig. 8(b), meet the reference voltages [$|v_{bco}{}^*|$ and $|v_{cao}{}^*|$ in Fig. 8(a)]; this guarantees that the currents/voltages are regulated at their reference values. Considering that this is a three-phase three-wire system, if two line–line voltages are regulated, the other line–line voltage will be regulated too.

The task of the control algorithm is to regulate the duration of each mode, such that the references of the currents and voltages are met. Fig. 9 shows the implemented control block diagram for generic module *X*. The inputs to Block 1 of the diagram are input and output current/voltage references; since the modules are connected in series at the input side, the input voltage references are divided by *n*; also, since the output side terminals are in parallel, and output current references are divided by *n*. Block 1's task is to sort the voltage/current references and generate $V_{CM1X}{}^*$, $I_{CM1X}{}^*$, $V_{DM1}{}^*$, $V_{DM2}{}^*$, $I_{DM1X}{}^*$, and $I_{DM2X}{}^*$, which are the references used in (39)–(47). These references are input to the next block, which calculates the mode durations for generic module *X* according to (39)–(47). The flowchart depicts the control logic for operating modes of each module.

Once the proper voltage/current references are generated, they are used by the control block diagram, as shown in Fig. 9(a). The inputs to Block 1 of the diagram are input and output current/voltage references; since the modules are connected in series at the input side, the input voltage references are divided by *n*; also, since the output side terminals are in parallel, and output current references are divided by *n*. Block 1's task is to sort the voltage/current references and generate $V_{CM1X}{}^*$, $I_{CM1X}{}^*$, $V_{DM1}{}^*$, $V_{DM2}{}^*$, $I_{DM1X}{}^*$, and $I_{DM2X}{}^*$, which are the references used in (39)–(47). Block 1 calculates these values for all modules *A*, *B*, and *C*. These values are then used by "Module *X* Mode Duration Calculator," which constantly calculates the proper mode durations such that the references ($V_{CM1X}{}^*$, $I_{CM1X}{}^*$, $V_{DM1}{}^*$, $V_{DM2}{}^*$, $I_{DM1X}{}^*$, and $I_{DM2X}{}^*$) can be met. Once the mode durations are calculated, they are continuously compared with *CntX* that is counting upwards from 0 to T_s. *CntX*'s counting waveform is shown in Fig. 9(b). *CntX* value determines the mode of operation. For instance, if *CntX* values are between t_{1X} and $t_{1X}+t_{2X}$, mode is assigned as 2*X*, which turns ON switch S_{inxm}. Hence, in order to determine the proper switches to turn ON, output zone needs to be determined, which can be done with respect to Fig. 4(a). Now that mode and zone are assigned, Fig. 4(b) determines the proper switching commands of the converter. For instance, if zone is 8 and mode is 2*X*, switches S_{1xm} and S_{5xm} need to be turned ON. Once *CntX* reaches T_s, it resets to zero and starts counting upwards again.

One counter is assigned to each module (*CntA*, *CntB*, and *CntC*). Since all the modules corresponding to each input phase, e.g., *A*1, *A*2, etc., behave identically, one counter per input phase is enough to determine the mode of operation for all modules at each moment. Hence, the switch selection is performed for module *X*, and then the switch commands of module *X* are applied to all submodules of module *X*, i.e., *X*1, *X*2, etc.

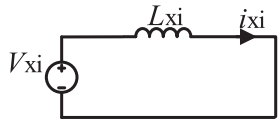

Fig. 10. Equivalent circuit of the input phase *X* during discharging modes.

E. Inductive Filter Analysis

The design procedure for inductive filters of input and output ports of the proposed ISOP modular converter is discussed in this part. At first, behavior of the input filter is presented. During discharging modes, the input phase currents freely flow through the input side diode-bridge and switch S_{inxm} in a short-circuit path. This can be observed in Figs. 5 and 7(b) and (c). The equivalent circuit of the input phases during discharging modes is shown in Fig. 10. In this figure, V_{Xi} is the line-neutral voltage of input phase *X*, where $X \in \{A, B, C\}$. Since this is a very short time interval compared to the line cycle, the ac source voltage is considered to be constant during this time interval. L_{Xi} is the input side inductance and i_{Xi} is the input phase current.

A KVL can be written for this circuit:

$$V_{Xi} = L_{Xi} \frac{di_{Xi}}{dt}. \tag{52}$$

After simplification, the following equations can be obtained:

$$L_{Xi} = \frac{V_{Xi} \times t_d}{\Delta i_{Xi}} \tag{53}$$

$$t_d = \frac{1}{f} - t_{1X} \tag{54}$$

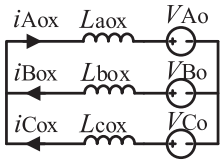

Fig. 11. Equivalent circuit of the output side during charging modes.

Where t_d is the total discharging time and Δi_{Xi} is the current ripple. The worst-case scenario, i.e., the maximum current ripple, happens when the expression $V_{Xi} \times t_d$ has the maximum value, which occurs when V_{Xi} is at its maximum value. This is because t_{1X} has a constant value under certain operating condition and so does t_d. Hence, the input inductance can be determined by

$$L_{Xi} = \frac{V_{Xi,\text{peak}} \times \left(\frac{1}{f} - t_{1X}\right)}{\Delta i_{Xi}}. \tag{55}$$

In order to analyze the output side inductive filter, the behavior of the converter is studied during charging mode. During charging mode, the output currents freely flow through the output side bridges in a short-circuit path. The equivalent circuit of the output side during the charging mode is shown in Fig. 11. In this figure, V_{Ao}, V_{Bo}, and V_{Co} are the voltages across the load (measured as phase-neutral). Since this is a very short time interval, these voltages are considered to be constant during this time interval. L_{aox}, L_{box}, and L_{cox} are the output side inductances, and i_{Aox}, i_{Box}, and i_{Cox} are the output currents of module X.

Three KVLs can be written for this circuit ($L_{aox} = L_{box} = L_{cox} = L_o$)

$$V_{Bo} - V_{Ao} = L_o \frac{di_{Aox}}{dt} + L_o \frac{di_{Box}}{dt} \tag{56}$$

$$V_{Co} - V_{Ao} = L_o \frac{di_{Aox}}{dt} + L_o \frac{di_{Cox}}{dt} \tag{57}$$

$$V_{Co} - V_{Bo} = L_o \frac{di_{Cox}}{dt} - L_o \frac{di_{Box}}{dt}. \tag{58}$$

After simplification, the following equation can be obtained:

$$(V_{Bo} - V_{Ao}) + (V_{Co} - V_{Ao}) = 3L_o \frac{di_{Aox}}{dt} \rightarrow$$

$$L_o = \frac{[(V_{Bo} - V_{Ao}) + (V_{Co} - V_{Ao})] \times t_{1x}}{3\Delta i_{Aox}} \tag{59}$$

where t_{1x} is the charging time, which is given in (39)–(41), and Δi_{Aox} is the output current ripple of the module X. The maximum current ripple happens when the expression $[(V_{Bo} - V_{Ao}) + (V_{Co} - V_{Ao})]$ has the maximum value, which would be equal to $\sqrt{3}V_o$. Hence, given that t_{1x} is constant for certain operating condition, the relation between the inductance L_o and current ripples can be written as

$$L_o = \frac{\sqrt{3}V_o \times t_{1x}}{3\Delta i_{Aox}}. \tag{60}$$

TABLE II
SPECIFICATIONS OF THE INVESTIGATED SYSTEM (SIMULATION)

Parameters		Value
Nominal Power (P_T)		25 [kW]
Link Frequency (f)		25 [kHz]
Equivalent Link Capacitance (C_{eq}) in each phase		0.47 [μF]
Input L-L Voltage (V_i)		850 [V], 60 [Hz]
Output L-L Voltage (V_o)		140 [V], 75 [Hz]
Input LCL Filter	L_G (grid side)	2.5 [mH]
	L_C (converter side)	0.3 [mH]
	C (star connection)	0.15 [μF]
Output L Filter		0.1 [mH]

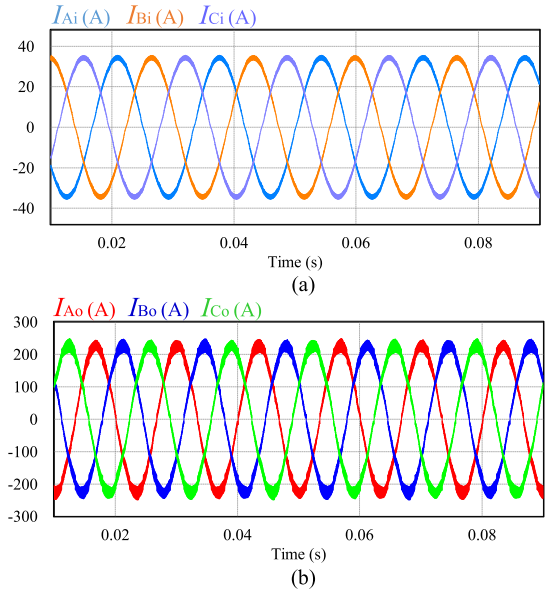

Fig. 12. (a) Three-phase input currents and (b) three-phase output currents of the modular converter with two power cells.

V. SIMULATION RESULTS

In order to evaluate the performance of the proposed topology, a three-phase ac–ac converter with two power cells ($n = 2$) in ISOP configuration is designed and simulated in PSIM. Specifications and component values of the investigated system are listed in Table II. According to (49), the selected equivalent link capacitance for each module is 0. 47 μF, which is very small for a 25-kW power converter and a significant contributor to lifetime and reliability improvement of the proposed modular power converter, compared to the dc-link-based power converters.

Fig. 12 (a) and (b) represents the input and output three-phase sinusoidal currents with the frequency of 60 and 75 Hz, respectively. Evidently, the proposed converter is capable of frequency transformation. The rms and total harmonic distortion values of the input and output currents are 24 A, 144 A, 2.5%, and 5.2%, respectively. For the input side, an LCL filter is employed to remove the unwanted harmonics, while an L filter is adopted for the output side.

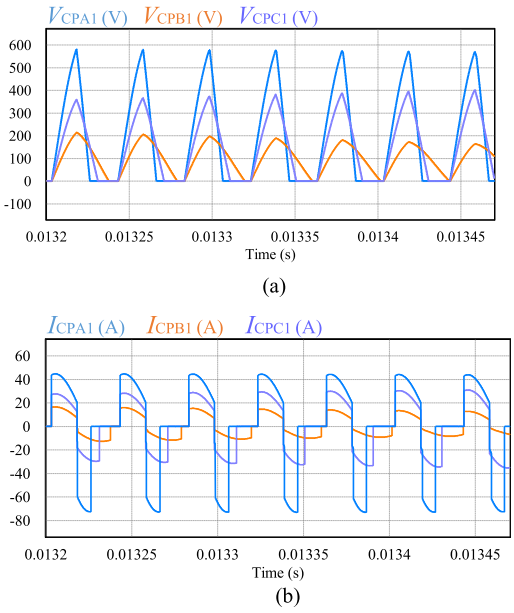

Fig. 13. (a) Link capacitors voltages of the modules $A1$, $B1$, and $C1$. (b) Link currents of modules $A1$, $B1$, and $C1$ in power cell 1.

Fig. 13(a) depicts the voltages across the link capacitors of modules $A1$, $B1$, and $C1$ in power cell 1; and Fig. 13(b) shows the currents that pass through the link capacitors in the three modules of the power cell 1. Evidently, the charging modes in all modules start and end synchronously, which is controlled according to Fig. 7. Once the link capacitors of each module are fully discharged, the link current and voltage remain zero until the next link cycle begins, ensuring DCVM. The maximum discharging current of the link capacitors that each module handles is equal to 1/3 of the output maximum current (i.e., 68 A). In fact, in a system with n power cells, the maximum discharging current that would flow through the link capacitors of each module is equal to $2/3n$ of the rated maximum output current. The coefficient $1/n$ is due to parallel connection of the output terminals of n power cells, such that each power cell handles $1/n$ of total power. The coefficient 2/3 comes from the fact that the output terminals of the three modules are connected in parallel such that the power conversion in each module is single-phase to three-phase and its power waveform is pulsating. Hence, the peak power that each module handles is 2/3 of the power of each power cell. This significantly reduces the current stress on the devices in each module.

Fig. 14 depicts the link capacitors voltages and currents of modules $A1$ and $A2$ to verify the identical operation of these two modules that are connected in series at the input side and in parallel at the output side. The three identical modes of operation in modules $A1$ and $A2$ are clear in Fig. 14. In Fig. 14, the waveforms are shifted up and down to clearly show the waveforms of each module. The link voltage and current of module $A1$ are shown in blue and black, respectively; and the link voltage and current of module $A2$ are shown in red and gray, respectively.

The unfiltered voltages across the input converter-side terminals of modules $A1$, $B1$, and $C1$ are depicted in Fig. 15(a).

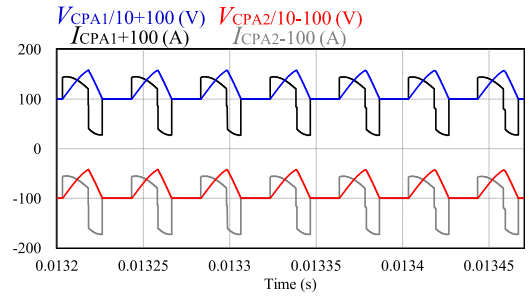

Fig. 14. Link capacitors voltages and currents of modules $A1$ and $A2$.

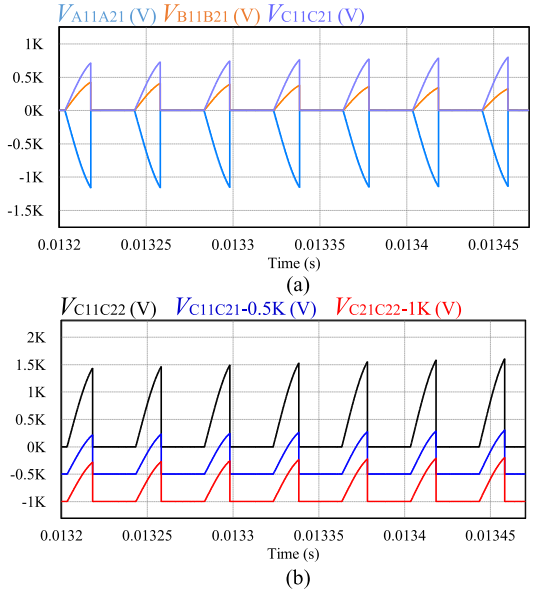

Fig. 15. (a) Unfiltered input converter-side terminals voltages of modules $A1$, $B1$, and $C1$. (b) Unfiltered input converter-side terminals voltages of modules $C1$ (blue) and $C2$ (red) and the total unfiltered line-neutral voltage at the input terminals (black).

Fig. 15(b) shows the unfiltered voltages across the input converter-side terminals of module $C1$ and $C2$, V_{C11C21} and V_{C21C22} (shifted down to clearly show the waveform), along with the total unfiltered voltage of phase C, V_{C11C22}. The total unfiltered line-neutral voltages of the input terminals of each module is equal to the summation of unfiltered input converter-side voltages of the modules 1, 2, …, n; this verifies the series connection of the terminals at the input side, which further reduces the voltage stress on the devices. For example, in Fig. 15(b), red waveform plus blue waveform would form the black waveform. Fig. 16(a) demonstrates the output side unfiltered line–line voltages of module $A1$. Moreover, Fig. 16(b) depicts the unfiltered voltages across terminals A_oX1–B_oX1 and A_oX2–B_oX2 ($X \in \{A, B, C\}$). This verifies that the output terminals of two parallel-connected modules in a power cell have the same unfiltered line–line voltage.

Figs. 17 and 18 verify the transient behavior of the converter. The control algorithm of the proposed converter can properly respond to load transients. When the load demand at the output side suddenly increases, the current references for the input side increase as well. The increase in the input and output current

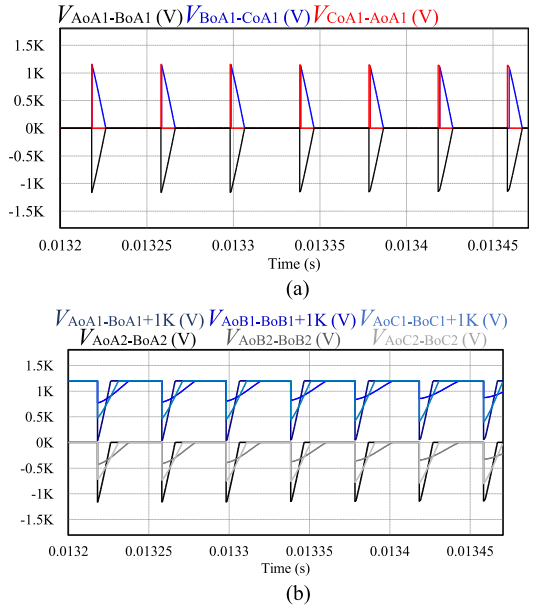

Fig. 16. (a) Output side unfiltered line-line voltages of modules $A1$. (b) Unfiltered voltages across terminals A_oX1–B_oX1 and A_oX2–B_oX2 ($X \in \{A, B, C\}$) in modules $A1$, $B1$, $C1$, $A2$, $B2$, and $C2$.

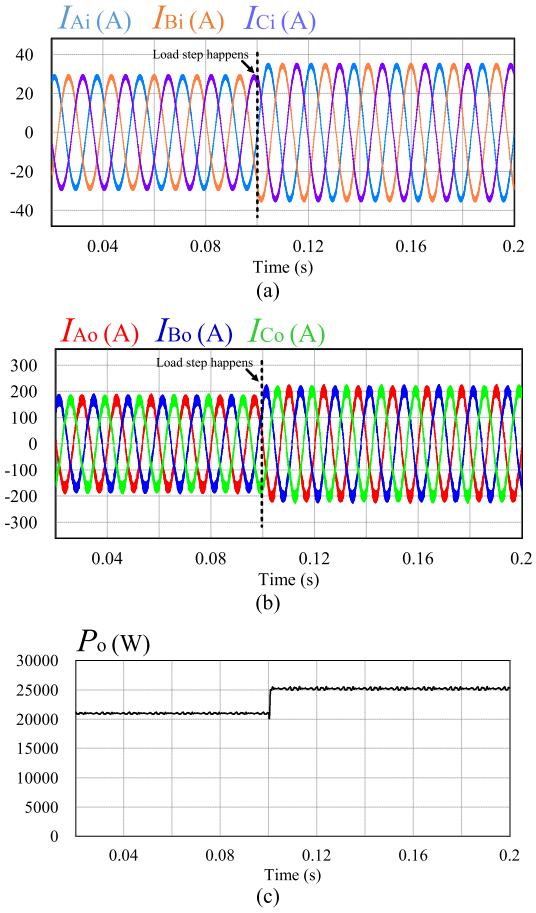

Fig. 17. Simulation results when the load changes from 80% of the rated power to 100% of the rated power. (a) Three-phase input currents. (b) Three-phase output currents. (c) Output power waveform.

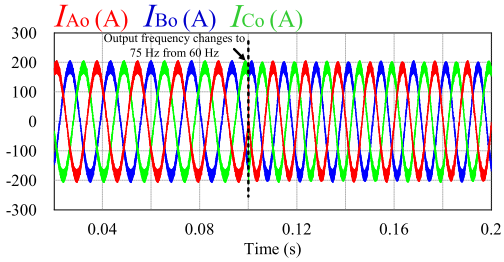

Fig. 18. Output current waveforms when the frequency changes from 60 to 75 Hz at $t = 0.1$ s.

references results in a change in the duration of operation modes such that the input inductors' currents increase (dtin (52) needs to increase, considering V_{xi} is constant). Duration of operation modes needs to change according to the amount of change in power during the transient response such that extra the energy stored in the link capacitors can transfer the right amount of power (energy over time) to the output to meet the demand. For instance, according to (10), V_{P1A} will increase in response to this event, to hold the equation, considering V_{CM1A} is constant and t_{1A} has dropped. t_{1A} has dropped in response to increased P_{CM1A}, according to (39).

Fig. 17 shows the three-phase input and output currents of the converter when a load transient happens. At $t = 0.1$ s, load changes from 80% of the rated power to 100% of the rated power. As can be observed, the implemented control is capable of responding to the load change. The frequency for the input and output currents is 60 and 75 Hz, respectively, during this test. Fig. 17(c) shows the output power waveform of the power converter that is obtained from the three-phase Watt meter with 1.5 kHz cut-off frequency in PSIM simulation. It is clear that the output power of the converter has increased in response to the load demand change.

Fig. 18 depicts the simulation results of the output current waveforms in response to a change in output frequency (industrial motor drive application). At $t = 0.1$ s, the desired frequency for the output current changes from 60 to 75 Hz, and as seen in Fig. 18, the control algorithm can smoothly change the frequency. This test verifies the frequency transformation capability of the proposed converter.

VI. Experimental Verification

A 1.6-kW prototype with two power cells ($n = 2$) is fabricated to verify the operation of the proposed modular power converter in a three-phase ac–ac conversion system, as shown in Fig. 19. The programmable FPGA part of a Zync-7000 All Programmable SoC core has been used to implement the digital control of the hardware setup. The converter specifications and component values are listed in Table III. The link frequency for the experimental tests is 25 kHz with the equivalent link capacitance of 0.07 μF in each module. The very small value of the link capacitances significantly improves the mean time between failures and consequently enhances the reliability of the proposed converter.

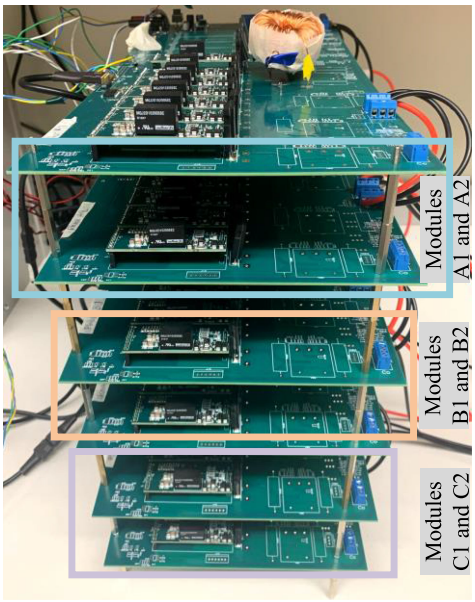

Fig. 19. Fabricated modular converter with two power cells.

TABLE III
SPECIFICATIONS OF THE INVESTIGATED SYSTEM (EXPERIMENTAL VERIFICATION)

Parameters		Value
Nominal Power (P_T)		1.6 [kW]
Link Frequency (f)		25 [kHz]
Equivalent Link Capacitance (C_{eq}) in each phase		0.07 [μF]
Input Line-Line Voltage (V_i)		260 [V]
Output Line-Line Voltage (V_o)		130 [V]
Input LCL Filter	L_G (grid side)	4 [mH]
	L_C (converter side)	0.7 [mH]
	C (star connection)	0.25 [μF]
Output L Filter		1 [mH]
Input Switches (S_{inx}, X ∈ {A, B, C}c)		C2M0040120D
Output Switches (S_{kxm}, X ∈ {A, B, C}, k ∈ {1-6}, m ∈ {1,2})		C2M0040120D
Diodes		C5D10170H

A. Transformer Implementation

In this part, the principles of transformer design for the implemented hardware prototype (specifications are listed in Table III) are discussed, which are adopted from the selected magnetic core manufacturer's design guidelines [43]. The product of window area (W_a) and effective core cross-sectional area (A_c) can be determined based on the frequency and the power that is handled by the transformer:

$$WaAc = \frac{P_o D_{cma}}{K_t B_{\max} f} \tag{61}$$

where P_o is the power handled by the transformer, D_{cma} is current density, $B_{\max}$ is the flux density, and K_t is a constant, which can be obtained from [43]. According to [43], K_t is considered 0. 0014 and D_{cma} is considered 750 cir.Mil/amp. Considering

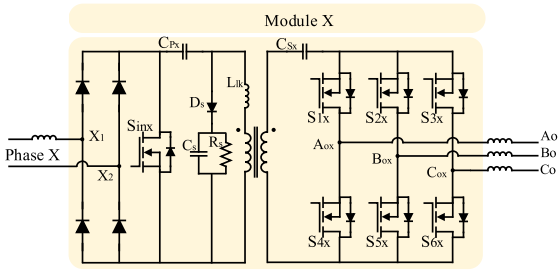

Fig. 20. Module X with RCD snubber.

link frequency of 25 kHz, $W_a A_c$ can be obtained as 4.75 cm^2. A Kool Mu Toroid core is selected from the manufacturer website [43]. The number of required primary turns can be calculated as follows:

$$N_1 = \frac{\Delta\varphi_m}{2 \times A_c \times B_{\max}} \tag{62}$$

where N_1 is the number of primary turns, A_c is effective cross-sectional area of the selected core, and $\Delta\varphi_m$ can be estimated from the simulation. The number of primary and secondary turns is equal to 71 turns such that 1:1 turn ratio is achieved.

B. Leakage Inductance Effect

In module X, when mode 1X begins, the link current that passes through the transformer has a sharp change from 0 to $|I_{Xi}|$. The leakage inductance of the transformer will cause a voltage spike due to this instantaneous change of current. Depending on how fast this change happens, the peak value of voltage spike across the leakage inductance can be determined as follows:

$$v_{\mathrm{lk},X} = L_{lk} \frac{\Delta i_{\mathrm{link}X}}{\Delta t} \tag{63}$$

where $v_{\mathrm{lk},X}$ is the voltage across the leakage inductance,$i_{\mathrm{link}X}$ is the link current, and Δt is the time that takes for the link current to jump to $|I_{Xi}|$. To suppress the unwanted voltage spike, a resistor-capacitor-diode (RCD) passive clamping circuit is designed and utilized in the hardware prototype to slow down the sharp changes in the current that passes through the leakage inductance [44], [45]. The RCD circuit in module X is shown in Fig. 20, and is designed according to [44], [45]. As soon as there is a sharp change in the link current (for example, when mode 1X begins), diode D_s becomes forward biased and C_s acts as a short circuit, which prevents the leakage inductance from experiencing a sharp change. The clamping circuit absorbs the current by turning on the clamping diode (D_s). Afterwards, the leakage inductance current starts increasing, and the rate of increase depends on the value of $R_s C_s$. This behavior is shown in Fig. 21. The clamping circuit is effectively increasing the rise time of the transformer current by introducing additional resistive losses. The design procedure of the RCD clamping circuit is thoroughly discussed in [44], [45].

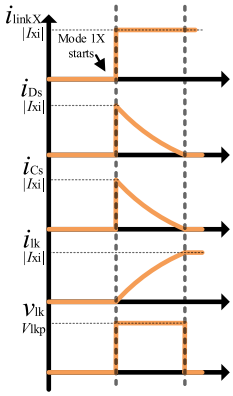

Fig. 21. Operating waveforms of RCD clamping circuit.

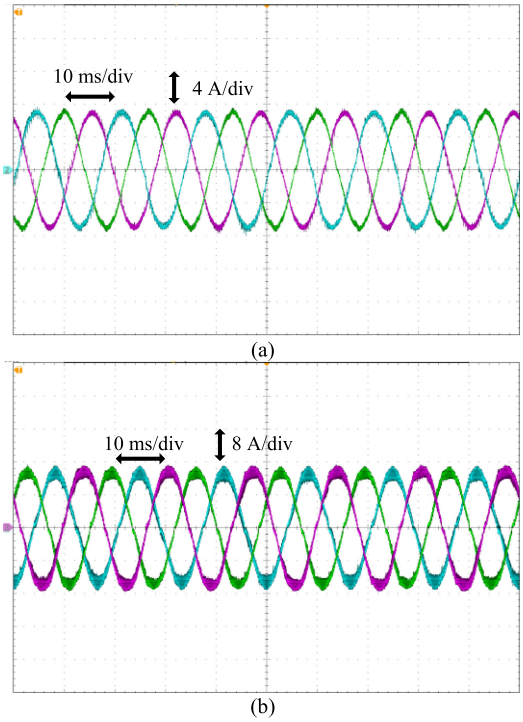

Fig. 22. (a) Three-phase input currents. (b) Three-phase output currents.

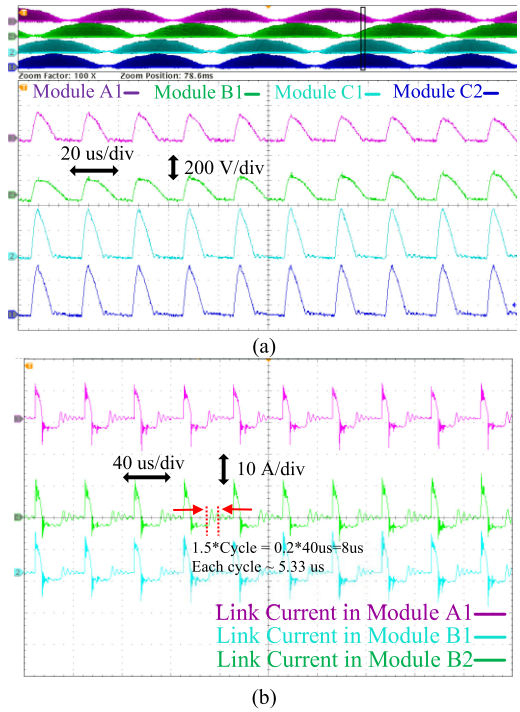

Fig. 23. (a) Link capacitors voltages in modules $A1$, $B1$, $C1$, and $C2$. (b) Link currents in modules $A1$, $B1$, and $B2$.

C. Experimental Results

Fig. 22 (a) and (b) shows the sinusoidal three-phase input and output currents. The output currents amplitude is almost twice the input current, which validates the presence of a high-current load at the output side. This justifies the parallel connection of the power cells at the output side for current sharing purpose.

The link capacitors voltages of modules $A1$, $B1$, $C1$, and $C2$ are depicted in Fig. 23(a). From the peak values of the link capacitors voltages, one can verify that at the given moment, the input phase C is carrying the largest current (absolute value) and the input phases A and B currents are almost equal. Also, it should be noted that phase B current is increasing, and phase A current is decreasing. The link capacitor voltages of modules $C1$ and $C2$ verify the identical behavior of the modules that are connected in series to the same input phase (in this figure, modules of phase C). Evidently, the link cycles of the modules start and end synchronously, similar to Fig. 13(a) of simulation results.

Fig. 23(b) depicts the link currents in modules $A1$, $B1$, and $B2$. The identical behavior of the modules corresponding to the same input phase (in this example, modules $B1$ and $B2$) can be observed in this figure as well. The maximum current that passes through the link capacitors of each module is equal to 1/3 of the maximum output current, since the currents are shared among the modules of two power cells ($n = 2$). Hence, the maximum discharging link current in each module is 4.8 A, while the maximum output current is measured to be 14.4 A. This reasoning is discussed in the simulation results section.

The ringing in the link current during the zero-operation mode is due to the resonance of an LC circuit formed by the link capacitance (forming the term C in LC resonance) and the leakage inductance of the transformer (forming the term L in LC resonance). According to Fig. 23(b), the period for these resonances is approximately 5.33 μs. The resonance period is theoretically equal to $2\pi\sqrt{L_{\rm lk}C_{\rm eq}}$, which is calculated as 5.25 μs in this system, considering that the link capacitance is 0. 07 μF and the leakage inductance is 10 μH. The ringing of the link current at the beginning of the charging mode as well as the beginning of the first discharging mode is because of the resonance of an LC circuit formed by the leakage inductance (forming the term L in LC resonance) and the parasitic capacitor of semiconductor devices and stray capacitance of the transformer (forming the term C in LC resonance).

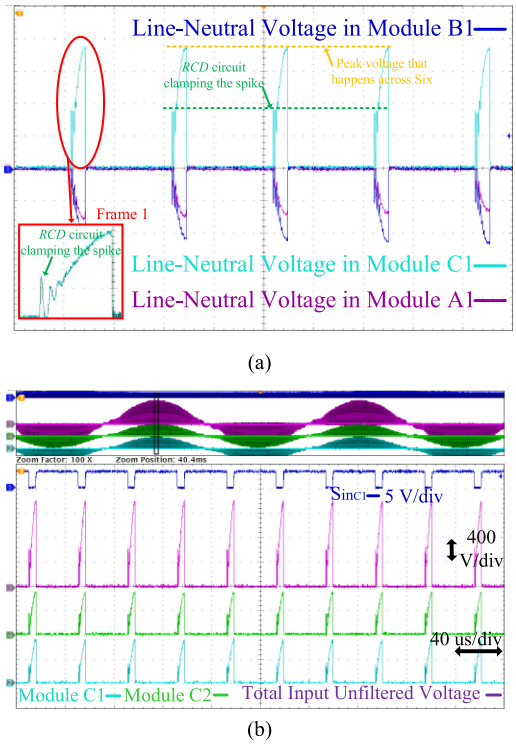

Fig. 24. (a) Unfiltered input converter-side terminals voltages of modules $A1$, $B1$, and $C1$. (b) Unfiltered input converter-side terminals voltages of modules $C1$ and $C2$ along with the total unfiltered line-neutral voltage of input phase C. S_{inC1} gate command (blue waveform) shows the charging mode when it is low and discharging mode when it is high.

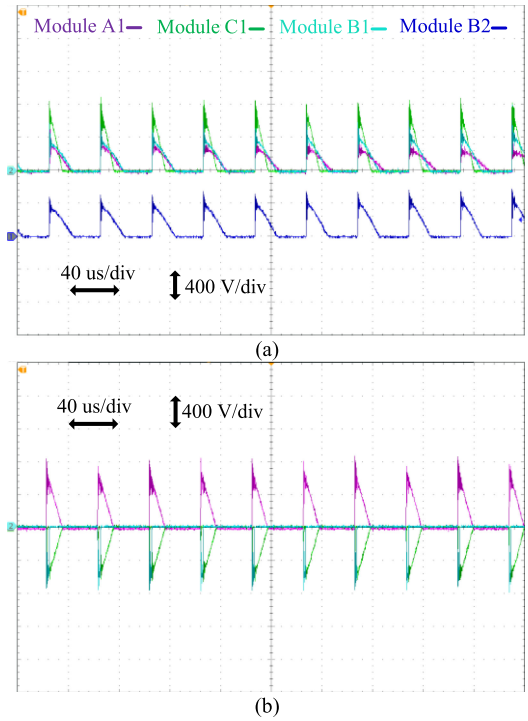

Fig. 25. (a) Unfiltered voltages across terminals A_oA1–B_oA1, A_oB1–B_oB1, A_oC1–B_oC1, and A_oB2–B_oB2 in modules $A1$, $B1$, $B2$, and $C1$. (b) Unfiltered line–line voltages in module $C1$.

Fig. 24(a) depicts the unfiltered voltages across the input converter-side terminals of the modules $A1$, $B1$, and $C1$. Red Frame 1 in Fig. 24(a) depicts the zoomed-in waveform of unfiltered line-neutral voltage at the input of module $C1$. The voltage spike at the beginning of this zoomed-in waveform is due to the leakage inductance of the transformer and the RCD clamping circuit, as discussed in part B of this section. The voltage clamping is achieved by employing the RCD clamping circuit. The voltage level to which the voltage spike is clamped is shown with dashed green line. The peak of this voltage spike is much lower than the peak of the link capacitor voltage.

Fig. 24(b) shows the unfiltered voltages across input converter-side terminals voltages of the module $C1$ and $C2$ along with the total unfiltered line-neutral voltage of input phase C. The blue waveform of Fig. 24(b) depicts S_{inC1} gate command; it is low (high) when the module is operating in the charging (discharging) mode. Evidently, summation of the unfiltered terminal voltages of modules $C1$ and $C2$, which are identical themselves, form the total unfiltered line-neutral voltage for the input phase C. This verifies the series connection of the input terminals. The same concept is true for the other two phases as well. This behavior is discussed in Fig. 15(b) of the simulation results section.

Fig. 25(a) illustrates the unfiltered voltages across terminals A_oA1–B_oA1, A_oB1–B_oB1, A_oC1–B_oC1, and A_oB2–B_oB2 in modules $A1$, $B1$, $B2$, and $C1$. Clearly, the unfiltered voltages across these terminals have identical behavior in modules $B1$ and $B2$. Furthermore, Fig. 25(b) shows the unfiltered line–line voltages of module $C1$ during a few switching cycles. Given that the three terminals of modules $C1$ and $C2$ are connected in parallel (at the left side of the inductors), the unfiltered line–line voltages of module $C2$ should be identical to those of module $C1$. The same concept is discussed in Fig. 16 of simulation results, as well.

D. Efficiency and Loss Analysis

The efficiency curve of the converter at different operating points is given in Fig. 26(a), which is obtained by Yokogawa WT1800 power analyzer. The efficiceny of the converter is approaching 91% when the output power of the converter is close to 1.6 kW.

The total power losses that are calculated from the experimental data are depicted in Fig. 26(b) with black line. The major sources of power loss in the proposed modular converter include: 1) losses related to input switches (snubbers, conduction, and switching), 2) losses related to output switches (snubbers, conduction, and switching), 3) input diodes, 4) RCD clamping circuit, and 5) HFT copper and core losses. In order to break down losses, the accurate Level 2 model of the MOSFET along with real parameters of MOSFETs of Table III, diodes of Table III, HFT, and RCD circuit are used in simulation. All these sources of loss except the switching losses and HFT core losses can be modeled and measured in the simulation. HFT core losses can be calculated using the curve fit equation tool that is released by the

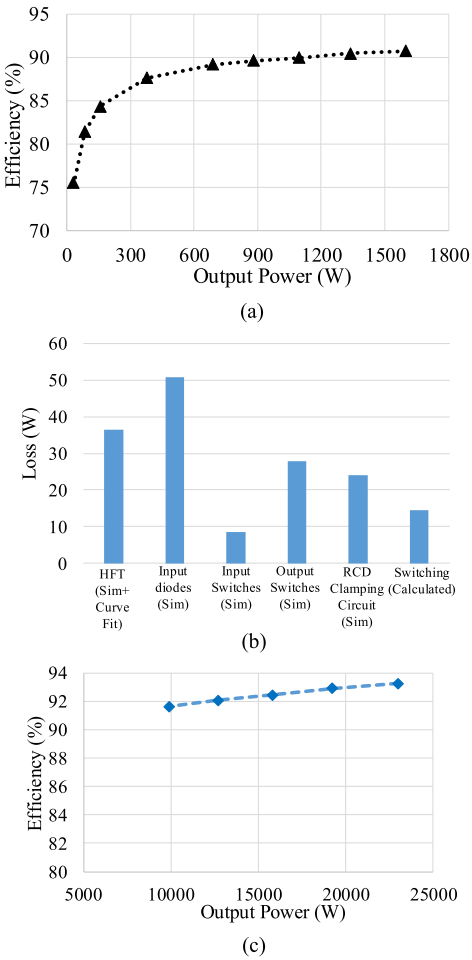

Fig. 26. (a) Efficiency curve of the 1.6 kW proposed modular converter. (b) Loss breakdown bar chart at 1.6 kW. (c) Efficiency curve of the 25 kW proposed modular converter (obtained from simulation).

manufacturing company of the magnetic core [45]. According to this tool, the core losses of the selected magentic core are 212 mW/cm^3 at full power. Given that the effective volume of the selected magnetic core is 21.3 cm^3, the total core losses for each transformer is 4.5 W at full power. The switching losses can be estimated as the difference between the actual experimental data and the losses that are calculated through simulations and curve fit equation tool. It should be noted that other sources of loss such as gate driver loss, ESR of capacitors, and ohmic loss corresponding to power path resistances are negligible, and are not considered in this analysis. Fig. 26(b) shows the bar chart of loss breakdown at 1.6 kW power.

Now that it is confirmed that the simulation model and curve fit equations can accurately estimate the power losses of the proposed converter, the same procedure is carried out to estimate the efficiency and losses associated with the full-scale 25 kW modular converter that was simulated in Section V. The estimated efficiency of the 25 kW converter at different power levels is shown in Fig. 26(c).

The efficiency of the proposed modular converter could be improved by using SiC MOSFETs with lower $R_{ds\ \mathrm{ON}}$ or using an SiC MOSFET with reverse conduction instead of input diodes (synchronous rectification), as shown in the bidirectional topology in Fig. 1(b). Also, in the bidirectional topology, the input side individual MOSFET (S_{inx}) is removed. According to Fig. 26(b), the input diode bridge conduction losses and input side MOSFET conduction losses are 50.88 and 8.56 W (at peak power), which in total stand for 40% of total losses. Using SiC MOSFETs in the bidirectional topology can significantly decrease the conduction losses. According to simulation, total conduction losses attributed to these components can be decreased to 30.76 W. Furthermore, using advanced clamping techniques for mitigation of leakage inductance to decrease the losses attributed to the snubber circuit can further improve the efficiency.

VII. Competitive Analysis

A. Reliability

High reliability is among the most important requirements of power electronics systems. Higher failure rates in power converters increase the maintenance cost and negatively affect the investment in power electronics systems. Among different components of a power converter, semiconductor switches and capacitors are the most vulnerable parts that can significantly affect the failure rates of entire power electronics system [46]. Specifically, electrolytic capacitors have the highest failure rates. A major advantage of the proposed modular converter is that it utilizes film capacitors with very small capacitances to perform the power conversion. This is a promising feature that improves the reliability of the proposed converter compared with the conventional electrolytic-capacitor-based power converters that require large capacitances. In a dc-link-based ac–ac converter, especially modular structures that are the topic of interest in this article, typically a large number of capacitors with large capacitances are required to maintain small voltage ripples across the dc-link and provide a decoupled control.

In this section, the total failure rate of the capacitors used in the proposed converter is estimated according to [47] (MIL-HDBK-217F). For the sake of comparison, the total failure rate of the capacitors in a back-to-back three-phase ac–ac MMC with two submodules in each leg incorporating 28 electrolytic capacitors with 510 μF capacitance, is also estimated here. The proposed modular converter of this article requires 12 film capacitors with 0.15 μF capacitance. The capacitance of the employed capacitors in the proposed modular converter is 3400 times smaller than that of the MMC. Fig. 27 demonstrates the total failure rates of the capacitors for 1.6 kW power rating; clearly, at ambient temperature of 50 °C, the total failure rate of electrolytic capacitors of MMC is 19 times the total failure rate of the film capacitors of the proposed modular converter. This significant difference further highlights the benefits of employing film capacitors with very small capacitances in the proposed modular converter. There is not a significant difference between the failure rates of switches in the proposed converter and MMC; therefore, the overall reliability comparison is mostly affected by the failure rates of the capacitors.

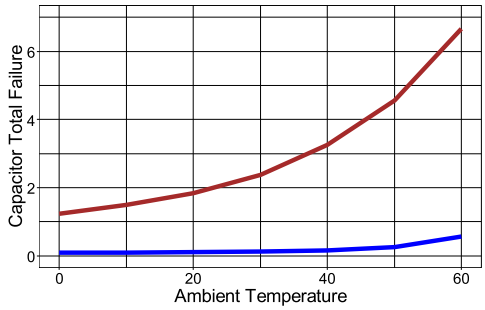

Fig. 27. Total failure rate of the electrolytic capacitors for MMCs (brown) and film capacitors for the proposed converter (blue) for the 1.6 kW power rating.

B. Volume and Weight

In this part, the volume and weight of the MMC that is introduced in reliability part is compared with those of the proposed modular converter. There is a huge difference between the volume/weight of the capacitors that are used in the conventional dc-link-based power converters, such as MMC, and the proposed modular converter. The MMC with two submodules in each leg incorporates total of 48 MOSFETs (two MOSFETs per submodule) and requires 28 electrolytic capacitors with 510 μF capacitance. The proposed modular converter of this article requires 12 film capacitors with 0.15 μF capacitance with 42 MOSFETs and 24 diodes. The weight and volume of these electrolytic capacitors in the MMC would be 2476 g and 1791 cm^3, which are 41.2 and 25 times larger than those of the proposed modular converter. The capacitors of the MMC are considered electrolytic type and those of the proposed modular converter are considered film.

The total weight and volume of the transformers and link capacitors of the proposed modular converter are 1200 g and 262.7 cm^3, which is still lower than the weight/volume of only the dc-link capacitors of MMC. The volume and weight of an isolated MMC (provided by low-frequency transformers), including transformer and dc-link capacitors, could reach 16 295 g and 3941.3 cm^3.

VIII. Conclusion

The modular and scalable structures of single-stage universal power converters for ac–ac conversion systems have not been thoroughly investigated. The existing universal power converter topologies cannot realize series connection of three-phase terminals for voltage sharing purposes, and they cannot offer a stackable and modular configuration. This article introduced a modular three-phase ac–ac power cell topology that is formed by three stackable capacitive-link modules. Using stackable modules to form the power cells enables scalable and modular design of the proposed converter. The proposed topology can realize both series and parallel connection of three-phase terminals in an ac–ac conversion system. Each module operates in DCVM and uses film capacitors with very small capacitances for transferring the power. This feature enhances the reliability and power density of the proposed power cell, compared with dc-link-based converters that typically employ bulky electrolytic capacitors with large capacitances. Furthermore, each module uses HFTs for isolation. It can accomplish voltage step-up or step-down as well as frequency transformation with arbitrary power factors, which are essential in industrial electric drives and shipboard power systems. An ISOP modular ac–ac configuration is proposed and investigated in this article, in which the input terminals of the power cells are placed in series to share the voltage among the power cells and the output terminals are placed in parallel to share the current among the power cells. The principles of the operation of the proposed modular converter along with design and control implementation considerations are described in detail in this article. The simulation results for a 25-kW three-phase ac–ac ISOP conversion system verify that the converter can accomplish the voltage and current sharing by stacking multiple power cells. Furthermore, experimental results of the scale-down 1.6-kW ac–ac hardware setup with two power cells in ISOP configuration demonstrate the operation of the proposed modular converter and validate its scalability feature.

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