An Improved ZVS High Step-Up Converter Based On Coupled Inductor and Built-In Transformer

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***Abstract*—A high step-up dc–dc converter with multiple magnetic devices and switched-capacitor voltage multiplier cell (SC VMC) is proposed in this article. By simultaneous implementation of a coupled inductor (CI) and a built-in transformer (BIT), the voltage gain is flexibly increased with an additional degree of freedom in comparison with the converters with only BIT or CI. To further increase the voltage gain, the secondary winding of the CI is inserted in series with the primary winding of the BIT. This new architecture leads to multiplication of the turns ratios of the CI and BIT in the voltage gain expression, as well. The SC VMC not only extends the voltage gain but also reduces the voltage stress across the MOSFETs. To have a better device utilization, the blocking capacitor is participated in voltage gain improvement. Moreover, through active clamp circuit, the leakage energy of the magnetic devices is recycled and zero voltage switching (ZVS) performance is obtained for the main and auxiliary MOSFETs. In such a case, the switching frequency can be increased to reduce the volume of the converter. Finally, a 400-W laboratory prototype with 25–400 V voltage conversion is fabricated to demonstrate the effectiveness of the proposed converter.**

***Index Terms*—Built-in transformer (BIT), coupled inductor (CI), high step-up, zero voltage switching (ZVS).**

I. Introduction

RENEWABLE energy sources, such as photovoltaic (PV) and fuel cell (FC), are attaining more attentions to deal with the problems of global warming, air pollution, shortage of fossil fuels, and increasing demand for electricity. Typically, the output voltage of PV and FC is lower than 50 V, which calls for high step-up dc–dc converters to provide 380–400 V voltage for the dc link of the front-end inverter [1]. The conventional boost converter can enhance the low input voltage to high output voltage with a simple and cheap structure. However, for getting high voltage gains, the duty cycle should be extremely high increasing the conduction losses and decreasing the converter control criteria. In addition, the MOSFET and diode are suffering from high voltage stress and hard switching. Therefore, semiconductors with higher ON-state resistance and high cost should be implemented. Consequently, due to increased losses at higher voltage gains, the conversion efficiency is decreased which limits its application, seriously [2]. Quadratic boost converters and Z-source converters can achieve high voltage gains with lower duty cycles in which the voltage stress across the implemented MOSFET is lower than the output voltage [3]–[5]. However, the imposed voltage across the MOSFET is still high and the conversion efficiency is at risk due to the implementation of the diodes at the low voltage (high current) side.

Voltage multiplier cells (VMCs) based on switched-capacitors (SCs) and switched inductors (SL) are simple and a low-cost alternative for extending voltage in the converters known as transformerless converters [6]–[11]. The SC (SL) units consist of two capacitors (inductors) and can be utilized as series modules to get a flexible voltage gain. However, the voltage and current specifications of the modules closer to the output are high, which makes the converter design more complex [6]–[8], [11]. This issue is solved by Cockcroft–Walton VMCs in [9], [10], making it possible to utilize modules with equal ratings. Altogether, the main drawbacks of the SC-based converters are low conversion efficiency and the pulsating current through the semiconductors at the instant of switching due to the presence of the capacitors.

As a promising solution for the problems of the aforementioned converters, coupled inductors (CIs) [12]–[24] have been utilized in too many step-up converters in recent researches where the input discrete inductor is usually replaced by the primary winding of the CI [14]–[24]. The turns ratio of CI participates in voltage gain extension along with the duty cycle. Increasing the turns ratio not only extends the voltage gain, but also decreases the voltage stress across the MOSFET. The leakage inductance provides zero current switching (ZCS) for the semiconductors alleviating the possible pulsating currents at the instant of switching and the high-frequency ringing phenomenon of the diodes. Passive clamp circuits are implemented to recycle the leakage energy, which avoids efficiency deration. The quadratic converters can achieve high voltage gains with the implementation of CIs [14]–[15]. However, as mentioned earlier, the conductions losses of the high current side diodes still exist. To further extend the voltage gain, the secondary windings of the CI are inserted within the VMC [16]–[24]. For example, in the introduced converter of [16], the VMC consists of two diodes, two capacitors, and the secondary winding of the CI with its output inserted in a stacked manner. Moreover, by implementing

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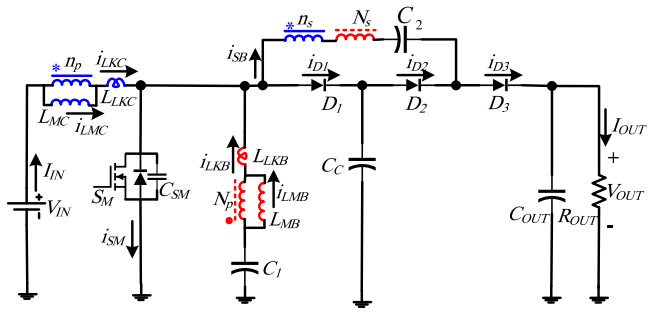


Fig. 1. High step-up converter in [33].

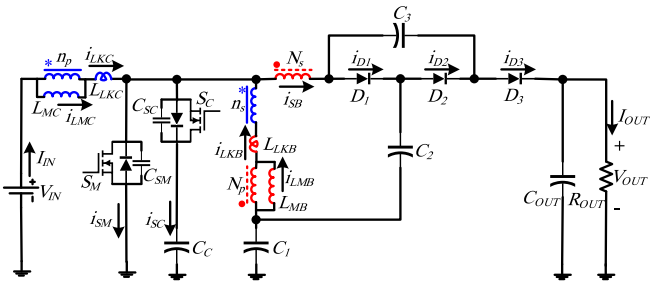


Fig. 2. Proposed high step-up converter.

a generalized structure of the proposed VMC, this converter can achieve an ultralarge voltage gain. Although the stacked output converters can achieve high voltage gain, balancing of the voltages of the output capacitors should be taken into account for dynamical performance which increases the control complexity. Implementaion of more diodes and capacitors in the VMC [17], three winding CI and voltage doubler [18], and two or more number of VMCs [19]–[23] has been also proposed to extend the voltage gain of the CI-assisted step-up dc–dc converters.

The utilization of a built-in transformer (BIT) with the VMC is another way to improve the voltage gain [24]–[26]. Due to zero average current of the primary windings of the BIT, the flux is balanced, which avoids the core saturation inherently. Therefore, low volume core can be selected to fabricate the BIT in comparison with the CI. Moreover, the rms current that flows through the primary winding of the BIT is lower than that for the CI reducing its windings' conduction losses.

Generally, to improve the power density and to reduce the size of the components, the switching frequency should be pushed to high values. Although, in the converters of [3]–[26], ZCS turn-ON of the MOSFETs is provided by the leakage inductance; however, this cannot minimize the switching losses sufficiently. Therefore, the operation of the MOSFETs at high frequencies is limited due to the increased switching losses. Converters with active clamp circuits have been introduced to provide ZVS [27]–[32]. The active clamp circuit not only absorbs the leakage energy but also implements the leakage current to make the body diode of the main MOSFET turn ON before the gate pulse comes.

The converter in Fig. 1 shows the recent achievement in the research topic [33]. With the turns ratio of the CI and BIT, two extra control variable are provided to improve the voltage gain along with the increased flexibility for achieving high voltage gains. The VMC consists of the series-connected secondary windings of CI and BIT to extend the voltage gain. In such a case, the summation of the turns ratios appears in the voltage gain. Moreover, the leakage energy is recycled through a passive clamp circuit, which limits the converter operation at high switching frequencies due to lack of zero voltage switching (ZVS) performance. Meanwhile, the blocking capacitor is not participated in voltage gain enhancement. Therefore, the novelty of this article is to increase the voltage gain of the introduced converter in [33] by inserting the secondary winding of the CI in series with the primary winding of the BIT. This new concept gives rise to multiplication of the turns ratios of the CI and BIT in the voltage gain expression as well. Also, to further increase the voltage gain and to reduce the voltage stress of the MOSFETs, the blocking capacitor is also served for voltage gain improvement and the secondary winding of the BIT is connected outside of the VMC that clamps the output voltage considerably. The active clamp circuit is also connected across the main MOSFET to assure ZVS performance of the MOSFETs. Altogether, the proposed converter has the following advantages in comparison with the converter of [33] having just an additional active clamp circuit.

1) The voltage gain is considerably increased, which enables the proposed converter operation at low duty cycles.
2) By inserting the secondary winding of CI in series with the primary winding of BIT, the voltage gain is proportional to the multiplication of the turns ratios of the CI and BIT.
3) Blocking capacitor participates in voltage gain enhancement in contrary to the one introduced in [33].
4) The voltage stress across the MOSFETs is severely decreased, enabling the designer to implement switching devices with lower ON-state resistance.
5) The ZVS performance of the main and auxiliary MOSFETs is achieved in the whole switching cycle.
6) The voltage stress across the diodes is considerably decreased.
7) The total volt–ampere (VA) rating of the semiconductor devices is decreased in comparison with the proposed converter in [33].
8) The efficiency is increased at higher voltage gains and input currents due to the lower conduction and switching losses.

This article is organized as follows. In Section II, the operational principle of the proposed converter is presented. In Section III, the steady-state analysis of the proposed converter is given. In Section IV, the performance comparison of the proposed converter in the state of the art is discussed. A numerical design example of the components and the experimental verification of the proposed converter are given in Sections V and VI, respectively, which are followed by the conclusion in Section VII.

II. Proposed Converter and Operational Principle

The circuit configuration of the proposed topology is shown in Fig. 2. $V_{\rm IN}$ and $I_{\rm IN}$ represent the dc input voltage and the average value of the input current, respectively. $V_{\rm OUT}$ and $I_{\rm OUT}$ denote

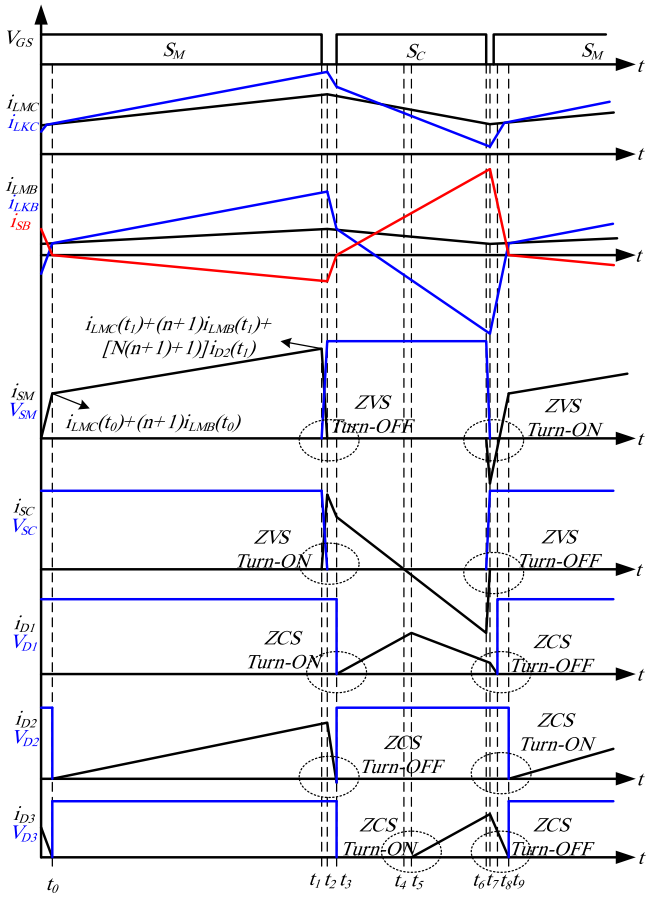


Fig. 3. Key waveforms of the proposed converter.

the output voltage and current, respectively. $L_{\rm MC}$ and $L_{\rm LKC}$ are the magnetizing inductance and the total primary referred leakage inductance of the CI, respectively. $L_{\rm MB}$ and $L_{\rm LKB}$ are the magnetizing inductance and the leakage inductance of the BIT, respectively. S_M and S_C notate the main and clamp MOSFETs, respectively. $C_{\rm SM}$ and $C_{\rm SC}$ are the parallel capacitors of S_M and S_C, respectively. C_1 is the blocking capacitor. Capacitors C_2 and C_3 along with diodes D_1 and D_2 form a VMC. C_C is the clamp capacitor and $C_{\rm OUT}$ notate the output capacitor. D_3 is the output diode and $R_{\rm OUT}$ represent the load resistance. The turns ratios of the CI and BIT are defined as $n = n_s/n_p$ and $N = N_s/N_p$, respectively.

To simplify the operational principle, the following assumptions are made.

1) All of the components are considered lossless, at this section.
2) The capacitors are large enough and the associated voltage ripples are negligible during a switching cycle.

Based on the aforementioned assumptions, the key waveforms of the proposed converter and its equivalent circuits are shown in Fig. 3 and 4, respectively.

Mode 1 [t_0–t_1]: During this mode, S_M is ON. $L_{\rm MC}$ and $L_{\rm MB}$ are charged by the positive voltages. A part of the stored energy in C_1 is charging C_3 through the secondary winding of BIT and D_2. At the same time, the capacitor C_1 is discharging. The current passing through S_M is the summation of the input current and currents through secondary windings of the CI and BIT, which is given by

$$i_{\rm LMC}(t) = \frac{V_{\rm IN}}{L_{\rm MC}}(t-t_0) + i_{\rm LMC}(t_0) \tag{1}$$

$$i_{\rm LMB}(t) = \frac{V_{C3}-V_{C1}-V_{C2}}{NL_{\rm MB}}(t-t_0) + i_{\rm LMB}(t_0) \tag{2}$$

$$i_{\rm LKB}(t) = \frac{nNV_{\rm IN}+(N+1)V_{C1}+V_{C2}-V_{C1}}{N(n^2L_{\rm LKC}+L_{\rm LKB})}(t-t_0) + i_{\rm LKB}(t_0) \tag{3}$$

$$i_{\rm LKC}(t) = i_{\rm LMC}(t) + ni_{\rm LKB}(t) \tag{4}$$

$$i_{D2}(t) = \frac{i_{\rm LKB}(t)-i_{\rm LMB}(t)}{N} \tag{5}$$

$$i_{\rm SM}(t) = i_{\rm LMC}(t) + (n+1)i_{\rm LMB}(t) + [N(n+1)+1]\,i_{D2}(t). \tag{6}$$

Mode 2 [t_1–t_2]: At t_1, S_M is turned OFF with ZVS performance. $i_{\rm SM}(t_1)$ starts to charge $C_{\rm SM}$ and discharge $C_{\rm SC}$ as well. $V_{\rm SM}$ is increasing from zero to $V_{\rm CC}$ and $V_{\rm SC}$ is decreasing from $V_{\rm CC}$ to zero

$$\Delta t_2 = t_2 - t_1 = \frac{(C_{\rm SM}+C_{\rm SC})V_{\rm CC}}{i_{\rm LMC}(t_1)+(n+1)i_{\rm LMB}(t_1)+[N(n+1)+1]\,i_{D2}(t_1)}. \tag{7}$$

Mode 3 [t_2–t_3] At t_2, $V_{\rm SC}$ is zero that makes its antiparallel diode conduct. Negative voltages are applied across $L_{\rm MC}$ and $L_{\rm MB}$ as well as $L_{\rm LKC}$ and $L_{\rm LKB}$. Therefore, their currents start decreasing. By decreasing $i_{\rm LMB}$ and $i_{\rm LKB}$, the current of $i_{\rm SB}$ approaches to zero, which controls the falling rate of i_{D2}

$$\frac{di_{D2}(t)}{dt} = \frac{nNV_{\rm IN}-[N(n+1)+1]\,V_{\rm CC}+(N+1)V_{C1}+V_{C2}-V_{C3}}{N^2[n^2L_{\rm LKC}+L_{\rm LKB}]}. \tag{8}$$

Mode 4 [t_3–t_4]: At t_3, the gate pulse of S_C comes and turns it ON with ZVS performance due to the conduction of its antiparallel diode. At the beginning of this mode while $i_{\rm SB}$ wants to change its direction, D_2 turns OFF with ZCS performance and the possible reverse recovery problems are alleviated. At the same time, D_1 starts to conduct. It is worth to mention that due to charge balance of the capacitors, D_2 cannot start conducting until the half of the time interval in which S_C is in ON state. During this mode, the charging/discharging state of the CI and BIT are the same as the previous mode and C_C is charged through the antiparallel diode of S_C with the decreasing current of $i_{\rm LKC}(t)+i_{\rm LKB}(t)-i_{D1}(t)$. C_2 is charged through the secondary winding of BIT and D_1. From the beginning of this mode until the decreasing current of $i_{\rm LKB}$ reaches the increasing current of $i_{\rm SB}$, C_1 is charged and for the rest of this mode is

discharged as well

$$i_{\mathrm{LMC}}(t) = \frac{V_{\mathrm{IN}} - V_{\mathrm{CC}}}{L_{\mathrm{MC}}}(t - t_3) + i_{\mathrm{LMC}}(t_3) \tag{9}$$

$$i_{\mathrm{LMB}}(t) = \frac{V_{CC} - V_{C1} - V_{C2}}{NL_{\mathrm{MB}}}(t - t_3) + i_{\mathrm{LMB}}(t_3) \tag{10}$$

$$i_{\mathrm{LKB}}(t) = \frac{\left\{ \begin{array}{l} nNV_{\mathrm{IN}} - [N(n+1)+1]\,V_{\mathrm{CC}} \\ +(N+1)V_{C1} + V_{C2} \end{array} \right\}}{N(n^2 L_{\mathrm{LKC}} + L_{\mathrm{LKB}})}(t - t_3) + i_{\mathrm{LKB}}(t_3) \tag{11}$$

$$i_{\mathrm{LKC}}(t) = i_{\mathrm{LMC}}(t) + n i_{\mathrm{LKB}}(t) \tag{12}$$

$$i_{D1}(t) = \frac{i_{\mathrm{LMB}}(t) - i_{\mathrm{LKB}}(t)}{N} \tag{13}$$

$$i_{\mathrm{SC}}(t) = i_{\mathrm{LKC}}(t) + i_{\mathrm{LKB}}(t) - i_{D1}(t). \tag{14}$$

Mode 5 [t_4–t_5]: At t_4, the decreasing positive current of C_C reaches zero and changes its direction. Consequently, it transfers a part of its energy to C_1, and meanwhile, delivering the other part of the energy from primary winding *Np* to secondary winding *Ns* of BIT to charge capacitor C_2 through diode D_1. The states of the other variables are the same as in the previous mode.

Mode 6 [t_5–t_6]: At t_5, D_3 turns ON and C_3 diverts a portion of the BIT energy to the output. At the beginning of this mode, the current of D_1 start decreasing

$$i_{D1}(t) + i_{D3}(t) = \frac{i_{\mathrm{LMB}}(t) - i_{\mathrm{LKB}}(t)}{N} \tag{15}$$

$$i_{\mathrm{SC}}(t) = i_{\mathrm{LKC}}(t) + i_{\mathrm{LKB}}(t) - i_{D1}(t) - i_{D3}(t). \tag{16}$$

Mode 7 [t_6–t_7] At t_6, S_C is turned OFF with ZVS performance due to C_{SC}. $i_{\mathrm{SC}}(t_6)$ charges C_{SC} and discharge C_{SM} as well. V_{SC} is increasing from zero to V_{CC} and V_{SM} is decreasing from V_{CC} to zero

$$\Delta t_7 = t_7 - t_6 = \frac{(C_{\mathrm{SM}} + C_{\mathrm{SC}})V_{\mathrm{CC}}}{i_{\mathrm{LKC}}(t_6) + i_{\mathrm{LKB}}(t_6) - i_{D1}(t_6) - i_{D3}(t_6)}. \tag{17}$$

Mode 8 [t_7–t_8]: At t_7, V_{SM} reaches zero that makes its antiparallel diode conduct. During this mode, the gate pulse of SM comes and it is turned ON with ZVS performance. Positive voltages are applied across the primary windings of the primary windings of the CI and BIT. Therefore, i_{LMC} and i_{LKC} as well as i_{LMB} and i_{LKB} are increasing. In this case, i_{SB} is decreased through the transformer effect, which controls the falling current rates of D_1 and D_3

$$\frac{di_{D1}(t)}{dt} = \frac{V_{\mathrm{OUT}} - (V_{C1} + V_{C2} + V_{C3})}{N^2[n^2 L_{\mathrm{LKC}} + L_{\mathrm{LKB}}]}. \tag{18}$$

Mode 9 [t_8–t_9]: At t_8, i_{D1} reaches zero and turns OFF with ZCS performance. i_{SB} continuous decreasing through D_3 and at t_9 while is changing its direction, D_3 turns OFF with ZCS. At the end of this mode, a switching cycle is completed

$$\frac{di_{D3}(t)}{dt} = \frac{V_{C3} - N(V_{C1} + nV_{\mathrm{IN}}) - V_{\mathrm{OUT}}}{N^2[n^2 L_{\mathrm{LKC}} + L_{\mathrm{LKB}}]}. \tag{19}$$

III. Steady-State Analysis

A. Voltage Gain

To simplify the analysis, the switching transitional intervals are neglected due to the fact that they are very short in comparison with the power delivery modes. Due to the charge balance law of the capacitors, the average current of the diodes is equal to I_{OUT} as well as the average value of i_{SB}. This hint is utilized for obtaining $I_{D3,\max}$ and $\Delta t_{(7-5)}$ that are needed for further analysis of voltage gain. According to Fig. 3, the following expressions can be written:

$$I_{D2,\mathrm{ave}} = I_{\mathrm{OUT}} = \frac{DI_{D2,\max}}{2} \Rightarrow I_{D2,\max} = I_{\mathrm{SB}}(t_1) = \frac{2I_{\mathrm{OUT}}}{D} \tag{20}$$

$$I_{\mathrm{SB,ave}} = I_{\mathrm{OUT}} = -\frac{DI_{\mathrm{SB}}(t_1)}{2} + \frac{(1-D)}{2} I_{\mathrm{SB}}(t_7) \Rightarrow I_{\mathrm{SB}}(t_7) = \frac{4I_{\mathrm{OUT}}}{1-D} \approx I_{D3,\max} \tag{21}$$

$$I_{D3,\mathrm{ave}} = I_{\mathrm{OUT}} = \frac{\Delta t_{(7-5)} I_{D3,\max}}{2T_S} \Rightarrow \Delta t_{(7-5)} = \frac{(1-D)T_S}{2}. \tag{22}$$

By applying the volt–second balance principle to L_{MC}, V_{CC} is obtained as follows:

$$V_{\mathrm{CC}} = \frac{V_{\mathrm{IN}}}{1-D}. \tag{23}$$

Additionally, according to the KVL, the following relationship can be written:

$$-V_{\mathrm{IN}} + (1+n)V_{\mathrm{LMC,ave}} + V_{\mathrm{LKC,ave}} - V_{\mathrm{LKB,ave}} - V_{\mathrm{LMB,ave}} + V_{C1} = 0 \tag{24}$$

where $V_{\mathrm{LMC,ave}}$, $V_{\mathrm{LKC,ave}}$, $V_{\mathrm{LKB,ave}}$, and $V_{\mathrm{LM,ave}}$ are the average voltages of the inductances in one switching cycle and according to the volt–second law, they are equal to zero. Therefore

$$V_{C1} = V_{\mathrm{IN}}. \tag{25}$$

According the waveforms of i_{D2} and i_{D3} and keeping in mind the equivalent circuits of Fig. 4(a) and (f), the following equations are derived:

$$\frac{1}{2} DT_S \times \frac{[N(n+1)+1]V_{\mathrm{IN}} + V_{C2} - V_{C3}}{N^2(n^2 L_{\mathrm{LKC}} + L_{\mathrm{LKB}})T_S} DT_S = I_{\mathrm{OUT}} \tag{26}$$

$$\frac{1}{2} \times \Delta t_{(7-5)} \times \frac{[N(n+1)+1](V_{\mathrm{CC}} - V_{\mathrm{IN}}) - V_{C2}}{N^2(n^2 L_{\mathrm{LKC}} + L_{\mathrm{LKB}})T_S}(1-D)T_S = I_{\mathrm{OUT}} \tag{27}$$

$$V_{C1} + V_{C2} + V_{C3} = V_{\mathrm{OUT}}. \tag{28}$$

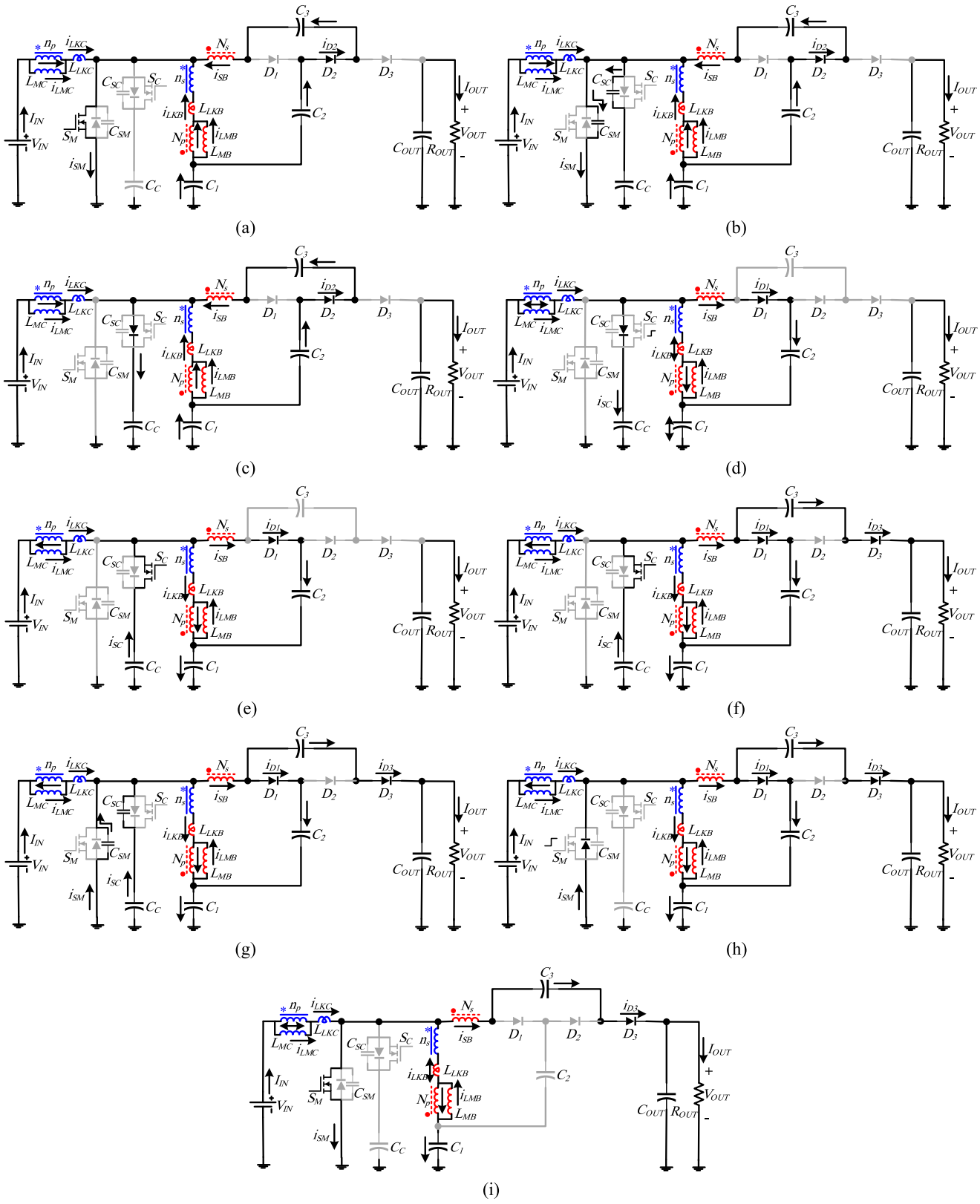


Fig. 4. Equivalent circuits of the proposed converter. (a) Mode 1. (b) Mode 2. (c)Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8. (i) Mode 9.

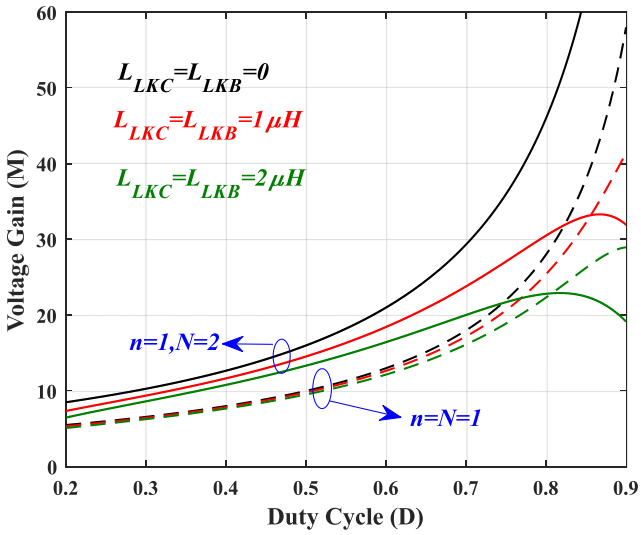


Fig. 5. Voltage gain of the proposed converter versus duty cycle (assuming $f_S = 100\,\text{kHz}$ and $R_{\text{OUT}} = 320\,\Omega$).

From (22), (23), and (25)–(28), the voltage gain of the proposed converter considering the leakage inductance is obtained as

$$M = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{N(n+1)(1+D)+2}{1-D} \times \frac{1}{1+\frac{2Q}{D^2}+\frac{8Q}{(1-D)^2}} \tag{29}$$

where $Q = N^2(n^2 L_{\text{LKC}} + L_{\text{LKB}}) f_S / R_{\text{OUT}}$. Fig. 5 shows the voltage gain of the proposed converter versus duty cycle. It is seen that the voltage gain is affected by the various values of the leakage inductances and turns ratios. By assuming the leakage inductance to be zero, the ideal voltage gain of the converter along with V_{C2} and V_{C3} are obtained as follows:

$$M = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{N(n+1)(1+D)+2}{1-D} \tag{30}$$

$$V_{C2} = DV_{C3} = \frac{[N(n+1)+1]}{1-D} V_{\text{IN}} = \frac{[N(n+1)+1]}{N(n+1)(1+D)+2} V_{\text{OUT}}. \tag{31}$$

B. Voltage and Current Stress Analysis

The voltage stresses of the semiconductors are obtained as

$$V_{\text{SM}} = V_{\text{SC}} = V_{\text{CC}} = \frac{V_{\text{IN}}}{1-D} = \frac{V_{\text{OUT}}}{N(n+1)(1+D)+2} \tag{32}$$

$$V_{D1} = V_{D2} = V_{D3} = V_{C3} = \frac{[N(n+1)+1]V_{\text{IN}}}{1-D} = \frac{[N(n+1)+1]V_{\text{OUT}}}{N(n+1)(1+D)+2}. \tag{33}$$

It is seen from (32) that the voltage stresses across the semiconductors are substantially lower than the high output voltage. Therefore, MOSFETs with low ON-state resistance and diodes with low forward voltage drop can be implemented, which reduces the cost and conduction losses as well.

$I_{\text{LMC,ave}}$ and $I_{\text{LMB,ave}}$ are obtained to be MI_{OUT} and NI_{OUT}, respectively. The values of $I_{D2,\max}$ and $I_{D3,\max}$ are given in (20) and (21). In addition

$$I_{D1,\max} = \frac{2I_{\text{OUT}}}{1-D} \tag{34}$$

$$I_{\text{SC,max}} = I_{\text{SM,max}} = \left\{ M + (n+1)N + \frac{2[N(n+1)+1]}{D} \right\} I_{\text{OUT}} + \left[\frac{1}{L_{\text{MC}}} + \frac{(n+1)^2}{L_{\text{MB}}} \right] \frac{DV_{\text{IN}}}{2f_S}. \tag{35}$$

Having the maximum of the currents along with the corresponding conduction time intervals, the time-domain equations are written, which consequently yields the rms values, in (39) shown at the bottom of the next page

$$I_{D1,\text{rms}} = 2I_{\text{OUT}} \sqrt{\frac{1}{3(1-D)}} \tag{36}$$

$$I_{D2,\text{rms}} = 2I_{\text{OUT}} \sqrt{\frac{1}{3D}} \tag{37}$$

$$I_{D3,\text{rms}} = 4I_{\text{OUT}} \sqrt{\frac{1}{6(1-D)}} \tag{38}$$

$$I_{\text{SC,rms}} = I_{\text{CC,rms}} = \left(\left\{ M + (n+1)N - \frac{4[N(n+1)+1]}{1-D} \right\} I_{\text{OUT}} - \left[\frac{1}{L_{\text{MC}}} + \frac{(n+1)^2}{L_{\text{MB}}} \right] \frac{DV_{\text{IN}}}{2f_S} \right) \sqrt{\frac{1-D}{3}} \tag{40}$$

$$I_{\text{SB,rms}} = \sqrt{{I_{D1,\text{rms}}}^2 + {I_{D2,\text{rms}}}^2 + {I_{D3,\text{rms}}}^2 + \frac{4{I_{\text{OUT}}}^2}{3(1-D)}} \tag{41}$$

$$I_{\text{LKB,rms}} = N\sqrt{{I_{\text{SB,rms}}}^2 - {I_{\text{OUT}}}^2} \tag{42}$$

$$I_{\text{LKC,rms}} = \sqrt{(MI_{\text{OUT}})^2 + n^2 {I_{\text{LKB,rms}}}^2} \tag{43}$$

$$I_{C3,\text{rms}} = \sqrt{{I_{D2,\text{rms}}}^2 + {I_{D3,\text{rms}}}^2} \tag{44}$$

$$I_{C2,\text{rms}} = \sqrt{{I_{D1,\text{rms}}}^2 + {I_{D2,\text{rms}}}^2} \tag{45}$$

$$I_{C1,\mathrm{rms}} = \sqrt{\begin{array}{c} {I_{C2,\mathrm{rms}}}^2 + {I_{\mathrm{LKB,rms}}}^2 + 2N{I_{D1,\mathrm{rms}}}^2 - 2N{I_{D2,\mathrm{rms}}}^2 \\ -4N\left(\frac{2-3D}{3(1-D)}\right){I_{OUT}}^2 \end{array}} \tag{46}$$

$$I_{\mathrm{Co,rms}} = \sqrt{{I_{D3,\mathrm{rms}}}^2 - {I_{\mathrm{OUT}}}^2}. \tag{47}$$

C. Efficiency Estimation

In fact, the parasitic resistances of the components along with the forward voltage drop of the diodes affect the voltage gain and the conversion efficiency. Through the rms currents given in (36)–(47), the efficiency of the proposed converter can be estimated [30].

The losses of the MOSFETs are only related to the conduction losses and the switching losses are zero due to soft-switching performance

$$P_{\mathrm{MOSFETs}} = R_{\mathrm{DSM}}{I_{\mathrm{SM,rms}}}^2 + R_{\mathrm{DSC}}{I_{\mathrm{SC,rms}}}^2 \tag{48}$$

where R_{DSM} and R_{DSC} are the ON-state resistances of S_M and S_C, respectively.

The diodes dissipate some portion of the power by ON-state resistance (R_D) and forward voltage drop (V_{FD}) that is written as

$$P_{\mathrm{Diodes}} = \sum_{i=1}^{3}\left(R_{Di}{I_{Di,\mathrm{rms}}}^2 + V_{\mathrm{FD}i}I_{Di,\mathrm{ave}}\right). \tag{49}$$

The associated dissipation of the CI and BIT is related to the windings' losses that is given by

$$P_{\mathrm{CI\&BIT}} = \underbrace{R_{\mathrm{CI},p}{I_{\mathrm{LKC,rms}}}^2 + R_{\mathrm{CI},s}{I_{\mathrm{LKB,rms}}}^2 + P_{\mathrm{Core}}}_{P_{CI}} + \underbrace{R_{\mathrm{BIT},p}{I_{\mathrm{LKB,rms}}}^2 + R_{\mathrm{BIT},s}{I_{\mathrm{SB,rms}}}^2 + P_{\mathrm{Core}}}_{P_{\mathrm{BIT}}} \tag{50}$$

where $R_{\mathrm{CI},P}$ and $R_{\mathrm{CI},S} = nR_{\mathrm{CI},P}$ represent the primary and secondary windings' resistances of CI, respectively, and $R_{\mathrm{BIT},P}$ and $R_{\mathrm{BIT},S} = NR_{\mathrm{BIT},S}$ notate the primary and secondary windings' resistances of BIT.

The conduction losses of capacitors are written as follows:

$$P_{\mathrm{Capacitors}} = R_{\mathrm{CC}}{I_{\mathrm{CC,rms}}}^2 + R_{\mathrm{Co}}{I_{\mathrm{Co,rms}}}^2 + \sum_{i=1}^{3} R_{Ci}{I_{Ci,\mathrm{rms}}}^2. \tag{51}$$

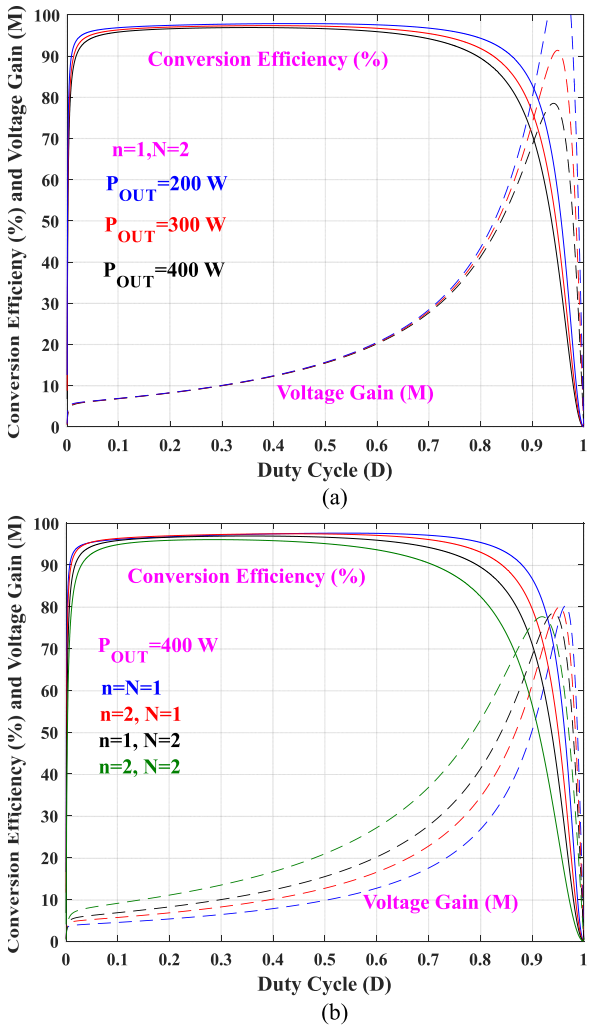


Fig. 6. Estimated conversion efficiency and the voltage gain of the proposed converter versus duty cycle with (a) different output powers and (b) different turn ratios.

Finally, the efficiency and the voltage gain of the proposed converter can be obtained from

$$\eta = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{OUT}} + P_{\mathrm{MOSFETs}} + P_{\mathrm{Diodes}} + P_{\mathrm{CI\&BIT}} + P_{\mathrm{Capacitors}}} \tag{52}$$

$$M = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \left[\frac{N(n+1)(1+D)+2}{1-D}\right]\eta. \tag{53}$$

Conversion efficiency and the voltage gain versus duty cycle are plotted in Fig. 6, according to the fabricated converter

$$I_{\mathrm{SM,rms}} = I_{\mathrm{OUT}}\sqrt{\begin{array}{c} \frac{4[N(n+1)+1]^2}{3D} + 2[M+(n+1)N][N(n+1)+1] \\ +D[M+(n+1)N]^2 \end{array}} \tag{39}$$

specifications that are given as follows:

$$V_{\rm IN} = 25\,{\rm V};\ f_S = 100\,{\rm kHz}$$
$$R_{\rm DSM} = R_{\rm DSC} = 2.3\,{\rm m\Omega}$$
$$R_{D1} = R_{D2} = R_{D3} = 12\,{\rm m\Omega}$$
$$V_{\rm FD1} = V_{\rm FD2} = V_{\rm FD3} = 1.2\,{\rm V}$$
$$R_{{\rm CI},P} = 10\,{\rm m\Omega}\ \text{(two parallel wires)}$$
$$R_{{\rm CI},S} = 2nR_{{\rm CI},P}$$
$$R_{{\rm BIT},P} = 22\,{\rm m\Omega}$$
$$R_{{\rm BIT},S} = NR_{{\rm BIT},P}$$
$$R_{\rm CC} = R_{C1} = R_{C2} = R_{C3} = 12\,{\rm m\Omega}$$
$$R_{\rm Co} = 100\,{\rm m\Omega}.$$

It is seen from Fig. 6(a) that by reducing the output power from 400 to 200 W, the conversion efficiency is improved and the voltage gain varies slightly. Moreover, according to Fig. 6(b), it is seen that at a given voltage gain, by implementing higher turns ratios, the duty ratio can be decreased, which results in relatively equal conversion efficiency and lower turns ratios.

By increasing the output power of these converters, the voltage gain is decreased and the duty cycle should be increased to regulate the output voltage. This will increase the conduction losses and the efficiency is deteriorated severely. For higher power applications, the interleaved dc–dc converters are more interesting due to shared thermal stress, reduced losses, and increased efficiency.

D. ZVS Realization

Due to the existence of $C_{\rm SM}$ and $C_{\rm SC}$, the ZVS turn-OFF of the MOSFETs is naturally provided. Moreover, the ZVS turn-ON of S_C is achieved because its antiparallel diode is ON before the gate pulse comes. The only constraint for providing ZVS turn-ON of S_C is to ensure that the gate pulse is applied after the interval in which $C_{\rm SM}$ and $C_{\rm SC}$ are fully charged and discharged, respectively. Hence from (7), the required time delay should satisfy the following inequality:

$$T_{{\rm delay}-S_C:{\rm ON}} \geq \Delta t_2. \tag{54}$$

To satisfy the ZVS turn-ON of SM, three following conditions should be provided.

1) The gate pulse of SM comes after $C_{\rm SM}$ and $C_{\rm SC}$ are fully discharged and charged, respectively. From equation (17), we have

$$T_{{\rm delay}-S_M:{\rm ON}} \geq \Delta t_7. \tag{55}$$

2) $i_{\rm LKC}(t_6)+i_{\rm LKB}(t_6)-i_{\rm SB}(t_6)$ should be negative to discharge $C_{\rm SM}$ and charge $C_{\rm SC}$

$$i_{\rm LKC}(t_6) + i_{\rm LKB}(t_6) - i_{\rm SB}(t_6) = i_{\rm LMC}(t_6) + (n+1)i_{\rm LMB}(t_6) - [N(n+1)+1]\, i_{\rm SB}(t_6). \tag{56}$$

According to Fig. (3), it is seen that $i_{\rm SB}(t_6) \approx i_{\rm SB}(t_7)$. Therefore, using (21), (56) can be simplified as follows:

$$i_{\rm LKC}(t_6) + i_{\rm LKB}(t_6) - i_{\rm SB}(t_6) = \frac{-2N(n+1)-2}{(1-D)} - \frac{DV_{\rm in}}{2f_S}\left[\frac{1}{L_{\rm MC}} + \frac{(n+1)^2}{L_{\rm MB}}\right] \leq 0. \tag{57}$$

Therefore, the second condition is always achieved.

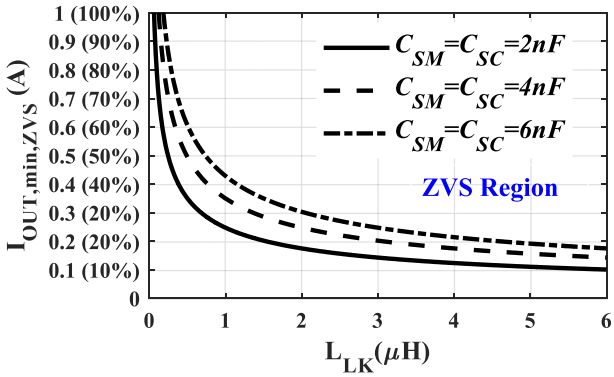


Fig. 7. ZVS region of the proposed converter with $n = 1$, $N = 2$, and $V_{\rm IN} = 25$ V.

3) The available inductive energy should be high enough so that $i_{\rm LKC}(t)+i_{\rm LKB}(t)-i_{\rm SB}(t)$ will still remain negative after $C_{\rm SM}$ and $C_{\rm SC}$ are fully discharged and charged, respectively. In such a case, the current flows through the antiparallel diode of SM and ZVS turn-ON is provided

$$\frac{n^2 L_{\rm LKC} + L_{\rm LKB}}{2}\left[i_{\rm LKB}(t_6)^2 - i_{\rm LKB}(t_8)^2\right] \geq \frac{C_{\rm SM} + C_{\rm SC}}{2} V_{\rm SM}{}^2. \tag{58}$$

At t_8, $i_{\rm SM}$ is zero and after that its direction is changed. Therefore, assuming the ripple content of $i_{\rm LKC}(t)$ and $i_{\rm LKB}(t)$ to be zero, we have

$$i_{\rm LKB}(t_6) = I_{\rm LMB} - NI_{\rm SB,max} = \frac{-N(3+D)}{1-D} I_{\rm OUT} \tag{59}$$

$$i_{\rm LKB}(t_8) = \frac{I_{\rm LMB} - NI_{\rm LMC}}{N(n+1)+1} = \frac{N(1-M)I_{\rm OUT}}{N(n+1)+1} = \frac{N(1+D)I_{\rm OUT}}{1-D}. \tag{60}$$

By substituting (32), (59), and (60) into (58) yields the following ZVS range as well:

$$I_{\rm OUT,min,ZVS} = \frac{V_{\rm IN}}{2N}\sqrt{\frac{C_{\rm SM} + C_{\rm SC}}{(n^2 L_{\rm LKC} + L_{\rm LKB})(2+D)}}. \tag{61}$$

Fig. 7 shows the ZVS region of the proposed converter with $n = 1$, $N = 2$, and $V_{\rm IN} = 25$ V. At higher output current, the ZVS is obtained with little leakage inductances. At light load conditions, higher values of leakage inductance should be selected to achieve soft switching. However, high leakage inductance decreases the voltage gain and, as a result, it should be selected reasonably. It is seen that for the fabricated converter with the leakage inductance of about 3 μH, the ZVS is obtained at 14%, 20%, and 25% of full load for the parallel capacitors of 2, 4, and 6 nF, respectively.

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER

Converter	[27]	[28]	[30]	[32]	[33]	Proposed
Technique	CI	CI	BIT	BIT	CI+BIT	CI+BIT
No. of MOSFETs	2	2	2	2	1	2
No. of Diodes	3	3	2	3	3	3
No. of Cores	1	1	2	2	2	2
No of Capacitors	4	4	4	5	4	5
ZVS	Yes	Yes	Yes	Yes	No	Yes
Voltage Gain (M)	$\frac{2n+1-nD}{1-D}$	$\frac{2n+2-nD}{1-D}$	$\frac{N+2}{1-D}$	$\frac{D(N-1)+N+2}{1-D}$	$\frac{N+n+2}{1-D}$	$\frac{N(n+1)(1+D)+2}{1-D}$
Voltage Stress Across MOSFETs	$\frac{V_{OUT}}{2n+1-nD}$	$\frac{V_{OUT}}{2n+2-nD}$	$\frac{V_{OUT}}{N+2}$	$\frac{V_{OUT}}{D(N-1)+N+2}$	$\frac{V_{OUT}}{N+n+2}$	$\frac{V_{OUT}}{N(n+1)(1+D)+2}$
Voltage Stress Across Diodes	$\frac{(n+1)V_{OUT}}{2n+2-nD}$	$\frac{(n+1)V_{OUT}}{2n+2-nD}$	$\frac{(N+1)V_{OUT}}{N+2}$	$\frac{(N+1)V_{OUT}}{D(N-1)+N+2}$	$\frac{(N+n+1)V_{OUT}}{N+n+2}$	$\frac{[N(n+1)+1]V_{OUT}}{N(n+1)(1+D)+2}$
Measured Efficiency	$\eta=95.5\%$ $V_{IN}=48V$ $V_{OUT}=400V$ $P_{OUT}=400W$ $f_S=100kHz$	$\eta=95.3\%$ $V_{IN}=40V$ $V_{OUT}=400V$ $P_{OUT}=400W$ $f_S=50kHz$	$\eta=94.8\%$ $V_{IN}=40V$ $V_{OUT}=400V$ $P_{OUT}=400W$ $f_S=100kHz$	$\eta=93.7\%$ $V_{IN}=28V$ $V_{OUT}=400V$ $P_{OUT}=225W$ $f_S=70kHz$	$\eta=95.7\%$ $V_{IN}=24V$ $V_{OUT}=400V$ $P_{OUT}=200W$ $f_S=100kHz$	$\eta=95.3\%$ $V_{IN}=25V$ $V_{OUT}=400V$ $P_{OUT}=400W$ $f_S=100kHz$

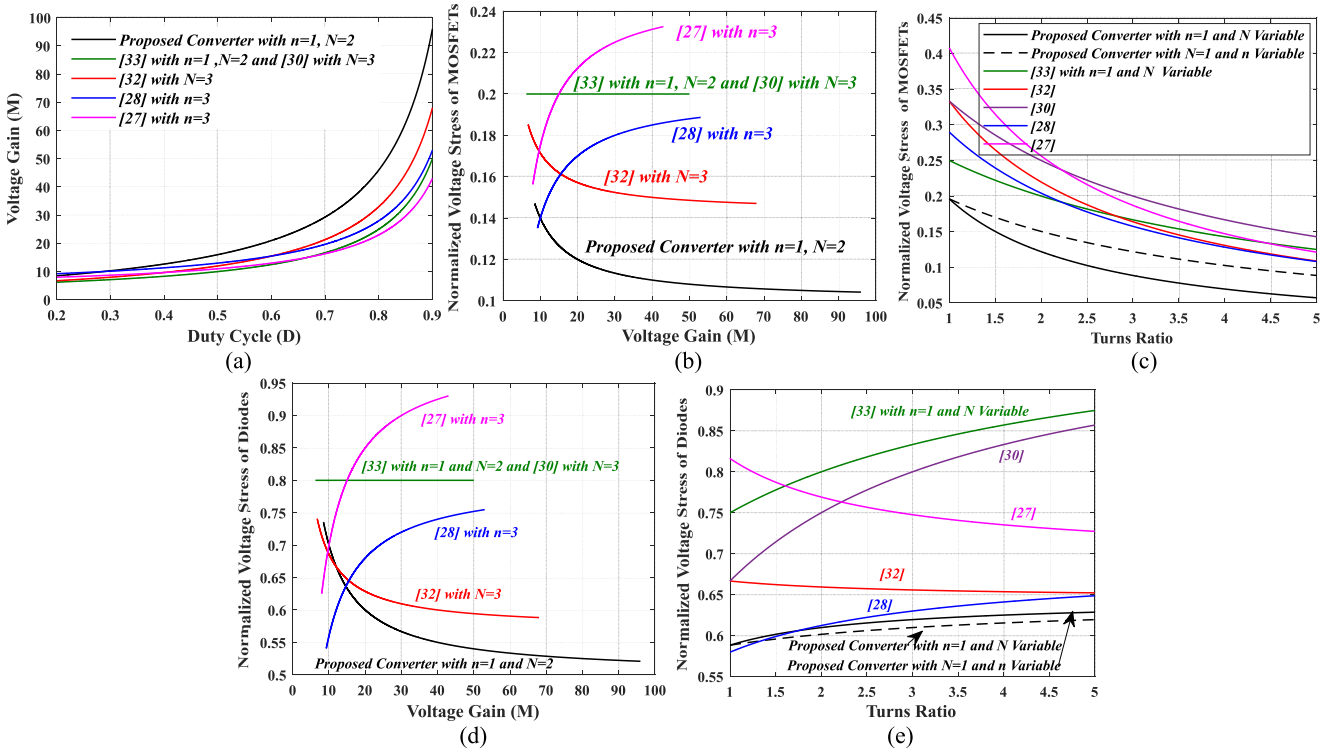


Fig. 8. Performance comparison of (a) voltage gain, (b) normalized voltage stresses across MOSFETs versus voltage gain with sweeping D from 20% to 90%, (c) normalized voltage stresses across MOSFETs versus turns ratio, (d) normalized voltage stresses across diodes versus voltage gain with sweeping D from 20% to 90%, and (e) normalized voltage stresses across diodes versus turns ratio.

IV. PERFORMANCE COMPARISON

A comparison is made between the proposed converter and the introduced converters in [27], [28], [30], [32], and [33], which is presented in Table I. The comparison of voltage gain and semiconductors' voltage stress is shown in Fig. 8. $n = 1$ and $N = 2$ are considered for the proposed converter and its main competitor in [33] whenever it is needed to assume a constant turns ratio. Furthermore, to have a fair comparison in such cases, the values of n or N in the other step-up converters are chosen to be 3.

The comparison of the voltage gain of the competitors is depicted in Fig. 8(a). It can be seen that the proposed converter has the highest voltage gain of all.

Fig. 8(b) and (c) shows the comparison of the normalized voltage stresses across the MOSFETs. In Fig. 8(b), the duty cycle is swept from 20% to 90%. It is seen that at a given voltage

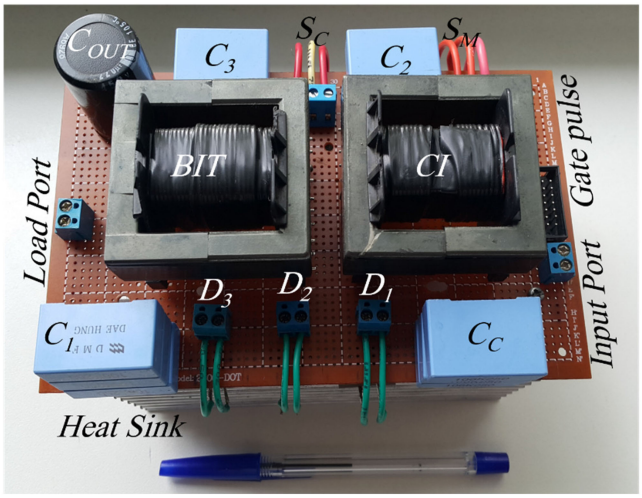


Fig. 9. Photograph of the developed converter.

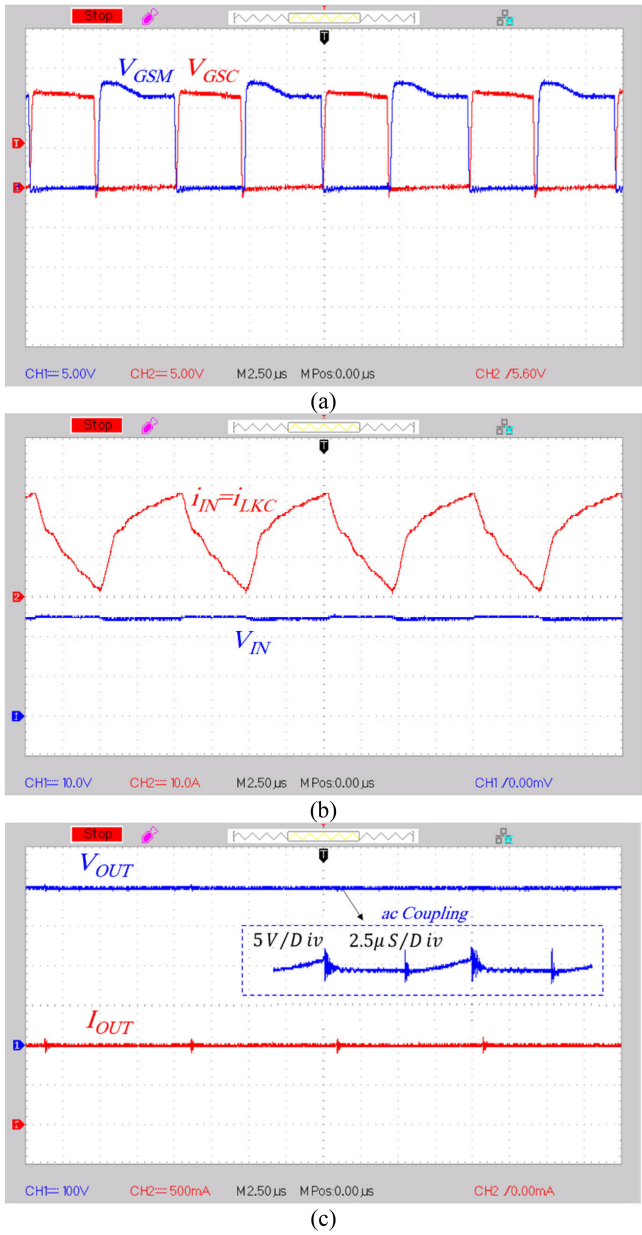


Fig. 10. Experimental results of (a) pulsewidth modulation (PWM) signals, (b) $i_{\rm IN}$ and $V_{\rm IN}$, and (c) $V_{\rm OUT}$ and $I_{\rm OUT}$.

gain, the proposed converter has the lowest voltage stress across the MOSFETs. In Fig. 8(c), the duty cycle of the competitors is chosen to be 55% and the MOSFETs voltage stress versus the turns ratio is given. It is clear that the proposed converter has the lowest voltage stress of all. Consequently, low-voltage-rated switching devices can be utilized to reduce conduction losses and cost.

Fig. 8(d) and (e) shows the comparison of the normalized voltage stresses across the diodes. Again, at a given voltage gain [see Fig. 8(d)] and a given turns ratio [see Fig. 8(c)], the lowest voltage stress is imposed across the diodes in the proposed converter. Hence, diodes with low forward voltage drop can be implemented, reducing the conduction losses and cost.

The proposed converter achieves a higher conversion efficiency than those in [30] and [32] even with much lower input voltage (higher current stress at a given power) than the converter proposed in [30] and higher switching frequency than the converter proposed in [32]. Although the proposed converter has lower conversion efficiency than that in [27] and [33]; however, it has a much lower input voltage than that in [27] and its operation output power is twice the one for the converted given in [33]. Moreover, the proposed converter achieves the same conversion efficiency obtained in [28] with twice switching frequency and a much lower input voltage.

As discussed above, the advantages of higher voltage gain, lower voltage stress, and high conversion efficiency are achieved by the proposed converter with relatively equal number of the components in comparison with its competitors especially [33].

V. Numerical Design

The components of the converter are designed based on 400 W maximum output power, 25–400 V voltage conversion, and 100 kHz switching frequency. $n = 1$ and $N = 2$ are considered as the turns ratios of the CI and BIT, respectively. According to (30), the nominal duty cycle is obtained as 50%. However, as discussed earlier, at high loads, the conduction losses of the components and the leakage inductances decrease the voltage gain and the duty cycle should be increased to compensate the voltage deviation. Therefore, the range of duty cycle is considered to be 50%–55%.

A. Design of CI and BIT

$L_{\rm MC}$ and $L_{\rm MB}$ are designed to assure continuous conduction mode operation at 10% of load current. At the boundary conduction mode, $I_{\rm LMC}$ and $I_{\rm LMB}$ are equal to half of their corresponding ripple content. Therefore

$$\begin{cases} I_{\rm LMC} = MI_{\rm OUT,BCM} = \dfrac{\Delta i_{\rm LMC}}{2} = \dfrac{DV_{\rm IN}}{2L_{\rm MC,min}f_S} \\ I_{\rm LMB} = NI_{\rm OUT,BCM} = \dfrac{\Delta i_{\rm LMB}}{2} = \dfrac{D(n+1)V_{\rm IN}}{2L_{\rm MB,min}f_S} \end{cases}. \quad (62)$$

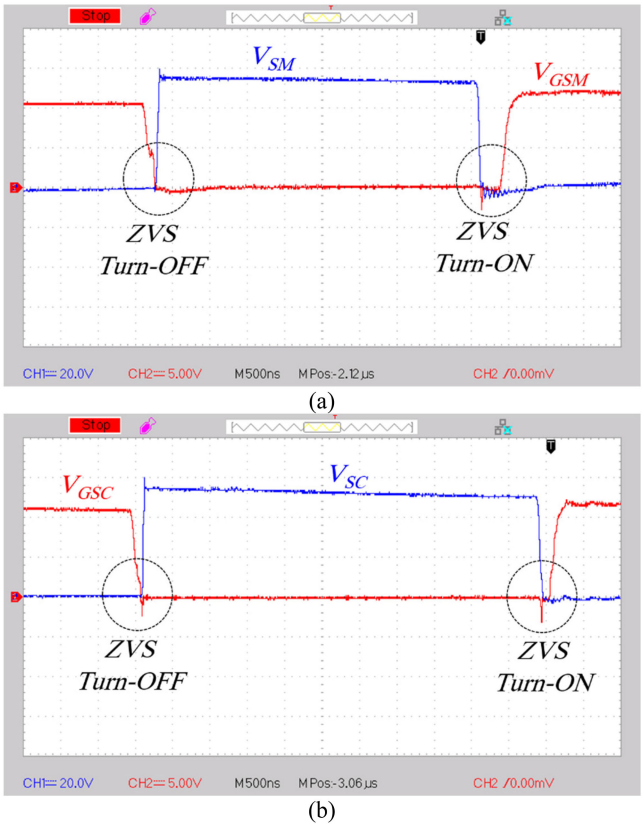


Fig. 11. Experimental results of (a) $V_{\rm SM}$ and $V_{\rm GSM}$, and (b) $V_{\rm SC}$ and $V_{\rm GSC}$.

From (62), by assuming that the voltage gain at low output power is closed to its ideal value, duty cycle will be around 50%. Hence, the minimum required magnetizing inductances are obtained to be

$$\begin{cases} L_{\rm MC,min} = \frac{DV_{\rm IN}}{2MI_{\rm OUT,BCM}f_S} = \frac{0.5\times25}{2\times16\times(0.1\times1)\times100000} = 39\,\mu{\rm H} \\ L_{\rm LMB,min} = \frac{D(n+1)V_{\rm IN}}{2NI_{\rm OUT,BCM}f_S} = \frac{0.5\times(1+1)\times25}{2\times2\times(0.1\times1)\times100000} = 625\,\mu{\rm H} \end{cases}. \tag{63}$$

The fabricated CI and BIT have the following specifications:

$$\text{CI}: \begin{cases} L_{\rm MC} = 47\,\mu{\rm H}; L_{\rm LKC} = 1.1\,\mu{\rm H} \\ R_{{\rm CI},P} = 10\,{\rm m}\Omega \text{ (two parallel twisted wires)}; R_{{\rm CI},S} = 20\,{\rm m}\Omega \end{cases}$$
$$\text{BIT}: \begin{cases} L_{\rm MB} = 627\,\mu{\rm H}; L_{\rm LKB} = 2\,\mu{\rm H} \\ R_{{\rm BIT},P} = 22\,{\rm m}\Omega\,; R_{{\rm BIT},S} = 44\,{\rm m}\Omega. \end{cases}$$

B. Design of Semiconductors

The MOSFETs and diodes are designed based on their corresponding voltage and current stresses derived in Section III-B.

According to (32), (35), (39) and (40), $V_{\rm SM} = V_{\rm SC} = 55\,{\rm V}$, $I_{\rm SM,max} = I_{\rm SC,max} = 39.65\,{\rm A}$, $I_{\rm SM,rms} = 21.92\,{\rm A}$, and $I_{\rm SC,rms} = 9\,{\rm A}$. Therefore, IPP023N08N5 ($V_{\rm DS} = 80\,{\rm V}$, $R_{\rm DS} = 2.3\,{\rm m}\Omega$) is chosen for S_M and S_C. Moreover, using (33), (34), and (36)–(38), $V_{D1} = V_{D2} = V_{D3} = 243\,{\rm V}$, $I_{D1,\rm rms} = 1.72\,{\rm A}$, $I_{D2,\rm rms} = 1.56\,{\rm A}$, $I_{D3,\rm rms} = 2.43\,{\rm A}$. MUR1540 ($V_{\rm FD} = 1.2\,{\rm V}, R_D = 12\,{\rm m}\Omega$) is selected for D_1, D_2, and D_3.

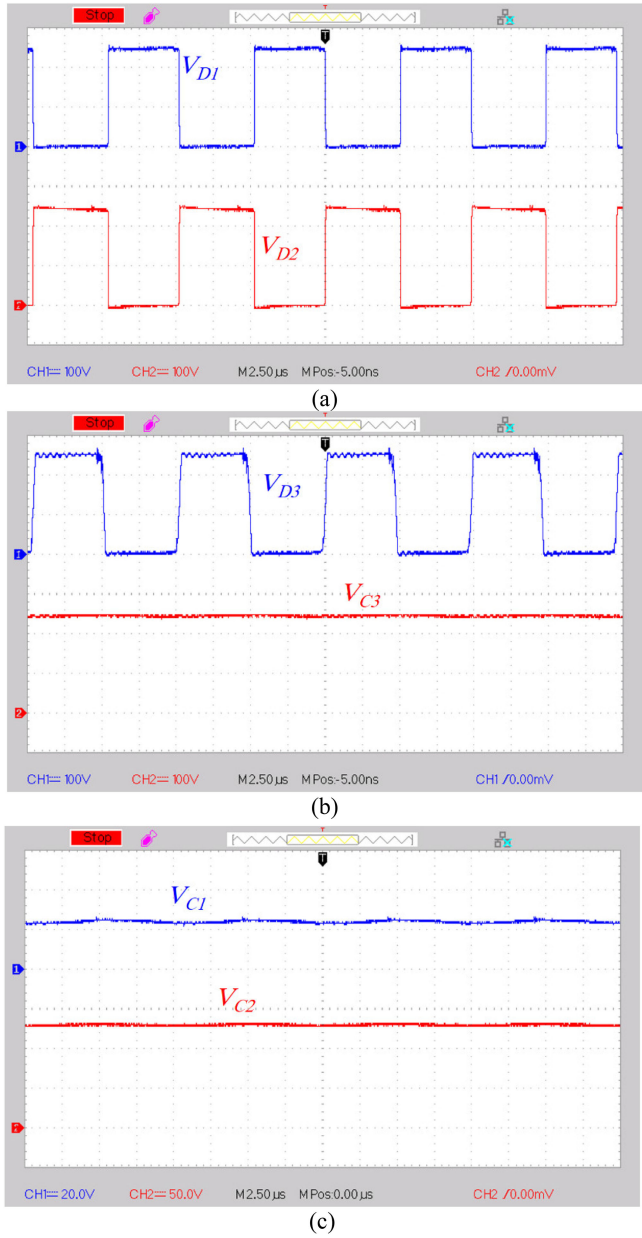


Fig. 12. Experimental results of (a) V_{D1} and V_{D2}, (b) V_{D3} and V_{C3}, and (c) V_{C1} and V_{C2}.

C. Design of Capacitors

The capacitors are designed based on their voltage ripple. According to (25), (31), and (32), the values of $V_{C1} = 25\,{\rm V}$, $V_{C2} = 133\,{\rm V}$, $V_{C3} = 243\,{\rm V}$, and $V_{\rm CC} = 55\,{\rm V}$ are obtained. Considering 5% voltage ripple for C_1 and 2% voltage ripple for C_2, C_3, and C_C, the capacitors are designed as follows:

$$C_1 \geq \frac{(N(1+D)+1)\,I_{\rm out}}{f_S \times (0.05V_{C1})} = 32.8\,\mu{\rm F} \tag{64}$$

$$C_2 \geq \frac{I_{\rm out}}{f_S \times (0.02V_{C2})} = 3.75\,\mu{\rm F} \tag{65}$$

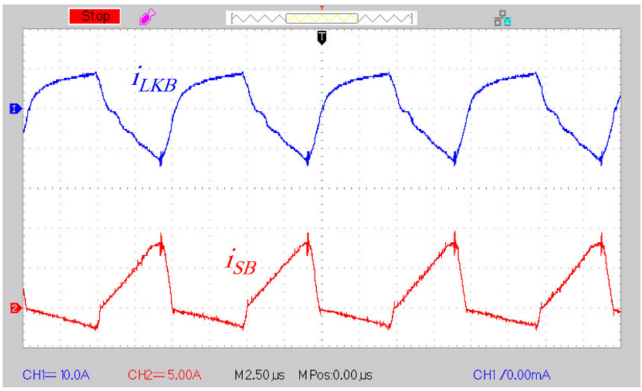
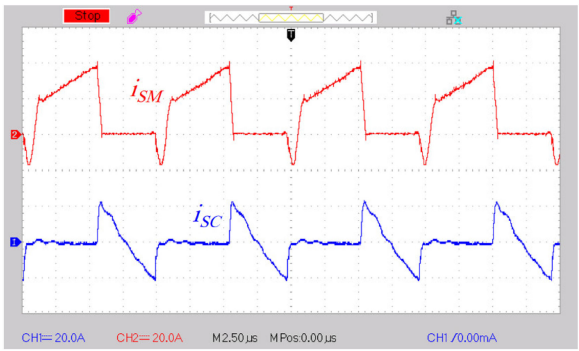
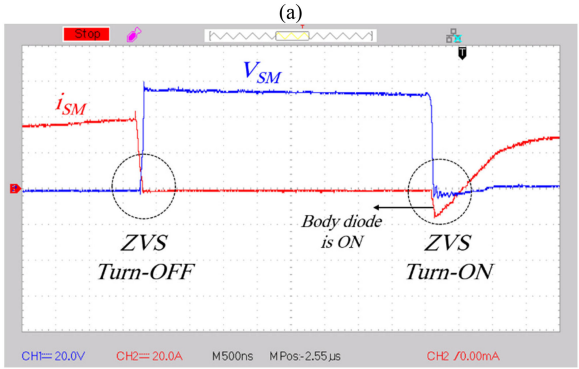


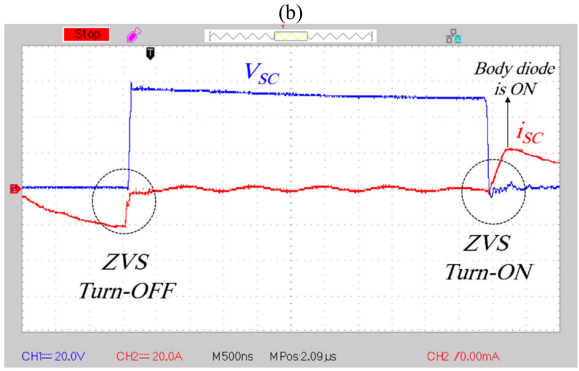
Fig. 13. Experimental results of i_{LKB} and i_{SB}.



(a)

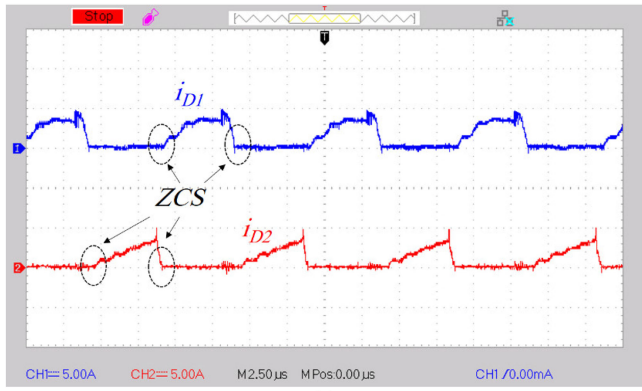


(b)

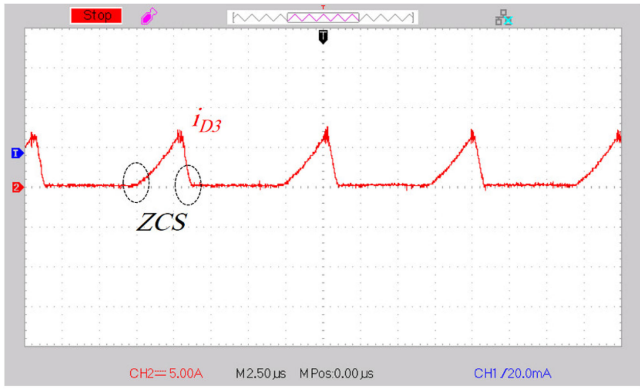


(c)

Fig. 14. Experimental results of (a) i_{SM} and i_{SC}, (b) i_{SM} and V_{SM}, and (c) i_{SC} and V_{SC}.



(a)



(b)

Fig. 15. Experimental results of (a) i_{D1} and i_{D2} and (b) i_{D3}.

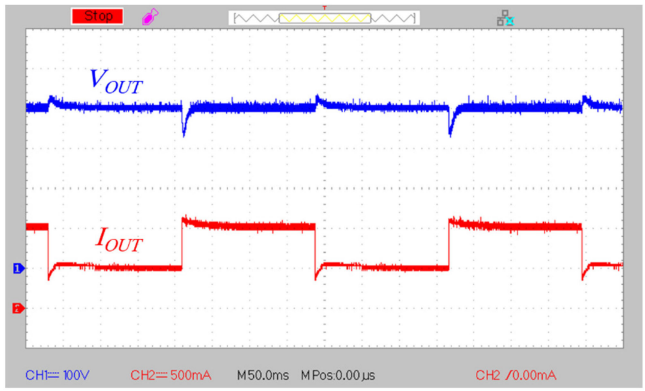


Fig. 16. Dynamic response of the proposed converter.

$$C_3 \geq \frac{I_{\mathrm{out}}}{f_S \times (0.02 V_{C3})} = 2\,\mu\mathrm{F} \tag{66}$$

$$C_C \geq \frac{(1-D)\left[M + (n+1)N + \frac{4((n+1)N+1)}{1-D}\right] I_{\mathrm{out}}}{4 f_S \times (0.02 V_{\mathrm{CC}})} = 25\,\mu\mathrm{F}. \tag{67}$$

In this design, available $30\ -\ \mu$F film capacitors are selected for C_1 and C_C. Moreover, to reduce the power dissipations, capacitors with lower ESR are preferred, which is yield by

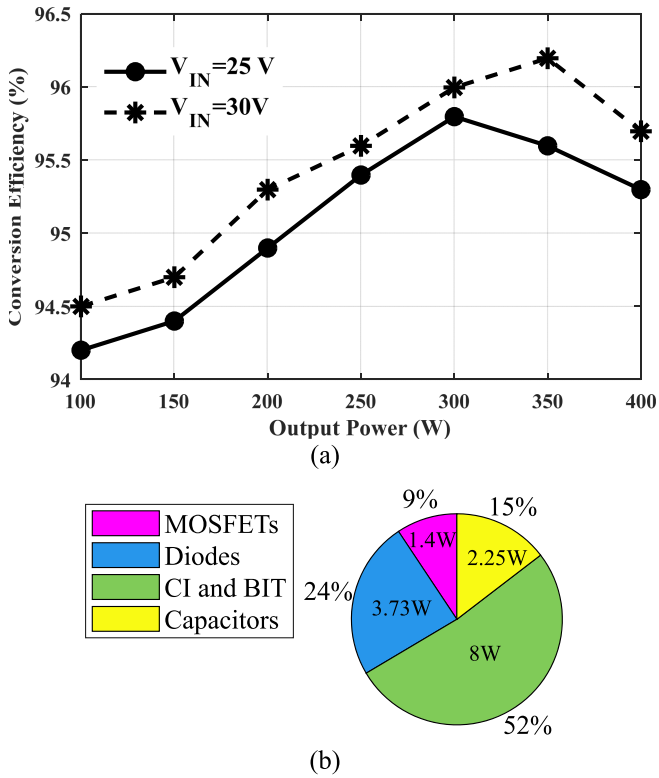


Fig. 17. (a) Conversion efficiency of the proposed converter. (b) Pie graph of the losses distribution at full load.

TABLE II
SPECIFICATIONS OF THE PROPOSED CONVERTER

Components	Parameters
Output Power (P_{OUT})	$400W$
Input/output Voltages (V_{IN} –V_{OUT})	$25V$ – $400V$
Switching Frequency (f_S)	$100kHz$
Power MOSFTEs (S_M and S_C)	$IPP023N08N5$
Diodes (D_1 , D_2 , D_3)	$MUR1540$
Capacitors (C_C ,C_1,C_2,C_3)	*Film Capacitors* $3\times10\,\mu F$,$3\times10\,\mu F$,$10\,\mu F$,$10\,\mu F$
Capacitors (C_{OUT})	*Electrolytic capacitor* : $220\,\mu F$
Coupled Inductors	Ferrite Core EE55; $n=1; L_{MC}=47\,\mu$H; $L_{LKC}1.1\mu H$; $R_{CI\_P}=12m\Omega; R_{CI\_S}=24m\Omega$.
Built-In Transformer	Ferrite Core EE55; $N=2; L_{MC}=627\,\mu$H; $L_{LKC}=2\mu H$; $R_{BIT\_P}=26m\Omega; R_{BIT\_S}=52m\Omega$.

selecting higher capacitances. Therefore, for each of C_2 and C_3, three $10\,\mu$F capacitors are connected in parallel.

VI. Experimental Verification

A 400-W prototype with 25–400 V voltage conversion is built in the laboratory to validate the carried analysis and the performance operation of the proposed converter. Fig. 9 shows the picture of the developed converter. The components specifications of the converter are provided in Table II.

Fig. 10 shows the experimental results of the input/output voltages and currents along with the PWM signals applied to the switches. It is clear that the proposed converter achieves the high voltage conversion of 25–400 V at 400 W output power.

Fig. 11 shows the experimental results of the gate pulses of the MOSFETs along with the corresponding drain–source voltage. The voltage stress across the power switches is about 56 V, which is much lower than the high output voltage. Moreover, the ZVS performance is satisfied during whole switching cycle.

Fig. 12 shows the experimental results of the voltages of the diodes and capacitors. The voltage stresses of the diodes are about 243 V, which are substantially lower than the output voltage. The voltages of capacitors are about $V_{C1}=25$ V, $V_{C2}=133$ V, and $V_{C3}=242$ V that are consistent with the theoretical values in Section V-A.

Fig. 13 shows currents passing through the primary and secondary windings of BIT, which confirms the key waveforms of Fig. 3.

Fig. 14(a) shows the passing current through the main and clamp MOSFETs. To further discuss the ZVS performance, the zoomed waveforms of the switches currents are presented along with the corresponding drain–source voltages in Fig. 14(b) and (c). It is seen from Fig. 14(b) that by providing a negative current before coming of the gate pulses of the main MOSFET, its body diode is turned ON and the ZVS turn ON is realized. Moreover, it is clear from Fig. 14(c) that at the turn-ON instant of the clamp MOSFET, its body diodes starts conducting, satisfying the natural ZVS turn-ON. The ZVS turn-OFF is also explored from the experimental results.

Fig. 15 shows the passing current through the diodes. It is clear that all of the diodes are operated with ZCS at the instants of ON and OFF, which alleviates the reverse current recovery problems and enhances the circuit performance.

Fig. 16 shows the experimental results of the proposed converter with output power variations between full load and half load. Duty cycle is adjusted to regulate the output voltage at the reference value of 400 V.

Fig. 17 shows the conversion efficiency of the proposed converter along with the pie graph distribution of the components. From Fig. 17(a), it is clear that the maximum efficiency is about 95.8% at 300 W output power and the full load efficiency is about 95.3%. Moreover, it is clear that by increasing of the input voltage from 25 to 30 V, the conversion efficiency is improved. At this condition, the maximum efficiency is about 96.2% at 350 W output power and the full load efficiency is about 95.7%. According to Fig. 17(b), the analytical total losses of the proposed converter at full load is about 15.44 W that yields the theoretical conversion efficiency of 96.3%. It is seen that the theoretical and experimented conversion efficiencies fairly approve each other.

VII. Conclusion

An improved ZVS high step-up converter has been proposed in this article. By implementing the CI and BIT concept, a flexible voltage gain is achieved in which for further extension of the voltage conversion ratio, the secondary winding of the CI

is inserted in series with the primary winding of BIT. In such a case, the voltage gain is proportional to the multiplication of the turns ratios of the CI and BIT, contrary to the introduced converter of [33]. Moreover, the blocking capacitor also participated to obtain higher voltage gain. The voltage stress across the MOSFETs is considerably decreased and by utilizing of the active clamp circuit, the ZVS performance is guaranteed for the power switches through whole switching cycle. Through extensive comparison discussion with some relevant topologies in [27], [28], [30], [32], and [33], it was approved that the proposed converter has the highest voltage gain and the lowest voltage stress across MOSFETs and diodes. Another point resulted from the comparison study is that by considering the handled power, input/output voltages, and switching frequency, the proposed converter has a high conversion efficiency of 95.3%, which is high in comparison with its competitors operating with higher input voltage and lower switching frequency. It is worth to mention that due to implementation of the CI instead of the input filter inductor, the input current ripple is high, which is accounted as the main disadvantage of the proposed converter. Performance operation of the proposed converter has been verified through a 25–400 V and 400-W laboratory prototype with a full load efficiency of 95.3%.

REFERENCES

[1] A. Ioinovici, *Power Electronics and Energy Conversion Systems*, vol. 1. Chichester, U.K.: Wiley, 2013.

[2] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: A comprehensive review of voltage boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.,* vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[3] V. F. Pires, A. Cordeiro, D. Foito, and J. F. Silva, "High step-up DC–DC converter for fuel cell vehicles based on merged quadratic boost–Ćuk," *IEEE Trans. Veh. Technol.*, vol. 68, no. 8, pp. 7521–7530, Aug. 2019.

[4] Y. Zhang, H. Liu, J. Li, M. Summer, and C. Xia, "DC–DC boost converter with a wide input rang and high voltage gain for fuel cell vehicles," *IEEE Trans. Power Electron.,* vol. 34, no. 5, pp. 4100–4111, May 2019.

[5] G. Zhang *et al.*, "A generalized additional voltage pumping solution for high-step-up converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6456–6467, Jul. 2019.

[6] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformer-less hybrid DC–DC PWM converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.

[7] A. A. Fardoun and H. I. Esam, "Ultra step-up dc-dc converter with reduced switch stress," *IEEE Trans. Ind. Appl.*, vol. 46, no. 5, pp. 2025–2034, Sep./Oct. 2010.

[8] T. Nouri, S. H. Hosseini, E. Babaei, and J. Ebrahimi, "A generalised transformerless ultra step-up DC-DC converter with reduced voltage stress on semiconductors," *IET Power Electron.,* vol. 7, no. 11, pp. 2791–2805, Nov. 2014.

[9] C. M. Young, M. H. Chen, T. A. Chang, and K. K. Jen, "Cascade cockcroft-walton voltage multiplier applied to transformerless high step-up DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 523–537, Feb. 2013.

[10] A. Rajaei, R. Khazan, M. Mahmoudian, M. Mardaneh, and M. Gitizadeh, "A dual inductor high step-up DC/DC converter based on the cockcroft–walton multiplier," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9699–9709, Nov. 2018.

[11] M. A. Salvador, T. B. Lazzarin, and R. F. Coelho, "High step-up DC–DC converter with active switched-inductor and passive switched-capacitor networks," *IEEE Trans. Ind. Electrons*, vol. 65, no. 7, pp. 5644–5654, Jul. 2018.

[12] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of high-stepup coupled-inductor boost converters," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 2, pp. 689–704, Jun. 2016.

[13] Y. Zheng and K. M. Smedley, "Analysis and design of a single-switch high step-up coupled-inductor boost converter," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 535–545, Jan. 2020.

[14] Y. Wang, Y. Qiu, Q. Bian, Y. Guan, and D. Xu, "A single switch quadratic boost high step up DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4387–4397, Jun. 2019.

[15] D. Yu, J. Yang, R. Xu, Z. Xia, H. H. Iu, and T. Fernando, "A family of module-integrated high step-up converters with dual coupled inductors," *IEEE Access*, vol. 6, pp. 16256–16266, 2018.

[16] Y. Hsieh, J. Chen, T. Liang, and L. Yang, "Novel high step-up DC–DC converter with coupled-inductor and switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 998–1007, Feb. 2012.

[17] T. Liang, S. Chen, L. Yang, J. Chen, and A. Ioinovici, "Ultra-large gain step-up switched-capacitor DC-DC converter with coupled inductor for alternative sources of energy," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 864–874, Apr. 2012.

[18] K. Tseng, J. Lin, and C. Huang, "High step-up converter with three-winding coupled inductor for fuel cell energy source applications," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 574–581, Feb. 2015.

[19] A. Ajami, H. Ardi, and A. Farakhor, "A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4255–4263, Aug. 2015.

[20] J. Ai and M. Lin, "Ultralarge gain step-up coupled-inductor DC–DC converter with an asymmetric voltage multiplier network for a sustainable energy system," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6896–6903, Sep. 2017.

[21] A. M. S. S. Andrade, L. Schuch, and M. L. da Silva Martins, "Analysis and design of high-efficiency hybrid high step-up DC–DC converter for distributed PV generation systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3860–3868, May 2019.

[22] W. Hassan, D. D. Lu, and W. Xiao, "Single-switch high step-up DC–DC converter with low and steady switch voltage stress," *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9326–9338, Dec. 2019.

[23] M. Chen, C. Yin, P. C. Loh, and A. Ioinovici, "Improved large DC gain converters with low voltage stress on switches based on coupled-inductor and voltage multiplier for renewable energy applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2824–2836, Sep. 2020.

[24] K. B. Park, G. W. Moon, and M. J. Youn, "Nonisolated high step-up boost converter integrated with SEPIC converter," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2266–2275, Sep. 2010.

[25] Y. Deng, Q. Rong, W. Li, Y. Zhao, J. Shi, and X. He, "Single-switch high step-up converters with built-in transformer voltage multiplier cell," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3557–3567, Aug. 2012.

[26] R. Moradpour, H. Ardi, and A. Tavakoli, "Design and implementation of a new sepic-based high step-up dc/dc converter for renewable energy applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1290–1297, Feb. 2017.

[27] S. Sathyan, H. M. Suryawanshi, M. S. Ballal, and A. B. Shitole," Soft-switching DC-DC converter for distributed energy sources with high step-up voltage capability," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7039–7050, Nov. 2015.

[28] L. He, Z. Zheng, and D. Guo, "High step-up DC–DC converter with active soft-switching and voltage-clamping for renewable energy systems," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9496–9505, Nov. 2018.

[29] A. Mirzaee and J. S. Moghani, "Coupled inductor-based high voltage gain DC–DC converter for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7045–7057, Jul. 2020.

[30] Y. Zheng, B. Brown, W. Xie, S. Li, and K. Smedley, "High step-up DC–DC converter with zero voltage switching and low input current ripple," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9416–9429, Sep. 2020.

[31] X. Zhang *et al.*, "Novel high step-up soft-switching DC–DC converter based on switched capacitor and coupled inductor," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9471–9481, Sep. 2020.

[32] K. Zaoskoufis and E. C. Tatakis, "An improved boost-based DC/DC converter with high voltage step-up ratio for DC microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1837–1853, Apr. 2021.

[33] Y. Lu, H. Liu, H. Hu, H. Wu, and Y. Xing, "Single-Switch high step-up converter with coupled-inductor and built-in transformer," in *Proc. IEEE 10th conf. Ind. Electron. Appl.*, Jun. 2015, pp. 1181–1186.

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