A Two-Phase Three-Level Buck Converter With Cross-Connected Flying Capacitors for Inductor Current Balancing

Chuang Wang, *Member, IEEE*, Yan Lu, *Senior Member, IEEE*, Mo Huang, *Senior Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*—The two-phase operation of a dc–dc converter has several benefits, when compared with the single phase, including higher efficiency, smaller ripple, faster response, etc. However, it suffers from unbalanced currents between the two phases. This article presents a two-phase three-level buck converter with cross-connected flying capacitors (X-C_{FLY}). The proposed converter suppresses the unbalanced inductor currents in a two-phase operation, through the alternate connection of flying capacitors across the branches. Meanwhile, two-phase and three-level techniques help to achieve a fast transient response and a small output ripple. In addition, we derive the transfer function of the proposed generalized multiphase three-level buck converter with interconnected C_{FLY} for analysis, and design accordingly its power stage and feedback loop. Finally, we validate the proposed converter through the fabrication in a 65 nm CMOS GP process. It achieves a low unbalanced current close to 5 mA and a small output ripple of 50 mV for a load current around 110 mA, and a peak efficiency of about 86%.**

***Index Terms*—Buck converter, cross-connected, current balancing, electromagnetic interference, envelope tracking, interconnected, two-phase three-level converter (2P3L).**

I. Introduction

RECENT 4G/5G wireless communication systems require small form-factor fast-transient supply modulator to improve the efficiency of the radio frequency power amplifiers [1]. The envelope tracking modulator is an attractive solution to provide a dynamically modulated supply [2]. Hybrid envelope tracking modulators widely reported [3]–[8] combine the switching converter and the linear amplifier in parallel. Usually, the switching converter provides the low-frequency current, and the linear amplifier provides the high-frequency current. However, the inefficient linear amplifier takes a portion of the total power amplifier current, and this makes the hybrid envelope tracking modulators suffers from low efficiency. Therefore, the individual [9] or paralleled [10], [11] switching converters increase the efficiency. Especially, multiphase (MP) or multilevel buck converters provide higher current and bandwidth. The work in [9] and [12] introduces single phase three-level (3L) buck converters, but single phase 3L buck converters generally provide the relatively limited current. Moreover, Kumar *et al*. in [12] also struggle for efficiency and speed performances. Thus, two-phase (2P) [13], 2P3L [14], 4P3L [15] buck converters, etc., are employed for higher current. However, they might have undesirable unbalanced inductor currents even with the current-sharing control [16]. In the worst case, one phase would become the load of the other. Thereby, some feedforward [17], [18] or feedback current-sharing controls [19]–[22] appeared for MP buck converters to ease this problem. However, the feedforward method highly relies on the accuracy of high-frequency reconstruction of each phase current and output current. Moreover, the feedback method highly depends on the accuracy of high-frequency sensing of each phase current. As either the current reconstruction or current sensing at high frequency is challenging, the additional current-balancing controls would significantly increase the control complexity.

Therefore, this article proposes a two-phase three-level (2P3L) buck converter with cross-connected flying capacitors (X-C_{FLY}). It not only suppresses the unbalanced inductor currents via alternately connecting the flying capacitors with the inductors of each phase, but also employs no extra component in the power stage. We organize the remaining of this article as follows. Section II describes the operation principle of the proposed converter. Section III derives the transfer function of the generalized multi-phase three-level (MP3L) buck converter with inter-connected C_{FLY} for analysis. Then, Section IV introduces the circuit implementation of the power stage and feedback control loop. Section V shows the measurement results. Finally, Section VI concludes this article.

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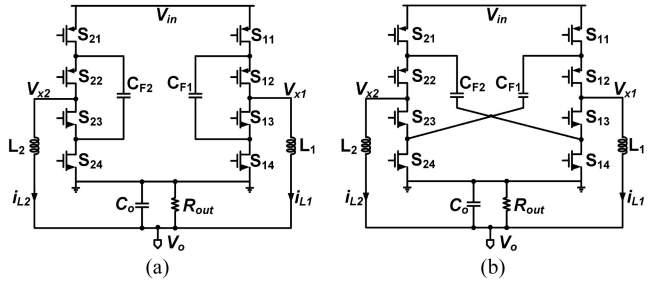

Fig. 1. (a) Conventional 2P3L buck converter. (b) Proposed 2P3L buck converter with X-C_{FLY}.

II. Operation Principle of the Proposed Converter

A. Converter Operation

Fig. 1 shows the conventional 2P3L buck converter, and the proposed 2P3L buck converter with X-C_{FLY}, respectively. To illustrate the operation principle, two operating states of the proposed 2P3L buck converter with X-C_{FLY} are shown in Fig. 2. For the sake of brevity and readability, we select the case of Fig. 2(a) for the detailed analysis. We can guarantee the operation states per cycle (same figure) by employing four interleaved pulsewidth modulation (PWM) signals D_1, D_2, D_{S1}, and D_{S2} to control the power switches S_{11} & S_{24}, S_{21} & S_{14}, S_{12} & S_{13}, S_{22} & S_{23}, respectively. Hence, the switching nodes V_{x1} and V_{x2} of the cross-connected topology follow $V_{\rm in} \rightarrow V_{CF1} \rightarrow V_{\rm in} \rightarrow V_{\rm in} - V_{CF2}$ and $V_{\rm in} \rightarrow V_{CF2} \rightarrow V_{\rm in} \rightarrow V_{\rm in} - V_{CF1}$, respectively. Obviously, the switching nodes V_{x1} and V_{x2} bring the interaction between two branches, and have similar amplitudes with those of the conventional 2P3L buck converter. Noticing that, D_1, and D_{S1} swap for the case in Fig. 2(b). Next, by applying the state-space average (SSA) method [23], i.e., the voltage-second balance law to the two inductors L_1 and L_2, there are

$$\begin{aligned}&(V_{\rm in} - V_o)(D_1 - 0.5) + (V_{CF1} - V_o)(1 - D_1)\\&+ (V_{in} - V_o)(D_{s1} - 0.5) + (V_{\rm in} - V_{CF2} - V_o)(1 - D_{s1}) = 0,\end{aligned} \tag{1}$$

$$\begin{aligned}&(V_{in} - V_o)(D_2 - 0.5) + (V_{CF2} - V_o)(1 - D_2) + (V_{in} - V_o)\\&(D_{s2} - 0.5) + (V_{\rm in} - V_{CF1} - V_o)(1 - D_{s2}) = 0.\end{aligned} \tag{2}$$

Here, we assume that good matching could make the mismatches of the two branches negligible. Hence, by setting the four duty cycles (the durations of zero voltage on V_{x1} or V_{x2}) $D_1 = D_2 = D_{S1} = D_{S2} = D$, and adding (1) and (2), the output voltage V_O will become as follows:

$$V_O = D \cdot V_{in}. \tag{3}$$

Obviously, it is the same as that of the conventional single-/multiphase two-/three-level buck converters. Then, bringing (3) into (1) or (2), will lead to the following:

$$V_{CF1} = V_{CF2} \tag{4}$$

illustrating that two flying capacitor voltages are ideally equal.

B. Inductor Current Balance

The proposed 2P3L buck converter with X-C_{FLY} is able to balance the inductor into one-twice of the output current automatically. Using the case in Fig. 2(b) for the detailed analysis, we discharge the flying capacitor C_{F1} by the first phase inductor current i_{L1} during state (i), but charge it with the second phase inductor current i_{L2} during state (iii). In a similar way, i_{L1} charges the flying capacitor C_{F2} during state (v), discharging with i_{L2} during state (vii). For example, if i_{L1} is larger than i_{L2}, the flying capacitor voltage V_{CF1} and V_{CF2} will decrease or increase, respectively, because of the unequal charged and discharged energy. Hence, in the next cycle the switching node V_{x1} (V_{CF1} in state (i) or $V_{in} - V_{CF2}$ in state (v)) decreases, while the switching node V_{x2} (V_{CF2} in state (vii) or $V_{in} - V_{CF1}$ in state (iii)) increases. This imposes i_{L1} to decrease and i_{L2} to increase accordingly. As a result, the two inductor currents i_{L1} and i_{L2} balance automatically. In brief, the constant capacitor average voltage in the steady state provides an inherent feedback loop to balance two inductor currents [24]–[26].

Next, we employ a large signal model to calculate quantitatively the inductor current mismatch ΔI_L. Considering again Fig. 2(b) for analysis, by applying KCL on the flying capacitor top plates and KVL in one period, we obtain four average equations as follows:

$$C_{F1}\frac{dV_{CF1}}{dt} = D_i \cdot I_{L1} - D_{iii} \cdot I_{L2}, \tag{5}$$

$$C_{F2}\frac{dV_{CF2}}{dt} = -D_v \cdot I_{L1} + D_{vii} \cdot I_{L2}, \tag{6}$$

$$\begin{aligned}L_1\frac{dI_{L1}}{dt} &= D_i \cdot V_{CF1} - V_O - R_{L1} \cdot I_{L1}\\&\quad + D_v \cdot (V_{in} - V_{CF2}) - V_O - R_{L1} \cdot I_{L1},\end{aligned} \tag{7}$$

$$\begin{aligned}L_2\frac{dI_{L2}}{dt} &= D_{iii} \cdot (V_{in} - V_{CF1}) - V_O - R_{L2} \cdot I_{L2}\\&\quad + D_{vii} \cdot V_{CF2} - V_O - R_{L2} \cdot I_{L2}\end{aligned} \tag{8}$$

where C_{F1} and C_{F2} are the flying capacitances, I_{L1} and I_{L2} are the average inductor currents for two phase inductors L_1 and L_2, respectively. V_{CF1} and V_{CF2} is the average flying capacitor voltage, D_i, D_{iii}, D_v, and D_{vii} are the duty ratios for state (i), (iii), (v), and (vii), respectively, $V_{\rm in}$ is the dc input voltage, R_{L1} and R_{L2} represent the inductor DCRs and other resistances, and V_O is the average output voltage. For simplicity, by assuming $L_1 = L_2 = L$, $R_{L1} = R_{L2} = R$, $C_{F1} = C_{F2} = C_F$, $D_i = D_{iii} = D_v = D_{vii} = D_x$, and subtracting (7) from (8), we can get the equation about the unbalanced current $\Delta I_L = I_{L1} - I_{L2}$ as

$$L\frac{d\Delta I_L}{dt} = 2D_x(V_{CF1} - V_{CF2}) - R \cdot \Delta I_L. \tag{9}$$

Differentiating (9) with respect to time and combining with (5) and (6) we obtain

$$\frac{d^2\Delta I_L}{dt^2} + \frac{R}{L}\frac{d\Delta I_L}{dt} + \frac{2{D_x}^2}{LC_F}\Delta I_L = 0. \tag{10}$$

Obviously, (10) is a second-order differential equation of ΔI_L and is in the form of damped harmonic oscillator [27]. Here, the

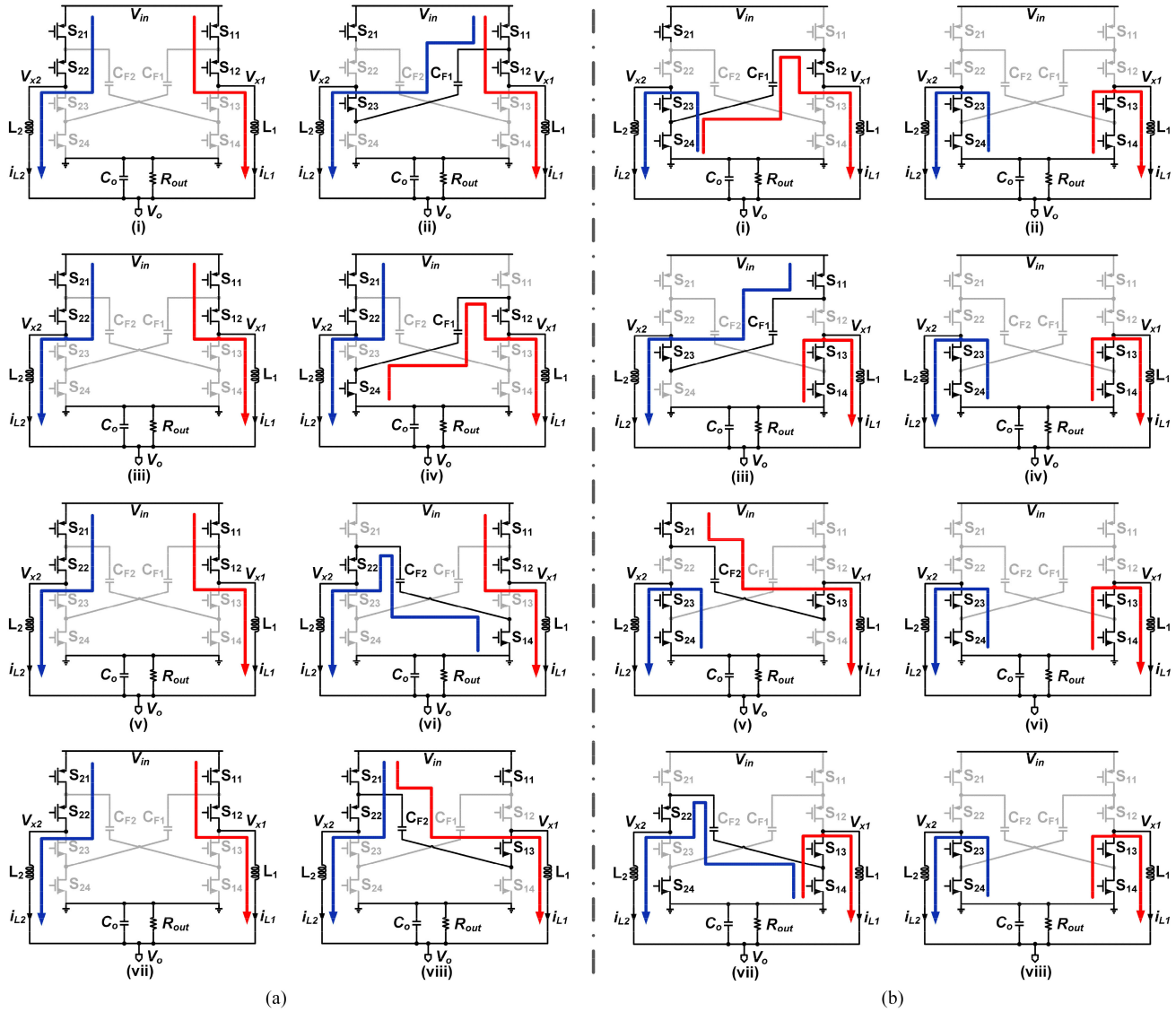

Fig. 2. Operating states of the proposed 2P3L buck converter with X-C_{FLY}: V_{x1} and V_{x2} fluctuate (a) between $V_{in}/2$ and V_{in}, and (b) between 0 and $V_{in}/2$.

damping factor is

$$\zeta = \frac{R}{2D_x}\sqrt{\frac{C_F}{2L}}. \tag{11}$$

Because $R \neq 0$, and $C_F \neq 0$, there is $\zeta \neq 0$, i.e., ΔI_L will damp to zero eventually.

In summary, the qualitative and quantitative analyses prove that the proposed converter ideally balances the unbalanced inductor currents in steady state in the specific duty cycle range, and potentially provides a feature of removing the challenging current reconstruction or current sensing at high frequency.

III. Generalized Multiphase Three-Level Buck Converter With Interconnected C_{FLY}

The proposed 2P3L buck converter with X-C_{FLY} can be extended into the MP3L buck converter with interconnected C_{FLY}, as illustrated in Fig. 3, by connecting the kth flying capacitor $C_{FLY\,k}$ in the kth phase to the nodes V_{ak} and $V_{b(k+1)}$, while the total number of phases is n. Here, we connect the flying

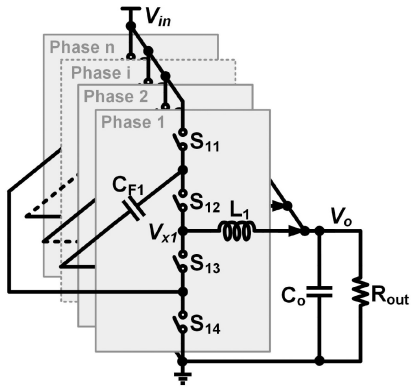

Fig. 3. Multiphase three-level buck converter with interconnected C_{FLY}.

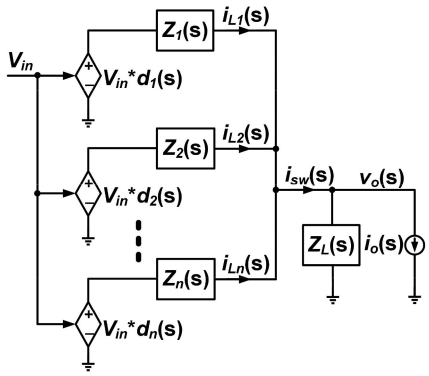

Fig. 4. s-domain model of MP3L buck converter with interconnected $C_{\rm FLY}$.

capacitor of the last phase between the last and the first phases, to form a loop. D_k and D_{Sk} are used to control the switch pairs of S_{k1} & $S_{(k+1)4}$ and S_{k2} & S_{k3}, to make the converter functional. Besides, the pulse signals have the same duty cycle. MP3L buck converter with interconnected $C_{\rm FLY}$ has the similar switching nodes V_{xk} as the 2P3L buck converter with X-$C_{\rm FLY}$, i.e., each node V_{xk} follows $V_{\rm in} \rightarrow V_{CFk} \rightarrow V_{in} \rightarrow V_{in}$-$V_{CF(k\text{-}1)}$ or follows $V_{CF{\rm k}} \rightarrow 0 \rightarrow V_{\rm in}$-$V_{CF(k\text{-}1)} \rightarrow 0$. Similarly, by applying the SSA method, we can deduce the equivalent SSA values of the node voltage V_{xk}. Taking $V_{\rm in} \rightarrow V_{CFk} \rightarrow V_{\rm in} \rightarrow V_{\rm in}$-$V_{CF(k\text{-}1)}$ as the example, we can obtain the following expression:

$$V_{xk} = (0.5 - D_k)\, V_{\rm in} + (1 - D_k)\, V_{CFk} + (0.5 - Ds_k)\, V_{\rm in} + (1 - Ds_k)\left(V_{\rm in} - V_{CF(k-1)}\right) \tag{12}$$

where $k = 1, 2, \ldots,$ or, n. A special case is when $k = 1$, $V_{CF0} = V_{CFn}$.

Taking the same assumption of the duty cycle in last section, the equivalent SSA values of the node voltage V_{xk} will simplify to

$$V_{xk|k=1,\ldots,n} = D_k \cdot V_{\rm in}. \tag{13}$$

Obviously, the generalized MP3L buck converter with interconnected $C_{\rm FLY}$ have the same SSA values of V_{xk} as those of the conventional MP2L/3L buck converter. In the steady state, the input voltage and flying capacitor voltage are approximately constant. Thus, we can obtain the s-domain model of the generalized MP3L buck converter with inter-connected $C_{\rm FLY}$ as in Fig. 4. In the s-domain

$$Z_k(s) = sL_k + {\rm DCR}_{Lk}, \tag{14}$$

$$Z_L(s) = \left(\frac{1}{sC_o} + {\rm ESR}_{Co}\right) \| R_{\rm out} \tag{15}$$

where ${\rm ESR}_{Co}$ is the equivalent-series-resistance (ESR) of the output capacitor C_O, ${\rm DCR}_{Lk}$ is the direct-current-resistance (DCR) of the inductor L_k, $R_{\rm out}$ is the load resistor.

For buck converter, the inductor currents i_{Lk}, and the output voltage v_o are usually the small-signal state quantities of interest. The open-loop transfer functions are defined at the bottom of the next page, where d_k ($k = 1, \ldots, n$) is the duty cycle perturbation and i_O(s) is the load current perturbation.

TABLE I
OPEN-LOOP TRANSFER FUNCTIONS

$$den = Z_k(\mathrm{s})^n + nZ_L(\mathrm{s})Z_k(\mathrm{s})^{n-1}$$

$$-Z_o = \frac{Z_L(\mathrm{s})Z_k(\mathrm{s})^{n-1}}{den}$$

$$G_{vd_k} = V_{in}\frac{Z_L(\mathrm{s})Z_k(\mathrm{s})^{n-1}}{den}$$

$$G_{i_{Lk}d_k} = V_{in}\frac{Z_k(\mathrm{s})^{n-1} + (n-1)Z_L(\mathrm{s})Z_k(\mathrm{s})^{n-2}}{den}$$

$$G_{\substack{i_{Lm}d_k \\ m\neq k}} = -V_{in}\frac{Z_L(\mathrm{s})Z_k(\mathrm{s})^{n-2}}{den}$$

$$G_{i_{Lk}i_o} = \frac{Z_L(\mathrm{s})}{Z_k(\mathrm{s}) + n\cdot Z_L(\mathrm{s})}$$

We obtain the open-loop transfer functions, derived as listed in Table I, by applying Kirchhoff's voltage/current law to the current loops and voltage nodes of the s-domain model and assuming that only one corresponding perturbation input exists with a negligible phase mismatch.

IV. CIRCUIT IMPLEMENTATION OF THE PROPOSED CONVERTER

Fig. 5 shows the circuit implementation of the proposed converter, including the power stage and feedback control loop.

A. Power Stage Design

According to the deduced transfer functions $G_{i_{Lk}i_o}$ in last section, we obtain the current transfer function $G_{i_{sw}i_o}$, which determines the ability of the total inductor current i_{sw} to track the load current i_o, for inductance selection, as follows:

$$G_{i_{sw}i_o} = \sum_{k=1}^{n} G_{i_{Lk}i_o} = \frac{Z_L(s)}{Z_k(s)/n + Z_L(s)}. \tag{16}$$

From this equation, the corner frequency becomes

$$f_{OL} = \frac{1}{2\pi\sqrt{(L_k/n)\, C_o}}. \tag{17}$$

Therefore, for $n = 2$ and $C_O = 1$ nF, we calculate L_1 and L_2 as 500 nH for an expected corner frequency f_{OL} around 10 MHz. Meanwhile, a switching frequency is set as 40 MHz. The input voltage $V_{\rm in}$ is set as 1.8 V aiming for the recent PA [28]. The power stage employs 1.8 V I/O devices in a 65 nm CMOS process rather than 1.2 V core devices as the power transistors. This is because the voltage stresses of S_{12}, S_{13}, S_{22} and S_{23} equal to the input voltage $V_{\rm in}$ and the voltage stresses of S_{11} and S_{21} in the start-up phase equal to V_{in}. Besides, we place two power switches S_{13} and S_{23} in deep N-wells with a voltage potential of 1.8 V, for removing the source-body voltage stress.

B. Output Control Loop Design

Here, the output control loop uses a voltage mode compensator with no inductor current information. This helps to explore the current balancing feature of the proposed X-connected

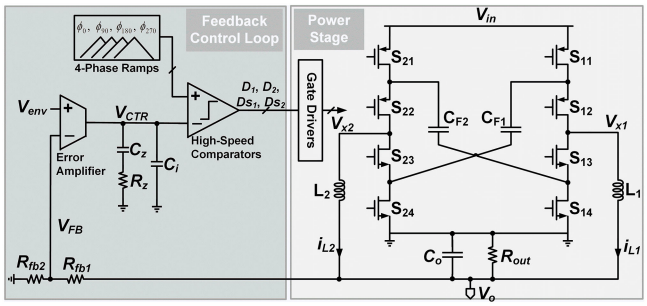

Fig. 5. Circuit implementation of the proposed converter.

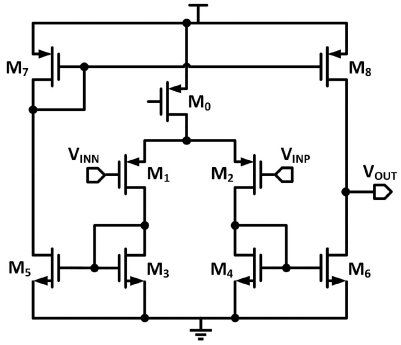

Fig. 6. Current mirrored operational transconductance amplifier.

topology. The feedback resistors R_{fb1} and R_{fb2} sense the output voltage with a feedback coefficient of 0.5. Then, the integrator, being composed of an error amplifier, two compensation capacitors C_z and C_i and one compensation resistor R_z, generates the control voltage V_{CTRL}. Then, we compare V_{CTRL} with four ramp waves by the high-speed comparators to generate four interleaving PWM signals, which accordingly control the corresponding power switches.

We obtain the error amplifier from Fig. 6 through a conventional current mirror operational transconductance amplifier [29]. The channel lengths of M_3–M_8 are set to 2 μm and the tail current is set to 4 μA. The error amplifier achieves a high gain of about 50 dB, and provides an appropriate output impendence R_{OTA} of about 500 kΩ as the first pole.

The high-speed comparator shown in Fig. 7 is achieved by a two stage push–pull comparator [30]. Three transistors M_{D1}, M_{D2}, and M_{D3}, with the body connected to their drain, act as the diodes to limit the voltage range of node B. When $V_{INP} > V_{INN}$, the voltage at node A goes up and the voltage at node

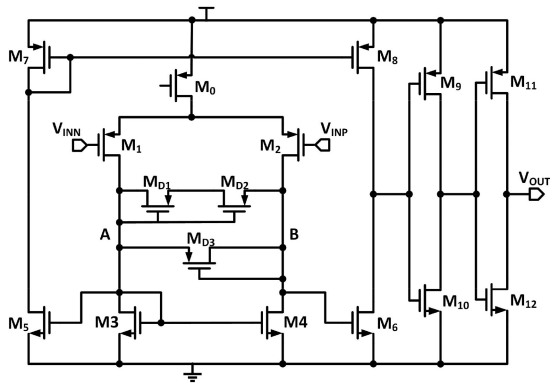

Fig. 7. Two-stage push-pull high-speed comparator.

B drops. Once the voltage difference between nodes A and B is large enough, the parasitic diode M_{D3} turns on and clamps the voltage of node B to a fixed value. Similarly, when $V_{INP} < V_{INN}$, the voltage at node A drops and the voltage at node B goes up. Once the voltage difference between nodes B and A is larger than the built-in potential of the two series parasitic diodes in M_{D1} and M_{D2}, they turn ON and clamp node B to another fixed value. As a result, the speed of the comparator improves with the limitation of the voltage range of node B. The maximum discharging slew rate of node V_{OUT} can be very high even though the tail current is small (that is why we use two series diodes to limit the upper voltage of node B). Two inverters follow this comparator to avoid any unsure output amplitude in case. With the reasonably designed sizes, a tail current of 4 μA and a load MOSFET capacitor of 1.2/0.26 μm, the two-stage push-pull comparator achieves a high speed of around 2.5 ns.

Fig. 8 shows the loop gain and phase of the proposed converter obtained by the co-simulation of periodic steady state and periodic stability. The proposed converter has a dc gain of about 45 dB, a bandwidth of about 9 MHz and a phase margin of about 45°. These reveals that the proposed converter with the above-mentioned parameters is stable.

V. Measurement Results

The proposed 2P3L buck converter with X-C_{FLY} [31], fabricated in 65nm GP 1P9M CMOS with I/O devices, has its chip photograph exhibited in Fig. 9 with a chip area close to 1.88 mm $\times$ 1.55 mm $\approx$ 2.95 mm^2. We use the common-centroid layout to eliminate the mismatch between the two phases, with the N-cap

$$
\begin{array}{cccccc}
 & & v_o & i_{L1} & \cdots & i_{Ln} \\
d_1: & G_{vd_1} = \frac{v_o}{d_1}\Big|_{\substack{d_{k,k\neq 1}=0 \\ i_o=0}} & G_{i_{L1}d_1} = \frac{i_{L1}}{d_1}\Big|_{\substack{d_{k,k\neq 1}=0 \\ i_o=0}} & \cdots & G_{i_{Ln}d_1} = \frac{i_{Ln}}{d_1}\Big|_{\substack{d_{k,k\neq 1}=0 \\ i_o=0}} \\
\vdots & \vdots & \vdots & \ddots & \vdots & \\
d_n: & G_{vd_n} = \frac{v_o}{d_n}\Big|_{\substack{d_{k,k\neq n}=0 \\ i_o=0}} & G_{i_{L1}d_n} = \frac{i_{L1}}{d_n}\Big|_{\substack{d_{k,k\neq n}=0 \\ i_o=0}} & \cdots & G_{i_{Ln}d_n} = \frac{i_{Ln}}{d_n}\Big|_{\substack{d_{k,k\neq n}=0 \\ i_o=0}} \\
i_o: & -Z_o = \frac{v_o}{i_o}\Big|_{d_k=0} & G_{i_{L1}i_o} = \frac{i_{L1}}{i_o}\Big|_{d_k=0} & \cdots & G_{i_{Ln}i_o} = \frac{i_{Ln}}{i_o}\Big|_{d_k=0}
\end{array}
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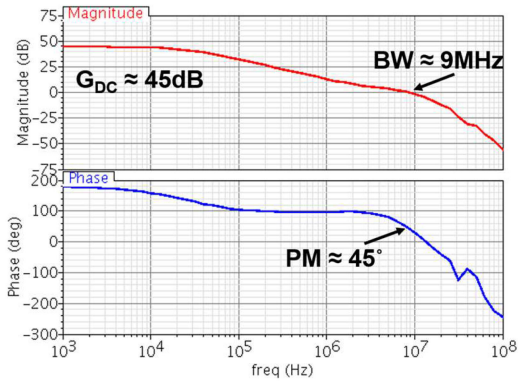

Fig. 8. Loop gain and phase of the proposed converter.

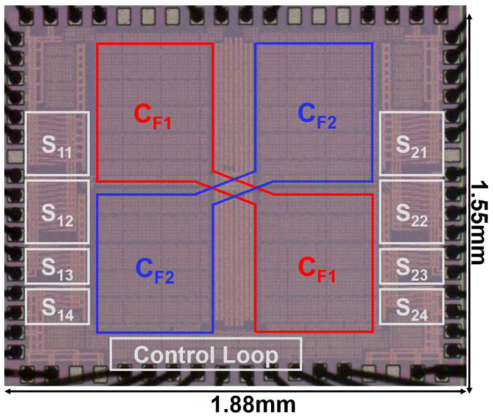

Fig. 9. Chip photograph of the proposed converter.

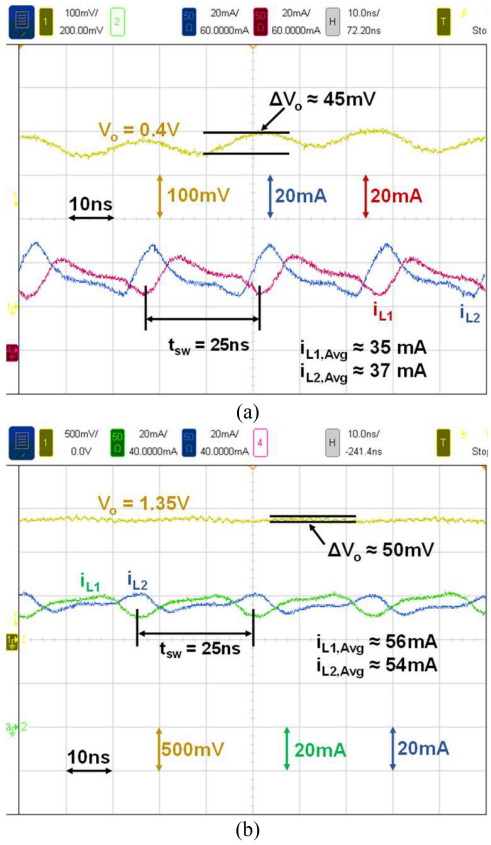

Fig. 10. Output voltage and inductor currents of the proposed converter for the output voltage of (a) 0.4 V, (b) 1.35 V.

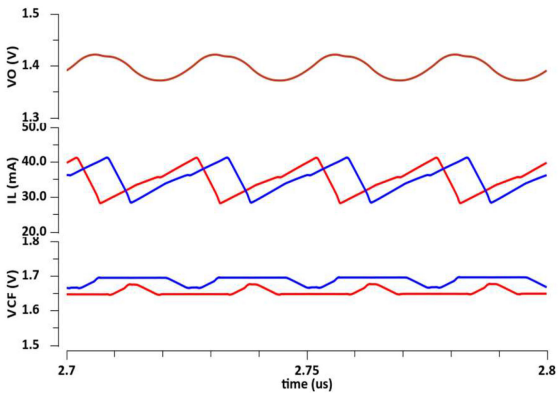

Fig. 11. Flying capacitor voltages for the output voltage of 1.4 V.

and MIM capacitors stacked to save silicon area. Besides, the output capacitor with a capacitance of 1 nF and an ESR of 10 mΩ, and the inductors with an inductance of 500 nH and a DCR of 1.15 mΩ are chosen. We assume the load PA requires a power of less than 0.2 W under a constant supply of 1.8 V [28], thus we can employ a cement resistor as the load to model the PA.

Fig. 10 plots the steady-state performance of the proposed converter for the output voltage of 0.4 and 1.35 V, with a switching frequency of 40 MHz. For the output voltage of 0.4 V with a load current around 72 mA, the output ripple will be close to 45 mV with the inductor currents balanced around 36 mA. For the output voltage of 1.35 V with a load current of 110 mA, the output ripple is close to 50 mV with the inductor currents balanced around 55 mA. Similar with [19], [21], [22], we use the unbalanced current ΔI_L, which is defined as the difference of two average inductor currents ($\Delta I_L = |I_{L1} - I_{L2}|$), to evaluate the balance capacity. For both cases, the unbalanced average currents are less than 5 mA, which might result from the mismatches caused by the process variations of the bond-wire inductors, on-chip and PCB power traces. Because the flying capacitor voltage is an important concern but the flying capacitors are on-chip and can hardly be measured, Fig. 11 shows the simulation result for the output voltage of 1.4 V with a load current of 70 mA. The flying capacitor voltage around 1.6 V rather than $V_{in}/2$ increases the voltage stress of power switches. Thus, to tolerate the voltage stress, we use 1.8 V I/O devices rather than core devices in a standard 65 nm process.

Fig. 12 displays the simulated inductor current mismatches of the proposed and conventional converters with inductance or duty cycle mismatches, including 100 nH inductance mismatch, or 0.02 duty cycle mismatch for the output voltage of around 1.5 V with a load current of 150 mA. The simulation results illustrate that the proposed converter only has the unbalanced average current not higher than 2 mA under inductance mismatch and close to 6 mA under the duty cycle mismatch, respectively.

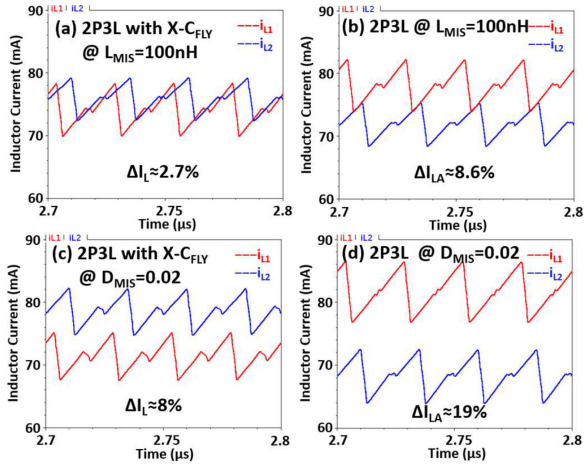

Fig. 12. Unbalanced current for the proposed and conventional 2P3L converters with 100-nH inductance mismatch, or 0.02 duty cycle mismatch.

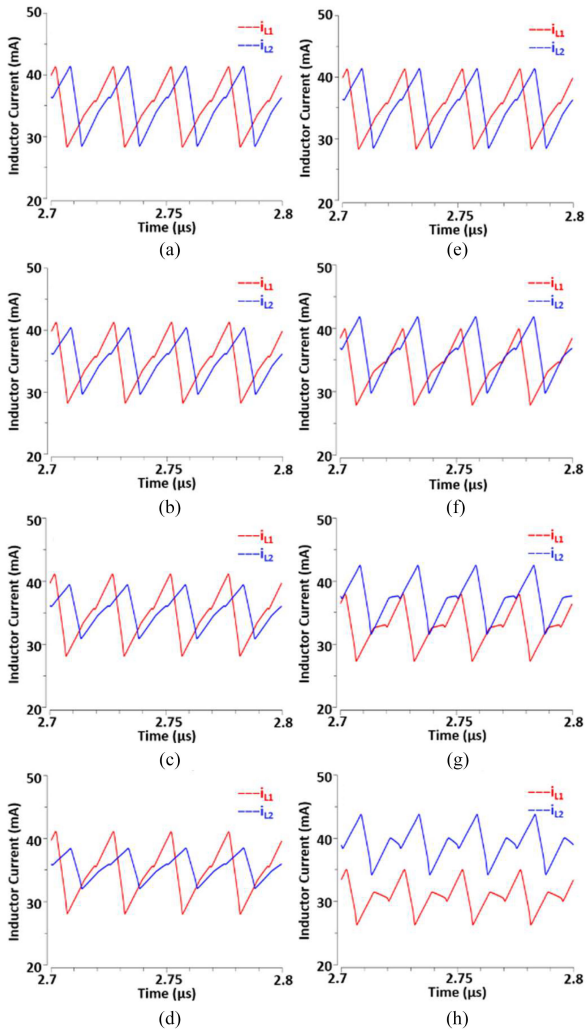

Fig. 13. Unbalanced current for the proposed converter with different degree of mismatch.

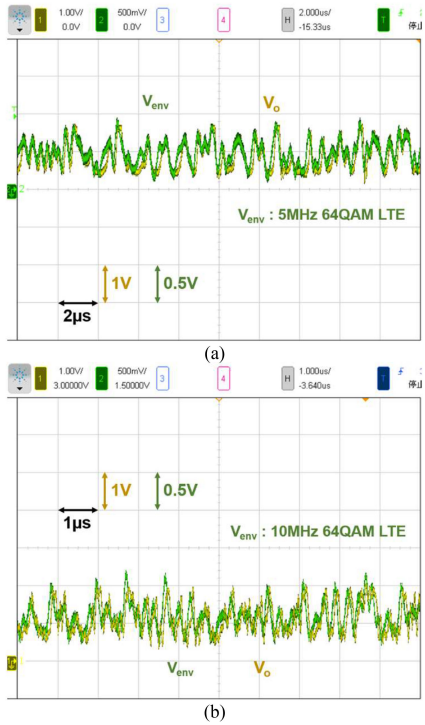

Fig. 14. Response of the proposed converter with (a) 5 MHz, (b) 10 MHz 64QAM LTE envelope signal.

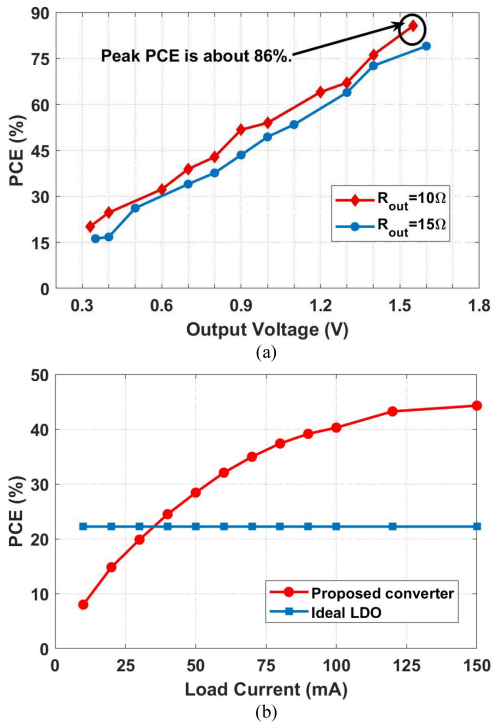

Fig. 15. (a) PCE of the proposed converter with the fixed load resistances versus the output voltage. (b) PCE versus the load current at $V_O = 0.4$ V.

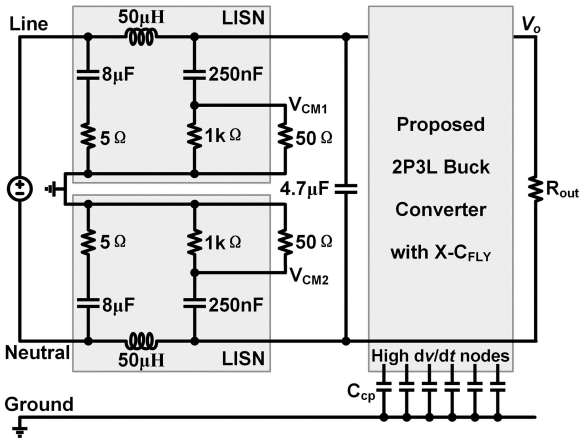

Fig. 16. Common mode noise simulation setup.

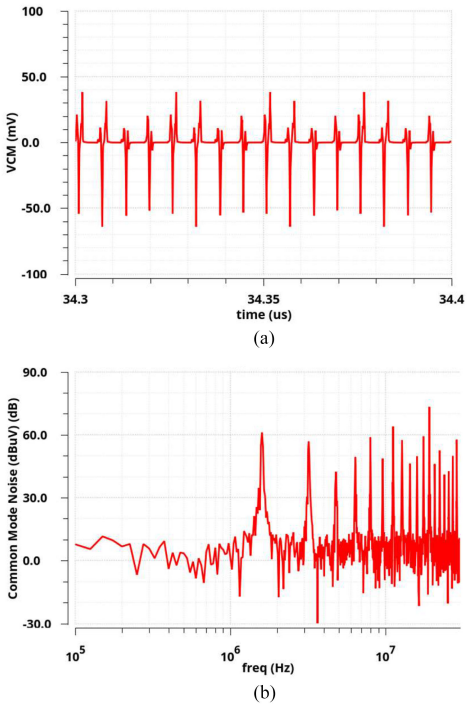

Fig. 17. Common mode noise in (a) time or (b) frequency domain.

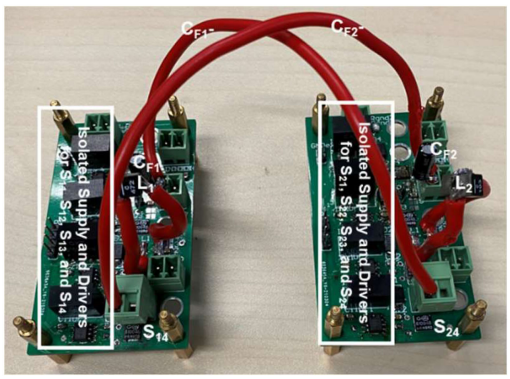

Fig. 18. Prototype with discrete components.

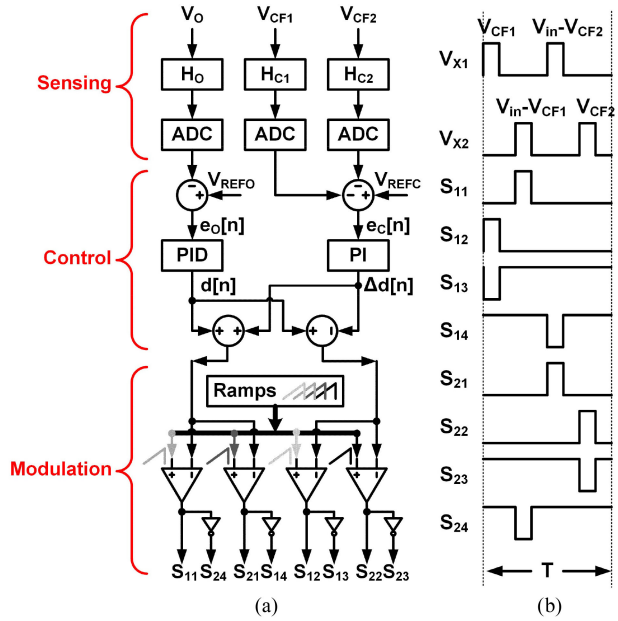

Fig. 19. (a) Digital control strategy and (b) gate signals for the discrete prototype with n-type FETs.

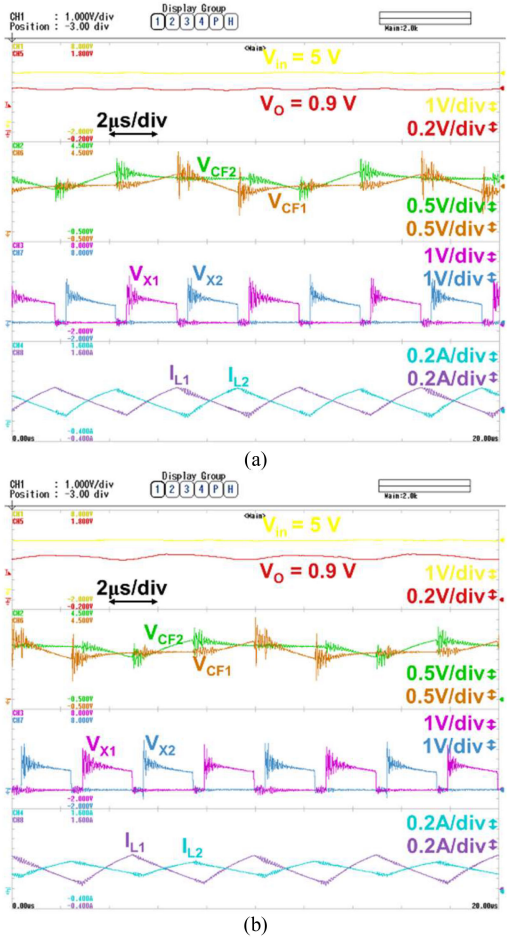

Fig. 20. Steady-state waveforms of the discrete prototype with two configurations (a) $L_1 = L_2 = 4.7\ \mu$H, and (b) $L_1 = 4.7\ \mu$H, $L_2 = 10\ \mu$H.

When compared with the conventional 2P3L buck converter, we reduce the unbalanced currents under various considerate mismatches by no less than 57.1%.

Furthermore, to explore the influence different degree of mismatch on the proposed converter, Fig. 13 shows the performance of the proposed converter with 100-, 250-, 500 nH inductance mismatch, or 0.02, 0.05, 0.1 duty cycle mismatch for the output voltage of around 1.4 V with a load current of 70 mA. It can be seen that the duty cycle mismatch is positively related to the unbalanced current, while the inductance mismatch (even serious mismatch) rarely affects the current balancing and only changes the inductor current ripple. The feature can be theoretically deduced as in Appendix.

Then, we employ the 5 or 10 MHz 64QAM LTE signal generated in MATLAB as the envelope reference and a resistive load to model the PA. Fig. 14 shows the response of the proposed converter with the 5- or 10 MHz 64QAM LTE signals. As seen, the proposed converter tracks the 5/10 MHz 64QAM LTE signal well and only a small lag of tens of nanoseconds exists. The amplitude ratio of the envelope $V_{\rm env}$ and the output V_O basically equals to the feedback coefficient of $\beta = 0.5$. The tracking error ($|\beta \cdot V_O - V_{\rm env}|/V_{\rm env}$) [4] for 5 MHz 64QAM LTE signal is about 5.6%.

The power conversion efficiency (PCE) is obtained by sweeping the value of the dc reference from 0.15 to 0.8 V, i.e., $V_O =$ 0.3–1.6 V, and shown in Fig. 15(a). The proposed converter achieves a peak PCE of slightly less than 86%. The PCE decreases with the output voltage because the output current and output power also decrease with the output voltage. Besides, this converter provides much higher efficiency than an LDO at low voltages with high output current, as shown in Fig. 15(b), where the proposed converter provides higher PCEs than an ideal LDO when the load current is larger than 35 mA.

Though the low input voltage limits each node's dv, the high switching frequency of 40 MHz might cause small dt, meaning the dv/dt might cause unignorable common mode noise. To explore the common mode noise, we configure the simulation setup as shown in Fig. 16. In details, we set the converter ground as the neutral and insert two line impedance stabilization networks for MIL-STD 461E standard to get the time/voltage domain common mode noise $\rm V_{CM} = (V_{CM1} + V_{CM2})/2$ [32]. Because common mode noise is caused by the parasitic capacitance between the high dv/dt node and the earth ground "Ground" [33], [34], we insert some capacitors ($\rm C_{cp}$) to analogue them. The parasitic capacitances are difficult to be measured directly [33]. Luckily, a converter's output power is basically positively related to its area S and the capacitance is defined as $\varepsilon S/(4k\pi d)$. So, we could assume that the parasitic capacitance is positively related to the output power. By scaling the power and the capacitance in the specific example [35], the parasitic capacitance in our converter is less than 0.1 pF. For an enough margin, we set $\rm C_{cp}$ as 0.25 pF. Besides, the 50 Ω resistor is used to analogue the impendence of Spectrum Analyzer [35]. As shown in Fig. 17(a), the converter gives the common mode noise with a peak magnitude of about 70 mV. By applying the discrete Fourier transform, the common mode noise in the frequency domain is got as in Fig. 17(b). In the frequency range of 100 KHz to 30 MHz, the peak common mode noise is no more than 75 dBμV, which is ought to be acceptable [36], [37] and meets the commercial standard CISPR (Comite International Special des Perturbations Radioelectrique) 22 Class A(QP) [38].

Table II shows the comparisons of the proposed converter with the state-of-the-art $\geq$ 10 MHz converters. This work without current-balancing control achieves a smaller unbalanced current of 5 mA for a load current of 110 mA. It also achieves a high peak PCE of 86%, which is comparable to that of [13] and [14]. This work has a high bandwidth close to 10 MHz, and we can potentially enhance it by utilizing a hysteresis controller or setting in parallel a Class-AB amplifier in the future. Two-phase and three-level techniques allow this work to obtain a small ripple of 50 mV. This value is smaller than that in [14] due to less load current. Similar to [14] and [15], we do not regulate the flying capacitor voltages for reducing the control complexity.

The absence of the flying capacitor voltage regulation in the controller of the aforesaid integrated prototype might not gain the full potential of the proposed converter. In fact, extra inner loop could be inserted at the outer output voltage loop to regulate the flying capacitors, to guarantee the voltage stress and to eliminate the subharmonic. For illustration, we built another prototype as shown in Fig. 18 by using the discrete devices, and design a digital control strategy as shown in Fig. 19(a) by using DSP. The strategy has two voltage loops, where the outer loop regulates the output voltage and the inner loop controls the flying capacitor voltages [39]–[43], to generate four pair complementary gate signals as shown in Fig. 19(b) for n-type GaN FETs. Because the flying capacitor voltages need to drift for inherent current balancing [27], the strategy controls the relationship of two flying capacitor voltages rather than the individual values. In this prototype, we set $\rm V_{in} = 5$ V, $\rm C_{F1} = C_{F2} = 11$ μF, $\rm C_o = 2$ μF, $\rm R_{out} = 1$ Ω, $\rm V_o = 0.9$ V, and $F_{\rm SW} = 100$ KHz. Fig. 20 shows the steady-state waveforms of the discrete prototype with two configurations (a) $\rm L_1 = L_2 =$ 4.7 μH, and (b) $\rm L_1 = 4.7$ μH, $\rm L_2 = 10$ μH. The steady-state waveforms of the discrete prototype are shown in Fig. 20. In each configuration, the flying capacitor voltages are around half input voltage, and the average inductor currents are the same, achieving the current balancing. Also, the inductance mismatch affects the inductor current ripple but rarely causes unbalanced current, meeting with the theoretical analysis in the Appendix.

Table III compares the proposed converter with the state-of-the-art converters with the current sharing control. We can see the feedforward control [17], [18] achieves the near-optimum current balancing for $<$ 1 MHz switching frequency, and the feedback control [19], [21], [22] achieves quite good current balancing with careful design. The proposed converter achieves the comparable current balancing with the current-balancing control but requires no current sensing.

VI. Conclusion

This article proposed a 2P3L buck converter with X-$\rm C_{FLY}$, which suppressed the unbalanced inductor currents via alternately connecting the flying capacitors with the inductors.

TABLE II
COMPARISON OF PROPOSED CONVERTER WITH THE STATE-OF-THE-ART $\geq$ 10 MHZ CONVERTERS

Reference	[9]	[12]	[13]	[14]	[15]	[16]	This work
CMOS Tech.	65 nm (I/O devices)	22 nm	180 nm	180 nm	130 nm	350 nm	65 nm (I/O devices)
Area (mm^2)	1.85×1.25	1.8×1	3.1×2.1	2.15×1.99	2.5×2	1.78×1.74	1.88×1.55
Topology	3L Buck	3L Buck	2P2L Buck with slew rate enhancer	2P3L Buck	4P3L Buck	2P2L Buck + Class AB	2P3L Buck with X-C_{FLY}
f_{SW}	50 MHz	250 MHz	40 MHz	29 MHz	50 – 200 MHz	10 MHz	40 MHz
C_{FLY}	5 nF	5 nF	N/A	Unknown	4.5 nF×4	N/A	~2.4 nF×2
C_O	10 nF	5 nF	Unknown	1 nF	10 nF	100 pF	1 nF
V_{in}	5 V	1.5 V	3.3 V	5 V	2.4 V	3.3 V	1.8 V
V_O	0.6 – 4.2 V	0.4 – 1.2 V	0.5 – 2.3 V	1 – 4 V	0.4 – 1.4 V	0.4 – 2.8 V	0.3 – 1.6 V
Max. I_{OUT}	714 mA	208 mA	870 mA	625 mA	416 mA	600 mA	210 mA
V_{RIPPLE} @ I_{OUT}	35 mV @ 70 mA	31 mV @ 10 mA	N/M	75 mV @ 380 mA	50 mV @ 100 mA	40 mV @ 100 mA	50 mV @ 110 mA
Peak PCE	90%	72%	85.8%	88.6%	77%	89%	~86%
Bandwidth	10MHz	N/A	10MHz	20MHz	N/A	4MHz	10MHz
V_{CF} Regulation	Yes	Yes	N/A	No*	No	N/A	No
Current-Balancing Control	N/A	N/A	Needed	Needed	None	Needed	Not Needed
ΔI_L @ I_{OUT}	N/A	N/A	Unknown	Unknown	Unknown	180 mA @ 400 mA	5 mA @ 110 mA

Note: *Duty cycle calibrator exists.

TABLE III
COMPARISON OF PROPOSED CONVERTER WITH THE STATE-OF-THE-ART CONVERTERS WITH CURRENT BALANCING CONTROL

Reference	[16]	[17]	[18]	[19]	[21]	[22]	This work	
CMOS Tech.	350 nm	Discrete	Discrete	180 nm	250 nm	Discrete	65 nm (I/O devices)	Discrete
Topology	2P2L Buck + Class AB	3P2L Buck	4P2L Buck	4P2L Buck	2P2L Buck	4P2L Buck-Boost	2P3L Buck with X-C_{FLY}	
Current-Balancing Control	Feedback	Feedforward	Feedforward	Feedback	Feedback	Feedback	Not Needed	
Sensing	Inductor Currents	DC-Link Current	DC-Link Current	Inductor Currents	Inductor Currents	Inductor Currents	Flying Capacitor Voltages	
C_O	100 pF	1500 µF	N/A	10 µF	47 µF	150 µF x 8	1 nF	2 µF
f_{SW}	10 MHz	5 KHz	200 KHz*	3 – 9.5 MHz	600 KHz	250 KHz	40 MHz	100 KHz
ΔI_L @ I_{OUT} @ V_{in} @ V_O	180 mA @ 400 mA @ 3.3 V @ 1.6 V	~ 0 @ 1 A @ N/A @ 24 V	~ 0 * @ 100 A @ N/A @ N/A	36 mA @ 1 A @ 2 V @ 0.8 V	14 mA # @ 700 mA @ 3.3 V @ 1.32 V	< 200 mA * @ 18 A @ 15 V @ 12 V	5 mA @ 110 mA @ 1.8 V @ 1.35 V	< 50 mA @ 0.9 A @ 5 V @ 0.9 V

Note: ∗means that data is read from figures.
#means simulation results.

Besides, we deduced the transfer function of the generalized MP3L buck converter with interconnected C_{FLY} for stability analysis and component selections. We built two prototypes of the proposed 2P3L buck converters with X-C_{FLY} are built. Fabricated and validated in a 65nm GP 1P9M CMOS technology, the integrated version reached a low unbalanced current close to 5 mA and a low output ripple of 50 mV for a load current around 110 mA, and a high peak efficiency of 86%. On the other hand, the discrete version with a digital control almost has no unbalanced current for a load current of 0.9 A even under unequal inductances, and its flying capacitor voltages are basically equal to half input voltage.

APPENDIX

We analyze the influence of inductance mismatch on current balancing by still employing the large signal model as (5)–(8) in Section II-B to quantitatively calculate the unbalanced current ΔI_L. By considering an inductor mismatch ΔL between L_1 and L_2 ($L_2 = L_1 + \Delta L$), and subtracting (7) from (8), we get the equation about the unbalanced current ΔI_L as follows:

$$L\frac{d\Delta I_L}{dt} + \Delta L\frac{dI_{L2}}{dt} = 2D_x\left(V_{CF1} - V_{CF2}\right) - R\cdot\Delta I_L. \tag{A1}$$

Differentiating (A1) with respect to time and combining with (5) and (6) we obtain the following:

$$\frac{d^2\Delta I_L}{dt^2}+\frac{R}{L}\frac{d\Delta I_L}{dt}+\frac{2{D_x}^2}{LC_F}\Delta I_L=-\Delta L\frac{d^2I_{L2}}{dt^2}. \quad \text{(A2)}$$

In the steady state and continuous current mode, the inductor current shape of inductor-based converter is triangle. Hence, the second derivative term of the inductor current is zero. Thus, (A2) is the same with the original (10), which gives a nonzero damping factor, ΔI_L will damp to zero eventually. So, the proposed converter operating in continuous current mode seems to have no balancing limit even under the serious mismatch of inductors.

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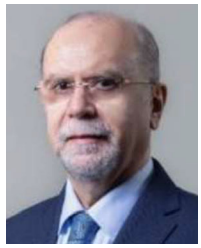

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