# Letters

# A Digital Signal Processing Based Detection Circuit for Short-Circuit Protection of SiC MOSFET

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***Abstract*—A short-circuit detection (SCD) circuit is proposed for power electronics systems that use silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs). The proposed SCD circuit incorporates a digital circuit for processing the voltage induced at the parasitic inductance of the source of SiC MOSFET to obtain an improved stable turn-OFF operation of the SiC MOSFET under SC condition. Compared with that of the conventional analog signal processing based SCD circuits, the proposed circuit has the advantages of having a turn-OFF operation which is robust to process, voltage, and temperature variations, being fully integrated without the use of external components and ease of design. The proposed circuit was implemented in a 350-nm Bipolar-CMOS-DMOS process. For functional verification, an SC test board integrating the proposed SCD circuit was developed. Experimental result validates that the proposed SCD circuit effectively functions under SC condition.**

***Index Terms*—Gate driver, parasitic inductance, short-circuit detection (SCD), silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET).**

## I. Introduction

SI-BASED power semiconductor devices, particularly silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs), have advantages over Si insulated gate bipolar transistors (IGBT) such as low switching loss, short reverse recovery time, low ON-resistance ($R_{ON}$) dependence on temperature, high current density, excellent thermal conductivity, and heat dissipation characteristics. Hence, a power system that uses SiC MOSFETs allows high-speed operation, and might be miniaturized, because the number of inductors and capacitors used in the system can be reduced. In addition, a power system using SiC MOSFET can be operated stably at a high temperature, and the cooling system can be lightweight [1].

However, a power system using an SiC MOSFET could be short-circuited by an erroneous signal generated by the control unit that operates the power system, or fault under load in the power system. During an SC operation, the drain current is significantly high because an SiC MOSFET has a high current density per unit area. The drain current in an SC can generate an enormous amount of heat in the channel junction, rapidly destroying the device. The time during which a device can stably tolerate an SC state without being destroyed is called SC immunity time. The SC immunity time of an SiC MOSFET is approximately 3 $\mu$s [2]. Therefore, a power system using an SiC MOSFET device requires an SC detection (SCD) circuit that can quickly detect an SC without affecting normal operation.

There are several types of SCD circuits that are often used in power systems. The first type is a gate-source voltage $V_{GS}$ sensing circuit for SCD that utilizes the presence of a Miller plateau region in the normal state and the SC state [3]. The second type is a desaturation detection circuit that detects an SC state using the characteristic that the drain-source $V_{DS}$ voltage is retained without dropping to a low-voltage during an SC state [4]. The third type is a circuit that senses the voltage induced by the parasitic inductance that exists in the source/emitter due to the drain/collector current of SiC MOSFET/IGBT, which is increased in an SC state [5]–[7]. Furthermore, by mixing or advancing the aforementioned several types of SCD circuits, new SCD circuits have been reported to improve the performance of the SCD [8], [9].

The $V_{GS}$ sensing circuit does not require an external circuit. However, it has a difficulty detecting an SC in high-speed operation applications, where a high gate current is used because of noise generation in the Miller plateau region by the parasitic elements in the gate-source loop. The desaturation detection circuit is applicable to high-speed operation applications, but its realization requires external devices and thus the power module size becomes large. The circuit that detects the voltage induced by the parasitic inductance can directly detect the drain current and detect an SC accurately and rapidly. However, it requires an additional circuit to distinguish between the normal and SC

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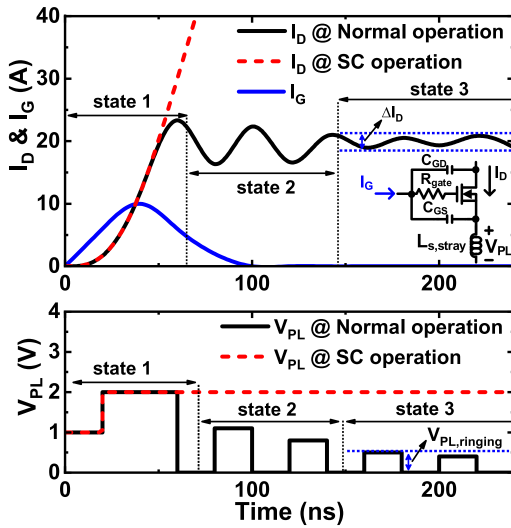


Fig. 1. $I_G$, $I_D$, and $V_{\mathrm{PL}}$ when an SiC MOSFET device is operating under normal condition and short-circuit condition.

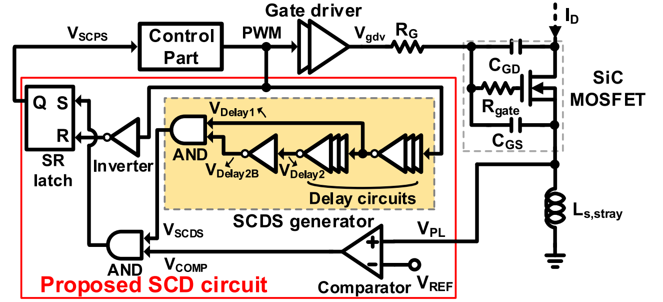


Fig. 2. Proposed short-circuit detection circuit.

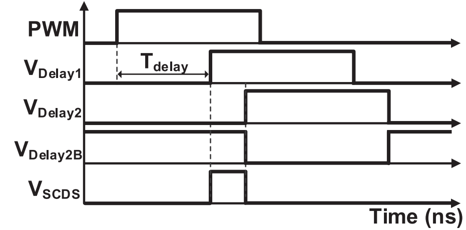


Fig. 3. Timing diagram of the input signal, the internal output signal, and the final output signal of the SCDS generator.

state because it senses the source of SiC MOSFET with multiple noise sources. The conventional circuit, which detects an SC using comparators and analog integrators, uses a large silicon chip area to realize an analog integrator, and the performance of the integrator circuit is dependent upon the process, voltage, and temperature (PVT) change. Therefore, the circuit has a reliability problem, in that the SCD performance will change unless a complicated compensation circuit is used, which requires an additional area.

In this letter, the authors propose a reliable SCD circuit suitable for an SiC MOSFET power system for high-speed operation application by applying a digital signal processing based circuit to distinguish between normal and SC operation of SiC MOSFET with the voltage induced at the parasitic inductance of the source of SiC MOSFET.

## II. Proposed Short-Circuit Detection Circuit

Fig. 1 shows the gate current $I_G$, drain current $I_D$, and the induced voltage $V_{\mathrm{PL}}$ that is generated by $I_G$ and $I_D$ at the parasitic inductance, $L_{s,\mathrm{stray}}$, when an SiC MOSFET device is normally turned ON. In State 1 shown in Fig. 1, $V_{\mathrm{PL}}$ is generated when a portion of $I_G$ flows through parasitic gate-source capacitance $C_{\mathrm{GS}}$ and $L_{s,\mathrm{stray}}$, and $V_{\mathrm{PL}}$ is generated due to the increase in $I_D$ as the SiC MOSFET is turned ON. In State 2, a ringing $I_D$ is generated by the parasitic inductance and capacitance when $I_D$ is increased and settled, and $V_{\mathrm{PL}}$ is generated according to the formula $L_{s,\mathrm{stray}} \times dI_D/dt$. In State 3, $V_{\mathrm{PL}}$ is generated by the ringing $I_D$ which is generated by other SiC MOSFETs that perform switching actions in the power system, wherein the $V_{\mathrm{PL}}$ is lower than that in States 1 and 2. When the device is turned ON in the SC state, the current at the SiC MOSFET device is continuously increased, and a high $V_{\mathrm{PL}}$ is generated in State 3. The authors propose a digital signal processing based SCD circuit that is stably operated without affecting the normal state operation. The approach uses the characteristic that the $V_{\mathrm{PL}}$ in State 3 is dependent upon the operation of the SiC MOSFET device in the normal state and SC state.

Fig. 2 shows the proposed SCD circuit. The short-circuit detection signal (SCDS) generator can generate a signal which can determine the SC state in State 3, following State 1 and State 2, by using an inverter buffer circuit that uses a pulsewidth modulation (PWM) signal output from the control part; and a digital circuit consisting of a variable time delay circuit, inverter, and an AND gate. Fig. 3 shows the timing diagram of the input signal, the internal output signal, and the final output signal of the SCDS generator. The PWM signal is delayed by the detection time delay $T_{\mathrm{delay}}$ through the first delay circuit and thus is put out as the $V_{\mathrm{Delay1}}$ output signal. The detection time delay $T_{\mathrm{delay}}$ to ignore the $V_{\mathrm{PL}}$ noise in State 1 and State 2 is required to distinguish normal state from the SC state in State 3. As shown in (1), $T_{\mathrm{delay}}$ is expressed as

$$T_{\mathrm{delay}} = (R_G + R_{\mathrm{gate}})(C_{\mathrm{GS}} + C_{\mathrm{GD}}) \ln\left(\frac{g_m V_{\mathrm{gdv}}}{g_m(V_{\mathrm{gdv}} - V_{\mathrm{TH}}) - I_{D.\mathrm{sat}}}\right) + t_{\mathrm{pd}} + t_{\mathrm{mar}} \quad (1)$$

where $R_{\mathrm{gate}}$, $C_{\mathrm{GD}}$, and $g_m$ are the internal gate resistance, parasitic gate-drain capacitance, transconductance of SiC MOSFET, respectively, $R_G$ is the external gate resistance, $V_{\mathrm{gdv}}$ is the gate driving peak voltage, and $I_{D.\mathrm{sat}}$ is the saturation current of SiC MOSFET in normal state operation [10]; $t_{\mathrm{pd}}$, which is the gate driver signal delay time, and $t_{\mathrm{mar}}$, the margin value until $I_D$ is saturated to $I_{D.\mathrm{sat}}$.

The second delay circuit and inverter are the delay circuit to generate the pulsewidth of the final output $V_{\mathrm{SCDS}}$ signal. The AND gate generates the final output $V_{\mathrm{SCDS}}$ signal when both the $V_{\mathrm{Delay1}}$ and $V_{\mathrm{Delay2B}}$ signals are high at the same time. The comparator in Fig. 2 compares the $V_{\mathrm{PL}}$ induced by the variation in $I_D$ with the $V_{\mathrm{REF}}$. When $V_{\mathrm{PL}}$ is higher than $V_{\mathrm{REF}}$, $V_{\mathrm{DD}}$ (i.e.,

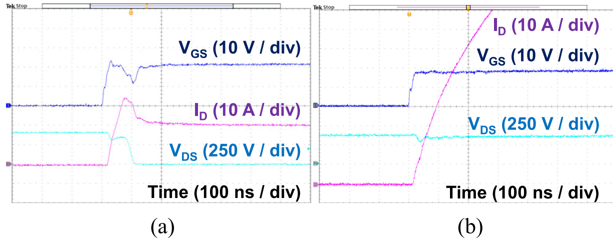


Fig. 4. $I_D$, $V_{\rm DS}$, and $V_{\rm GS}$ of SiC MOSFET (a) under normal operation, (b) under short-circuit operation.

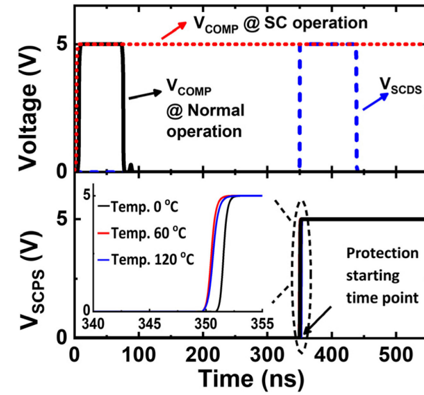


Fig. 5. Simulated $V_{\rm COMP}$, $V_{\rm SCDS}$, and $V_{\rm SCPS}$ waveforms of the proposed SC detection circuit.

logic "high") is put out from the output signal $V_{\rm COMP}$. The $V_{\rm REF}$ of the comparator is configured to have a margin in the maximum induced voltage, $V_{\rm PL,ringing}$, which is generated by the change in the drain current ($\Delta I_D$) due to other switching devices in the power system in the normal state. Hence, the normal state and SC state in State 3 may be determined without an error.

In the normal state, $V_{\rm PL}$ is higher than $V_{\rm REF}$, and $V_{\rm COMP}$ is logic "high" in State 1 and State 2, but $V_{\rm SCDS}$, the SCDS generator output signal, is logic "low." Therefore, the output signal of the SR latch, $V_{\rm SCPS}$, is logic "low," and thus it does not affect the gate driver in the normal state. In State 3, in the normal state, the $V_{\rm SCDS}$ is logic "high," but $V_{\rm PL}$ is lower than $V_{\rm REF}$, and thus the $V_{\rm COMP}$ is logic "low." Therefore, the SR latch output value is "low," and it does not affect the gate driver in the normal state. In the SC state, as shown in Fig. 3, $V_{\rm SCDS}$ is logic "high" and $V_{\rm PL}$ is higher than $V_{\rm REF}$ in State 3, and thus $V_{\rm COMP}$ is logic "high." Therefore, the SR latch is set, and the output signal of the SR latch, $V_{\rm SCPS}$, changes "high" to detect an SC state.

To verify the proposed SCD circuit, a simulation was performed by configuring a simulation test bench. To increase the reliability of the simulation, $C_{\rm GS} = 1.5$ nF, $C_{\rm GD} = 2$ nF, and $R_{\rm gate} = 6.3\ \Omega$ were applied by referring to the datasheet of an ROHM's 1200-V/80-m$\Omega$ SiC MOSFET (part number: SCT2080KE), which is used in the SC experiment. Through electromagnetic simulation, the parasitic inductance by routing, $L_{s,\rm stray}$, was set to 3.6 nH by the modeling from the source of the SiC MOSFET to the ground on a printed circuit board. As in the actual realization environment, a gate driver output peak voltage $V_{\rm gdv}$ of 20 V was applied as a pulse signal and the $R_G$ was 5 $\Omega$. In the proposed design, $V_{\rm REF}$ was set to 0.8 V by considering the slope of the $I_D$ of Fig. 4(b) and the value of $L_{s,\rm stray}$. To simulate the $I_D$ in the normal state and the SC state, a double pulse test and an SC test were conducted by using the SCT2080KE SiC MOSFET under the conditions of $V_{\rm gdv} = 20$ V, $R_G = 5\ \Omega$, load inductance $L_{\rm load} = 500\ \mu$H, and dc-bus voltage $V_{\rm dc} = 400$ V. As shown in Fig. 4(a), in the normal state, $I_D$ increased in the region where $V_{\rm GS}$ was from the threshold voltage $V_{\rm TH}$ to the entry of the Miller plateau, and then $I_D$ was gradually saturated. When an SC test was performed by turning ON the switch that was connected in parallel to $L_{\rm load}$, the $I_D$ continuously increased without being saturated, and thus an overcurrent flowed through the SiC MOSFET, as shown in Fig. 4(b). An empirical model of $I_D$ was built based on these measurements from the normal state and the SC state to perform the simulation.

As shown in Fig. 5, the simulation was performed by applying the $I_D$ for the normal state and the SC state, respectively. From the time when the $I_D$ under the normal operation was saturated, the signal of the output voltage of the comparator, $V_{\rm COMP}$, was changed from "high" to "low" in the normal state, while $V_{\rm COMP}$ remained "high" in the SC state. When the SC state discriminating signal, $V_{\rm SCDS}$, was generated after $T_{\rm delay}$, the SC state detection signal, $V_{\rm SCPS}$, was not put out in the SC state, but it was put out by the proposed circuit. The proposed SCD circuit was designed to adjust the $T_{\rm delay}$ within the range of 150–450 ns through a variable delay circuit. Hence, the proposed SCD circuit can generate the output signal $V_{\rm SCPS}$ at the protection starting time point, from 150 to 450 ns. Therefore, the proposed circuit can be applied to the SiC MOSFET used in this experiment and other SiC MOSFETs. As shown in Fig. 5, the simulated $V_{\rm SCPS}$ waveform depending on temperature is plotted at the design setting when the start time of the protection is 350 ns. The proposed SCD circuit puts out $V_{\rm SCPS}$ at a constant time even without an additional compensating circuit. The proposed circuit can ensure improved stable turn-OFF characteristics of the SiC switching device compared with that of the conventional analog signal processing based SCD circuits.

## III. Experimental Results

The proposed SCD circuit was implemented using a 350-nm Bipolar-CMOS-DMOS process. The chip size was $300 \times 400\ \mu$m$^2$. A 5-V supply voltage is applied to the proposed SCD circuit. As shown in Fig. 6, an SC test board was developed to verify the proposed SC circuit. It consisted of the chip of the proposed SC circuit, ROHM's 1200-V/80-m$\Omega$ SiC MOSFET (part number: SCT2080KE) for a device under test (DUT), a gate driver, a control part, a Pearson current monitor, and dc-link capacitor. The DUT is driven by Texas Instrument's UCC21732 gate driver with a protection function to ensure the safety of the SC experiment. The control block provides a single pulse signal to the gate driver and the Pearson current monitor is adopted to measure the drain current $I_D$ waveform. The dc-link capacitor is connected to the drain terminal of the DUT using a wide copper plate with a considerably low resistance. $V_{\rm dc} = 400$ V, $R_G = 5\ \Omega$, and no load is used for SC test. To perform an SC experiment,

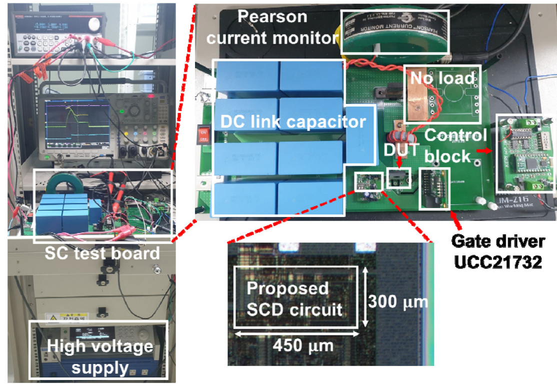


Fig. 6. Experimental environment to verify the proposed SCD circuit.

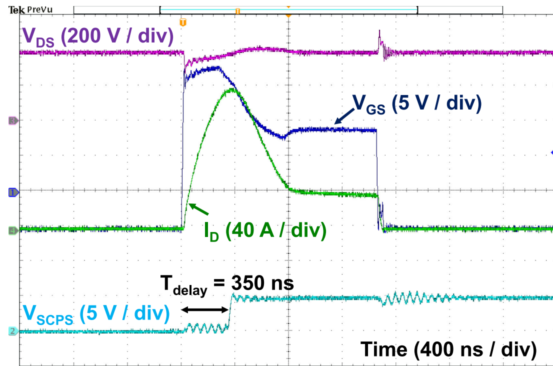


Fig. 7. Measured results of the proposed SCD circuit.

the dc-link capacitor is disconnected from a high-voltage supply after it has charged the dc-link capacitor up to 400 V. Then, a single pulse signal from the control block is applied to the gate driver, which provides a 20-V single pulse signal to the gate of the SiC MOSFET. As shown in Fig. 7, when the $V_{\rm GS}$ is higher than that of the $V_{\rm TH}$ of the SiC MOSFET, the drain current $I_D$ increases abruptly due to SC condition. Therefore, the proposed SCD circuit processes the $V_{\rm PL}$ induced at the parasitic source inductance and generates the output signal $V_{\rm SCPS}$ 350 ns after applying the 20-V single pulse signal to the gate of the SiC MOSFET, as expected from the simulation result. Due to the two-level turn OFF technique for protection of the UCC21732 gate driver used to prevent the DUT from being destroyed under SC test, the gate voltage $V_{\rm GS}$ is clamped and accordingly, the drain current $I_D$ decreases. The experimental result of SC test validates that the proposed SCD circuit works effectively under SC condition.

Fig. 8 shows the measured $I_D$, $V_{\rm PL}$, $V_{\rm REF}$, $V_{\rm SCPS}$, and $V_{\rm DS}$ outcomes under normal operation. As shown in Fig. 8(a), the difference between the $V_{\rm REF}$ voltage and the largest value of the $V_{\rm PL}$ voltage is 0.67 V around 350 ns of $T_{\rm delay}$ sensing the SC state. Therefore, as shown in Fig. 8(b), $V_{\rm SCPS}$ of the SCD circuit remains "low" and does not work incorrectly under normal operation.

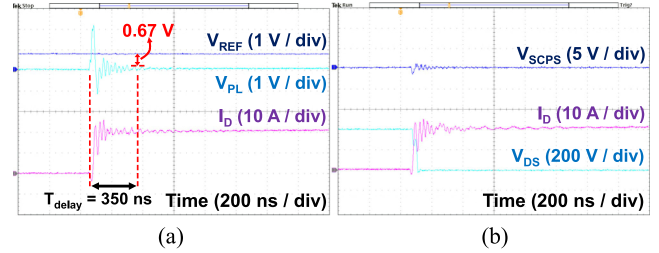


Fig. 8. Measured (a) $V_{\rm PL}$, $V_{\rm REF}$, $I_D$, and (b) $V_{\rm SCPS}$, $V_{\rm DS}$, $I_D$ under normal operation.

## IV. Conclusion

An SCD circuit suitable for SiC MOSFET applications is presented. The proposed SCD circuit incorporates a digital filtering method for the voltage induced at the parasitic inductance of the source terminal of SiC MOSFET to provide an improved stable turn-OFF performance of the SiC MOSFET under SC condition. Compared with that of the conventional analog signal processing based SCD circuits, the proposed circuit is advantageous in terms of having a protection starting time point which is robust to PVT variations, being fully integrated without the use of external components and ease of design. This SCD circuit could be utilized in SiC power modules, which has reliable turn-OFF characteristics, small size, and low cost, and can be used for successful implementation into electric vehicles.

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