Unified Pulsewidth-Cycle Control Strategy to Achieve Mixed DCM/CRM Operation and Consistent Valley Switching for Boost PFC Converter

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***Abstract*—This article proposes a unified pulsewidth-cycle (UPWC) control strategy to achieve mixed-mode operation and consistent valley switching (VS) for boost power factor correction converter. Compared with conventional single-mode controllers, it has a unified scheme to achieve single discontinuous conduction mode (DCM), single critical conduction mode (CRM), or mixed DCM/CRM operations in each half-line cycle. To regulate the input current as a sinusoid, the UPWC controller adopts a variable pulsewidth and a near-constant switching cycle under DCM, while adopts a constant pulsewidth and a variable switching cycle under CRM. To facilitate analysis, normalized mapping of operation modes is provided, along with the final pulsewidth and switching cycle. Furthermore, to ensure consistent VS, a controlled zero current detection method is proposed to fix the turn-ON point of the power switch. No matter in DCM or CRM, consistent VS reduces both the switching loss and current distortion caused by parasitic resonance. To further reduce the current distortion caused by fixing the turn-ON point, a compensation gain is provided that reshapes the input current as a sinusoid. Finally, through mixed DCM/CRM operation and consistent VS, the proposed UPWC controller achieves preferable performances in the power range, efficiency, power factor, and current distortion.**

***Index Terms*—Boost, critical conduction mode (CRM), discontinuous conduction mode (DCM), efficiency, harmonic distortion power factor correction (PFC), valley switching (VS).**

I. Introduction

POWER factor correction (PFC) converters are widely used in modern electronic devices. Depending on the continuity of inductor current, they can operate in discontinuous conduction mode (DCM), critical conduction mode (CRM), and continuous conduction mode (CCM). Among them, CCM operation requires a large inductor and suffers from hard switching and reverse recovery issues, which degrade the efficiency at light load. Comparatively, DCM and CRM operations mainly suit low-to-medium power applications. An important reason is that they reduce the reverse recovery problem and provide a quasi-resonant condition that facilitates valley switching (VS) [1], [2]. For boost PFC converters, VS is based on parasitic resonance at the end of each switching cycle. The optimal turn-ON point is the instant when the drain voltage reaches its valley value. Whether at light load or high switching frequency, VS can reduce the switching loss and effectively improve the power efficiency [3]–[5].

Based on zero current detection (ZCD), a lot of works have successfully realized VS under CRM operation [6], [7]. In achieving VS and unity power factor (PF), conventional constant ON-time (CoT) control is straightforward and easy for implementation. However, VS is based on a parasitic resonance that leads to a negative current in the duration, which accumulates for considerable input current distortion in applications with high line frequency (such as 360–800 Hz in-seat power supply). To offset the negative current during VS, variable ON-time (VoT) controls are proposed to enlarge the ON-time and input current accordingly [8]–[10]. Furthermore, with consideration of nonlinear effects and operation conditions, online monitoring and adaptive LUT methods are proposed to revise the ON-time that further reduce the input current distortion [11], [12].

Another issue under CRM is the variable switching frequency, which changes heavily in PFC applications [13], [14]. The switching frequency becomes very high at light load and near the zero crossing of line voltage. This can cause considerable zero-crossing distortion, which is observed and studied in some literature works [10], [11], [15], [16]. The increased switching frequency also causes more power loss, which offsets the effect of VS and degrades the overall efficiency. Furthermore, an ultra-high switching frequency can lead to potential switching failure that can even harm the devices. To address the high-dynamic switching frequency, some recent studies try to inject harmonics into the input current so that to modulate the required switching frequency. Although these approaches sacrifice the PF a little, the final products are proved to consistently meet industrial standards, such as IEC 61000-3-2 and IEEE Std 519 [17]–[19]. To achieve unity PF with a reduced variation of switching frequency, it is not reasonable to operate the converter in a single CRM.

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Compared with the CRM operation, DCM can be controlled with a constant switching frequency. Similarly, both CoT and VoT can be adopted to regulate the input current under DCM. While CoT is simple for implementation, the achieved PF is low, especially when the line voltage is high. Comparatively, a suitable VoT can regulate the input current under DCM as a sinusoid and achieve unity PF [20], [21]. However, conventional pulsewidth modulation (PWM) induces a fixed turn-ON point, which leads to VS failure and unpredictable turn-ON states of the next cycle. This not only degrades the efficiency but also induces considerable input current distortion [22]–[24]. Conventionally, a resistor–capacitor–snubber (*RCS*) circuit is required to reduce the input current distortion, but this further degrades the power efficiency. Without *RCS*, a valley skipping strategy is recently proposed to achieve VS under CoT [25]. However, the literature has not provided verification for the PF, which is questionable since the prototype is not based on VoT.

As a conclusion, some latest issues in achieving unity PF under DCM and CRM include the high dynamic switching cycle under CRM and the realization of VS under DCM. Besides, both DCM and CRM operations induce a limited power range: the maximum power under DCM is always limited by PWM saturation, while the power range under CRM can easily be limited by the high dynamic switching frequency (considering the speed of power devices). These issues can be addressed by mixed-mode operation, which is recently explored in some pieces of literature [26], [27]. However, DCM and CRM require different control laws to achieve unity PF. To improve the PF while guaranteeing smooth transition of operation modes, a unified control scheme is required. Besides, to reduce the switching loss and current distortion under mixed DCM/CRM operation, consistent VS should be realized.

To achieve unity PF with mixed DCM/CRM operation and consistent VS, this article first investigates conventional single-mode controls in achieving unity PF, while detailed analyses are given for the turn-ON point with consideration of parasitic resonance. Furthermore, a unified pulsewidth-cycle (UPWC) control strategy is proposed. Compared with conventional single-mode controls, it has a unified scheme to achieve single DCM, single CRM, or mixed DCM/CRM operations in each half-line cycle. To regulate the input current as a sinusoid, it adopts a variable pulsewidth and a near-constant switching cycle under DCM, while adopts a constant pulsewidth and a variable switching cycle under CRM. Both the pulsewidth and switching cycle are continuous at the DCM/CRM boundary, which ensures a smooth transition of operation mode. Along with the final pulsewidth and switching cycle, normalized mapping of operation modes is provided. Furthermore, to ensure consistent VS, a controlled ZCD (c-ZCD) method is proposed to fix the turn-ON point of the power switch, while a compensation gain is provided to reduce the distortion caused by fixing the turn-ON point. Finally, the proposed UPWC controller combines advantages of conventional single-mode controls in achieving unity PF while ensures consistent VS in the whole power range. This reduces the variation of switching cycle and switching loss, while improves the power range, efficiency, current distortion, and PF.

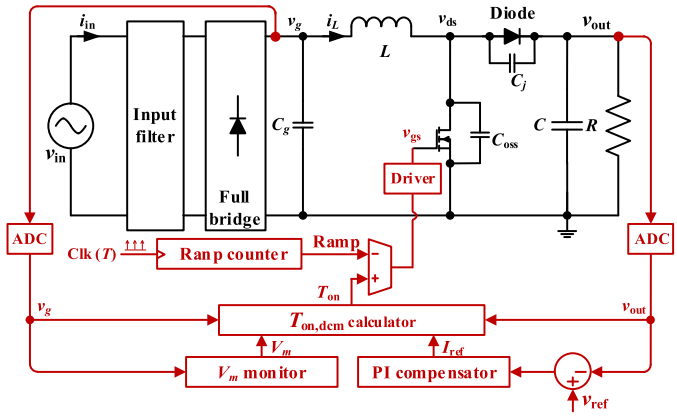

Fig. 1. Conventional VoT control to regulate the input current of boost PFC converter under DCM.

This article is organized as follows. Section II investigates conventional control strategies for single DCM and CRM boost PFC converters, along with analysis for parasitic resonance. In Section III, the UPWC control strategy is proposed to achieve mixed DCM/CRM operation and consistent VS. Detailed analyses are given for operation mode mapping and the influence of turn-ON point. Besides, a compensation gain is derived to further reduce the current distortion caused by fixing the turn-ON point. In Section IV, the effectiveness of the proposed UPWC control is verified by comparisons of experimental results. Finally, a brief conclusion is given in Section V.

II. Conventional Control Strategies for Single DCM and Single CRM Boost PFC Converters

For boost PFC converters operating in DCM and CRM, different control strategies are required to achieve sinusoidal input current. Conventionally, CoT and variable switching cycle are needed to achieve unity PF under CRM, whereas under DCM, VoT and constant switching cycle are required. As a result, single DCM and CRM operations induce different control schemes that are incompatible.

In the following, conventional control strategies for single DCM and CRM operations are introduced for boost PFC converter. These strategies should regulate the input current as a sinusoid and achieve a unity PF. However, when considering parasitic resonance, the achieved input current can be distorted.

A. Conventional VoT Control to Regulate the Input Current Under DCM

A basic boost PFC converter with VoT control to achieve DCM is given in Fig. 1. Owing to the input filter and full-bridge, the input current absolute value is regulated as the shape of the inductor current average value, i.e., $|i_{\rm in}| = \bar{i}_L$. Therefore, to improve the PF, the inductor current average value should be regulated as a sinusoid.

The control process is given in the following. First, the output voltage ($v_{\rm out}$) is sampled and compared to a reference voltage ($v_{\rm ref}$), where the error is input to the PI compensator. Then, a

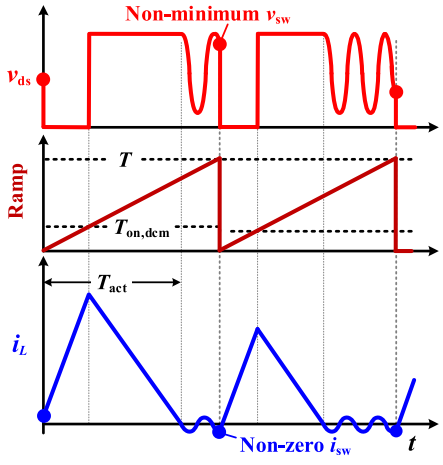

Fig. 2. Switching node voltage and inductor current under VoT control with consideration of parasitic resonance.

reference current ($I_{\rm ref}$) is calculated to modulate the magnitude of the input current ($i_{\rm in}$). Meanwhile, the magnitude of the line voltage (v_g) is acquired by a V_m monitor. Without the consideration of voltage on the full bridge, V_m is the magnitude of both v_g and input voltage ($v_{\rm in}$). Both $I_{\rm ref}$ and V_m are updated every half-line cycle and in pace with the line voltage. Furthermore, a suitable ON-time is calculated by the $T_{\rm on,dcm}$ calculator, which shall regulate $i_{\rm in}$ as $I_{\rm ref}\sin(\omega t)$. Finally, the calculated ON-time is compared to a ramp signal to carry out PWM. The ramp signal has a constant cycle of T, thus the converter operates with a fixed switching frequency.

With a constant switching cycle of T, the absolute value of the input current under DCM is given by

$$|i_{\rm in}| = \bar{i}_L = \frac{{T_{\rm on,dcm}}^2 v_g v_{\rm out}}{2(v_{\rm out}-v_g)LT} \tag{1}$$

where $T_{\rm on,dcm}$ is the ON-time to drive the main switch. To regulate the input current as $I_{\rm ref}\sin(\omega t)$, the controller adopts (2) to calculate the required ON-time

$$\begin{aligned} T_{\rm on,dcm} &= \sqrt{\frac{2|I_{\rm ref}\sin(\omega t)|LT(v_{\rm out}-v_g)}{v_g v_{\rm out}}} \\ &= \sqrt{\frac{2I_{\rm ref}LT(v_{\rm out}-v_g)}{V_m v_{\rm out}}}. \end{aligned} \tag{2}$$

This VoT should regulate the input current as a sinusoid. With VoT control, nearly unity PF can be achieved under DCM operation. However, parasitic resonance can be caused by the main inductor, output capacitance of the power transistor ($C_{\rm oss}$), and junction capacitance of the diode (C_j). The resonance can change the turn-ON voltage and current of the next switching cycle, leading to a degraded efficiency and considerable input current distortion. Detailed analysis is given in the following.

As shown in Fig. 2, the resonance occurs after i_L reaches zero. Assuming the current rising time and falling time accumulate for $T_{\rm act}$ (namely active current time), the resonance will last for T-$T_{\rm act}$, which determines both the turn-ON current $i_{\rm sw}$ and turn-ON voltage $v_{\rm sw}$.

Since the resonance lasts for T-$T_{\rm act}$, the switching node voltage ($v_{\rm ds}$) and the inductor current (i_L) during the resonance are given by:

$$\begin{cases} v_{\rm ds}(t) = v_g + (v_{\rm out}-v_g)\cos[\omega_r(t-T_{\rm act})] \\ i_L(t) = -\frac{v_{\rm out}-v_g}{Z_r}\sin[\omega_r(t-T_{\rm act})] \end{cases} \tag{3}$$

where $Z_r = \sqrt{L/(C_{\rm oss}+C_j)}$ and $\omega_r = 1/\sqrt{L(C_{\rm oss}+C_j)}$. Furthermore, $v_{\rm sw}$ and $i_{\rm sw}$ are the voltage and current at time $t = T$ as

$$\begin{cases} v_{\rm sw} = v_{ds}(T) = v_g + (v_{\rm out}-v_g)\cos[\omega_r(T-T_{\rm act})] \\ i_{\rm sw} = i_L(T) = -\frac{v_{\rm out}-v_g}{Z_r}\sin[\omega_r(T-T_{\rm act})]. \end{cases} \tag{4}$$

In the above equations, both $v_{\rm sw}$ and $i_{\rm sw}$ change along with T-$T_{\rm act}$. Based on voltage-second balancing, the relationship between $T_{\rm act}$ and $T_{\rm on,dcm}$ is (influenced by $i_{\rm sw}$)

$$i_{\rm sw} + \frac{v_g T_{\rm on,dcm}}{L} = \frac{v_{\rm out}-v_g}{L}(T_{\rm act}-T_{\rm on,dcm}). \tag{5}$$

Furthermore, $T_{\rm act}$ is derived with consideration of $i_{\rm sw}$

$$T_{\rm act} = \frac{i_{\rm sw}L + v_{\rm out}T_{\rm on,dcm}}{v_{\rm out}-v_g}. \tag{6}$$

Substituting (6) into (4) gives the relationship between $v_{\rm sw}$ and $i_{\rm sw}$ by

$$\begin{cases} v_{\rm sw} = v_g + (v_{\rm out}-v_g)\cos[\omega_r(T-\frac{i_{\rm sw}L+v_{\rm out}T_{\rm on,dcm}}{v_{\rm out}-v_g})] \\ i_{\rm sw} = -\frac{v_{\rm out}-v_g}{Z_r}\sin[\omega_r(T-\frac{i_{\rm sw}L+v_{\rm out}T_{\rm on,dcm}}{v_{\rm out}-v_g})]. \end{cases} \tag{7}$$

This result is valid only when $v_g \geq 0.5v_{\rm out}$ since it is derived without consideration of the body diode of the main power switch. According to (7), the minimum value of $v_{\rm ds}$ is $2v_g$-$v_{\rm out}$, which would become negative when $v_g < 0.5v_{\rm out}$. However, this cannot happen in a practical circuit since $v_{\rm ds}$ is always clamped by the body diode of the main power switch.

When $v_g < 0.5v_{\rm out}$, the actual resonance is very similar to (3) with $v_{\rm out} = 2v_g$. Besides, owing to the reverse clamping time, the phase is modified by $0.5\pi - (v_{\rm out}-v_g)/v_g$. Furthermore, with similar derivations, $v_{\rm ds}$ and $i_{\rm ds}$ are given by

$$\begin{cases} v_{\rm sw} = v_g + v_g\cos[\omega_r(T-\frac{i_{\rm sw}L+v_{\rm out}T_{\rm on,dcm}}{v_{\rm out}-v_g}) - \frac{v_{\rm out}-v_g}{v_g} + \frac{\pi}{2}] \\ i_{\rm sw} = -\frac{v_g}{Z_r}\sin[\omega_r(T-\frac{i_{\rm sw}L+v_{\rm out}T_{\rm on,dcm}}{v_{\rm out}-v_g}) - \frac{v_{\rm out}-v_g}{v_g} + \frac{\pi}{2}]. \end{cases} \tag{8}$$

Based on specifications in Section IV (i.e., $v_{\rm out} = 400$ V, $L = 202$ μH, $C_{\rm oss} = 85$ pF, $C_j = 38$ pF), variations of $v_{\rm sw}$ and $i_{\rm sw}$ with $T_{\rm on,dcm}$ are calculated and plotted in Fig. 3. The results are plotted with $v_g = 100$ V, $v_g = 200$ V, and $v_g = 300$ V, respectively.

With a constant T, both $v_{\rm sw}$ and $i_{\rm sw}$ dramatically change along with $T_{\rm on,dcm}$. With $v_g = 100$ V, variation of $v_{\rm sw}$ is from 0 to 200 V, while variation of $i_{\rm sw}$ is from -0.08 to 0.08 A. With $v_g = 200$ V, variation of $v_{\rm sw}$ is from 0 to 400 V, while variation of $i_{\rm sw}$ is from -0.15 to 0.15 A. With $v_g = 300$ V, variation of $v_{\rm sw}$ is from 200 to 400 V, while variation of $i_{\rm sw}$ is from -0.08 to 0.08 A. In PFC applications, both v_g and $T_{\rm on,dcm}$ change dynamically in each line cycle, which further complicates variations of $v_{\rm sw}$ and $i_{\rm sw}$.

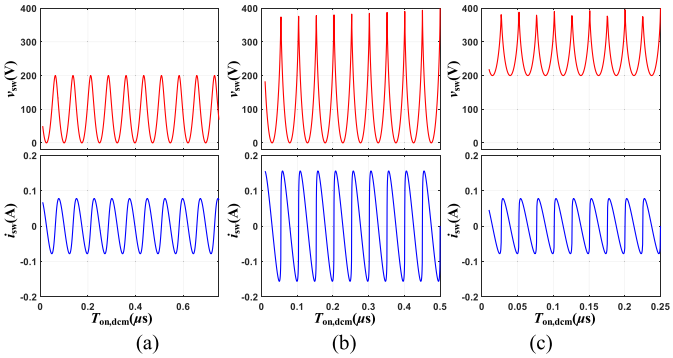

Fig. 3. Variations of $v_{\rm sw}$ and $i_{\rm sw}$ with $T_{\rm on,dcm}$. (a) $v_g = 100$ V. (b) $v_g = 200$ V. (c) $v_g = 300$ V.

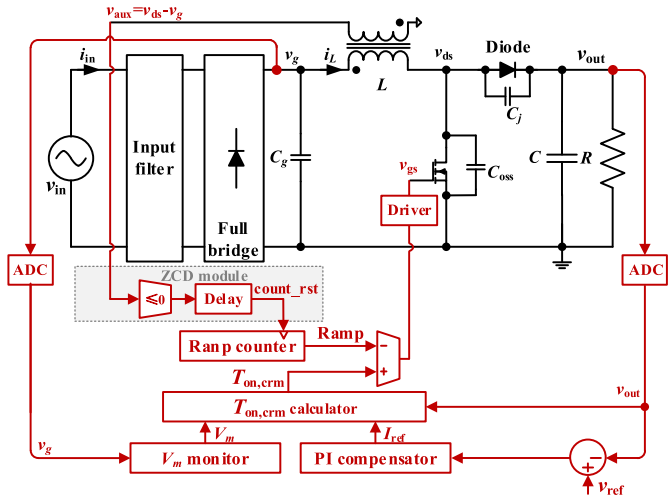

Fig. 4. Conventional CoT control (with equivalent pulse cycle modulation) to regulate the input current of boost PFC converter under CRM.

The changing $v_{\rm sw}$ and $i_{\rm sw}$ lead to unpredictable PF, input current distortion, and efficiency under DCM. Specifically, a high $v_{\rm sw}$ induces considerable loss on power transistor, and the dissipated power is given by

$$P_{\rm sw,oss} = \frac{C_{\rm oss} {v_{\rm sw}}^2}{2T}. \tag{9}$$

Besides, a nonzero $i_{\rm sw}$ can change the inductor current average value and induce input current distortion. To reduce this issue, the *RCS* circuit is required to dissipate the resonant energy. However, this induces more power consumption that degrades the efficiency, especially at light load.

Despite the parasitic resonance is unpreferable under DCM, it can be actively utilized to achieve VS under CRM.

B. Conventional CoT Control to Regulate the Input Current Under CRM

For boost PFC converter, CoT control with ZCD can be used to achieve sinusoidal input current under CRM. While this strategy is usually realized through S-R flip-flop modulation, Fig. 4 presents an equivalent approach, which is based on variable pulse cycle modulation. This is equivalent to the conventional S-R flip-flop method, but it facilitates the derivation of UPWC control in Section III. The V_m monitor and PI compensator are identical to those in Fig. 1.

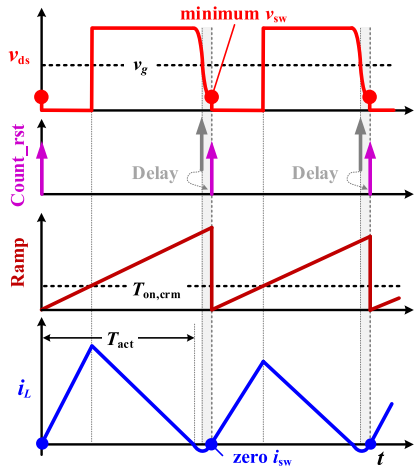

Fig. 5. Switching node voltage and inductor current under CoT control with consideration of parasitic resonance.

The $T_{\rm on,crm}$ calculator outputs an appropriate ON-time to regulate the input current under CRM. Since the inductor current average value is half of its peak value under CRM, the required ON-time is given by

$$T_{\rm on,crm} = \frac{2I_{\rm ref}|\sin(\omega t)|L}{V_m|\sin(\omega t)|} = \frac{2I_{\rm ref}L}{V_m}. \tag{10}$$

Since $I_{\rm ref}$ and V_m are updated every half-line cycle, the calculated $T_{\rm on,crm}$ maintains constant in each half-line cycle that forms CoT control.

Furthermore, compared with the VoT controller in Fig. 1, the ramp counter in Fig. 4 is reset by the ZCD module instead of using a clock with a constant cycle. The ZCD module consists of a simple comparator, a delay unit, and an auxiliary winding on the main inductor. The auxiliary winding acquires the auxiliary voltage $v_{\rm aux} = v_{\rm ds}$-v_g, where the winding ratio is neglected to simplify the analysis. Once $v_{\rm ds}$ is lower than v_g, $v_{\rm aux} \le 0$ becomes valid and the rising edge is delayed by 1/4 of the parasitic resonance period. Furthermore, the output count_rst resets the ramp counter to initiate a new switching cycle.

With ZCD to determine the turn-ON point of each cycle, VS is achieved, as shown in Fig. 5. Effective VS not only reduces the switching loss, but also fixes the initial current of each cycle to zero, and thus reduces the current distortion.

However, with CoT to achieve CRM, the achieved switching cycle can change dramatically with the line voltage and current. Based on voltage-second balancing, the achieved switching cycle is given by

$$T_{\rm CRM} = \frac{v_{\rm out}}{v_{\rm out} - v_g} T_{\rm on,crm} = \frac{2I_{\rm ref}Lv_{\rm out}}{V_m(v_{\rm out} - v_g)}. \tag{11}$$

Obviously, $T_{\rm CRM}$ could change dramatically with v_g, $I_{\rm ref}$, and V_m. It becomes very small at light load and near the zero crossing of line voltage. The increased frequency can induce more power

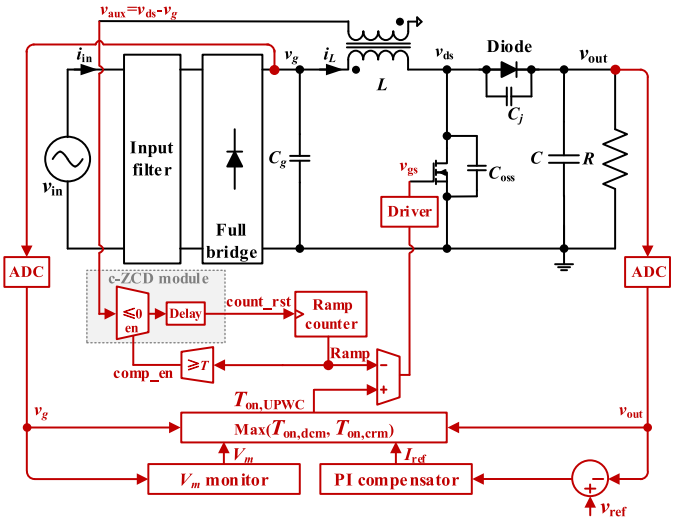

Fig. 6. Scheme of the proposed UPWC control strategy for boost PFC converter.

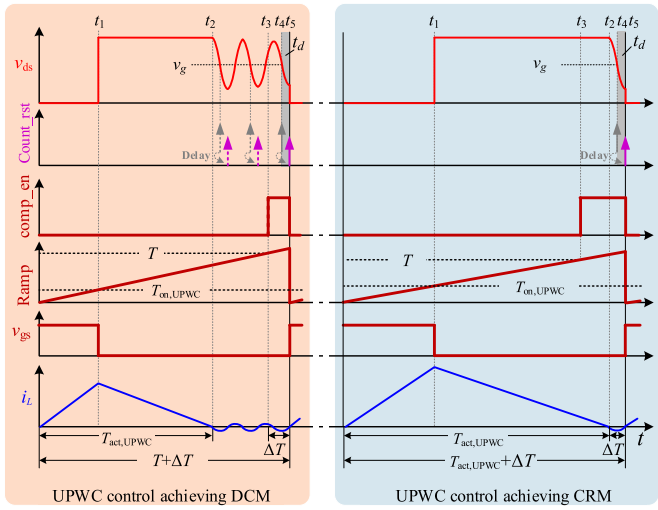

Fig. 7. UPWC control process achieving DCM and CRM operations.

loss and zero-crossing distortion (considering the speed of power switches). Besides, an ultrahigh switching frequency can lead to potential switching failure that even harm the devices.

As a conclusion of Section II, with conventional VoT to achieve DCM, the converter benefits from a constant switching cycle. However, the fixed turn-ON point leads to VS failure, unpredictable input current distortion, and power loss. Although VS can easily be achieved under CRM operation, the high dynamic switching cycle can induce unpreferable power loss and zero-crossing distortion, especially at light load. To combine the advantages of different controls and achieve consistent VS, a UPWC control strategy is proposed in the following.

III. UPWC Control Strategy to Achieve Mixed DCM/CRM Operation and Consistent VS

To address the aforementioned issues, the proposed UPWC controller adopts a unified scheme to achieve mixed DCM/CRM operation and consistent VS. Depending on the operation condition, the UPWC controller achieves single DCM, single CRM, or mixed DCM/CRM operations in each half-line cycle. Through the mixing of operation modes, it features reduced variation of switching cycle and enlarged power range. No matter in DCM and CRM, consistent VS is achieved by a c-ZCD method.

A. UPWC Control Scheme and the Modulation Process

To regulate the input current as a sinusoid, the proposed UPWC controller adopts a variable pulsewidth and a near-constant switching cycle under DCM, while adopts a constant pulsewidth and a variable switching cycle under CRM.

The unified control scheme is given in Fig. 6. In the voltage loop, the V_m monitor and PI compensator are identical to those in Figs. 1 and 4. In the current loop, both $T_{\mathrm{on,dcm}}$ and $T_{\mathrm{on,crm}}$ are calculated, and the greater value is adopted as the final ON-time. Meanwhile, compared with CoT control in Fig. 4, the current detection part is controlled by an enable logic, which utilizes an additional comparator to detect if Ramp $\geq T$. In this way, the reset signal (count_rst) can become valid only when the switching cycle is longer than T.

The transition between DCM and CRM operations is ensured by comparison between $T_{\mathrm{on,dcm}}$ and $T_{\mathrm{on,crm}}$ and the greater value is adopted as the final ON-time

$$T_{\mathrm{on,UPWC}} = \max(T_{\mathrm{on,dcm}}, T_{\mathrm{on,crm}}) = \max\left(\sqrt{\frac{2I_{\mathrm{ref}}LT(v_{\mathrm{out}}-v_g)}{V_m v_{\mathrm{out}}}}, \frac{2I_{\mathrm{ref}}L}{V_m}\right). \quad (12)$$

Furthermore, compared with (6), the active current time under UPWC is renewed as (since consistent VS ensures $i_{\mathrm{sw}}=0$)

$$T_{\mathrm{act,UPWC}} = \frac{v_{\mathrm{out}}}{v_{\mathrm{out}}-v_g} T_{\mathrm{on,UPWC}}. \quad (13)$$

When $T_{\mathrm{on,dcm}} > T_{\mathrm{on,crm}}$, $T_{\mathrm{on,UPWC}}$ is set as $T_{\mathrm{on,dcm}}$, which derives

$$T_{\mathrm{act,UPWC}} = \frac{v_{\mathrm{out}}}{v_{\mathrm{out}}-v_g} T_{\mathrm{on,dcm}} = \sqrt{\frac{2I_{\mathrm{ref}}LTv_{\mathrm{out}}}{V_m(v_{\mathrm{out}}-v_g)}} < T. \quad (14)$$

Since $T_{\mathrm{act,UPWC}} < T$, count_rst can become valid only when Ramp $\geq T$, the converter achieves DCM operation with a switching cycle of T.

When $T_{\mathrm{on,dcm}} < T_{\mathrm{on,crm}}$, $T_{\mathrm{on,UPWC}}$ is set as $T_{\mathrm{on,crm}}$, which derives

$$T_{\mathrm{act,UPWC}} = \frac{v_{\mathrm{out}}}{v_{\mathrm{out}}-v_g} T_{\mathrm{on,crm}} = \frac{2I_{\mathrm{ref}}Lv_{\mathrm{out}}}{V_m(v_{\mathrm{out}}-v_g)} > T. \quad (15)$$

Since the current is always active during T, the zero-crossing point must be detected after T, resulting in a switching cycle of $T_{\mathrm{act,UPWC}}$.

The detailed UPWC control process is given in Fig. 7, including the processes under DCM and CRM, respectively. The achieved switching cycle is $T+\Delta T$ under DCM and $T_{\mathrm{act,UPWC}}+\Delta T$ under CRM. The additional ΔT is induced by

fixing the turn-ON point as the VS point, and it satisfies

$$\begin{cases} 0.5\pi/\omega_r < \Delta T < 2.5\pi/\omega_r \ \text{ under DCM} \\ \Delta T = \pi/\omega_r \ \text{ under CRM} \end{cases} \tag{16}$$

where $\omega_r = 1/\sqrt{L(C_{\rm oss}+C_j)}$ is the parasitic resonance frequency caused by $C_{\rm oss}$, C_j, and L.

Furthermore, signal variations with time are as follows: (note that t_3 is ahead of t_2 when operating in CRM).

Before t_1: The main switch is ON while the diode is OFF. The inductor current rises with a constant slope of v_g/L.

t_1–t_2: The main switch is OFF while the diode is ON. The inductor current falls with a constant slope of $(v_{\rm out}\text{-}v_g)/L$.

t_2–t_5: Both the main switch and the diode are OFF. The inductor current and the switching node voltage resonant with a frequency of ω_r.

t_3–t_5: The Ramp signal is higher than T, which enables the c-ZCD module to detect if $v_{ds} \le v_g$ until the next switching cycle.

t_4–t_5: The rising edge of $v_{ds} \le v_g$ is detected. After a delay of $t_d = 0.5\pi/\omega_r$, the main switch is turned ON, which initiates a new switching cycle at time $t = t_5$.

With the proposed UPWC control, VS is consistently achieved in every switching cycle. At time $t = t_5$, the inductor current equals zero, while the node voltage reaches its minimum value. This reduces the switching loss and avoids current distortion caused by the parasitic resonance.

B. Normalized Mapping of Operation Modes Under UPWC Control

With UPWC control to achieve mixed CRM/DCM operation, the operation mode could change according to different conditions. Detailed mapping of operation modes under UPWC control is given in the following. In order to simplify the analysis, ΔT is neglected in the mapping of operation modes.

Based on previous analysis, the operation mode is dependent on the relationship between (2) and (10). The ON-time calculator chooses the higher value of $T_{\rm on,dcm}$ and $T_{\rm on,crm}$ as the final ON-time. When $T_{\rm on,dcm} > T_{\rm on,crm}$, the converter achieves DCM operation with a switching cycle of T. When $T_{\rm on,dcm} \le T_{\rm on,crm}$, the converter achieves CRM operation with a switching cycle of $T_{\rm act,UPWC}$.

Furthermore, the normalized ON-time and switching cycle under UPWC control are simplified as (17), where F_I is the ratio between $I_{\rm ref}$ and $V_mT/(2L)$, and F_V is the ratio between v_g and $v_{\rm out}$. Obviously, F_I is updated every half-line cycle, whereas F_V is updated every switching cycle

$$\begin{cases} T_{\rm on,UPWC} = \max(T_{\rm on,dcm}, T_{\rm on,crm}) \\ T_{\rm on,dcm} = \sqrt{F_I(1-F_V)}T, \quad T_{\rm on,crm} = F_IT \\ T_{\rm UPWC} = \begin{cases} T \ \text{under DCM} \\ \frac{F_IT}{1-F_V} \ \text{under CRM} \end{cases} \\ F_I = \frac{2I_{\rm ref}L}{V_mT} = I_{\rm ref}/(\frac{V_mT}{2L}), \quad F_V = \frac{v_g}{v_{\rm out}}. \end{cases} \tag{17}$$

At the boundary of DCM and CRM operations, the ON-time is continuous, which gives $\sqrt{F_I(1-F_V)}T = F_IT$, i.e., $1 - F_V = F_I$. Furthermore, the boundary on-time is derived as

$$T_{\rm on,boundary} = (1-F_V)T. \tag{18}$$

Based on (17), variations of $T_{\rm on,UPWC}$ and $T_{\rm UPWC}$ with F_V are plotted in Fig. 8. The converter achieves DCM operation when $T_{\rm on,UPWC} < T_{\rm on,boundary}$, whereas achieves CRM operation when $T_{\rm on,UPWC} \ge T_{\rm on,boundary}$.

Depending on the magnitude of F_I, the converter achieves single DCM, single CRM, or mixed DCM/CRM operations in each half-line cycle. When $F_I < 1\text{-}V_m/v_{\rm out}$, the converter achieves DCM operation, since $T_{\rm on,boundary} > T_{\rm on,dcm} > T_{\rm on,crm}$ is valid in the whole operation region. As shown in Fig. 8(a), the ON-time is set as $T_{\rm on,dcm}$, i.e., $\sqrt{F_I(1-F_V)}T$. The final switching cycle is T, which is clamped by the signal comp_en (see the left part of Fig. 7). When $1\text{-}V_m/v_{\rm out} \le F_I < 1$, the converter achieves mixed DCM/CRM operation, since the relationship between $T_{\rm on,dcm}$ and $T_{\rm on,crm}$ changes in the operation region. As shown in Fig. 8(b), the ON-time equals $T_{\rm on,dcm}$ when F_V is low, and it shifts to $T_{\rm on,crm}$ when F_V is high. While the ON-time shifts, the switching cycle also changes from T to $F_IT/(1\text{-}F_V)$. When $F_I \ge 1$, the converter achieves a single CRM operation since $T_{\rm on,dcm} \le T_{\rm on,crm} \le T_{\rm on,boundary}$ is valid in the whole operation region. As shown in Fig. 8(c), the ON-time is set as $T_{\rm on,crm}$, i.e., F_IT. The final switching cycle is $F_IT/(1\text{-}F_V)$, which is always higher than T.

C. Variations of the Input Power and Switching Cycle

Assuming unity PF is achieved while the magnitude of the input current is regulated as $I_{\rm ref}$, then the input power is $P_{\rm in} = I_{\rm ref}V_m/2$. Furthermore, based on (17), the input power is derived as

$$P_{\rm in} = \frac{1}{2}\frac{F_IV_mT}{2L}V_m = \frac{F_I{v_{\rm out}}^2T}{4L}\left(\frac{V_m}{v_{\rm out}}\right)^2. \tag{19}$$

With (17) and (19), simulations for the input power and switching cycle are provided to comply specifications of the prototype. Based on Table I in Section IV, the maximum power rate is 320 W. The input voltage changes from 85 Vac to 265 Vac, while the output voltage is 400 Vdc. Furthermore, variations of the input power and switching cycle are simulated and plotted in Fig. 9.

In Fig. 9(a), variation of the input power is plotted with F_I and $V_m/v_{\rm out}$ (i.e., the maximum F_V in a half-line cycle). With $V_m \in [85\sqrt{2}, 265\sqrt{2}]$ V, $v_{\rm out} = 400$ V, and a maximum input power of 320 W, the operation region is restricted within the

TABLE I
MAIN SPECIFICATIONS OF THE PROTOTYPE

Input voltage $v_{\rm in}$	85-265 VAC
Output voltage $v_{\rm out}$	400 VDC
Maximum power rate $P_{\rm max}$	320 W
Output capacitance $C_{\rm out}$	180 μF
Boost inductance L	202 μH
Fundamental switching cycle T	10 μs
Transistor output capacitance $C_{\rm oss}$ ($@v_{\rm gs}$=0 V, $v_{\rm ds}$=250 V)	85 pF
Diode junction capacitance C_j	38 pF

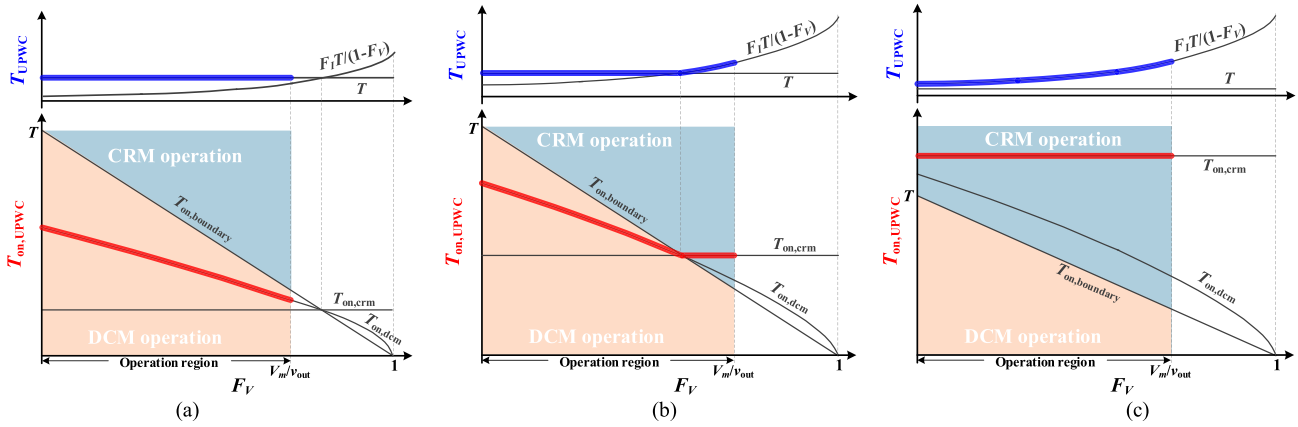

Fig. 8. Variation of $T_{\mathrm{on,UPWC}}$ and T_{UPWC} with F_V under UPWC control. (a) Single DCM operation when $F_I < 1\text{-}V_m/v_{\mathrm{out}}$. (b) Mixed CRM/DCM operation when $1\text{-}V_m/v_{\mathrm{out}} \le F_I < 1$. (c) Single CRM operation when $F_I \ge 1$.

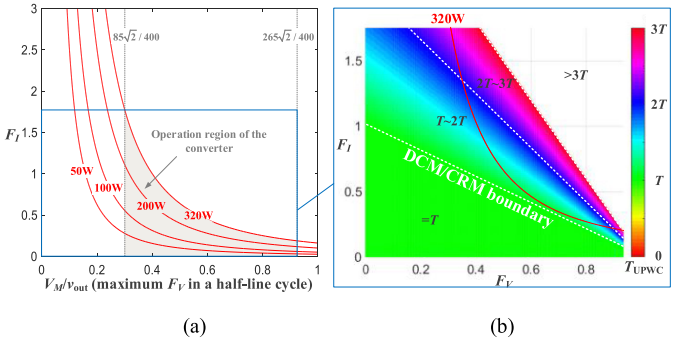

Fig. 9. Simulated input power and switching cycle. (a) Variation of input power with F_I and V_m/v_{out}. (b) Variation of switching cycle with F_I and F_V.

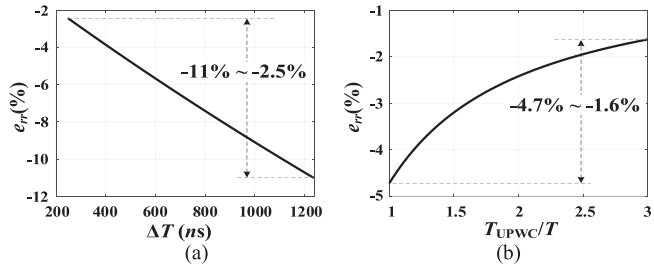

Fig. 10. Variation of e_{rr} with ΔT and T_{UPWC} (a) under DCM and (b) under CRM.

shadow area. Furthermore, variation of switching cycle with F_I and F_V is plotted in Fig. 9(b). Within the operation region, the minimum switching cycle is T (i.e.,10 μs), while the maximum switching cycle rarely exceeds $2T$.

D. Influence of ΔT *and the Compensation to Reshape the Input Current*

The proposed UPWC control strategy slightly changes the switching cycle that deviates the input current. The switching cycle is enlarged by ΔT, which is neglected in the previous analysis. Based on geometric approximation, ΔT damps the input current as

$$|i_{\mathrm{in,damp}}| = \frac{T_{\mathrm{UPWC}}}{T_{\mathrm{UPWC}} + \Delta T} I_{\mathrm{ref}} |\sin(\omega t)|. \tag{20}$$

Furthermore, the relative error is given by

$$e_{rr} = \frac{|i_{\mathrm{in,damp}}| - I_{\mathrm{ref}}|\sin(\omega t)|}{I_{\mathrm{ref}}|\sin(\omega t)|} = \frac{-\Delta T}{T_{\mathrm{UPWC}} + \Delta T}. \tag{21}$$

The error changes with ΔT under DCM, where T_{UPWC} is constant. It changes with T_{UPWC} under CRM, where ΔT is constant. Based on (16) and specifications in Section IV, variation of ΔT is within [248 ns, 1238 ns] under DCM, and it equals 495 n*s* under CRM. Furthermore, variation e_{rr} is plotted in Fig. 10. No matter in DCM or in CRM, the relative error is always negative. Thus, the actual input current is always damped, resulting in considerable input current distortion.

To offset the damping effect, the reference current should be compensated by a gain of *k*. Furthermore, compared with (20), the resulting input current is given by

$$|i_{\mathrm{in,damp}}| = \frac{T_{\mathrm{UPWC}}}{T_{\mathrm{UPWC}} + \Delta T} k I_{\mathrm{ref}} |\sin(\omega t)|. \tag{22}$$

Assuming the final damped input current is regulated as $i_{\mathrm{in,damp}} = I_{\mathrm{ref}} \sin(\omega t)$, the required compensation factor is given by

$$k = \frac{T_{\mathrm{UPWC}} + \Delta T}{T_{\mathrm{UPWC}}}. \tag{23}$$

By multiplying (23) to the reference current, the influence of ΔT on the input current can be reduced, which further reshapes the input current as a sinusoid. The final compensated UPWC control algorithm is given in Fig. 11.

With the final UPWC control algorithm, the input current under both DCM and CRM can be regulated as a sinusoid. With a unified control algorithm, the switching cycle and ON-time are continuous at the DCM/CRM boundary, which ensures a smooth transition of operation modes. Finally, the proposed UPWC controller achieves mixed-mode operation and consistent VS,

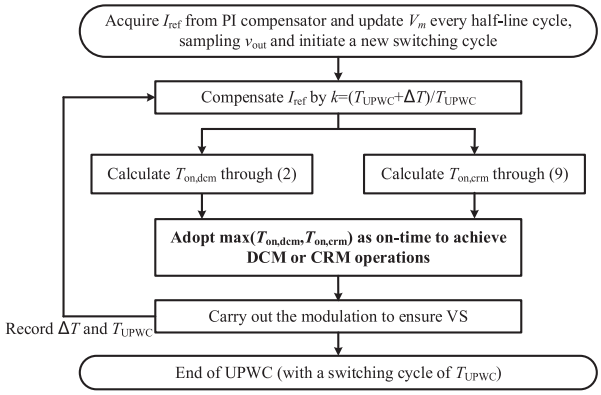

Fig. 11. UPWC control algorithm to achieve mixed DCM/CRM operations.

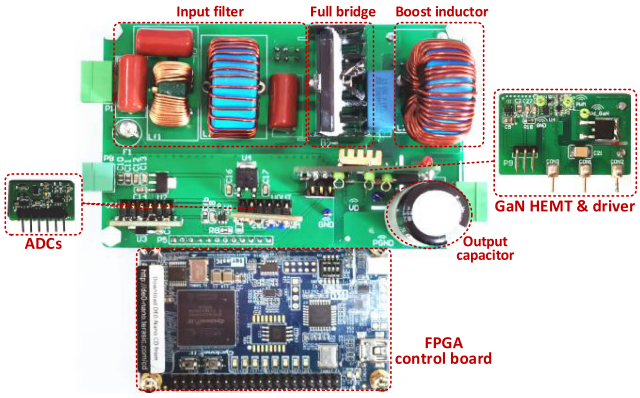

Fig. 12. Photograph of the experimental prototype.

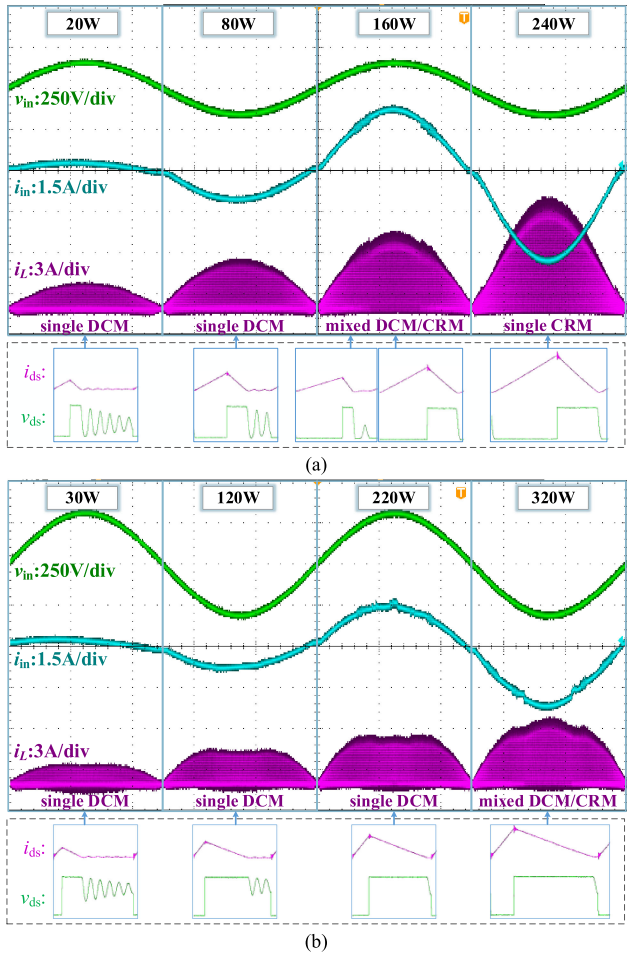

Fig. 13. Inductor current and input current with UPWC control to achieve mixed DCM/CRM operation. (a) $v_{\rm in}$ = 110 Vac. (b) $v_{\rm in}$ = 220 Vac.

where detailed comparisons and evaluations are given in the following section.

IV. Experimental Details

An experimental prototype is built to verify the effectiveness of the proposed UPWC control strategy, as shown in Fig. 12.

Two ADC (LTC2314-14) modules are used to convert the analog values to digital signals. Digital values are processed by an FPGA (Cyclone IV) board. A 180 μF capacitor (450LXW180MEFR18X45) is utilized as the output capacitor. The magnetic core of the inductor is NPH107060 from POCO. The power switch is GS66508T (650V E-mode GaN power transistor) from GaN systems, and the power diode is STPSC8H065 (650 V SiC Schottky diode) from ST Microelectronics.

The main specifications of the prototype are given in Table I. The maximum power rate is 320 W, and the output voltage is 400 V. The fundamental switching cycle for UPWC control is set as 10 μs. With typical $C_{\rm oss}$ and C_j, the resonant frequency is calculated by $\omega_r = 1/\sqrt{L(C_{\rm oss}+C_j)} \approx 6.34$ Mrad/s, i.e., 1.01 MHz.

With an identical power stage, different control strategies are carried out by the FPGA control board. In the following, the proposed UPWC control strategy is compared with: 1) conventional VoT control to achieve single DCM operation; 2) conventional CoT control to achieve single CRM and VS. Detailed comparisons include the measured waveforms under different loads, turn-ON point, switching cycle, efficiency, PF, and total harmonic distortion of input current.

A. Mixed DCM/CRM Operation With the Proposed UPWC Control Strategy

With a unified control scheme, the proposed UPWC controller can smoothly transit between DCM and CRM operations, while achieves sinusoidal input current and valid VS. The inductor and input currents under the mixed-mode operation are given in Fig. 13. The results are measured under $v_{\rm in}$ = 110 Vac and $v_{\rm in}$ = 220 Vac, respectively.

As indicated by the zoom-in plots, the proposed UPWC controller achieves consistent VS, no matter in DCM or in CRM. With $v_{\rm in}$ = 110 Vac, the operational power is between 20 and 240 W. The converter achieves single DCM under 20 and 80 W, mixed DCM/CRM under 160 W, and single CRM under 240 W. With $v_{\rm in}$ = 220 Vac, the operational power is between 30 and 320 W. The converter achieves single DCM under 30, 120, and 220 W, while achieves mixed DCM/CRM under 320 W. When

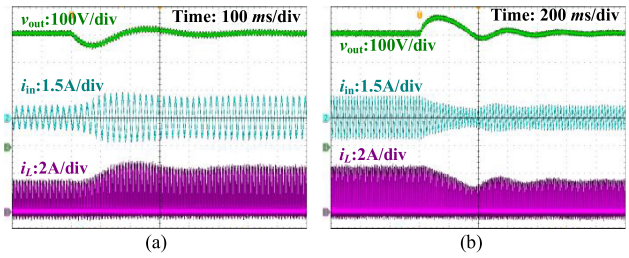

Fig. 14. Transient response when the load steps (a) from 80 to 160 W and (b) from160 to 80 W.

transiting between DCM and CRM operations, relatively minor distortion is induced.

Furthermore, the transient response of the converter is given in Fig. 14. When the load steps from 80 to 160 W, the output voltage restabilizes in about 300 ms. The maximum deviation during the transient is about -40 V (-10% compared with 400 Vdc output). When the load steps from 160 to 80 W, the output voltage deviates by $+60$V, and restabilizes in about 600 ms. The transient response can further be optimized by reducing the output capacitance and optimizing the PI compensator.

B. Comparison With Conventional VoT Control to Achieve Single DCM Operation

With identical power stage and VoT control to achieve a single DCM operation, the results are given in Fig. 15. They are also measured under $v_{\rm in} = 110$ Vac and $v_{\rm in} = 220$ Vac, respectively.

As indicated by the zoom-in plots, VoT control fails to achieve VS, which leads to unpredictable $v_{\rm sw}$ and $i_{\rm sw}$. The operational power under VoT control is between 20 and 120 W with $v_{\rm in} = 110$ Vac. With $v_{\rm in} = 220$ Vac, the operational power is between 30 and 220 W. Higher power is not operational owing to PWM saturation, which limits the maximum input current. Besides, some input current distortion is found in the results. The reason lies in the fixed switching cycle that leads to VS failure.

Furthermore, variations of turn-ON point under UPWC and conventional VoT controls are measured to verify the effectiveness of VS. The results in a half-line cycle are given in Fig. 16, which are measured under 120 W with $v_{\rm in} = 110$ Vac and $v_{\rm in} = 220$ Vac, respectively.

The results under $v_{\rm in} = 110$ Vac are given in Fig. 16(a). With conventional VoT control, the maximum $v_{\rm sw}$ is about 340 V, while $i_{\rm sw}$ changes from -100 to 150 mA. When the power switch is turned ON, the extra-dissipated power in a half-line cycle is 700 mW maximum. With UPWC control, the maximum $v_{\rm sw}$ is about 40 V while $i_{\rm sw}$ changes from -80 to 50 mA in a half-line cycle. When the power switch is turned ON, the extra-dissipated power is 40 mW maximum.

The results under $v_{\rm in} = 220$ Vac are given in Fig. 16(b). With conventional VoT control, the maximum $v_{\rm sw}$ is about 350 V while $i_{\rm sw}$ changes from -50 to 80 mA. When the power switch is turned ON, the extra-dissipated power in a half-line cycle is 700 mW maximum. With UPWC control, the maximum $v_{\rm sw}$ is about 240 V while $i_{\rm sw}$ changes from -50 to 30 mA in a half-line cycle. When the power switch is turned ON, the extra-dissipated power is 400 mW maximum.

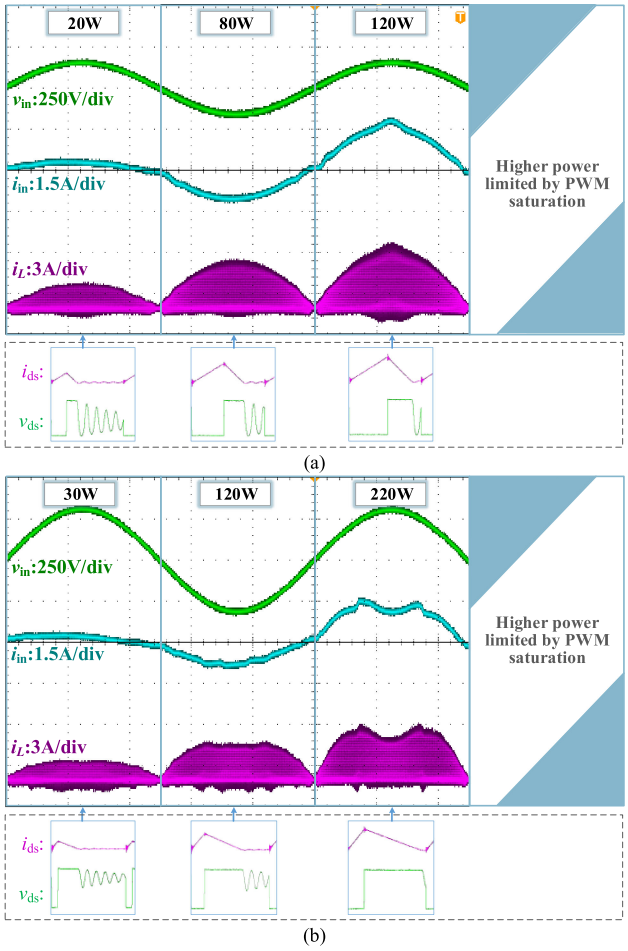

Fig. 15. Inductor current and input current with VoT control to achieve single DCM operation. (a) $v_{\rm in} = 110$ Vac. (b) $v_{\rm in} = 220$ Vac.

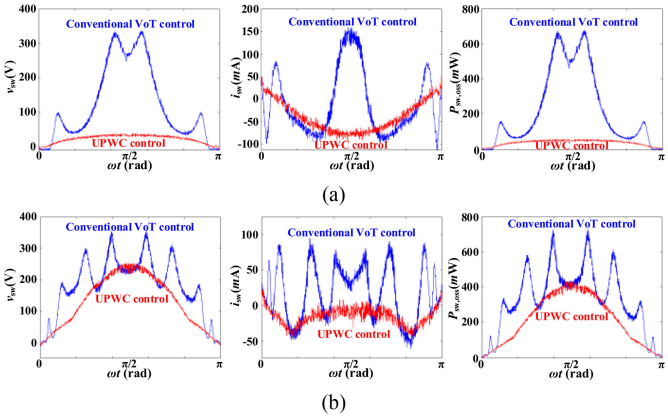

Fig. 16. Variation of $v_{\rm sw}$, $i_{\rm sw}$, and $P_{\rm sw,oss}$ in half a line cycle under 120 W. (a) $v_{\rm in} = 110$ Vac. (b) $v_{\rm in} = 220$ Vac.

According to the results, the proposed UPWC controller can fix $v_{\rm sw}$ to its minimum value and reduce the magnitude of $i_{\rm sw}$. Since $v_{\rm sw}$ is fixed to its minimum value, the UPWC controller

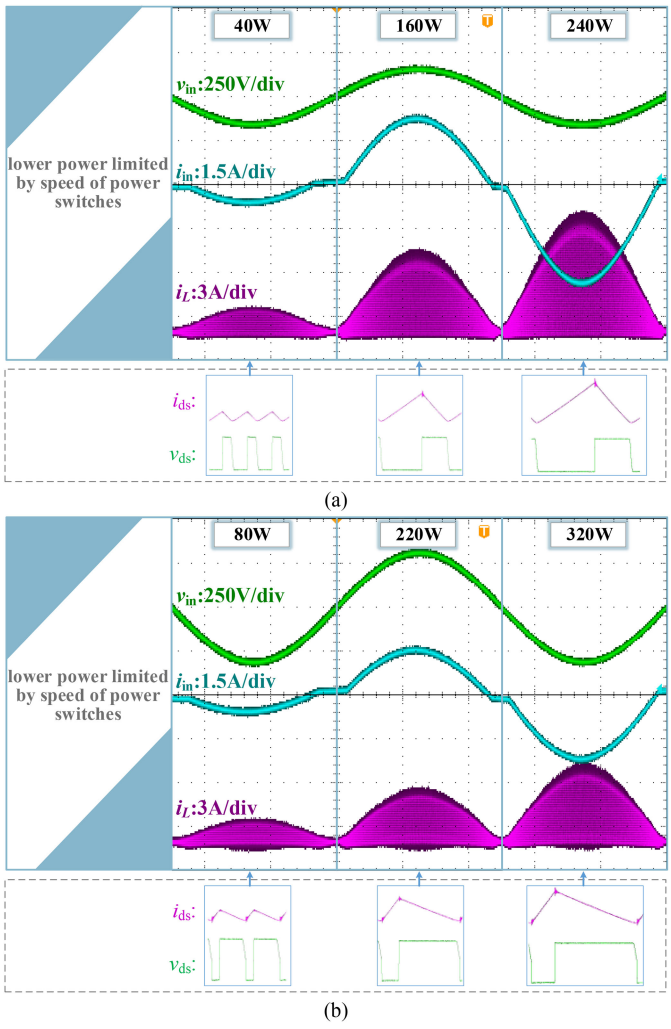

Fig. 17. Inductor current and input current with CoT control to achieve a single CRM operation. (a) 110 Vac. (b) 220 Vac.

reduces the power loss when the power switch is turned ON. With a smaller magnitude and variation rate of i_{sw}, the UPWC controller can reduce the input current distortion and improve the PF.

C. Comparison With Conventional CoT Control to Achieve Single CRM Operation

With identical power stage and CoT control to achieve a single CRM operation, the results are measured under $v_{in} = 110$ Vac and $v_{in} = 220$ Vac, as shown in Fig. 17.

As indicated by the zoom-in plots, CoT control also achieves VS in each switching cycle. The operational power under CoT control is between 40 and 240 W with $v_{in} = 110$ Vac. With $v_{in} = 220$ Vac, the operational power is between 80 and 320 W. Lower power is not operational owing to the limited speed of power switches, which increases heavily at light load. Besides, some zero-crossing distortion is found in the input current. The reason lies in the increased switching frequency and the negative resonant current near the zero-crossing point.

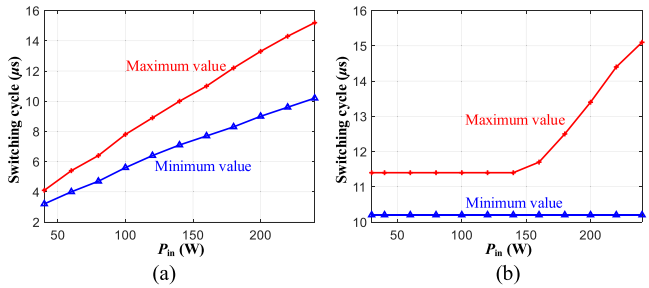

Fig. 18. Maximum and minimum switching cycles in a half-line cycle under 110 Vac input. (a) Conventional CoT control. (b) UPWC control.

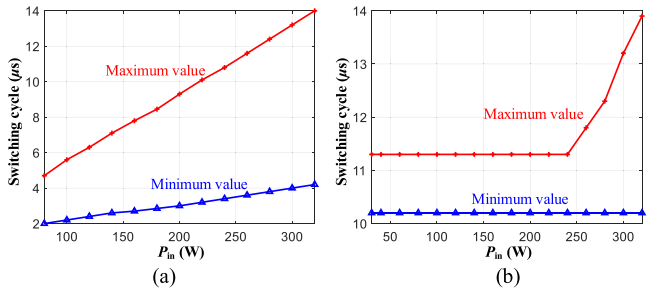

Fig. 19. Maximum and minimum switching cycles in a half-line cycle under 220 Vac input. (a) Conventional CoT control. (b) UPWC control.

Compared with CoT control achieving a single CRM, the proposed UPWC controller can reduce the variation of the switching cycle through partial DCM operation. At different power rates, the maximum and minimum switching cycles within a half-line cycle under 110 Vac and 220 Vac inputs are given in Figs. 18 and 19, respectively.

With 110 Vac input and conventional CoT control, the maximum switching cycle changes linearly from 4 to 15 μs, while the minimum switching cycle changes linearly from 3.2 to 10 μs. Owing to switching loss of the limited speed of the power device, the operational power is clamped above 40 W. With 110 Vac input and UPWC control, the maximum switching cycle changes from 11.4 to 15 μs, while the minimum switching cycle is always around 10.2 μs. The switching cycle is clamped above 10 μs, which reduces the switching loss and the requirement for speed of power devices. As a result, the minimum operational power extends to 20 W.

With 220 Vac input, the gap between maximum and minimum switching cycles enlarges under CoT control. In a half-line cycle, the maximum switching cycle changes linearly from 4.7 to 14 μs, while the minimum switching cycle changes from 2 to 4.2 μs. Owing to the limited speed of the power device and switching loss, the operational power is clamped above 80 W. With 220 Vac input and UPWC control, the maximum switching cycle changes from 11.3 to 13.9 μs, while the minimum switching cycle is around 10.2μs. Since the switching cycle is clamped above 10 μs, the minimum operational power extends to 30 W.

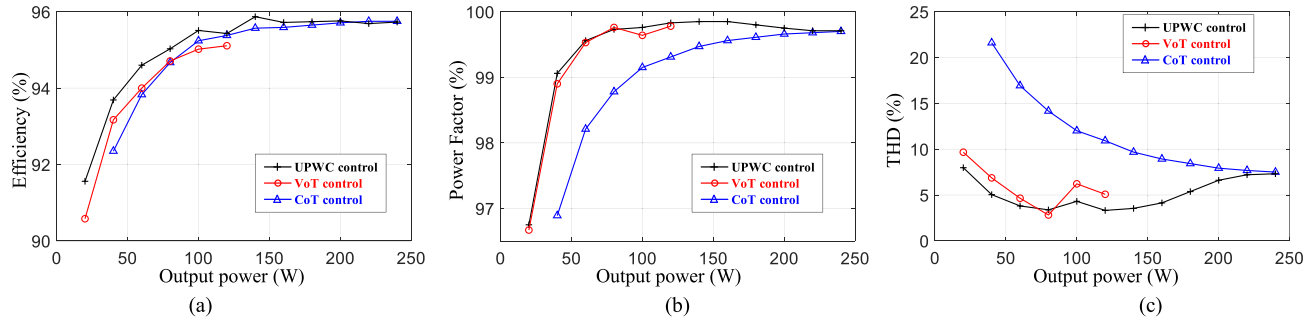

Fig. 20. Comparisons of different controls at $v_{\rm in}$=110 Vac and different powers. (a) Efficiency (b) PF. (b) Total harmonic distortion.

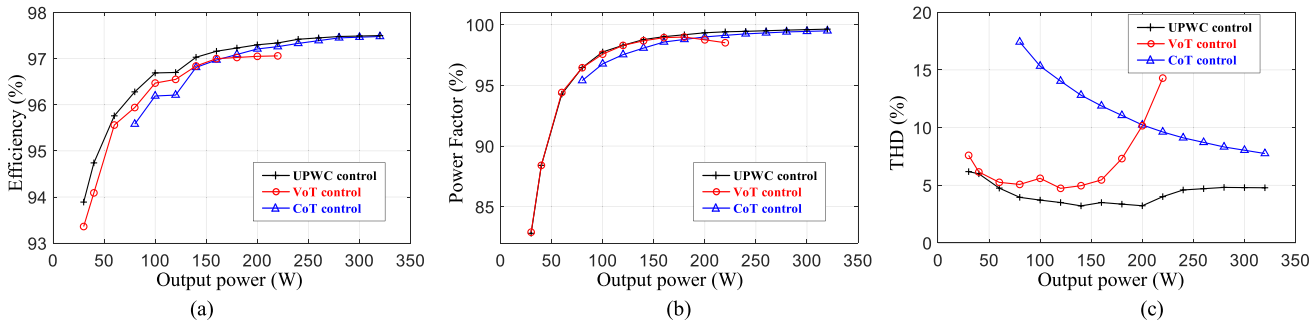

Fig. 21. Comparisons of different controls at $v_{\rm in}$=220 Vac and different powers. (a) Efficiency. (b) PF. (b) Total harmonic distortion.

D. Comprehensive Comparisons of Efficiency, PF, THD, Power Range, and Hardware Cost

Comprehensive comparisons are given for different control strategies in aspects of efficiency, PF, THD, power range, and hardware cost. For $v_{\rm in}$ = 110 Vac and $v_{\rm in}$ = 220 Vac, the measured results are given in Figs. 20 and 21, respectively.

In the aspect of efficiency, the proposed UPWC control strategy achieves the best performance compared with other controls. Considerable improvement is found when the power rate is low. Compared with VoT control to achieve DCM, it reduces the turn-ON loss of the main switch. Compared with CoT control to achieve CRM, it clamps the switching cycle above T, resulting in a reduced switching frequency. This reduces the overall switching loss (consists turn-ON and turn-OFF losses), especially at light load. Although the improvement in overall efficiency is less than 1%, the reduced energy loss can still benefit the heat on the power transistor and improve the system reliability.

In the aspect of PF and THD, the proposed UPWC control strategy has the highest PF and lowest THD in most conditions. Compared with single-mode controllers, the improvement is achieved through effective VS and near-constant switching cycle at light load. With 110 Vac input, the PF under UPWC control changes from 96.8% to 99.9%, while the average THD is 5.1% in the whole power range. With 220 Vac input, the PF under UPWC control is 99.6% maximum and it maintains above 95% in most conditions. The achieved average THD is 4.3% in the whole power range. The PF under 220 Vac input is mainly degraded by the phase distortion of input current, which is determined by the input filter and input resistance of the boost stage. Compared with 110 Vac input, the equivalent input resistance of the boost stage is higher under 220 Vac, which leads to considerable phase distortion of input current that dominates the PF.

In the aspect of power range, the proposed UPWC control strategy maintains single DCM at light load, while achieves mixed DCM/CRM or single CRM at heavy load. Furthermore, it extends the operational power range to the sum of VoT and CoT controls. For VoT control to achieve DCM, the maximum power rate is mainly limited by PWM saturation. For CoT control to achieve CRM, the minimum power rate is mainly limited by the speed of power devices.

Furthermore, Table II compares the performance of the proposed UPWC control with other papers. Through DCM/CRM/mixed-mode operation, the proposed UPWC controller features a reduced variation of switching frequency and consistent VS. Therefore, it extends the power range and achieves preferable performances in the whole power range.

Finally, in the aspect of hardware cost, the UPWC control induces more hardware than conventional VoT and CoT controls. Since all control strategies are implemented through FPGA, the usage of logic elements and registers is compared in Table III. The UPWC controller requires 17.8%–34.5% more in total logic elements, and 25.3%–31.4% more in total registers.

As a conclusion, compared with conventional VoT and CoT controls, the proposed UPWC control strategy extends the power range through mixed DCM/CRM operations. Furthermore, through consistent VS and clamping the switching cycle,

TABLE II
COMPARISON WITH OTHER CONTROLS (@220 VAC INPUT)

		This paper	[11]	[12]	[18]	[19]	[23]	[25]
Output voltage (VDC)		400	400	400	400	400	400	380
Tested power range (W)		30-320	40-200	32-160	24-120	120	18-55	48-108
Switching frequency f_{sw} (kHz)		70-100	N/A	N/A	30-160	30@120W	N/A	N/A
Efficiency (%)	@20% load	96.0	N/A	94.3	N/A	N/A	93	N/A
	@100% load	97.5	N/A	98.2	97.3	97.8	N/A	N/A
PF (%)	@20% load	94.8	94.7	88.8	N/A	N/A	99.1	N/A
	@100% load	99.6	99.6	99.2	92.8	92.5	N/A	N/A
THD (%)	@20% load	4.5	11.1	13.5	N/A	N/A	13.5@40% load	4.9 @44%load
	@100% load	4.7	2.1	2.9	N/A	N/A	8	2.7
Controller realization		FPGA	DSP	DSP	Analog	DSP	MCU	Digital
Operation mode		DCM/CRM/mixed	CRM	CRM	CRM	CRM	DCM	DCM
Features		Reduced variation of switching frequency, valley switching	Adaptive to parameter variations, valley switching		Quasi-fixed f_{sw} in a half-line cycle		Valley switching	Valley skipping

TABLE III
USAGE OF LOGIC ELEMENTS AND REGISTERS OF DIFFERENT CONTROLS

Control strategies	Conventional VoT control	Conventional CoT control	UPWC control
Total logic elements	6141	5376	7232
Total registers	4396	4193	5509

the UPWC controller optimizes the efficiency, PF, and THD in all power range. Nevertheless, it induces higher hardware costs owing to its increased calculations.

V. CONCLUSION

This article presents a UPWC control strategy for a boost PFC converter, where both pulsewidth and switching cycle are modulated to achieve unity PF and consistent VS. Depending on the power rate, it achieves single DCM, mixed DCM/CRM, and single CRM operations in a half-line cycle. No matter in DCM or CRM, consistent VS reduces both the switching loss and current distortion caused by parasitic resonance. Furthermore, compared with conventional VoT control to achieve DCM, the proposed UPWC controller has an enlarged power rate, reduced current distortion, and reduced turn-ON loss of power switch. While compared with conventional CoT control to achieve CRM, it greatly reduces the variation of the switching cycle by partial DCM operation. This reduces the zero-crossing distortion and switching loss at light load, and further allows for a lower power rate. Finally, the proposed UPWC control strategy achieves preferable performances in aspects of efficiency, PF, THD, and power range.

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