Letters

Understanding Electrical Parameter Degradations of P-GaN HEMT Under Repetitive Short-Circuit Stresses

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***Abstract*—In this letter, comprehensive static and dynamic electrical parameter degradations of p-GaN gate high electron mobility transistor (HEMT) under repetitive short-circuit (SC) stresses are presented. Meanwhile, the mechanisms behind those degradations are first distinguished. The results indicate that both the gate region and the access region are damaged by the SC stresses, dominating the shifts of electrical parameters. Moreover, a method by modeling the output capacitance is proposed to characterize damages in access region. Finally, the switching characteristics after the stresses are investigated, it is found that the switching speed benefits from the increase in the gate leakage current. Considering the aging of p-GaN HEMT under long-term operation conditions, all the damages brought by repetitive SC stresses should be eliminated to prevent the failure of p-GaN gate and the increase in conduction loss.**

***Index Terms*—Electrical parameter degradations, P-GaN high electron mobility transistor (HEMT), repetitive short circuit.**

I. Introduction

Enhancement-mode (E-mode) GaN-based high electron mobility transistors (HEMTs) have been applied in power electronic systems to achieve energy saving by improving the operation frequency and energy conversion efficiency [1]. However, reliability problems are always the obstacles that constrain the further development of GaN-based power devices since the related investigations are still insufficient [2], [3]. In some application scenarios, such as *LLC* resonant circuits, reliability problems of GaN HEMTs may appear due to circuit faults, bringing the failure and degradations to power electronic systems. As one of the circuit faults, short-circuit (SC) fault is incident due to the failure of load and the fault of gate control signal [4]. Thus, the investigations of GaN HEMT under SC conditions are indispensable.

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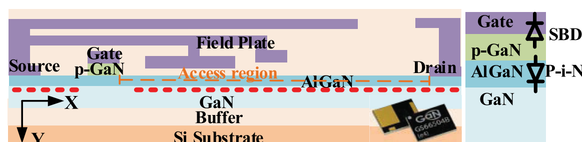

Fig. 1. (a) Schematic cross-sectional view of the investigated p-GaN HEMT. (b) Model of gate stack.

E-mode GaN HEMT with p-GaN gate layer and Schottky type gate contact is one kind of commercially available GaN power devices of great application potential. Previous investigations on the reliability problems of p-GaN HEMT caused by SC were mainly focused on the robustness and failure mode under single-event SC condition[5]–[7]. Some investigations also reported the degradations of electrical parameters including threshold voltage ($V_{\rm th}$), ON-state resistance ($R_{\rm ON}$), gate leakage current ($I_{\rm gss}$), and drain leakage current ($I_{\rm dss}$) under repetitive SC conditions [8], [9]. However, the work in [8] mainly showed degradation phenomena, and the work in [9] mainly investigated the p-GaN devices with ohmic gate contact. The degradation phenomena in above reports were still incomprehensive, even worse, physics-based analyses remained simple and insufficient.

In this letter, the electrical parameter degradations of p-GaN HEMT with Schottky-type gate contact under repetitive SC stresses are comprehensively investigated by experiments and technology computer-aided design (TCAD) simulations.

II. Device Structure and Experiments

Fig. 1(a) shows the schematic cross section view of the investigated 650 V/15 A p-GaN HEMT from GaNSystem, Inc., (GS66504B). The gate stack of this device can be modeled as a metal/p-GaN Schottky barrier diode (SBD) and a P-i-N (p-GaN/AlGaN/GaN) diode in series, as shown in Fig. 1(b). In the TCAD simulations, the physics-based models have been calibrated and the results well match the typical experimental data [10]. Fig. 2(a) shows the topology of the SC test circuit.

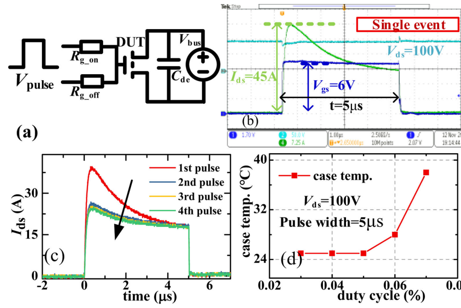

Fig. 2. (a) Topology of the test circuit. (b) Typical single-pulse SC waveforms. (c) $I_{\rm ds}$ degradations. (d) Case temperature rise.

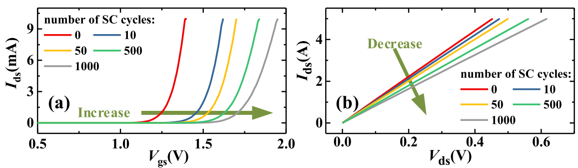

Fig. 3. Shifts of (a) $I_{\rm ds}$–$V_{\rm gs}$ and (b) $I_{\rm ds}$–$V_{\rm ds}$ curves after the stresses.

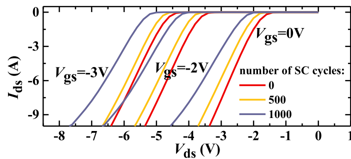

Fig. 4. Degradations of reverse conduction characteristics.

Fig. 2(b) shows the typical single-pulse SC waveforms including gate to source voltage ($V_{\rm gs}$), drain to source voltage ($V_{\rm ds}$), and drain to source current ($I_{\rm ds}$), when the bus voltage ($V_{\rm bus}$) equals to 100 V. Fig. 2(c) shows the $I_{\rm ds}$ waveforms under repetitive SC condition with duty cycle of 0.05% and pulsewidth of 5 μs. The duty cycle should be controlled within a small value during the experiments since high duty cycle leads to high case temperature ($T_{\rm case}$), as shown in Fig. 2(d). During the experiments, the device is heated by a ceramic heater and the tube case temperature is monitored by a thermocouple. All the typical electrical parameters are measured by Keysight B1505A.

III. Results and Discussions

A. Static Electrical Performance Degradations and Analysis

Typical electrical performances of the investigated device are acquired after repetitive SC stresses. Fig. 3 shows the shifts of $I_{\rm ds}$–$V_{\rm gs}$ and $I_{\rm ds}$–$V_{\rm ds}$ curves. It is observed that both $V_{\rm th}$ (extracted at $V_{\rm ds} = 0.1$ V and $I_{\rm ds} = 1$ mA) and $R_{\rm ON}$ (extracted at $V_{\rm gs} = 6$ V and $I_{\rm ds} = 5$ A) are increased. Fig. 4 shows that the reverse conduction characteristics, the reverse voltage drop ($V_{\rm ds_r}$, extracted at $I_{\rm ds} = -1$ mA), and reverse ON-state resistance ($R_{\rm ON_r}$, slope of the curves, extracted at $I_{\rm ds} = -5$ A) are also increased, which result from the combined influences of $V_{\rm th}$ and $R_{\rm ON}$. Moreover, $I_{\rm dss}$ with $V_{\rm ds}$ increasing ($V_{\rm gs} = 0$) and $I_{\rm gss}$ with $V_{\rm gs}$ increasing ($V_{\rm ds} = 0$ V) are also presented, as shown in Fig. 5; the results indicate that $I_{\rm dss}$ remains stable but $I_{\rm gss}$ is increased after the SC stresses.

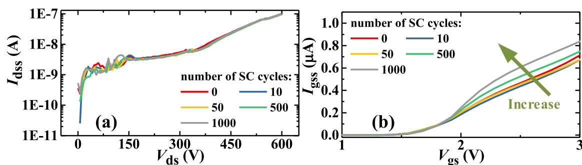

Fig. 5. Variations of (a) $I_{\rm dss}$ and (b) $I_{\rm gss}$ after the stresses.

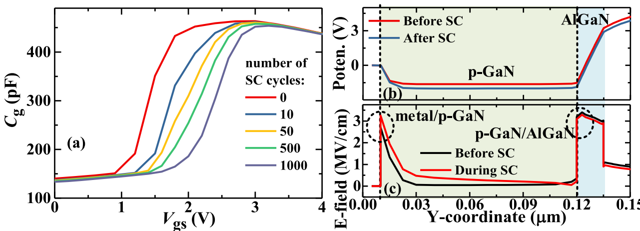

Fig. 6. Analyses on p-GaN gate. (a) Measured $C_{\rm g}$ with $V_{\rm gs}$ increasing. (b) Potential and (c) E-field distributions in p-GaN gate region.

As reported, the path of $I_{\rm dss}$ locates in buffer layer [11], thus the stable performance of $I_{\rm dss}$ indicates that the buffer layer is little damaged by the SC stresses. Accordingly, gate region and barrier layer are considered to be damaged by SC stresses. To distinguish these damages, further experiments and TCAD simulations have been carried out.

The measured gate capacitance ($C_{\rm g}$) with $V_{\rm gs}$ increasing in Fig. 6(a) presents positive shifts, which consist with the phenomena of $V_{\rm th}$. Since the lift-up points of $C_{\rm g}$–$V_{\rm gs}$ curves represent the formation of channel under gate region [12], it can be understood that the gate region is indeed influenced by the SC stresses. As modeled in Fig. 1(b), the p-GaN layer between the SBD and P-i-N diode is floating, the SC induced carries can be stored there, then leading to the change of potential distribution in p-GaN layer, as shown in Fig. 6(b). Therefore, the potential in channel under gate region can be changed and the $V_{\rm th}$ is influenced. Meanwhile, as shown in Fig. 6(c), the E-field along p-GaN/AlGaN interface is also a large value under the SC stresses, which leads to the ionization of acceptor traps there. Then, the ionized charges can be depleted by the high drain to gate voltage bias. Once the stresses are withdrawn, the resetting of charges under gate region needs some time, thus $V_{\rm th}$ is influenced. These results prove the analyses in [13] and [14].

On the other hand, when positive $V_{\rm gs}$ is applied, the SBD in gate stack is reversely biased. Hence, $I_{\rm gss}$ is determined by the reverse leakage current of reversely biased SBD. During the SC stresses, the E-Field along the metal/p-GaN interface can be enhanced, as shown in Fig. 6(c), which can active more interface states to help carriers cross through the metal/p-GaN junction. In this way, the reverse leakage current of SBD is increased, accordingly, $I_{\rm gss}$ is increased.

Similar with the phenomena of current collapse, the degradations of $R_{\rm ON}$ may result from the damages in access region [15], which are different from the damages in p-GaN gate region. To distinguish the damages in gate region and in access region, $T_{\rm case}$ has been changed during the experiments. As shown in Fig. 7(a), the SC stresses and temperature stress are applied at the same time at the beginning. In 1 min, the device can be heated to the

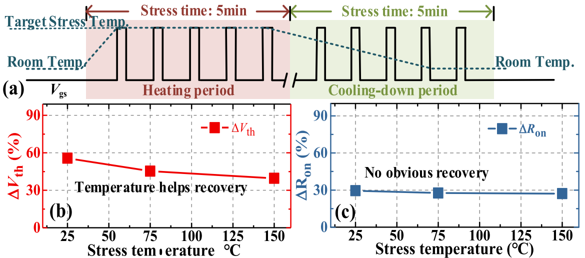

Fig. 7. Repetitive SC stresses under different T_{case}. (a) Stress strategy. Measured (b) V_{th} and (c) R_{ON} after 10-min SC stresses.

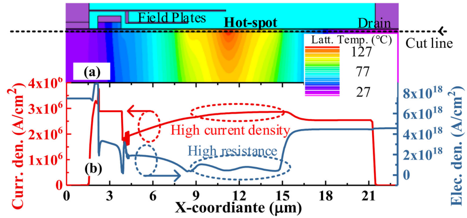

Fig. 8. TCAD simulation results under SC condition. (a) Lattice temperature distribution. (b) Extracted current density values and electron density values along AlGaN/GaN interface at the peak I_{ds}.

target T_{case}. After 5 min of SC stresses, the temperature stress is withdrawn. Then, the device is cooling down still with SC stress for 5 min and T_{case} falls back to initial value. The results shown in Fig. 7(b) and (c) signify that the degradations of V_{th} are changed by high T_{case} while the degradations of R_{ON} are not. Thus, the mechanisms behind the degradations of R_{ON} are indeed different from those of V_{th}, which are further validated by simulations.

Fig. 8(a) shows the simulation results of lattice temperature (T_{lat}) distributions when the SC stress is present with $V_{\mathrm{gs}} = 6$ V and $V_{\mathrm{ds}} = 100$ V. The pulsewidth and peak current in the simulations are 5 μs and 24 A, respectively. The model named *lat.temp* in the software is used to calculate T_{lat}. It can be seen that T_{lat} is high under the end of field plate in access region, which results from the high power caused by high current density and high resistance there, as shown in Fig. 8(b). Since the heat in the center of the hot area is not significantly conducted in the short time interval, a hot spot appears, leading to the high risk of damage in access region.

Considering the damages in access region can influence the values of capacitances, and the shifts of output capacitance ($C_{\mathrm{oss}} = C_{\mathrm{gs}} + C_{\mathrm{ds}}$) can be used to characterize these damages. Fig. 9(a) shows the measured C_{oss} with V_{ds} increasing after the SC stresses. Each rapid change in the slope indicates the change of depletion region [16], according to which the lateral direction of the p-GaN HEMT is divided into six regions, as shown in Fig. 9(b). It can be seen that the shifts of curves exist from region B to region E, thus damages in these subdivided regions are characterized. By using the formula in following equation, the charges in region D are calculated to be $2 \times 10^{18}\mathrm{cm}^{-3}$:

$$D_{\mathrm{trap}} = C_{\mathrm{oss}}\Delta V_{\mathrm{ds}}/\left(qd_{\mathrm{AlGaN}}W\right) \tag{1}$$

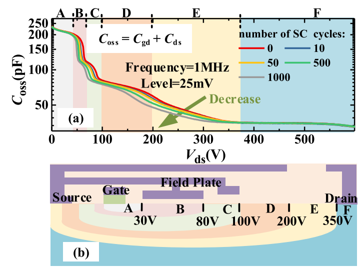

Fig. 9. Characterizing the damages. (a) Segmental shifts of C_{oss}. (b) Sketch of the division of the depletion region according to the sudden changes of the C_{oss} versus V_{ds} curves.

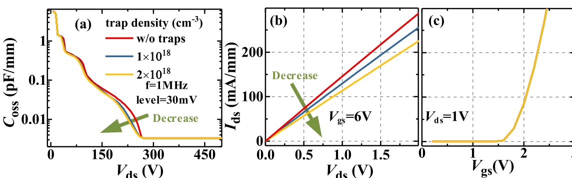

Fig. 10. Simulated (a) C_{oss}, (b) I_{ds}–V_{ds} curves, and (c) I_{ds}–V_{gs} curves with acceptor traps in AlGaN barrier layer.

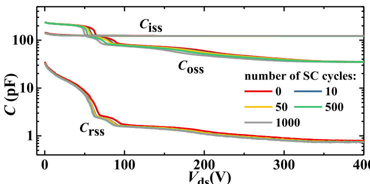

Fig. 11. Variations of C_{iss}, C_{oss}, and C_{rss}.

where D_{trap} is the charge density, d_{AlGaN} is the thickness of the AlGaN barrier (assuming as 15 nm), and W is the total width of the investigated device (assuming as 15 mm).

Further simulations have been carried out to prove above-mentioned analysis. As Fig. 10 shows, with traps in barrier layer (only access region), the simulated degradation trends of C_{oss} and R_{ON} consist with the measured results, however, the simulated V_{th} shows no shifts. The results prove that there are damages in access region and the degradations of V_{th} result from different reasons.

To conclude, the repetitive SC stresses bring damages to both p-GaN gate region and access region. The trapping and carrier storage in p-GaN gate region lead to the increase in V_{th}, whereas the damages in metal/p-GaN interface lead to the increase in I_{gss}. On the other hand, the trapping in access region leads to the increase in R_{ON}. The degradations of V_{th} and R_{ON} bring combined influences to $V_{\mathrm{ds_r}}$ and $R_{\mathrm{ON_r}}$.

B. Dynamic Electrical Performance Degradations and Analysis

Terminal capacitances of the investigated devices after SC stresses are measured, as shown in Fig. 11, and the input capacitance ($C_{\mathrm{iss}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}$) shows nearly no changes, whereas the C_{oss} and reverse capacitance ($C_{\mathrm{rss}} = C_{\mathrm{gd}}$) show negative shifts. Since the trapping effect in gate to drain access region influences

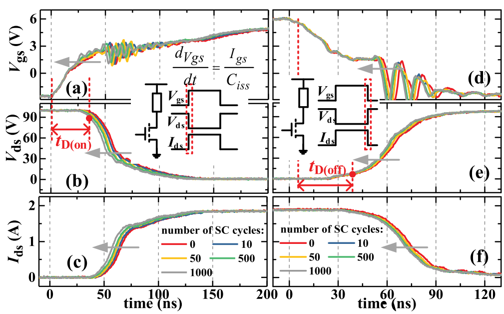

Fig. 12. Measured switching performances after the SC stresses. (a) V_{gs}, (b) V_{ds}, and (c) I_{ds} of turn-ON process. (d) V_{gs}, (e) V_{ds}, and (f) I_{ds} of turn-OFF process.

TABLE I
SUMMARY OF THE DEGRADATIONS OF ELECTRICAL PARAMETERS

V_{th}	R_{on}	$R_{\mathrm{on_r}}$	I_{gss}	I_{dss}	C_{gd}	C_{oss}	C_{iss}	$t_{\mathrm{D(on)}}$	$t_{\mathrm{D(off)}}$
Incr.	Incr.	Incr.	Incr.	-	Decr.	Decr.	-	Decr.	Decr.

drain to source capacitance (C_{ds}) and gate to drain capacitance (C_{gd}), the shifts of C_{rss} and C_{oss} are observed. On the other hand, the trapping effect in p-GaN gate brings little influence to C_{gs}, which is determined by the smaller series depletion capacitances under p-GaN region. In this way, C_{iss} performs stably.

Switching characteristics with resistive load after the SC stresses are also investigated. The measurements are carried out by using self-designed printed circuit board. Fig. 12(a)–(c) shows the turn-ON process, whereas Fig. 12(d)–(f) shows the turn-OFF process. Both the turn-ON delay time ($t_{\mathrm{D(ON)}}$) and turn-OFF delay time ($t_{\mathrm{D(OFF)}}$) become smaller after the SC stresses. Generally, higher V_{th} leads to reduced dV_{gs}/dt [17], which is different from the measured phenomenon here. In fact, the damages of gate brought by SC stresses also lead to the increase in I_{gss}. Once the gate current is larger, dV_{gs}/dt can be larger during the switching processes [18]. In this way, smaller $t_{\mathrm{D(ON)}}$ and $t_{\mathrm{D(OFF)}}$ are observed. The results indicate that, for switching characteristics, the influences of I_{gss} variations are more significant than the influences of V_{th} and R_{ON} variations.

In summary, the degradation trends of the investigated electrical parameters are shown in Table I, where the increase trend is marked as "Incr.," and the decrease trend is marked as "Decr." Although the increases in I_{gss} bring benefits to $t_{\mathrm{D(ON)}}$ and $t_{\mathrm{D(OFF)}}$, they still should be avoided to prevent the failure of p-GaN gate considering the device aging. Moreover, when the devices are applied in power electronic systems, the increases in R_{ON} and $R_{\mathrm{ON\cdot r}}$ can lead to the increase in conduction loss and limit the advantages of p-GaN HEMT. For further developments of p-GaN HEMT, eliminating the influences of SC stresses is highly required, which can be achieved by designing the device structure or adding protection circuit.

IV. CONCLUSION

The behaviors of Schottky gate p-GaN HEMT under repetitive SC stresses are investigated in this letter. The investigations indicate that the trapping and carrier storage in p-GaN gate region lead to the increases in V_{th} while the damages in metal/p-GaN interface lead to the increases in I_{gss}. Meanwhile, the damages in access region lead to the increases in R_{ON} and C_{oss}. The degradations of V_{th} and R_{ON} bring combined influences to $V_{\mathrm{ds_r}}$ and $R_{\mathrm{ON_r}}$. Moreover, a method by modeling the shifts of C_{oss} is proposed to characterize the damages in access region, which is of value for further modeling the long-term operation life time. Finally, the switching characteristics after the repetitive SC stresses are investigated, some benefits of $t_{\mathrm{D(ON)}}$ and $t_{\mathrm{D(OFF)}}$ can be achieved from the increases in I_{gss}. However, all the degradations of electrical parameters brought by repetitive SC stresses should be eliminated to prevent the failure of p-GaN gate and the increase in conduction loss.

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