# Research on Topology and Control Method of Transformer-Free Dual-Frequency Grid-Connected Inverter

Liyong Yang, Peng Zhang, and Shuo Liu

***Abstract*—In order to suppress leakage current and improve the efficiency of the transformer-free grid-connected inverter, a novel topology and control method is proposed. The proposed inverter consists of a power inverter unit and an auxiliary converter unit, and the two units are connected by a capacitor on the dc side. The power inverter unit transmits power to the grid at a low switching frequency for reducing power losses. The auxiliary converter unit operates at a high switching frequency, and adopts a feedforward control method to eliminate the grid current switching ripples. The voltage of parasitic capacitance between the photovoltaic array and the ground is stabilized by the auxiliary converter unit with the bipolar modulation scheme, so the leakage current can be suppressed more effectively. A 1-kW prototype was built and tested, and the experimental results are finally presented to show the performance of the proposed inverter.**

***Index Terms*—Common-mode model, dual-frequency grid-connected inverter, leakage current, power quality.**

## I. Introduction

SOLAR photovoltaic (PV) is an important renewable energy source with many advantages such as environment-friendly characteristic, low maintenance cost, easy installation, etc. [1]–[4]. Therefore, the low-power and medium-power PV generation systems play an important role in the development of distributed electric power systems [5]–[8]. As the power interfaces in grid-connected PV systems, the transformer-free inverters have the advantages of high efficiency, low cost, small size, and light weight [9], [10]. However, the leakage current of the transformer-free grid-connected inverter must be suppressed. If the leakage current is higher than a certain level, it will pose a threat to other grid-connected systems or maintenance personnel [11], [12].

Efficiency and power density are important indicators for evaluating converter performance. To improve conversion efficiency, increase power density and reduce leakage current, many new topologies and modulation schemes of transformer-free grid-connected inverters are proposed [13]. To suppress leakage current, PV panels are isolated from the ac grid by introducing freewheeling paths in many reported topologies, such as H5 topology of SMA [14], high efficient and reliable inverter concept (HERIC) topology of Sunways [15], diverse H6s [16], [17], etc. For above topologies, it is obvious that the lower the switching frequency, the higher the efficiency of the inverter, and the larger the size of the passive components. Therefore, there is a tradeoff between efficiency and power density [18]–[21].

Soft switching technology is an effective method to solve the tradeoff between power density and efficiency. However, it may reduce the reliability of the inverter and increase the complexity of the circuit [23]. In [24], an $S_{3L}$ three-level inverter based on soft switching technology is proposed, and switching losses of switches and diodes can be avoided by adding some passive components. Unfortunately, the two-stage differential mode (DM) voltage degrades the performance of the output DM and common mode (CM) voltage. In [25], the concept of auxiliary resonant commutation poles is introduced into PV inverters, which can reduce switching losses. However, its impact on the CM performance of PV inverters has not been discussed yet.

The pulse width modulation scheme has great influence on the performance of the inverter. For a two-level single-phase grid-connected inverter, bipolar pulse width modulation (BP-PWM) scheme can be adopted to reduce leakage current [22]. However, compared with unipolar width modulation (UP-PWM) scheme, larger output filters are required when BP-PWM scheme is adopted. In addition, it should be noted that the potential of the freewheeling path should be clamped to half of the input voltage, instead of only disconnecting the PV array from the grid, during the freewheeling period [26], [27].

The reactive power injection is also an important challenge in grid-friendly PV systems [28]. The BP-PWM scheme can provide reactive power. Unfortunately, compared with the UP-PWM scheme, it will generate additional switching losses and larger current ripple [29]. Therefore, many attempts have been made to improve the modulation scheme. For H5 inverter, a novel combination of UP-PWM and BP-PWM scheme is proposed in [30], but it has not completely eliminated the adverse effects of the BP-PWM scheme.

In order to solve the tradeoff between efficiency and power density of the grid-connected inverter with isolation transformer, a parallel dual-frequency inverter is proposed in [31] and [32], which uses feedforward compensation to eliminate switching

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TABLE I
MAIN PARAMETERS OF THE HERIC INVERTER

| Parameters | HERIC inverter |
|---|---|
| Grid voltage $V_g$ (RMS) | 110 V |
| Grid current amplitude $i_{Gm}$ | 15 A |
| DC-link voltage $V_{DC}$ | 200 V |
| Switching frequency $f_s$ | 7 kHz |
| Modulation method | Unipolar SPWM |
| Filter inductance $L$ | 3 mH |
| Switches (Si-IGBT) | AUIRGPS4070D0 |

TABLE II
MAIN PARAMETERS OF THE HERIC + *CP* INVERTER

| Parameters | HERIC+$C_P$ inverter |
|---|---|
| Grid voltage $V_g$ (RMS) | 110 V |
| Grid current amplitude $i_{Gm}$ | 15 A |
| DC-link voltage $V_{DC}$ | 200 V |
| Switching frequency $f_s$ | 7 kHz |
| Modulation method | Unipolar SPWM |
| Filter inductance $L$ | 3 mH |
| Parallel capacitance $C_P$ | 0.5 μF |
| Switches (Si-IGBT) | AUIRGPS4070D0 |

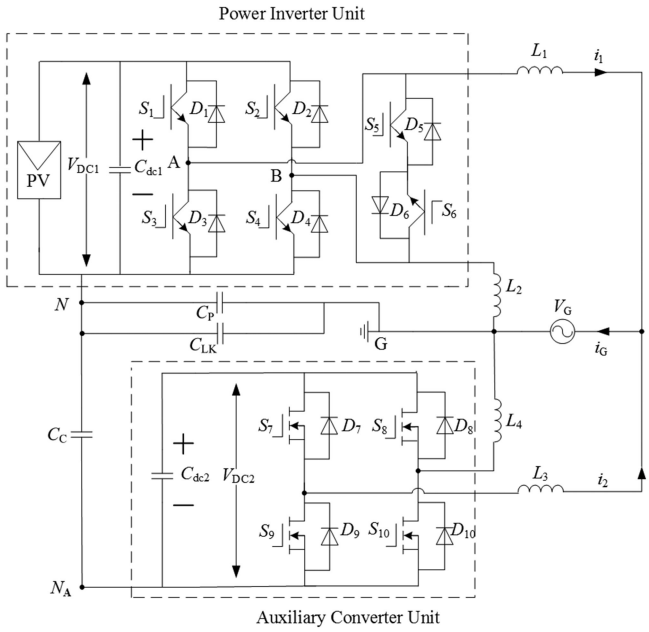


Fig. 1. Transformer-free dual-frequency grid-connected inverter system.

harmonics without extracting current harmonics as current reference. The dual-frequency inverter includes a power inverter unit and an auxiliary converter unit. The dc electrical energy is injected into the power grid by the power inverter unit at a low switching frequency. The auxiliary converter unit with a high switching frequency adopts the feedforward control method to generate harmonic elimination current to ensure the power quality. It provides a new idea to reduce switching losses of power devices and improve power quality.

The HERIC topology has the advantages of low conduction loss, high conversion efficiency, high reliability, and low leakage current [33]. Therefore, based on the HERIC topology and parallel dual-frequency inverter, a transformer-free dual-frequency grid-connected inverter is proposed in this article. Different from [31] and [32], the new contributions of this article are as follows.

1) To suppress leakage current of the transformer-free grid-connected inverter more effectively, a novel topology is proposed which includes a power inverter unit and an auxiliary unit. The power inverter unit adopts the HERIC topology. The two units are connected by connection capacitor $C_C$, and the parallel capacitor $C_P$ is inserted between the negative terminal of the dc-link and the ground.
2) For the proposed topology, the principle of suppressing leakage current is explained by the leakage current model, and the impact of parametric variation of passive elements over the leakage current is discussed. The leakage current suppression effect is verified by experimental results.

The rest of this article has been organized as six sections. In Section II, the topology, modulation scheme and leakage current model of the proposed inverter are introduced. In Section III, the principle of leakage current suppression is analyzed in detail, and the impact of parametric variation of passive elements over the leakage current is discussed. The harmonic elimination principle and control strategy of the proposed inverter is introduced in Section IV. The experimental results are shown in Section V, which validates the correctness of the theoretical analysis. Finally, the conclusion is given in Section VI.

## II. TOPOLOGY AND LEAKAGE CURRENT MODEL OF THE TRANSFORMER-FREE DUAL-FREQUENCY GRID-CONNECTED INVERTER

### A. Topology of the Proposed Inverter

The topology of the transformer-free dual-frequency grid-connected inverter is shown in Fig. 1, which consists of a power inverter unit and an auxiliary converter unit. The power inverter unit adopts the HERIC topology. In the power inverter unit, $S_{1-6}$ are six power devices with corresponding antiparallel diodes $D_{1-6}$. $L_1$ and $L_2$ are the filter inductances, $L_1 = L_2$. The PV-array is disconnected from the load by $S_5$ and $S_6$ during periods of zero output voltage of the inverter. The auxiliary converter unit consists of four power switches ($S_{7\text{-}10}$) with antiparallel diodes $D_{7\text{-}10}$, which adopts the BP-PWM scheme. $L_3$ and $L_4$ are the filter inductances, $L_3 = L_4$. For the sake of simplicity, $L_P$ represents the total filter inductance of the power inverter unit, which is equal to $L_1 + L_2$. Similarly, $L_A$ represents the total filter inductance of the auxiliary converter unit, which is equal to $L_3 + L_4$. The two units are connected in parallel with the grid through the filter inductors. From Fig. 1, the filters of these two units are *L* type, so there is no need to consider the inherent resonance of the *LCL* filter.

The dc electrical energy is injected to the power grid by the power inverter. In order to reduce its switching losses, the power inverter unit operates at a low switching frequency (2.5 kHz). Moreover, based on the feedforward compensation control, the switching current ripple and low order current harmonics of the power inverter unit are eliminated by the output current of

the auxiliary converter unit with a high switching frequency. Therefore, the proposed inverter is named as transformer-free dual-frequency grid-connected inverter.

In Fig. 1, $N$ and $N_A$ are the negative terminals of the dc-link of the power inverter unit and auxiliary converter unit, respectively. $V_{\mathrm{GNA}}$ represents the voltage between $N_A$ and ground, $V_{\mathrm{GN}}$ represents the voltage between $N$ and ground. Since the auxiliary converter unit adopts BP-PWM scheme, there are only fundamental component and dc component in $V_{\mathrm{GNA}}$. While the power inverter unit adopts the hybrid modulation scheme, $V_{\mathrm{GN}}$ includes dc component, fundamental component, and high frequency harmonic components.

In Fig. 1, $C_{\mathrm{LK}}$ is the parasitic capacitance between the PV array and $G$ and $C_{\mathrm{P}}$ is the parallel capacitor, which is inserted between $N$ and $G$. The negative terminals of the two units are connected through the capacitor $C_{\mathrm{C}}$. Therefore, the voltage $V_{\mathrm{GN}}$ can be stabilized by $C_{\mathrm{C}}$ and the auxiliary converter unit during the zero-voltage state of the power inverter unit. Moreover, the dc circulating current between $N$ and $N_A$ is blocked by $C_{\mathrm{C}}$. This is the reason why the leakage current of the proposed inverter is smaller than that of the traditional HERIC inverter [22].

Compared with HERIC inverter, an additional auxiliary converter unit is used in the proposed dual-frequency inverter. Therefore, the number of power devices in the proposed inverter is greater than the number of power devices in the HERIC inverter. However, since the operating current of the auxiliary converter unit is about 1/10 of the rated current, its cost is much lower than that of the power inverter unit. In addition, the auxiliary converter unit adopts a feedforward control method to eliminate the grid current switching ripple, so the total inductance of the proposed inverter is smaller than that of the HERIC inverter, which is beneficial to reduce its volume and cost.

Therefore, compared with the HERIC inverter, the volume and cost of the proposed inverter will not increase significantly.

### B. Modulation Scheme and Leakage Current Model

As mentioned above, the auxiliary converter unit adopts BP-PWM scheme, $V_{\mathrm{GNA}}$ is independent of the states of the $S_{7\text{–}10}$. According to Fig. 1, $V_{\mathrm{GNA}}$ can be given by

$$V_{\mathrm{GNA}} = \frac{V_{\mathrm{DC2}} - V_{\mathrm{G}}}{2} \tag{1}$$

where $V_{\mathrm{DC2}}$ is the dc-link voltage of the auxiliary converter unit, and $V_{\mathrm{G}}$ is grid voltage.

The simplified equivalent circuit of the proposed inverter is shown in Fig. 2**.** For simplicity, the auxiliary converter unit is approximated as a voltage source in Fig. 2, where $L_{\mathrm{EA}}$ is the equivalent inductance of the auxiliary converter unit, $L_{\mathrm{EA}} = L_{\mathrm{A}}/2$, and $R_C$ is the equivalent resistance of $C_{\mathrm{c}}$.

The power inverter unit adopts the hybrid modulation scheme shown in Fig. 3, where $i_1$ is the output current. This modulation scheme has the advantages of high efficiency, good current quality, and proper reactive power capability [34]. Under nonunity power factor, the operation can be divided into four regions and eight modes, as shown in Fig. 3.

In regions **II** and **IV**, the hybrid modulation scheme is same as the conventional UP-PWM modulation scheme to generate the active power. However, in regions **I** and **III**, the reactive power is provided only by controlling the ac bypass switches $S_5$ and $S_6$, and $S_{1\text{–}4}$ are turned OFF.

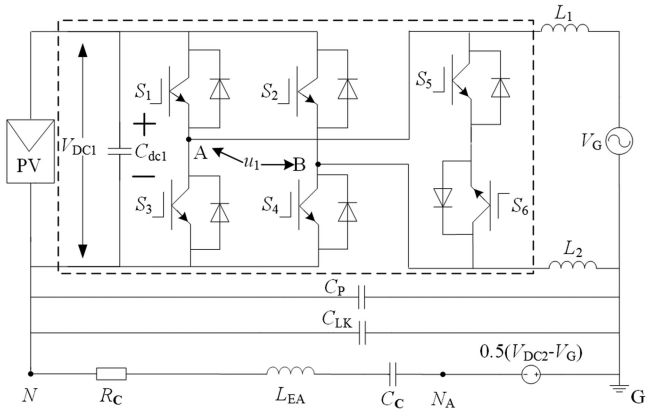


Fig. 2. Simplified equivalent circuit of the proposed inverter.

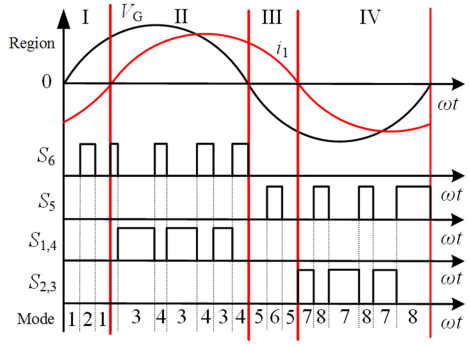


Fig. 3. Hybrid modulation for the power inverter unit.

*Region I:* The output current $i_1$ is negative. Meanwhile, the grid voltage $V_{\mathrm{G}}$ is positive, i.e., generating the reactive power. According to *Mode 1*, $S_{1\text{–}6}$ are OFF, the output current $i_1$ flows through $D_1$ and $D_4$, the output voltage $u_1$ is equal to $V_{\mathrm{DC1}}$, and the corresponding leakage current model is shown in Fig. 4(a), where the $L_{\mathrm{EP}}$ is the equivalent inductance of the power inverter unit, $L_{\mathrm{EP}} = L_{\mathrm{P}}/2$, $i_{\mathrm{CP}}$ and $i_{\mathrm{CA}}$ are the CM currents of the power inverter unit and auxiliary converter unit, respectively. For *Mode 2,* $S_{1\text{–}4}$ are OFF, $S_{5\text{-}6}$ are ON, the output current $i_1$ flows through $S_5$ and $D_6$, the output voltage $u_1$ is equal to 0, and the leakage current model is shown in Fig. 4(b).

*Region II:* The output current $i_1$ is positive and the grid voltage $V_{\mathrm{G}}$ is positive, i.e., generating the active power. In *Mode 3*, $S_1$, $S_4$ and $S_6$ are ON, $S_2$, $S_3$ and $S_5$ are OFF, the output current $i_1$ flows through $S_1$ and $S_4$, the output voltage $u_1$ is equal to $V_{\mathrm{DC1}}$, and its corresponding leakage current model is shown in Fig. 4(a). For *Mode 4*, $S_6$ is ON, other power devices are OFF, the output current $i_1$ flows through $S_6$ and $D_5$, the output voltage $u_1$ is equal to 0, and the leakage current model is shown in Fig. 4(b).

*Region III:* The output current $i_1$ is positive and the grid voltage $V_G$ is negative, and the inverter generates the reactive power. With *Mode 5*, $S_{1\text{–}6}$ are OFF, the output current $i_1$ flows through $D_2$ and $D_3$, the output voltage $u_1$ is equal to $-V_{\mathrm{DC1}}$, and its corresponding leakage current model is shown in Fig. 4(a).

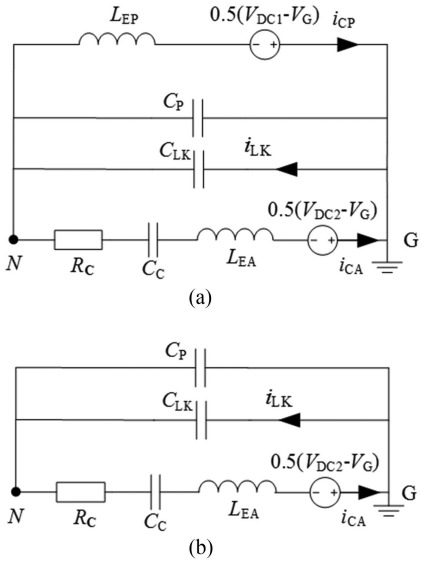


Fig. 4. Leakage current model. (a) Model 1. (b) Model 2.

For *Mode 6*, $S_{1-4}$ are OFF, $S_{5-6}$ are ON, the output current $i_1$ flows through $S_6$ and $D_5$, the output voltage $u_1$ is equal to 0, and the leakage current model is shown in Fig. 4(b).

*Region IV:* The output current $i_1$ is negative, and the grid voltage $V_G$ is negative, i.e., generating the active power. According to *Mode 7*, $S_2$, $S_3$, $S_5$ are ON, $S_1$, $S_4$, $S_6$ are OFF, the output current $i_1$ flows through $S_2$ and $S_3$, the output voltage $u_1$ is equal to $-V_{\rm DC1}$, and its corresponding leakage current model is shown in Fig. 4(a). In *Mode 8*, $S_5$ is ON, other power devices are OFF, the output current $i_1$ flows through $S_5$ and $D_6$, the output voltage $u_1$ is equal to 0, and the leakage current model is shown in Fig. 4(b).

## III. Leakage Current Suppression Principle and Parameter Design of Passive Components

### A. Capacitor $C_C$ Voltage Analysis

In grid connected applications, the parasitic capacitance $C_{\rm LK}$ and the capacitance $C_P$ is nF level. However, $C_C$ is set to $\mu$F level, $C_C = 50\ \mu$F in the prototype. Therefore, for simplicity, the influence of $C_{\rm LK}$ and $C_P$ on voltage across *Cc* is ignored in the following analysis.

Taking *Region II* as an example, there are always two stages in one switching period. Due to the symmetry of operation regions and modes, other regions are similar.

*Stage I:* $S_1$, $S_4$ are ON, $S_2$, $S_3$, $S_5$, and $S_6$ are OFF, the output current $i_1$ flows through $S_1$ and $S_4$, and the corresponding equivalent model is shown in Fig. 4(a). According to Kirchhoff's voltage law, the voltage of capacitor $C_C$, $V_{\rm CC}$, can be represented by the following differential equation:

$$L_\Sigma C_C \frac{d^2V_{\rm CC}}{dt} + R_C C_C \frac{dV_{\rm CC}}{dt} + V_{\rm CC} = 0.5\left(V_{\rm DC2} - V_{\rm DC1}\right) \tag{2}$$

where $L_\Sigma$ is total equivalent inductance of leakage current model, $L_\Sigma = L_{\rm EP}+L_{\rm EA}$.

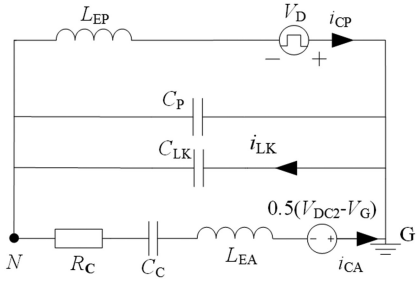


Fig. 5. Leakage current analysis circuit.

If

$$R_{\sum 1} > 2\sqrt{\frac{L_{\rm EA}}{C_C}} \tag{3}$$

where $R_{\Sigma 1}$ is the sum of all resistances in the corresponding equivalent model, $R_\Sigma = R_{\rm LP}+R_{\rm LA}+R_C$.

Define $\lambda_{1,2}$ as

$$\lambda_{1,2} = -\frac{R_{\Sigma 1}}{2L_{\rm EA}} \pm \sqrt{\left(\frac{R_{\Sigma 1}}{2L_{\rm EA}}\right)^2 - \frac{1}{L_{\rm EA}C_{\rm C}}}. \tag{4}$$

Then, the solution of differential equation (2) can be expressed as

$$V_{\rm CC} = 0.5\left(V_{\rm DC2} - V_{\rm DC1}\right) + K_1 e^{\lambda_1 t} + K_2 e^{\lambda_2 t} \tag{5}$$

where $K_1$ and $K_2$ are constants determined by the initial conditions. It can be seen that $V_{\rm CC}$ should stabilize at 0.5 ($V_{\rm DC2} - V_{\rm DC1}$) after enough switching periods.

*Stage II:* $S_6$ is ON, other power devices are OFF, the output current $i_1$ flows through $S_6$ and $D_5$, and the corresponding leakage current model is shown in Fig. 4(b). According to Fig. 4(b), it can be concluded that $V_{\rm CC}$ remains unchanged in this stage.

### B. Leakage Current Suppression of the Proposed Inverter

Based on whether the dc and ac sides of the power inverter unit are decoupled, the aforementioned eight operation modes can be classified into two categories: nondecoupling modes and dc-decoupling modes.

For the nondecoupling modes, *Mode 1*, *Mode 3*, *Mode 5*, and *Mode 7*, the dc and ac sides are directly connected by the filter inductors, and $V_{\rm GN}$ is $V_{\rm DC1}$/2. However, for the dc decoupling modes, *Mode 2*, *Mode 4*, *Mode 6*, and *Mode 8*, the dc and ac sides are decoupled by $S_5 + D_6$ or $S_6 + D_5$. Obviously, the leakage current is caused by the commutation between the nondecoupling mode and the dc decoupling mode.

As shown in Fig. 2, the different decoupling modes of the power inverter unit correspond to the different switching states of the circuit in the dashed box, and the CM voltage between *A*(*B*) and *N* is determined by these switching states.

Therefore, the steady-state leakage current of the proposed inverter can be analyzed by the circuit shown in Fig. 5, where $V_D$ is the equivalent CM voltage caused by mode commutation.

Since the harmonic leakage current is caused by $V_D$, the transfer function from $V_D$ to $i_{\rm LK}$ can be used to evaluate the

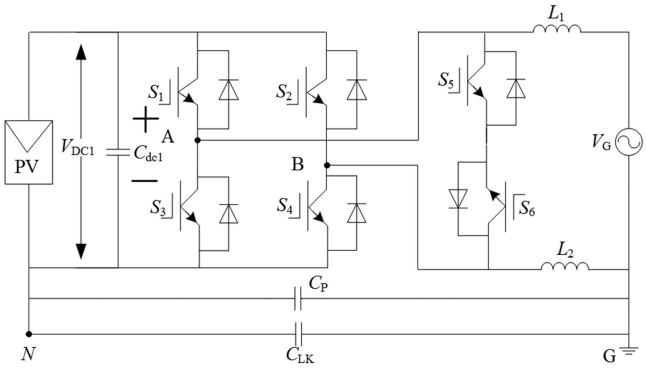


Fig. 6. HERIC + $C_P$ scheme.

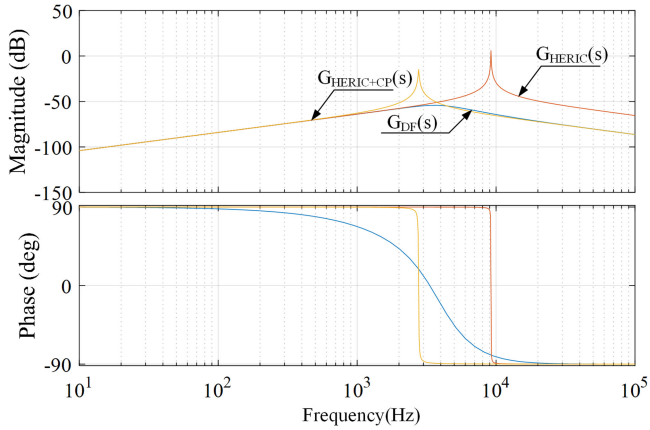


Fig. 7. Bode plots of $G_{\mathrm{DF}}(s)$, $G_{\mathrm{HERIC}+CP}(s)$, and $G_{\mathrm{HERIC}}(s)$.

ability to suppress leakage current, which can be derived as

$$G_{\mathrm{DF}}(s)=\frac{\frac{C_{\mathrm{LK}}}{C_{\mathrm{LK}}+C_P}}{G_{\mathrm{CPPV}}(s)+G_{\mathrm{EP}}(s)\left(\frac{G_{\mathrm{CPPV}}(s)}{G_{\mathrm{EA}}(s)}+1\right)} \tag{6}$$

where the expressions of $G_{\mathrm{EP}}(s)$, $G_{\mathrm{CPPV}}(s)$, and $G_{\mathrm{EA}}(s)$ are as follows:

$$G_{\mathrm{EP}}(s)=R_{\mathrm{LP}}+L_{\mathrm{EP}}s \tag{7}$$

$$G_{\mathrm{CPPV}}(s)=\frac{1}{C_P s+C_{\mathrm{LK}}s} \tag{8}$$

$$G_{\mathrm{EA}}(s)=R_C+R_{\mathrm{LA}}+L_{\mathrm{EA}}s+\frac{1}{C_C s} \tag{9}$$

where $R_{\mathrm{LA}}$ and $R_{\mathrm{LP}}$ are the resistances of inductors $L_{\mathrm{EP}}$ and $L_{\mathrm{EA}}$, respectively. For simplicity, $R_{\mathrm{LA}}$ and $R_{\mathrm{LP}}$ are not shown in Fig. 5.

The following is an analysis of how the proposed inverter improves the leakage current suppression effect. To illustrate the role of the auxiliary converter unit in suppressing leakage current, Fig. 6 shows the HERIC + $C_P$ scheme.

The transfer function from $V_H$ to $i_{\mathrm{LK}}$ of HERIC + $C_P$ scheme is

$$G_{\mathrm{HERIC+CP}}(s)=\frac{1}{G_{\mathrm{CPPV}}(s)+G_{\mathrm{EP}}(s)}\frac{C_{\mathrm{LK}}}{C_{\mathrm{LK}}+C_{\mathrm{P}}}. \tag{10}$$

Likewise, the corresponding transfer function of the conventional HERIC inverter is given by

$$G_{\mathrm{HERIC}}(s)=\frac{1}{G_{\mathrm{CLK}}(s)+G_{\mathrm{EP}}(s)}. \tag{11}$$

By using the parameters listed in Tables I, II, and III, Bode plots of $G_{\mathrm{HERIC}}(s)$, $G_{\mathrm{HERIC+CP}}(s)$, and $G_{\mathrm{DF}}(s)$ can be shown as in Fig. 7.

As can be seen from Fig. 7, both the traditional HERIC scheme and the HERIC + $C_P$ scheme have resonant amplitude gain peaks. The amplitude gain peak are 8.8 and −14.3 dB, respectively. Compared with the HERIC scheme, the HERIC + $C_P$ scheme and the proposed inverter can improve the leakage current suppression effect. In the high frequency range, Bode plots of the $G_{\mathrm{DF}}(s)$ and $G_{\mathrm{HERIC}+CP}(s)$ are similar. However, the proposed inverter almost eliminates resonance and reduces the amplitude gain around the resonant frequency of $G_{\mathrm{HERIC}+CP}(s)$, which shows the role of the auxiliary converter unit in suppressing leakage current. Hence, the proposed inverter has the best leakage current suppression effect.

### C. Impact of Parametric Variation of Passive Components

The passive components used in the proposed inverter include $L_1$, $L_2$, $L_3$, $L_4$, $C_C$, and $C_P$.

$L_1$, $L_2$, $L_3$, and $L_4$ are the filter inductances of the power inverter unit and the auxiliary converter unit. $V_{\mathrm{DC2min}}$ represents the minimum dc-link voltage of the auxiliary unit that can completely eliminate the switching ripple in the current $i_1$. According to [32], the changes of these filter inductances can cause the change of $V_{\mathrm{DC2min}}$. When $V_{\mathrm{DC2}}$ is higher than $V_{\mathrm{DC2min}}$, the performance of the inverter is not affected by the change of filter inductances. However, when $V_{\mathrm{DC2}}$ is lower than $V_{\mathrm{DC2min}}$, the switching ripple of $i_1$ cannot be completely eliminated by $i_2$, which can decrease power quality. Therefore, in order to ensure the power quality, $V_{\mathrm{DC2}}$ can be set to $k{*}V_{\mathrm{DC2min}}$, and $k$ can be determined by application conditions.

For the parallel capacitor $C_P$, it is obvious that the larger the $C_P$, the smaller the voltage $V_{\mathrm{CP}}$ across the $C_{\mathrm{LK}}$, and the smaller the leakage current $i_{\mathrm{LK}}$. But the total current flowing through the capacitors $C_P$ and $C_{\mathrm{LK}}$ becomes larger with the increase of $C_P$, which is denoted by $i_T$. The increase of $i_T$ will reduce the grid-connected current quality and increase the switching losses. Therefore, the parallel capacitor $C_P$ can be determined by $i_T$. In this article, the $i_T$ value is $0.005{*}i_{\mathrm{GN}}$, and the corresponding $C_P$ is 0.5 $\mu$F.

Using the parameters listed in Table III, the impact of parametric variation of passive components on leakage current is discussed in the following.

Fig. 8 shows the Bode plots of $G_{\mathrm{DF}}(s)$ under the parametric variation of passive components. When $L_1$ and $L_2$ change from 1.5 mH (0.5∗3 mH) to 4.5 mH (1.5∗3 mH), the Bode plots of $G_{\mathrm{DF}}(s)$ are shown in Fig. 8(a). It can be seen that the larger the filter inductances, the more effective the leakage current suppression. When the change of $L_1$ and $L_2$ is reduced to 1.5 mH, the maximum magnitude is −48 dB. This means that the leakage current suppression effect of the proposed inverter is still better

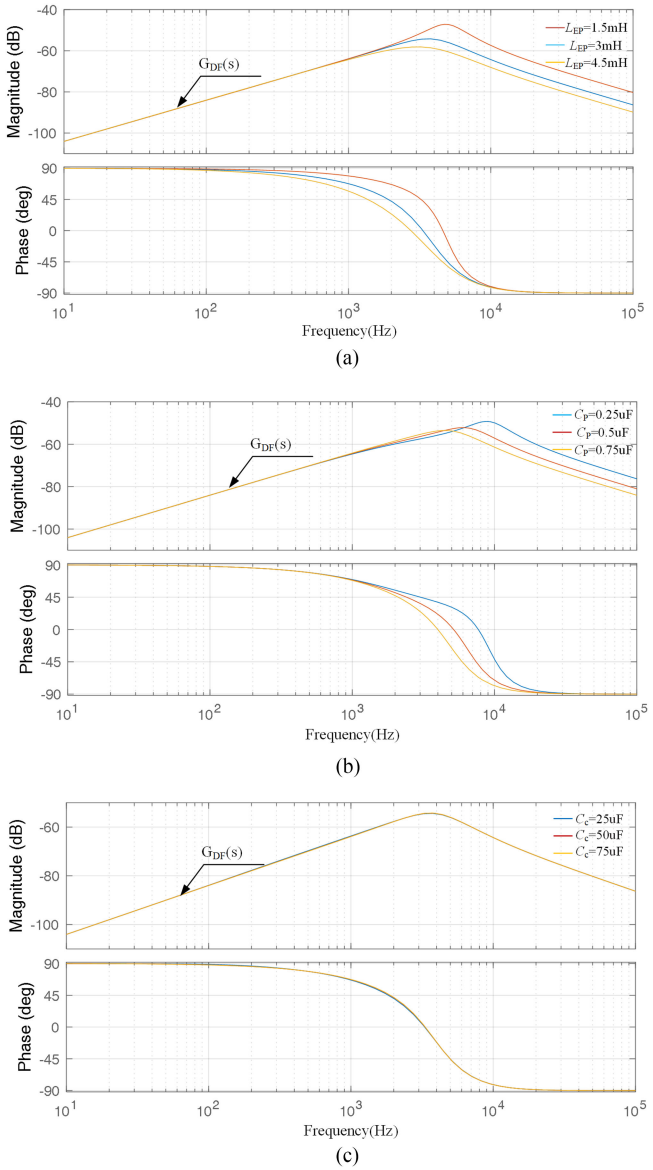


Fig. 8. Bode plots of $G_{\mathrm{DF}}$ $(s)$ under the parametric variation of passive components. (a) $L_1$ and $L_2$ change from 1.5 to 4.5 mH. (b) $C_P$ changes from 0.25 to 0.75 $\mu$F. (c) $C_C$ changes from 25 to 75 $\mu$F.

than that of HERIC and HERIC + $C_P$ scheme. The changes of $L_3$ and $L_4$ have similar impact on the leakage current.

When $C_P$ changes from 0.25 $\mu$F (0.5∗0.5 $\mu$F) to 0.75 $\mu$F (1.5∗0.5 $\mu$F), the Bode plots of $G_{\mathrm{DF}}$ $(s)$ are shown in Fig. 8(b). Similarly, the larger the capacitance $C_P$, the more effective the leakage current suppression. When the $C_P$ is reduced to 0.25 $\mu$F, the maximum magnitude is −48 dB. Compared with HERIC and HERIC + $C_P$ scheme, the proposed inverter can still suppress leakage current more effectively.

When $C_C$ changes from 25 $\mu$F (0.5∗50 $\mu$F) to 75 $\mu$F (1.5∗50 $\mu$F), the Bode plots of $G_{\mathrm{DF}}$ $(s)$ are shown in Fig. 8(c). It can be seen that when $C_C$ changes in the above range, the suppression effect of leakage current has almost no change.

Therefore, the proposed inverter has good robustness to parametric variation of passive components.

## IV. Harmonic Elimination Principle and Control Strategy of the Proposed Inverter

### A. Harmonic Elimination Principle

For the proposed inverter, it can be seen that the grid current $i_G$ is the sum of harmonic elimination current $i_2$ and the power inverter unit output current $i_1$, $i_{\mathrm{G}}$ can be expressed as

$$i_G = i_1 + i_2. \tag{12}$$

The current $i_1$ can be decomposed into fundamental component $i_{11}$ and switching current ripple $i_{\mathrm{H}}$, i.e.,

$$i_1 = i_{11} + i_H. \tag{13}$$

The voltage across inductance $L_p$ can be expressed as

$$u_{\mathrm{LP}} = u_1 - V_G \tag{14}$$

where $u_1$ is the output voltage of the power inverter unit.

In the steady state, the fundamental current component $i_{11}$ can be expressed as

$$i_{11} = \frac{1}{L_P}\int u_{11}(t)dt \tag{15}$$

where $u_{11}$ is the fundamental component of $u_{\mathrm{LP}}$.

Correspondingly, $i_H$ is generated by the harmonic voltage $u_H$ in $u_{\mathrm{LP}}$, which is mainly caused by PWM modulation with a low switching frequency.

According to (13) and (14), $i_H$ can be deduced as

$$i_H(t) = \int_0^t \frac{u_H}{L_p}dt = \int_0^t \frac{u_1 - V_G - L_P\frac{di_{11}}{dt}}{L_P}dt. \tag{16}$$

Because the switching frequency of the auxiliary converter unit is much higher than that of the power inverter unit, for the convenience of analysis, the switching voltage harmonic of the auxiliary converter unit is ignored, so its output voltage $u_2$ can be approximated as

$$u_2 = u_{\mathrm{MA}}V_{\mathrm{DC2}} \tag{17}$$

where $u_{\mathrm{MA}}$ and $V_{\mathrm{DC2}}$ are the modulation signal and dc-link voltage of the auxiliary converter unit, respectively.

According to (17), if $u_{\mathrm{MA}}$ is determined by

$$u_{\mathrm{MA}} = \frac{L_A}{V_{\mathrm{DC2}}L_P}\left(V_G + L_p\frac{di_{11}}{dt} - u_1\right) + \frac{1}{V_{\mathrm{DC2}}}V_G. \tag{18}$$

$i_2$ can be expressed as

$$i_2 = \int_0^t \frac{u_2 - V_G}{L_A}dt. \tag{19}$$

Substituting (17)–(19) into (16), the following relation can be obtained:

$$i_2 = -i_H. \tag{20}$$

According to (12), (13), and (20), the grid current $i_G$ is

$$i_G = i_{11}. \tag{21}$$

It can be seen from (21) that if $u_{\mathrm{MA}}$ is generated by (18), the grid current $i_G$ is equal to the fundamental current $i_{11}$, which means that the switching current ripple $i_H$ in $i_1$ is eliminated

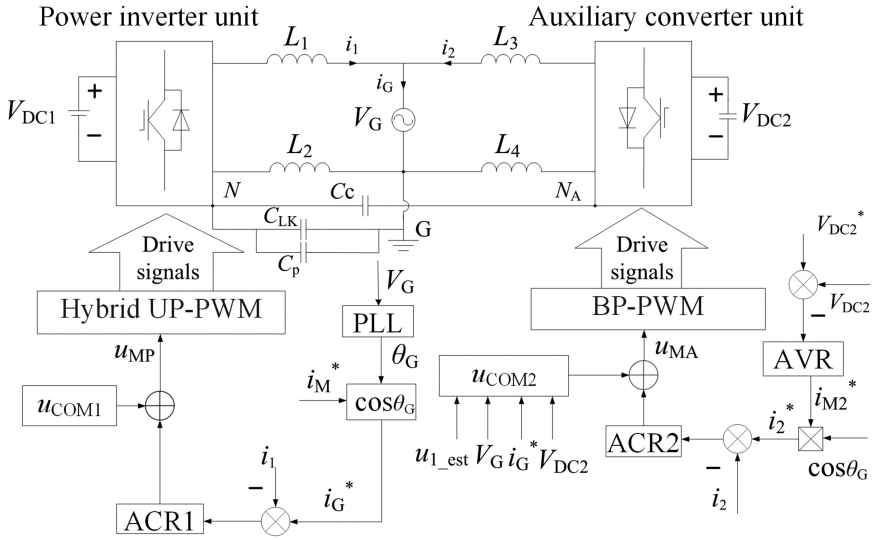


Fig. 9. Control block diagram of the proposed inverter.

by the auxiliary converter. The parameter design methods of the proposed inverter are similar to the double frequency grid inverter, which has been introduced in [32].

### B. Control Scheme of the Proposed Inverter

The control block diagram of the proposed inverter is shown in Fig. 9. It is composed of two relatively independent control loops, *i.e.*, power inverter current loop, and auxiliary converter voltage loop.

The power inverter current loop is used to control the output current $i_1$ of the power inverter unit, its reference is denoted by $i_G{}^*$, which is determined by

$$i_G^* = i_M^* \cos(\theta_G) \tag{22}$$

where $i_M{}^*$ is the grid current amplitude reference, the phase of the grid voltage $\theta_G$ is the output of phase-locked loop (PLL}, which is implemented by the second-order generalized integrator.

The difference between $i_G{}^*$ and $i_1$ is used as the input of the current controller ACR1, which adopts the proportional resonant (PR) regulator. The output signal of ACR1 is denoted by $u_{\mathrm{ACR1}}$. The feedforward compensation $u_{\mathrm{COM1}}$ is obtained by

$$u_{\mathrm{COM1}} = \frac{V_G}{V_{\mathrm{DC1}}}. \tag{23}$$

The modulation signal $u_{\mathrm{MP}}$ is the sum of $u_{\mathrm{COM1}}$ and $u_{\mathrm{ACR1}}$.The hybrid modulation scheme in Section **II** is adopted to generate the drive signals for the power inverter bridge.

The voltage regulator AVR in control loops of auxiliary converter unit is used to ensure the dc-link voltage $V_{\mathrm{DC2}}$ to track its reference $V_{\mathrm{DC2}}{}^*$.

The current reference $i_2{}^*$ of the auxiliary converter unit is obtained by

$$i_2^* = i_{\mathrm{M2}}^* \cos(\theta_G) \tag{24}$$

where $i_{\mathrm{M2}}{}^*$ is the output of AVR.

The output of the current controller ACR2 is implemented by multiresonant PR regulator, its output is represented by $u_{\mathrm{ACR2}}$. The modulation signal $u_{\mathrm{MA}}$ is the sum of $u_{\mathrm{ACR2}}$ and the feedforward compensation $u_{\mathrm{COM2}}$, which is given by

$$u_{\mathrm{COM2}} = \frac{V_G}{V_{\mathrm{DC2}}} + u_E \tag{25}$$

where $u_E$ is used to eliminate the switching current ripple in $i_1$. According to (18), $u_E$ is calculated by

$$u_E = \frac{L_A}{V_{\mathrm{DC2}} L_P}\left(V_G + L_p \frac{di_G^*}{dt} - u_{1\_\mathrm{est}}\right) + \frac{1}{V_{\mathrm{DC2}}} V_G \tag{26}$$

where $u_{1\_\mathrm{est}}$ is the estimation of power inverter output voltage $u_1$, which is obtained by the switching state of the power inverter unit. Therefore, $u_1$ can be estimated by the drive signal without sampling the output voltage of the power inverter unit, which can reduce the difficulty of the control system design. It is worth to note that since there is a differential term ($di_{11}/dt$) in (18), to reduce the influence of the measure noise, $i_{11}$ in (18) is replaced by $i_G{}^*$ in (26).

In addition, the frequency characteristics near the cutoff frequencies of the auxiliary converter unit and the power inverter unit are not affected by the feedforward elimination harmonic compensation. Therefore, the parameters of ACR1, ACR2, and AVR can be designed by the traditional methods.

From the aforementioned analysis, it can be seen that the switching current ripple of the power inverter unit can be eliminated by the auxiliary converter unit using feedforward compensation method. The well-known harmonic elimination techniques include active power filters, active notch filters [36], selective harmonic elimination methods, and so on. Compared with these technologies, the method used in the proposed inverter has the following advantages.

1) This method is based on the feedforward harmonic elimination technology, which can effectively suppress higher frequency grid-connected current harmonics.

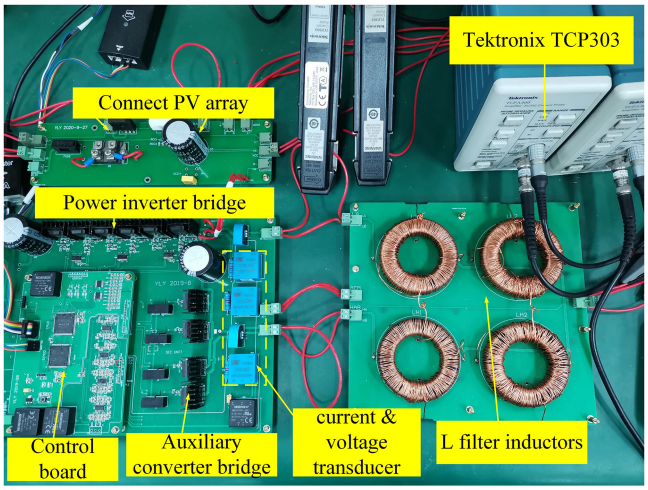


Fig. 10. Photograph of the experimental prototype.

TABLE III
MAIN PARAMETERS OF TRANSFORMER-FREE DUAL-FREQUENCY GRID-CONNECTED INVERTER

| Block | Parameters | Value |
|---|---|---|
| Power inverter unit | DC-link voltage $V_{DC1}$ | 200 V |
| | Filter inductor $L_P$ | 3 mH |
| | Switching frequency $f_{s1}$ | 2.5 kHz |
| | Connection capacitance $Cc$ | 50 μF |
| | Parallel capacitance $C_P$ | 0.5 μF |
| | Switches (Si-IGBT) | AUIRGPS4070D0 |
| Auxiliary converter unit | DC-link voltage $V_{DC2}$ | 250 V |
| | Filter inductor $L_A$ | 1 mH |
| | Switching frequency $f_{s2}$ | 60 kHz |
| | Switches (SiC-MOSFET) | IMW65R027M1H |
| Grid | Grid frequency $f_G$ | 50 Hz |
| | Grid voltage $V_G$ | 150 V |
| | Rated power $P_N$ | 1.0 kW |
| | Parasitic capacitance $C_{LK}$ | 100 nF |

2) Since there is no need to extract current or voltage harmonics as a reference value, this method does not have strict requirements related to current control bandwidth, switching frequency of the power inverter unit, and current sampling accuracy.
3) Since the *LCL* filter is not used, the influence of the grid impedance on the resonant frequency of the *LCL* filter is eliminated, so this harmonic elimination technology has good robustness to the change of the grid impedance [32].

## V. EXPERIMENT RESULTS

To verify the effectiveness of the proposed inverter, a prototype of a 1-kW transformer-free dual-frequency grid-connected inverter was built, which is shown in Fig. 10. Its main parameters and types of power devices are listed in Table III.

### *A. CM Performance of the Transformer-Free Dual-Frequency Grid-Connected Inverter*

Experimental waveforms of $V_{GNA}$ and $V_{DC2}$ in steady state are shown in Fig. 11(a). The dc-link voltage $V_{DC2}$ is stabilized at

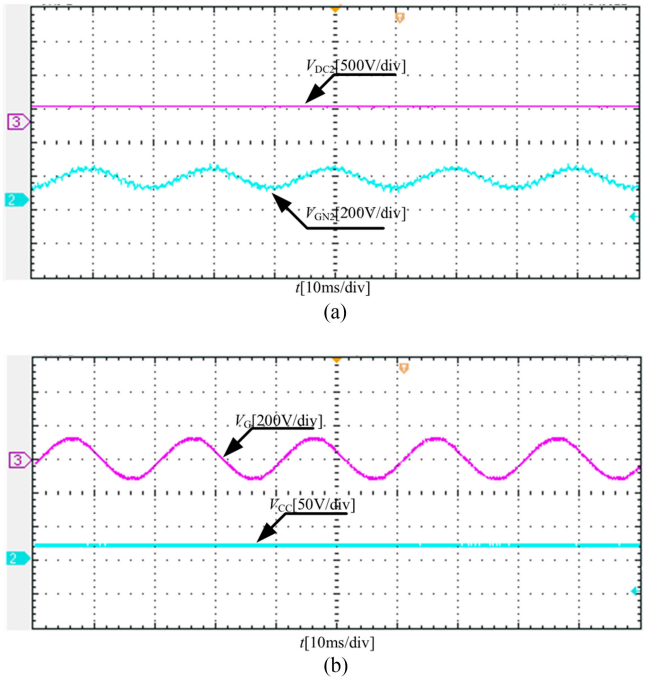


Fig. 11. Experimental waveforms of voltages in leakage current model. (a) $V_{GNA}$ and $V_{DC2}$. (b) $V_G$ and $V_{CC}$.

250 V under the control of the auxiliary converter voltage loop. $V_{GNA}$ is composed of an ac component and a dc component. The amplitude and frequency of the fundamental component are 77.5 V and 50 Hz, respectively. The dc component of $V_{GNA}$ is $V_{DC2}$ /2 (125 V).

It can be concluded that voltage $V_{GNA}$ is independent of the state of $S_{7-10}$. Therefore, it is reasonable that the auxiliary converter unit is equivalent as a voltage source in the above analysis.

Fig. 11(b) shows the waveforms of $V_{CC}$ and $V_G$ in steady state. It is can be seen that the dc component of $V_{CC}$ is about 25 V, which is equal to 0.5 ($V_{DC2} - V_{DC1}$). This experimental result verifies the correctness of (5) in Section III.

The CM characteristic experimental results are shown in in Fig. 12. According to Section **II**, the fundamental component of leakage current $i_{LK}$ depends on the amplitude of voltage $V_{GN}$. In the case of $V_{DC1} = 200$ V and power factor cos $\varphi = 1$, the waveforms of $V_{GN}$ and $i_{LK}$ of the proposed inverter are shown in Fig. 12(a). Obviously, the amplitude of the fundamental component of $V_{GN}$ is 77.52 V, and the dc component in voltage $V_{GN}$ is 100 V. The amplitude of the fundamental component in current $i_{LK}$ is about 8.43 mA, and its rms value is about 5.96 mA.

The waveforms of $V_{GN}$ and $i_{LK}$ of the HERIC+$C_P$ scheme are shown in Fig. 12(b). The rms value of leakage current is 56.3 mA and its peak value is 80 mA. Fig. 12(c) shows the waveforms of the CM characteristic experiment of the conventional HERIC. It can be seen that the rms value of leakage current is 84 mA, and its peak value is 120 mA.

For the above three inverter schemes, the fast Fourier transform (FFT) analysis is shown in Fig. 13. The amplitudes of the fundamental component of $V_{GN}$ are same. The total harmonic distortions (THDs) of $V_{GN}$ of HERIC, HERIC + $C_P$,

TABLE IV
CALCULATION RESULTS OF POWER LOSSES WHEN THE GRID CURRENT AMPLITUDE IS 15 A

| Parameters | transformer-free dual-frequency grid-connected inverter | | HERIC inverter |
|---|---|---|---|
| | Power inverter unit | Auxiliary converter unit | Power inverter unit |
| Grid current $i_o$ (RMS) | 10.60 A | 1.46 A | 10.60 A |
| Switching loss $P_{sw}$ | 9.43 W | 7.58 W | 26.4 W |
| Conduction loss $P_{con}$ | 22.45 W | 1.2 W | 22.45 W |
| Parasitic resistance loss of inductor $P_L$ | 6.74 W | 0.043 W | 6.74 W |
| Total power loss $P_{total}$ | 47.44 W | | 55.59 W |

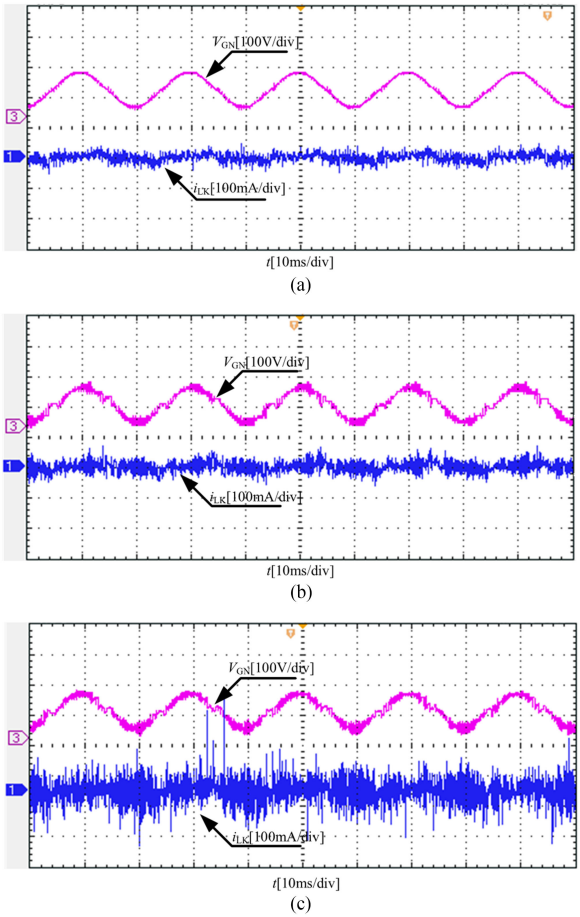


Fig. 12. Experimental waveforms of $V_{GN}$ and $i_{LK}$ in CM characteristic experiment. (a) Proposed inverter. (b) HERIC + $C_P$ scheme. (c) HERIC scheme.

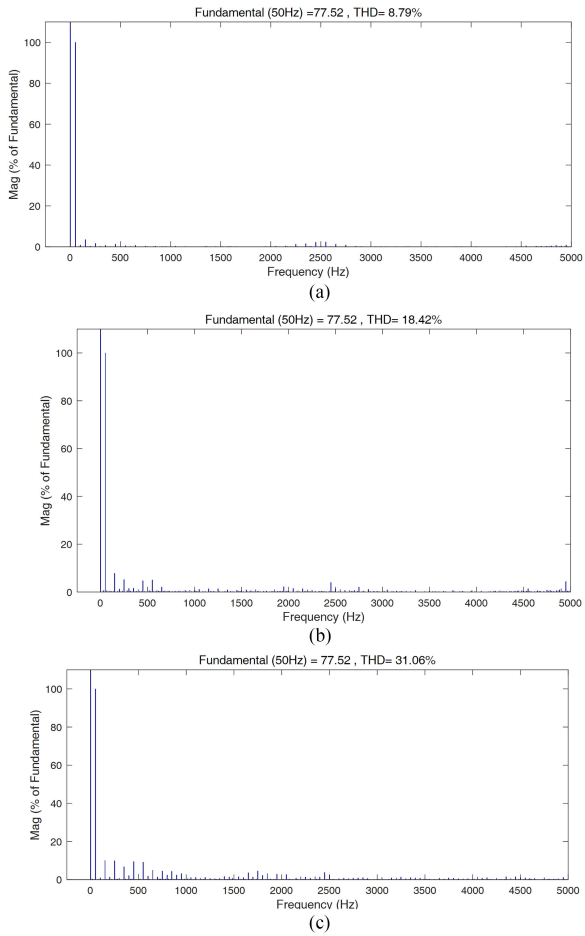


Fig. 13. FFT analysis of the voltage $V_{GN}$. (a) Proposed inverter. (b) HERIC + $C_P$ scheme. (c) HERIC scheme.

and the proposed topology are 31.06%, 18.42%, and 8.79%, respectively. It also can be seen from Fig. 13 that compared with the other two schemes, the proposed inverter can suppress the harmonic components of $V_{GN}$ and $i_{LK}$ more effectively. Therefore, the leakage current analysis in Section **II**-B is verified by the above experimental results.

### *B. Suppression of Grid Current Harmonics*

The experimental waveforms of the grid current harmonic suppression experiment are shown in Fig. 14. When the power factor cos $\varphi = 1$, the waveforms of $i_1$, $i_2$, and $i_G$ are shown in Fig. 14(a). The amplitude of current $i_1$ is 15 A, and its switching ripple is significant. Compared with $i_1$, the ripple of the grid current $i_G$ is effectively reduced. The fundamental components of $i_G$ and $i_1$ are equal, so the active power is injected to the grid by the power inverter unit of the dual-frequency inverter.

Fig. 14(b) shows zoomed-in view of $i_1$, $i_2$, and $i_G$, and it can be observed that the switching current ripple of $i_1$ is opposite to the current $i_2$ and the peak value of current $i_2$ is about 2 A.

The FFT analysis of $i_1$ and $i_G$ are shown in Fig. 15, which further shows the role of the auxiliary converter unit in suppressing current harmonics. Fig. 15(b) shows the spectrum of grid current

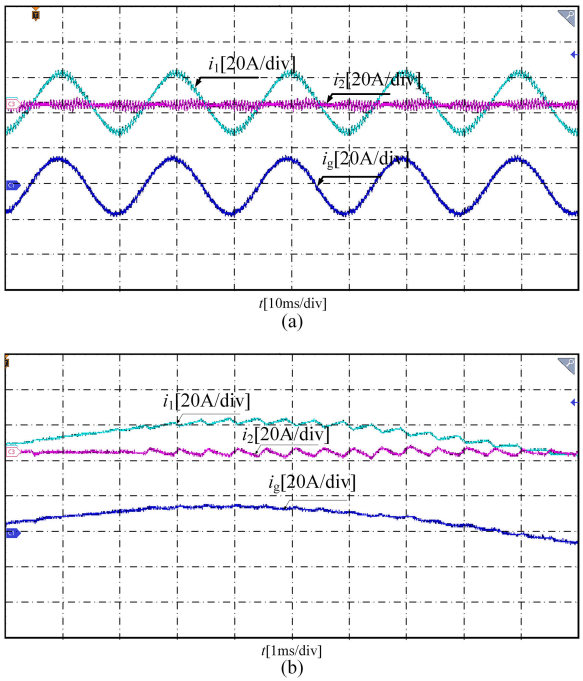


Fig. 14. Experimental waveforms of the current harmonic suppression. (a) $i_1$, $i_2$, and $i_G$. (b) Zoomed-in view of $i_1$, $i_2$, and $i_G$.

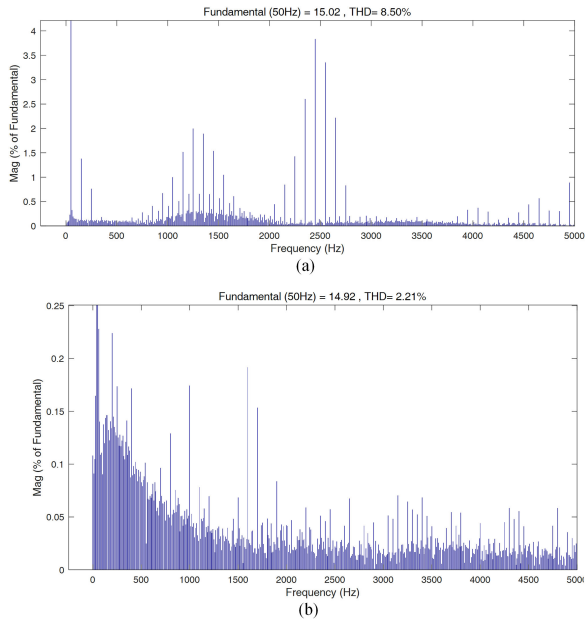


Fig. 15. FFT analysis of the grid current harmonics suppression. (a) Spectrum of $i_1$. (b) Spectrum of $i_G$.

$i_{\mathrm{G}}$. Compared with $i_1$, the THD of $i_G$ is 2.21% and the switching harmonics around 2.5 kHz drops from 4% to 0.05%.

It is shown from the above experimental results that the proposed dual-frequency inverter can effectively suppress the switching ripple in $i_1$, and ensure the power quality.

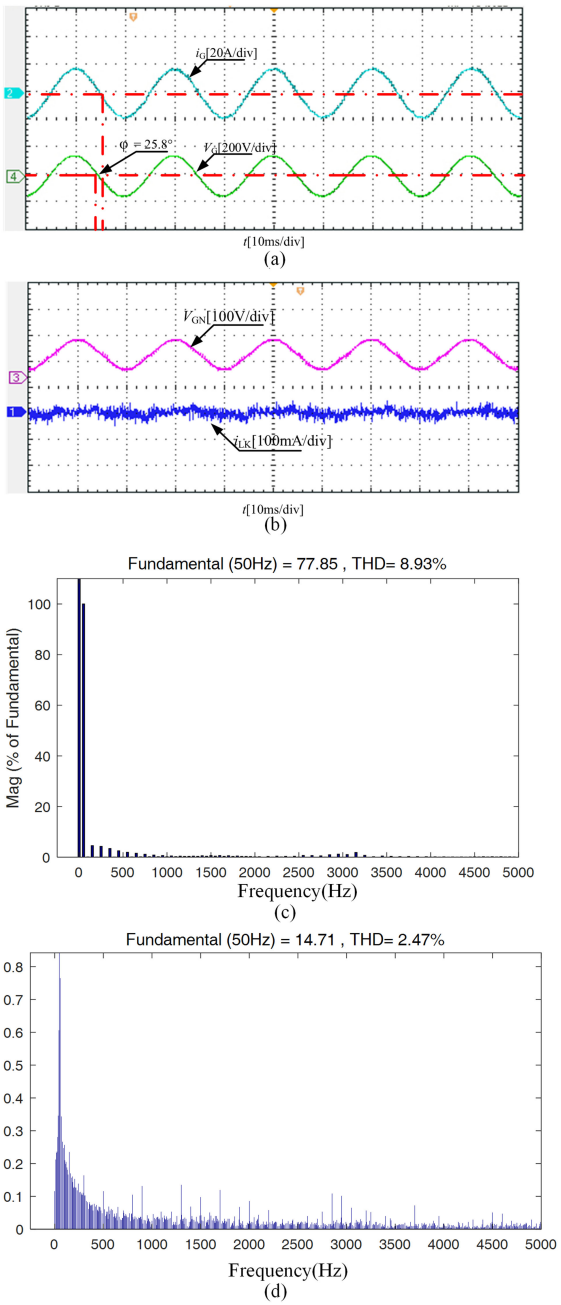


Fig. 16 Waveforms of reactive power control experiments when cos $\varphi = 0.9$. (a) $i_{\mathrm{G}}$ and $V_{\mathrm{G}}$. (b) $V_{\mathrm{GN}}$ and $i_{\mathrm{LK}}$. (c) spectrum of $V_{\mathrm{GN}}$. (d) Spectrum of $i_{\mathrm{G}}$.

### C. Reactive Power Control Capability

As defined in international standards (e.g., VDE-AR-N4105), the power factor in power generation systems or units must be adjustable within a range of 0.9 to 1 [30]. Therefore, in order to verify the ability to provide reactive power of the proposed topology, reactive power control experiments are carried out when the power factor changes from 0.9 to 1. Fig. 16 shows the experimental results at a nonunity power factor (i.e., cos $\varphi = 0.9$).

The waveforms of $V_G$ and $i_G$ are shown in Fig. 16(a). It can be seen that the phase difference between the grid voltage and

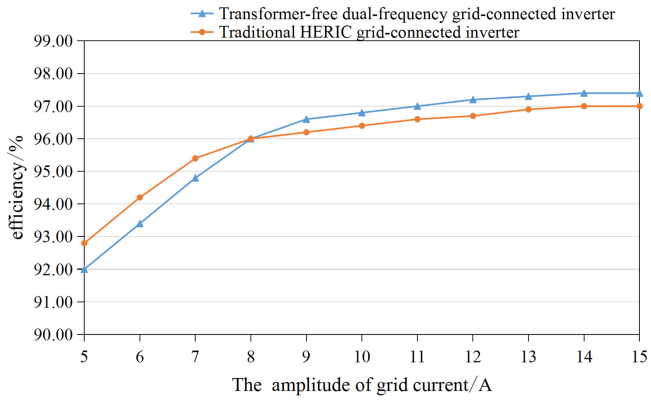


Fig. 17. Efficiency curves of the proposed inverter and the traditional HERIC inverter.

grid current is 25.8°, which corresponds to cos $\varphi = 0.9$. The waveforms of $V_{\rm GN}$ and $i_{\rm LK}$ are shown in Fig. 16(b), which are similar to the waveforms of $V_{\rm GN}$ and $i_{\rm LK}$ at unity power factor [Fig. 12(a)].

The spectrums of $V_{\rm GN}$ and $i_G$ and are shown in Fig. 16(c) and (d). Compared with Fig. 13(a), the amplitude of the fundamental component of $V_{\rm GN}$ remains approximately unchanged, and its THD is 8.93%. The THD of $i_G$ is 2.47%, which is slightly larger than the THD of $i_G$ at unity power factor.

Therefore, it can be seen that the proposed inverter can provide reactive power without affecting leakage current suppression performance and power quality.

### D. Efficiency Analysis

To compare the efficiency of the proposed inverter with the traditional HERIC inverter, the following experimental results are presented.

Considering that the grid current quality should comply with grid code requirements, the switching frequency of traditional HERIC inverter is 7 kHz, its main parameters are listed in Table I.

Fig. 17 shows the efficiency curves of the proposed inverter and the conventional HERIC inverter. It can be seen from Fig. 17 that when the grid current amplitude is larger than 8 A, the efficiency of proposed inverter is higher than that of the traditional HERIC inverter. However, when the grid current is smaller than 8 A, the efficiency of the proposed inverter is lower than that of the HERIC inverter. The reason is expressed as follows.

According to [35], when the amplitude of grid current is 15 A (rated current), the power losses distribution of the two inverters are calculated, which is shown in Table IV. According to Table IV, the total losses of auxiliary converter unit are small. Moreover, it is obvious that the conduction loss of power inverter unit is the same as that of HERIC inverter, but its switching frequency is lower than that of HERIC inverter. Therefore, the total loss of the proposed inverter is lower than that of the traditional HERIC inverter. The efficiency of the proposed inverter is about 0.4% higher than that of the traditional HERIC inverter when the grid current is 15 A.

However, when the amplitude of grid current is smaller than 8 A, the power loss of the auxiliary unit is larger than the difference between the power loss of the HERIC inverter and the power loss of the inverter unit. Therefore, the loss of the proposed inverter is larger than the loss of the HERIC inverter.

## VI. Conclusion

In this article, a transformer-free dual-frequency grid-connected inverter including a power inverter unit and an auxiliary converter unit is proposed. The power inverter unit adopts the HERIC topology. The two units are connected by connection capacitor $C_C$, and the parallel capacitor $C_P$ is inserted between the negative terminal of the dc-link of the power inverter unit and the ground. Since the auxiliary converter unit adopts BP-PWM scheme, the dc-link voltage of the power inverter unit can be stabilized during the zero-voltage state, so the leakage current can be suppressed more effectively. The power inverter unit transmits power to the grid at a low switching frequency for reducing power loss. The auxiliary converter unit adopts a feedforward method to eliminate grid switching current ripples and improve the power quality. From the experimental results and theoretical analysis, the advantages of the proposed inverter are as follows.

1) Compared with HERIC inverter, leakage current can be more effectively suppressed.
2) DC power is injected into the grid by the power inverter unit with low switching frequency, which can reduce the switching loss.
3) The switching current ripple can be eliminated without extracting current or voltage harmonics. The proposed inverter does not have strict requirements on current control bandwidth, switching frequency, and current sampling accuracy.
4) The feedforward harmonic elimination technique has good robustness against grid impedance variation and the grid voltage harmonics.
5) Since the filters in the proposed inverter are *L*-type, there is no inherent resonance problem, which exists in the *LCL*-type inverter.

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