Open Circuit Switch Fault Detection in Flying Capacitor and Cascaded H-Bridge Multilevel Converters

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***Abstract*—This article proposes a simple and fast active power device open circuit fault detection and localization technique. The proposed technique applies to the family of flying capacitor multilevel converters (FCMCs), including dc/dc FCMCs, single or multi-phase H-bridge FCMCs, and cascaded H-bridge multilevel converters. The localization technique needs to sense the voltage and direction of current at the output terminals of converters to detect and localize the fault. A circuit with multiple window detectors is utilized to track the output voltage level and current direction with high bandwidth. The algorithm compares the measured and expected terminal voltage, considering the commanded switch states and the terminal current direction. Once potential fault locations are identified, healthy switches are filtered out from the set of potential faulty switches over successive switching transitions. The proposed technique is experimentally validated on a single phase H-bridge FCMC. The switch state commands and pulsewidth modulation (PWM) is handled by a DSP while the fault detection and localization algorithm is implemented on a separate field programmable gate array (FPGA). The asynchronous operation of the DSP and FPGA is discussed.**

***Index Terms*—DC-AC power converters, dc-dc power converters, digital signal processing, fault detection, fault location, field programmable gate arrays.**

I. Introduction

In HIGH power and/or high frequency applications, multilevel converters (MC) topologies are attractive to overcome voltage and switching frequency limitations of available power semiconductor devices in conventional two level bridge type converters [1], [2]. Increasing the number of switching cells with appropriate switching techniques reduces the voltage stress on the power semiconductors, increases the number of output voltage levels, and reduces output distortion. A number of multilevel converter topologies have been developed and investigated, including diode clamped MCs, flying capacitor multilevel converters (FCMCs), modular multilevel converters (MMC), cascaded multilevel converters (CMC), and stacked multicell converters [3]. MCs are most often applied at medium or higher voltages, but there is increased interest in application at lower power and voltage levels for fast switching converters [4].

Switched mode power converters are vital units of many electric systems and their failure can lead to costly repair, hazardous incidents, and power interruptions [5]. Solid state switches are one of the most failure prone components of power converters with electro-thermal stresses as the main cause of their failure [5]. Short circuit faults (SCFs) usually cause immediate damage and impact the operation of the converter. These are normally detected using standard fast response hardware approaches, such as desaturation protection. In open circuit faults (OCFs), the time scale upon which its influence on internal or terminal quantities manifests is slower than the SCF; therefore, algorithmic approaches implemented in the drive controller can be used.

A variety of OCF detection and localization techniques for MCs have been proposed [5]–[16]. These techniques can be broadly grouped into four categories: 1) comparison of the predicted values of internal states such as capacitor voltages with measured values; 2) the use of advanced techniques such as wavelets, fuzzy logic, and neural networks; 3) analysis of the harmonic spectrum of the output voltage or current; and 4) comparison of the expected or commanded output voltage with measured values.

For the first category, measured internal states are compared to predicted values of the states to detect OCFs in a number of converter topologies including FCMC [6], MMC [7], and H-FCMC [8]. Model predictive control (MPC), using a converter model, is utilized to predict the capacitors' voltages and currents one or more controller steps ahead and the deviation of the measured values from the predicted ones outside predefined thresholds indicates a fault in the converter. MPC is usually associated with high computational cost, as the system response to all possible switch configurations must be calculated. As the number of possible switch states increases in MCs, the computational burden increases. Another downside of this approach is that it needs sensors for all measured internal states. It also needs sufficient changes in the value of internal states to exceed the predefined thresholds to discriminate a fault and its location in the system. Due to the slow dynamics of OCFs, such deviation normally takes several fundamental cycles to be distinguishable. Another challenge is uncertainty

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in the estimates of the converter's parameters due to the tolerance of the components, aging, and operational effects such as temperature.

The second category lumps together advanced methods such as wavelets, fuzzy logic, or neural networks utilized for OCF detection and localization [9], [10]. The limitations of this category of techniques is similar to the first category based on MPC algorithms. These methods are complex to apply and suffer from high computational cost. The also typically require a number of additional sensors. Acquiring sufficient experimental training data to localize the fault is also problematic.

Compared to the previously mentioned categories, the third and fourth categories are attractive because only one or two additional sensors are needed to monitor the output terminal voltage or current, versus for every internal state, i.e., every internal capacitor. Different fault detection techniques differentiate the third and fourth categories. In the third category, harmonic spectrum analysis of the output terminal voltage of an FCMC was proposed in [11]. The method presented has an advantage of being able to detect SCFs but cannot be extended for more than three switching cells. It also cannot discriminate between short circuit and OCFs. This method requires up to three periods of the modulation waveform to detect and localize an OCF. The computation of the harmonic spectrum requires significant computation, high measurement bandwidth, and high sensitivity. Some researchers have attempted to remove this impediment by using a filtered terminal voltage [12].

In the fourth category, for a given switch configuration or switch state, the deviation of the measured output terminal voltage from the predicted value can be utilized to detect failure in the system. This concept has been utilized in [13]–[16]. Typically, the deviation of the output terminal voltage is high, e.g., on the order of the voltage of the flying capacitors, which reduces the need for precision terminal voltage measurements and increases the noise immunity. In these methods, fast sampling and high bandwidth voltage/current sensors are required in order to detect voltage transitions from one switch configuration or state to another. Oscilloscope voltage and current probes were utilized for tracking terminal voltage and current in [14] and [15]. Using high bandwidth sensors, such as oscilloscope voltage and current probes, is not realistic for a commercial product due to their size and price. Even relatively fast analog to digital converter (ADCs) [14] may miss output voltage level transitions or narrow pulses, and face synchronization and delay issues within a processor(s) or PWM unit. The sampling and bandwidth requirements will be intensified as the switching frequency and voltage conversion ratio increases. Alternatively, a simple and fast windows detector circuit may be used to detect the output terminal voltage transitions, which works asynchronously from the processor(s) or PWM units [13].

In this article, we propose a new, simple, general, and fast OCF detection strategy, one that can detect and localize the fault exactly for FCMCs and cascaded H-bridge (CHB) converters. The proposed algorithm just uses the terminal voltage and direction of terminal current. The detection and localization strategy is presented with simulation results for an H-bridge FCMC, buck FCMC, three-phase FCMC, and single phase buck CHB.

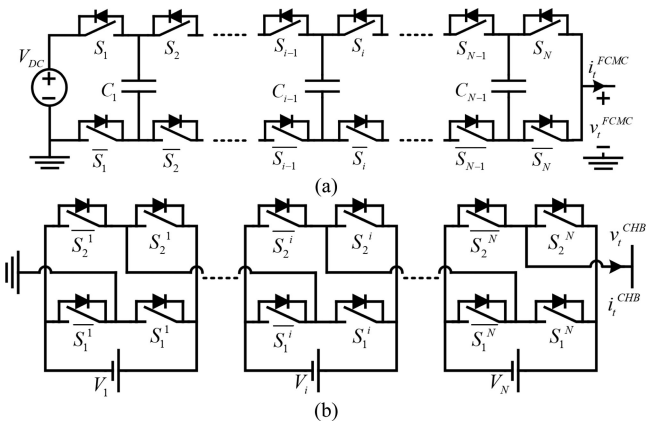

Fig. 1. Generalized legs consisting of switching cells. (a) FCMC. (b) CHB.

The method is experimentally demonstrated on a single-phase FCMC. A solution for the asynchronous sampling of the terminal voltage and feedback delay is presented. While the FCMC PWM was generated with a DSP, the proposed OCF detection and localization algorithm was implemented on a FPGA. Output terminal voltage sensing is provided by a windows detector circuit [13]. The DSP, FPGA, and windows detector are operating asynchronously in the experimental set up.

II. Systems Description

The operational principles of a generalized leg of an N-cell FCMC and CHB are reviewed in this section. Their behavior with an OCF is also discussed.

A. FCMC and CHB

Legs of an N-cell FCMC and CHB are shown in Fig. 1(a) and (b), respectively. In general, conventional types of these families of converters are derived from these basic switching blocks.

Each N-cell FCMC leg with input voltage $V_{\rm DC}$ has $2N$ active switches, $2N$ antiparallel diodes and $N-1$ capacitors $C_1, C_2, \ldots C_{N-1}$. The leg's switching state $S^{\rm FCMC}$ is denoted as $[S_1, S_2, \ldots S_N]$ with $\overline{S_i}$ acting in a complimentary manner of switch S_i. The ON switches in the positive conduction switches vector $S^{\rm CHB} = [{S_1}^1, \overline{{S_2}^1}, \ldots {S_1}^N, \overline{{S_2}^N}]$ are conducting while the output terminal current ${i_t}^{\rm FCMC} > 0$ and in the negative conduction switches vector, $V_1, \ldots V_N$ when ${i_t}^{\rm FCMC} < 0$. The output terminal voltage of the FCMC leg in the normal operation condition ${v_{tn}}^{\rm FCMC}$ can be calculated as

$$ {v_{tn}}^{\rm FCMC} = S_1 V_{\rm DC} + \sum_{i=1}^{N-1} (S_{i+1} - S_i)\, V_{C_i} \qquad (1) $$

considering voltages of capacitors $V_{C_1}, V_{C_2}, \ldots V_{C_{N-1}}$.

The switching state of the N-cell CHB leg with N sources $V_1, \ldots V_N$ and $4N$ switches may be represented as a switching vector $S^{\rm CHB} = [{S_1}^1, \overline{{S_2}^1}, \ldots {S_1}^N, \overline{{S_2}^N}]$ where ${S_1}^i$ and $\overline{{S_2}^i}$ belong to the ith cell. The $\overline{{S_m}^i}$ switches act in a complementary manner to the ${S_m}^i$ switches, where $m = \{1, 2\}$. The ON switches in $S_P{}^{\rm CHB} = [{S_1}^1, \overline{{S_2}^1}, \ldots {S_1}^N, \overline{{S_2}^N}]$ are conducting when

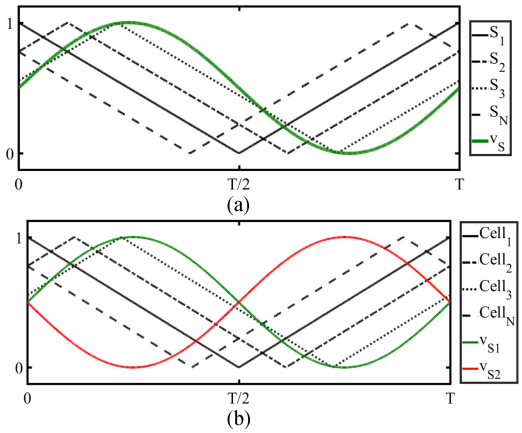

Fig. 2. PSPWM carriers (SN and CellN) and sinusoidal modulating waveforms (v_s and v_{s1}, v_{s2}). (a) Monopolar FCMC. (b) Bipolar CHB.

terminal current ${i_t}^{\mathrm{CHB}}$ is in the positive direction and the ON switches in the switch set ${S_N}^{\mathrm{CHB}} = [\overline{{S_1}^1}, {S_2}^1, \ldots \overline{{S_1}^N}, {S_2}^N]$ are conducting for negative output terminal currents. The output terminal voltage of the CHB leg in the normal operation condition is

$$ {v_{tn}}^{\mathrm{CHB}} = \sum_{i=1}^{N} \left({S_1}^i - {S_2}^i\right) V_i. \tag{2} $$

B. Modulation

In this article, phase shifted pulse width modulation (PSPWM) with a switching frequency of F_s is used as a simple and efficient modulation technique to synthesize the desired output voltage waveform. Examples of the implementation of PSPWM for single phase FCMC and CHB inverters are reviewed here. For PSPWM, in total we have N triangular carriers shifted $2\pi/N$ from each other in phase. In the FCMC, each carrier is driving switch a pair $S_i\overline{S_i}$ by comparing the modulating waveform $v_S$with the appropriate carrier. For the CHB, each carrier is associated with switches ${S_1}^i\overline{{S_1}^i}{S_2}^i\overline{{S_2}^i}$ in the ith cell. For bipolar modulation, two modulation waveforms v_{S1} and v_{S2} phase shifted by π are driving the ${S_1}^i\overline{{S_1}^i}$ pair and ${S_2}^i\overline{{S_2}^i}$ pair, respectively.

PSPWM is fundamentally similar for other types of these families of converters. The PSPWM for an N cell FCMC and bipolar PSPWM for a single phase CHB inverter are depicted in Fig. 2.

In the FCMC, using PSPWM guarantees natural voltage balancing of the capacitors. Capacitor voltages can be derived as

$$ V_{Ci} = \frac{(N-i)\,V_{\mathrm{DC}}}{N}. \tag{3} $$

Given the natural voltage balancing, (1) will be simplified to

$$ {v_{tn}}^{\mathrm{FCMC}} = \frac{(N-1)V_{\mathrm{DC}}}{N} \sum_{i=1}^{N} S_i. \tag{4} $$

The output terminal voltages of the FCMC and CHB have $2N-1$ levels.

C. Converter Response to OCF

If an OCF occurs in a switch conducting the terminal current and that switch is gated ON, its complimentary switch's antiparallel diode will conduct instead. For instance, in the FCMC leg in Fig. 1(a), if ${i_t}^{\mathrm{FCMC}} > 0$ and an OCF occurs in the set of positive conducting switches $S_i \in {S_P}^{\mathrm{FCMC}}$, which are commanded ON, the antiparallel diode of $\overline{S_i} \in {S_N}^{\mathrm{FCMC}}$ will conduct and the output terminal voltage ${v_{tf}}^{\mathrm{FCMC}}$ will deviate from the expected voltage (1). As an example for the CHB leg in Fig. 1(b), if the terminal current is ${i_t}^{\mathrm{CHB}} < 0$ and an OCF occurs in the set of negative terminal current conducting switches, $\overline{{S_1}^i} \in {S_N}^{\mathrm{CHB}}$, the antiparallel diode of ${S_1}^i \in {S_N}^{\mathrm{CHB}}$ will carry ${i_t}^{\mathrm{CHB}}$ instead of $\overline{{S_1}^i}$ despite it being gated ON. As a result, the output terminal voltage ${v_{tf}}^{\mathrm{CHB}}$ will deviate from the expected value (2). If a switch with an OCF is not in the path of terminal current or if it is commanded OFF, it has no impact on the terminal voltage.

The deviation of the FCMC output terminal voltage $\Delta {v_t}^{\mathrm{FCMC}}$ from its expected value due to an OCF occurring in a switch which is commanded ON and is expected to carry the terminal current is given by (5)

$$ \begin{aligned} \Delta {v_t}^{\mathrm{FCMC}} &= {v_{tn}}^{\mathrm{FCMC}} - {v_{tf}}^{\mathrm{FCMC}} \\ &= \begin{cases} V_{C_i} - V_{C_{i-1}} & i_t > 0 \quad \& \quad OC\ in\ S \in {S_P}^{\mathrm{FCMC}} \\ V_{C_{i-1}} - V_{C_i} & i_t < 0 \quad \& \quad OC\ in\ S \in {S_N}^{\mathrm{FCMC}} \end{cases} \end{aligned} \tag{5} $$

where $V_{C_0} = V_{\mathrm{DC}}$.

The output terminal voltage deviation for an OCF in a switch in ith cell of a CHB can be derived as

$$ \begin{aligned} \Delta {v_t}^{\mathrm{CHB}} &= {v_{tn}}^{\mathrm{CHB}} - {v_{tf}}^{\mathrm{CHB}} \\ &= \begin{cases} -V_i & i_t > 0 \quad \& \quad OC\ in\ S^i \in {S_P}^{\mathrm{CHB}} \\ V_i & i_t < 0 \quad \& \quad OC\ in\ S^i \in {S_N}^{\mathrm{CHB}} \end{cases}. \end{aligned} \tag{6} $$

D. OCF Detection and Localization Challenges

For detection and localization of OCF in FCMC the deviation, $|\Delta {v_m}^{\mathrm{FCMC}}| = |{v_{tn}}^{\mathrm{FCMC}} - {v_m}^{\mathrm{FCMC}}|$, of the predicted output terminal voltage ${v_{tn}}^{\mathrm{FCMC}}(1)$ from the measured terminal voltage ${v_m}^{\mathrm{FCMC}}$ will be used to detect and localize the OCF. If the deviation $|\Delta {v_m}^{\mathrm{FCMC}}|$ is greater than a predefined threshold ε at each switching instance, an OCF has occurred in the converter.

Then for the localization, $\Delta {v_t}^{\mathrm{FCMC}}$ for all switches in the path of the current can be calculated using (5) and compared to $\Delta {v_m}^{\mathrm{FCMC}}$. A switch with the closest $\Delta {v_t}^{\mathrm{FCMC}}$ to $\Delta {v_m}^{\mathrm{FCMC}}$ will be identified as the faulty switch. However, the desired operational mode of a FCMC is when the voltages of the capacitors are balanced in a way that blocking voltages across all switches are the same ($V_{C_i} - V_{C_{i-1}} = V_{\mathrm{DC}}/N$). The above method is insufficient for localization in this mode of operation as an OCF in different switches may lead to similar $\Delta {v_t}^{\mathrm{FCMC}}$, which is equal to V_{DC}/N. Hence, this algorithm cannot find the location of the OCF.

For the CHB family of converters, an OCF can also be detected by monitoring the deviation of the expected and measured output

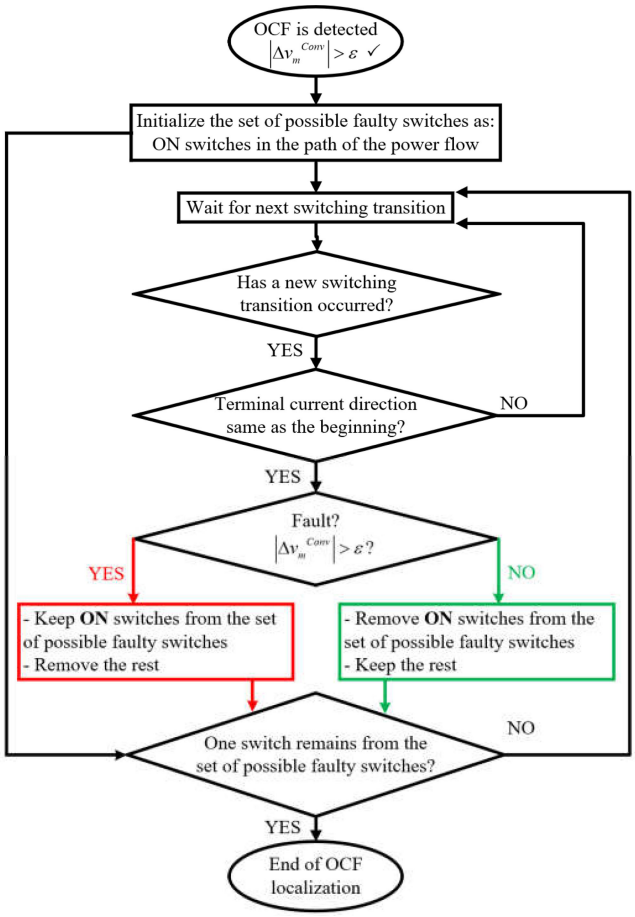

Fig. 3. Proposed OCF localization algorithm flowchart.

terminal voltage. Localization of the of the OC fault faces a similar issue as in FCMCs if two or more voltage sources V_i are similar to each other and equal to V.

III. OCF Localization

In this section, the proposed OCF fault localization algorithm is described. Additionally, the analytical bounding voltage deviation threshold levels and times for the fault detection and localization are determined.

A. OCF Localization Algorithm

For the OCF localization, to overcome the output terminal voltage similarity issue, a simple and straightforward algorithm is proposed that can be implemented for FCMC and CHB families of converters by observing a vector representing potential faulty switches in the next successive switching states after the OCF detection. A flowchart of the algorithm is depicted in Fig. 3. The proposed algorithm is the same for both FCMC and CHB families of converters. Because of this the superscript, Conv., is used instead of FCMC or CHB superscripts.

The main idea behind this algorithm is generating the possible faulty switches vector $\overrightarrow{F^k} = [{f_i}^k]$ where f_i is the fault flag of the ith switch at switching instance k after the OCF detection. A fault flag $f_i = 1$ corresponds to a possible faulty switch and $f_i = 0$ for a healthy one. Over successive switching transitions after the OCF detection, healthy switches can be filtered out from $\overrightarrow{F}$ by setting their corresponding f_i to 0 by comparing the converter predicted terminal voltage with the measured output terminal voltage considering the terminal current direction.

The algorithm will start right after the OCF detection with k set to 0. A switch vector $\overrightarrow{S^k} = [{S_i}^k]$ is defined to indicate the commanded state of switches of the converter. The size of $\overrightarrow{S^k}$ is half the total number of switches in the converter, and ${S_i}^k$ is the status of a switch which will be 1 for ON switches and 0 for OFF switches. Depending on the direction of terminal current at $k = 0$, $\overrightarrow{S^k}$ is equal to ${S_P}^{\text{Conv.}}$ if ${i_t}^{\text{Conv.}} > 0$, or ${S_N}^{\text{Conv.}}$ if ${i_t}^{\text{Conv.}} < 0$. As switching transitions proceed the algorithm continues and updates $\overrightarrow{F^k}$ until just one member of $\overrightarrow{F^k}$ remains 1. The last remaining member of $\overrightarrow{F^k}$ with a value of one corresponds to the switch with an OCF. The proposed fault detection algorithm is shown in Fig. 3 and summarized as the following:

1- If $|\Delta {v_m}^{Conv.}| > \varepsilon$; an OCF is detected
Start the algorithm, $k = 0$
$\begin{cases} \text{if} \quad {\text{i}_\text{t}}^{\text{Conv.}} > 0, \ \overrightarrow{S^k} = {S_P}^{\text{Conv.}} \\ \text{if} \quad {\text{i}_\text{t}}^{\text{Conv.}} < 0, \ \overrightarrow{S^k} = {S_N}^{\text{Conv.}} \end{cases}$, and $\overrightarrow{F^0} = \overrightarrow{S^0}$.

2- If $\overrightarrow{F^k}$ will have just one element with value 1; stop the algorithm and the fault is in the switch associated to that unique element/switch with value 1. Else, move to Step 3.

3- In the next switching state; If the direction of ${i_t}^{\text{Conv.}}$ is the same as Step. 1; $k = k + 1$

$$\begin{cases} if \quad |\Delta {v_m}^{\text{Conv.}}| > \varepsilon, \ \overrightarrow{F^k} = \overrightarrow{F^{k-1}} . \overrightarrow{S^k} \\ if \quad |\Delta {v_m}^{\text{Conv.}}| < \varepsilon, \ \overrightarrow{F^k} = \overrightarrow{F^{k-1}} . (1 - \overrightarrow{S^k}) \end{cases}$$

where, the dot operator denotes an elementwise logic AND between two vectors.

4- Jump to Step. 2.

B. Voltage Deviation Threshold Bounds

A voltage deviation threshold, ε, must be selected for detection of the OCF, $|\Delta {v_m}^{\text{FCMC}}| = |{v_{tn}}^{\text{FCMC}} - {v_m}^{\text{FCMC}}| > \varepsilon$. For CHB converters, ε must be selected to be less than one half of the smallest dc voltage source in a commutation cell minus the measurement noise in the system for proper discrimination of faults. To avoid falsely detecting an OCF, ε must also be set at a level higher than the measurement noise in the system. A larger ε is less prone to measurement noise.

For FCMC the selection of ε is more complex due to the voltage ripple of the flying capacitors. During normal operation without an OCF, two successive output terminal voltage levels have V_{DC}/N difference from each other. To discriminate between successive output voltage levels ε should not exceed $V_{\text{DC}}/2N$. In addition, during normal operation the maximum output terminal voltage ripple $V_{t.\text{ripple.normal}}$ occurs when the maximum terminal current $i_{t.\max}$ passes through all the flying capacitors. This occurs when the duty cycle is 50% and all the capacitors are in the path of the power flow. The maximum output

terminal voltage ripple $V_{t.\mathrm{ripple.normal}}$ can be calculated from (7) which should be lower than $V_{\mathrm{DC}}/2N$ for a well-designed converter. The voltage deviation threshold should be set larger than the maximum output terminal voltage ripple. Hence the value of ε should be chosen between $V_{t.\mathrm{ripple.normal}}$ and $V_{\mathrm{DC}}/2N$ for the OCF detection

$$V_{t.\mathrm{ripple.normal}} \leq \frac{i_{t.\max}}{2NF_S}\sum_{i=1}^{N-1}\frac{1}{C_i}. \tag{7}$$

The selection of ε also is influenced by the OCF localization algorithm. The operational condition of capacitors (C_k) with adjacent healthy switches $(S_k, \overline{S_k}, S_{k+1}, \overline{S_{k+1}})$ remains the same as during normal operating conditions. However, capacitors with a faulty adjacent switch will pass all the terminal current through them unidirectionally. During normal operation the current alternates direction through the capacitors. This changes the maximum terminal voltage ripple, $V_{t.\mathrm{ripple.OCF}}$, for the post OCF condition. Assuming that the OCF occurs in a switch, S_{m+1}, between two capacitors, $C_m \& C_{m+1}$, with an approximate maximum localization time of T_s the maximum $V_{t.\mathrm{ripple.OCF}}$ can be estimated as (8)

$$\begin{aligned} V_{t.\mathrm{ripple.OCF}} &< \left(\frac{i_{t.\max}}{2F_S\chi}+\frac{i_{t.\max}}{2NF_S\eta}\right)\\ \chi &= \left(\frac{C_mC_{m+1}}{C_m+C_{m+1}}\right)\\ \eta &= \left(\frac{C_dC_e}{C_d+C_e}\right), (m\neq e\neq d)\in\{1,\dots N-1\}. \end{aligned} \tag{8}$$

If all C_i have a same capacitance C, χ and η will be simplified to $0.5C$. Otherwise, the maximum value of $V_{t.\mathrm{ripple.OCF}}$ has to be defined using a direct search method due to limited number of possible values for $V_{t.\mathrm{ripple.OCF}}$. Each possibility of adjacent capacitor pairs (C_mC_{m+1}) are plugged in χ and the remaining capacitances in $\eta$to define the maximum value of (8). The voltage deviation threshold, ε, can take a value between the maximum $V_{t.\mathrm{ripple.OCF}}$ and $V_{\mathrm{DC}}/2N$. The calculated $V_{t.\mathrm{ripple.OCF}}$ has to be less than $V_{\mathrm{DC}}/2N$ to avoid false OCF localization in the proposed algorithm. In the experimental set up, the noise level also has to be considered and ε has to be greater than the noise level as well.

C. Minimum and Maximum Time Bounds for OCF Detection and Localization

An OCF in a switch cannot be detected until the faulty switch is turned ON and it is in the power flow path. This provides a starting point for determining the minimum and maximum time bounds for detecting an OCF. The minimum time to detect an OCF in a switch is the sum of the hardware command propagation, measurement, and processing delays which can be termed t_{hw}. If an OCF occurs just as a switch is transitioning to its ON state and it is in the power path just t_{hw}will be required to detect it. As a point of reference in the experimental setup in the article the propagation delay is $\sim$0.5 μs and the measurement and processing delay is $\sim$1 μs. The maximum time to detect an OCF is the time between when the OCF fault occurs and the time when the switch is commanded ON and is in the path of the power flow.

The minimum and maximum time bounds to localize the OCF after detection can also be determined. The localization time, t_l, bounds depend on the PWM number of commutation cells, switching frequency, and duty cycle. For both CHB and FCMC, the minimum required localization time is when the duty cycle D is less than $1/N$while for FCMC just one switch is ON in the power flow path and all other switches are OFF. For duties cycles less than $1/N$ just one switch is ON and in the power flow path and all other switches are OFF. For these duty cycles the fault can be detected immediately with just the hardware delay, t_{hw}.

The maximum localization time bound occurs for duty cycles greater than $(N-1)/N$ which means all switches can be ON or just one switch is OFF in each switching state. For these duty cycles the localization algorithm needs to wait for all switches to cycle through a single OFF switching state to find the location of the OCF. Using PSPWM modulation, it takes $2N-1$ switch transitions to check all switches which is less than the PWM period $(T_s = 1/F_s)$. The localization time is then bounded in the range of $t_{\mathrm{hw}} < t_l < T_s + t_{\mathrm{hw}}$.

IV. Simulation Results

To show the execution of the proposed OCF localization algorithm, the step by step operation for a single-phase H-bridge FCMC is first presented. Then, simulation results for detection and localization of an OCF in a buck FCMC, and three-phase FCMC inverters and single phase CHB are shown. Circuits of the simulated converters are shown in Fig. 4.

A. Single Phase HB-FCMC

To demonstrate the proposed OCF detection and localization algorithm a seven-level HB-FCMC [Fig. 4(a)] with $V_{\mathrm{DC}} = 300$ V, $C = 200$ μF, $R_{\mathrm{load}} = 50$ Ω, $L_{\mathrm{load}} = 10$ mH, $F_m = 60$ Hz, and $F_S = 1$ kHz is used. The terminal voltage for normal v_n and faulted v_f operation and current i_t of the converter are shown in Fig. 5(a). Using (4), the expected terminal voltage in each switching state is

$${v_n}^{\mathrm{HB-FCMC}} = \left(\frac{S_1+S_2+S_3+S_4+S_5+S_6}{3}-1\right)V_{\mathrm{DC}}. \tag{9}$$

An OCF is applied on S_5 at $\overline{t_f} = 18$ ms where the bar above a variable indicates negative logic. The variation of the elements of $\overrightarrow{F^k}$ with each switching instance, the faulted terminal voltage and its expected value in normal operation, and fault detection/localization results are shown in Fig. 5(b) between 17.8 and 20 ms. The OCF detection and localization algorithm flow is as follows.

1) OCF detected and localization begins, $|\Delta {v_t}^{\mathrm{FCMC}}| > \varepsilon$ at $t_d = 18.12$ ms
$$\begin{cases} {i_t}^{\mathrm{Conv.}} > 0 \quad => \\ \overrightarrow{S^0} = {S_P}^{\mathrm{Conv.}} = [S_1, S_2, S_3, S_4, S_5, S_6] \end{cases}.$$
2) Fault flag evolution for each switch transition is

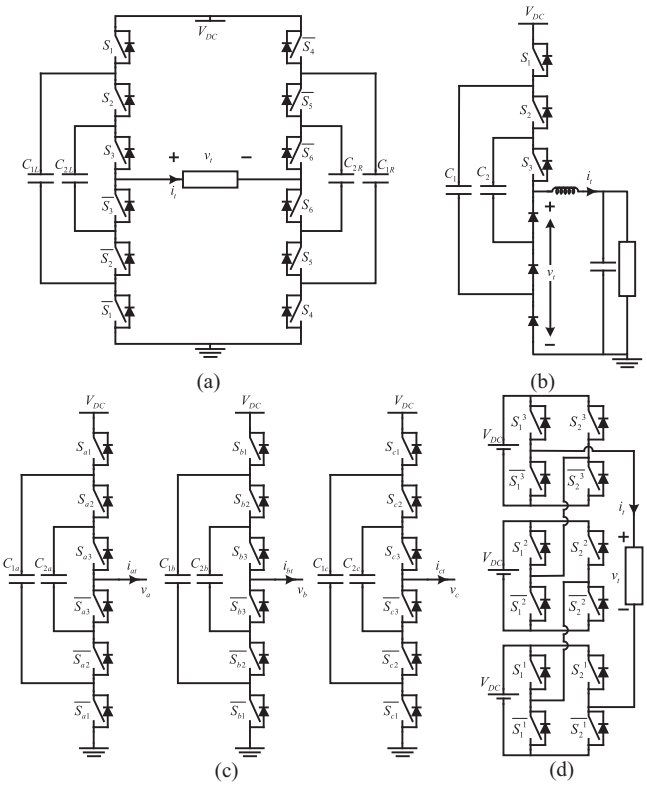

Fig. 4. Simulated circuits. (a) H-Bridge FCMC. (b) Buck FCMC. (c) Three-phase FCMC. (d) Single phase CHB.

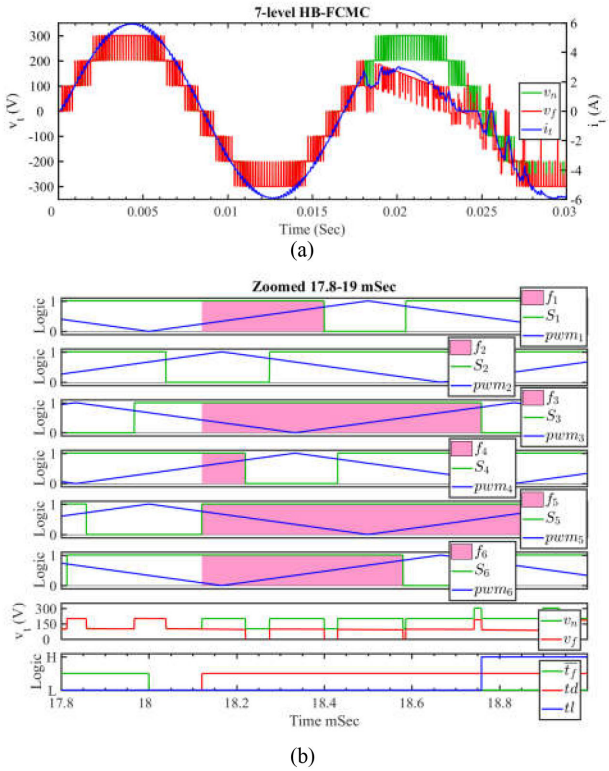

Fig. 5. OCF detection/localization for seven-level single phase HB-FCMC with a fault occurring at $\overline{t_f} = 18$ ms. (a) Terminal current and voltage (normal and faulted). (b) Switching function logic and associated fault flags for each switch, terminal voltage, and fault occurrence, detection and localization zoomed between 17.8 and 19 ms. Red in a fault flag indicates a high fault flag state

$$\overrightarrow{F^0} = [101111], \quad {i_t}^{\text{Conv.}} > 0$$
$${i_t}^{\text{Conv.}} > 0 \;\Rightarrow\; \overrightarrow{F^1} = \overrightarrow{F^0}.[101011] = [101011].$$
$${i_t}^{\text{Conv.}} > 0 \;\Rightarrow\; \overrightarrow{F^2} = \overrightarrow{F^1}.[111011] = [101011]$$
$${i_t}^{\text{Conv.}} > 0 \;\Rightarrow\; \overrightarrow{F^3} = \overrightarrow{F^2}.[011011] = [001011]$$
$${i_t}^{\text{Conv.}} > 0 \;\Rightarrow\; \overrightarrow{F^4} = \overrightarrow{F^3}.[001010] = [001010]$$
$${i_t}^{\text{Conv.}} > 0 \;\Rightarrow\; \overrightarrow{F^5} = \overrightarrow{F^4}.[111110] = [001010]$$
$${i_t}^{\text{Conv.}} > 0 \;\Rightarrow\; \overrightarrow{F^6} = \overrightarrow{F^5}.[111111] = [001010]$$
$${i_t}^{\text{Conv.}} > 0 \; amp; \Rightarrow\; \overrightarrow{F^7} = \overrightarrow{F^6}.[110111] = [000010].$$

At the seventh switching transition ($t_l = 18.76$ ms) after the fault detection, f_5 in $\overrightarrow{F^7}$ is the only nonzero element. Hence, the OCF is localized in S_5 which is associated to f_5 after $t_l - t_f = 0.56$ ms.

B. Buck-FCMC

A four-level buck FCMC shown in Fig. 4(b) is simulated in this section and the results are shown in Fig. 6. Using (4), the expected terminal voltage in each switching state is

$$v_n{}^{\text{Buck-FCMC}} = \left(\frac{S_1 + S_2 + S_3}{3}\right) V_{\text{DC}}. \tag{10}$$

An OCF occurs in switch S_3 at $\overline{t_f} = 75$ ms, and is detected instantaneously at $t_d = 75$ ms. The fault is localized after 0.45 ms at $t_l = 75.45$ ms.

C. Three-Phase FCMC

Simulation results of a seven-level three-phase FCMC are presented in Fig. 6. For this type of converter, the line to line voltages and the terminal current directions have to be measured. Using (4), the expected line to line terminal voltage in each switching state is

$$v_{\text{abn}}{}^{\text{Buck-FCMC}} = (S_{a1} + S_{a2} + S_{a3} - S_{b1} - S_{b2} - S_{b3})\,\frac{V_{\text{DC}}}{3} \tag{11}$$

$$v_{\text{bcn}}{}^{\text{Buck-FCMC}} = (S_{b1} + S_{b2} + S_{b3} - S_{c1} - S_{c2} - S_{c3})\,\frac{V_{\text{DC}}}{3} \tag{12}$$

$$v_{\text{can}}{}^{\text{Buck-FCMC}} = (S_{c1} + S_{c2} + S_{c3} - S_{a1} - S_{a2} - S_{a3})\,\frac{V_{\text{DC}}}{3}. \tag{13}$$

An OCF occurs in S_{c3} at $\overline{t_f} = 25$ ms. It is detected instantaneously at $t_d = 25$ ms, and localized after 0.6 ms at $t_l = 25.6$ ms. As can be seen in Fig. 7(a), no deviation in line "a" to "b" voltage v_{ab} occurs as the fault was on leg "c." So, at the beginning of the localization algorithm all switches for phases "a" and "b" will be removed from $\overrightarrow{F^k}$ and the algorithm will only search for possible faulty switches in the set containing just switches in leg "c."

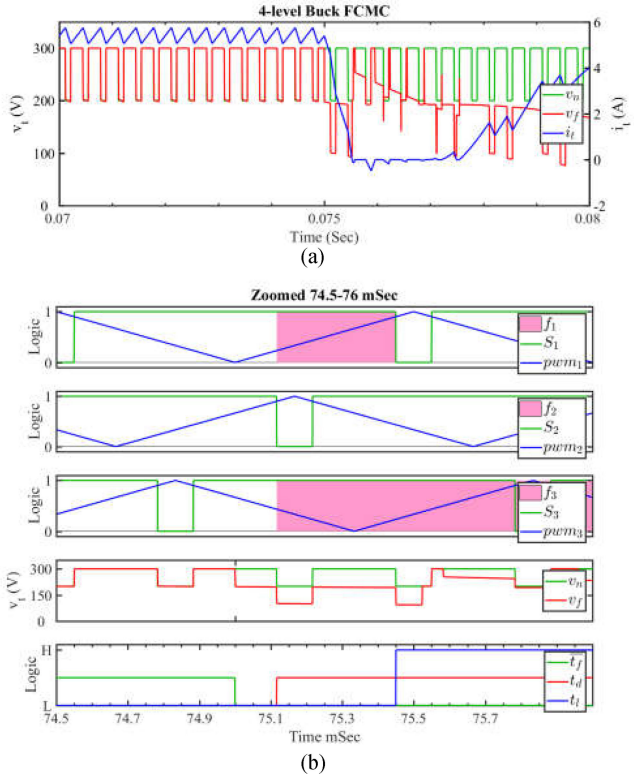

Fig. 6. OCF detection/localization for four-level buck FCMC with a fault occurring at $\overline{t_f} = 75$ ms. (a) Terminal current and voltage. (b) Switching function and fault vector logic, terminal voltage, and fault occurrence, detection, and localization zoomed between 74.5 and 76 ms. Red in a fault flag indicates a high fault flag state.

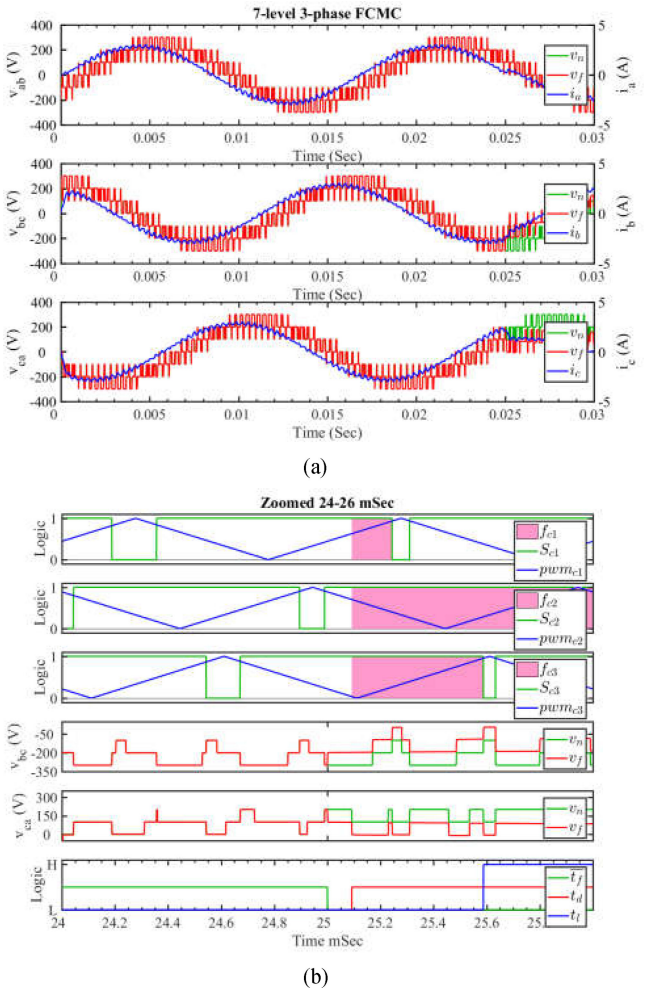

Fig. 7. OCF detection and localization for seven-level three-phase FCMC with a fault occurring at $\overline{t_f} = 25$ ms. (a) Terminal current and voltage. (b) Switching function and fault vector logic, terminal voltage, and fault occurrence, detection, and localization zoomed between 24 and 26 ms. Red in a fault flag indicates a high fault flag state.

D. CHB

A single phase seven-level CHB [Fig. 4(c)] is simulated in this section and results are depicted in Fig. 8. The expected output terminal voltage of the converter can be calculated using (2) as

$$v_n{}^{\mathrm{CHB}} = \left(\frac{S_1 + S_3 + S_5 - S_2 - S_4 - S_6}{3}\right) V_{\mathrm{DC}}. \quad (14)$$

The OCF occurs in switch ${S_1}^2$ at $\overline{t_f} = 21.2$ ms, is detected instantaneously $(t_d = 21.2\ \mathrm{ms})$, and localized after 0.8 ms at $t_l = 22$ ms.

V. Experimental Results

In this section, experimental results are presented for a seven-level single phase HB-FCMC [Fig. 4(a)]s. The converter was controlled and PWM generated using a 150 MHz TI TMS320F28335 DSP. Steady state operation and natural balancing of the capacitors are achieved using PSPWM as discussed in Section II with a carrier frequency of $F_s = 1$ kHz, modulation index of $m = 1$, and modulation frequency of $F_m = 60$ Hz. Due to safety concerns, the dc link voltage is limited to 150 V. The converter is connected to a 100 Ω resistive load. The proposed fault detection and localization algorithm was implemented on DE2-115 FPGA development board equipped with a 50 MHz Altera Cyclone-IV EP4CE115F29C7N as an independent processor from the main DSP to study the practical challenges of the OCF detection and localization process as an add-on unit. To detect the output terminal voltage levels and instantaneous current direction, a simple high bandwidth bidirectional windows detector circuit is proposed in [13] for MCs is used. The experimental setup is shown in Fig. 9.

A. FPGA Logic

The FPGA required no special communication protocol, synchronization, or intermediate buffer/amplifier to read the gate signals from the DSP, nor voltage levels and current directions from the windows detector circuit. TTL 0-3.3 V logic signals from the DSP and windows detector circuit were directly fed to the FPGA input pins. In simulation, all tasks run in parallel and samples are gathered instantaneously. In an actual physical implementation, the speed of sampling is limited to the clock and edge detection of the FPGA. In addition, the DSP, FPGA, and

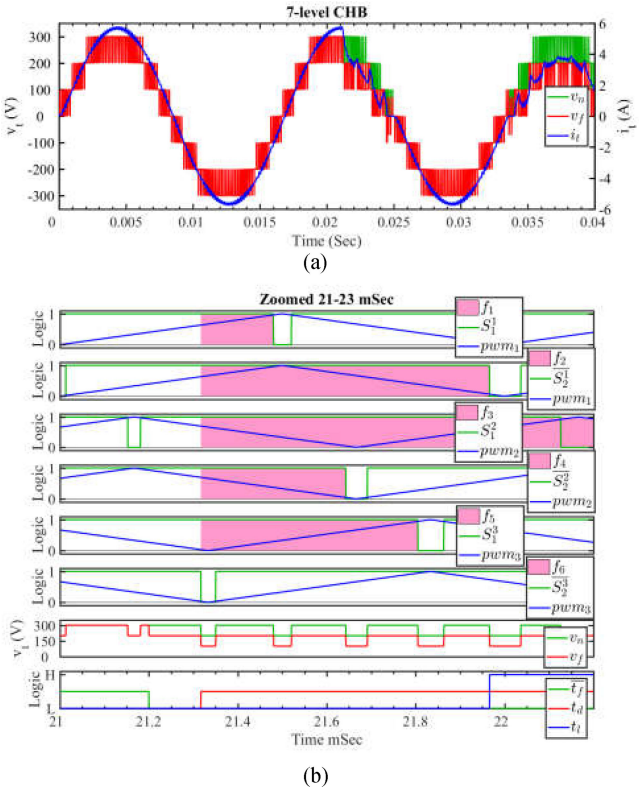

Fig. 8. OCF detection and localization for seven-level CHB with a fault occurring at $\overline{t_f} = 21.2$ms. (a) Terminal current and voltage. (b) Switching function and fault vector logic, terminal voltage, and fault occurrence, detection, and localization zoomed between 21 and 23 ms. Red in a fault flag indicates a high fault flag state.

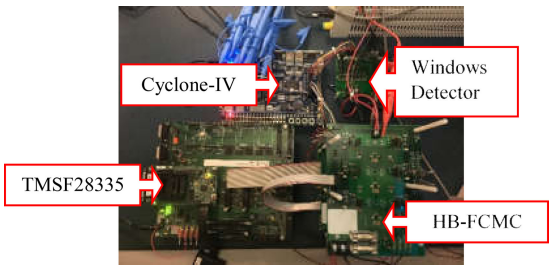

Fig. 9. Experimental set up.

windows detector circuit are not synchronized with each other and operate at different speeds. To compensate for this asynchronism, additional logic must be added to the FPGA. The very top level of very high-speed integrated circuits program hardware description language (VHDL) code data flow is illustrated in Fig. 10.

B. Dead Time and Asynchronous Edge Detection

In a physical implementation, there is dead-time in-between the transition of two complimentary switches. During this period both switches are gated OFF. One of the primary assumptions in the proposed algorithm is that two complimentary switches always act in compliment with each other. To overcome this

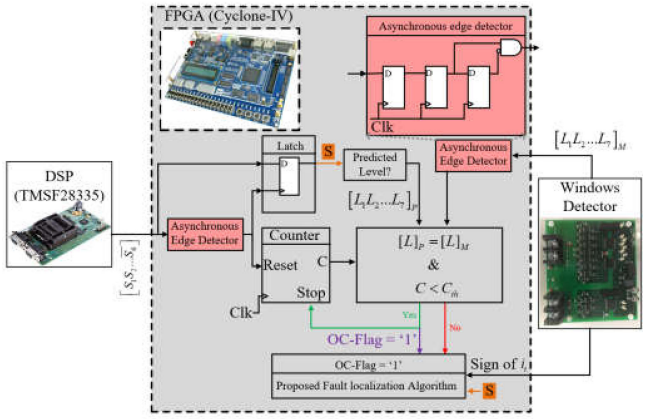

Fig. 10. Top level flow of parallel signals inside the FPGA.

issue, just the rising edge of the gate signals needs to be detected as a starting point of new switching transition. As soon as any rising edge of each of the 12 gating signals is detected, the FPGA will detect that a new switching state has been reached and will update the predicted output terminal voltage level to be compared with the signal from the windows detector to perform the comparison in the current switching transition. This task theoretically can be implemented by two D-flip flops in series and an AND gate with one inverted input to indicate a rising edge between the current state and the previous one. However, in reality as the switching transition edges are not synchronized with the FPGA clock, some rising edges will be too close to the FPGA clock transitions. This can cause the flip flops to operate in a metastable state, theoretically taking infinite time to reach their stable value. To avoid this issue, an additional D-flip flop is added in series with the original configuration. The 3-D-flip flops form an asynchronous edge detector guaranteeing all rising edges are detectable.

C. Propagation Delay

Although the FPGA receives PWM signals from the DSP without any intermediate circuitry, the output of the windows detector circuit [13] has a delay compared to the commanded switch state due to the delay introduced by components in the signal and power stages such as optical isolators, gate drives, etc. The measured propagation delay between a commanded signal and the output of the windows detector circuit is 500 μs. To overcome this delay, a counter inside the FPGA provides a blanking time after each switching transition to let the system to reach its new stable state to compare the predicted output terminal voltage level to the measured one from the windows detector. In the results presented, the blanking time was set to 600 μs. Using a PSPWM or similar modulation technique with no control on minimum pulse width, may result in switch gate commands narrower than the turn-ON/OFF time of the switches. The blanking time avoids detecting an OCF, even though a switch is commanded with a narrow pulse. Its state would not be changed.

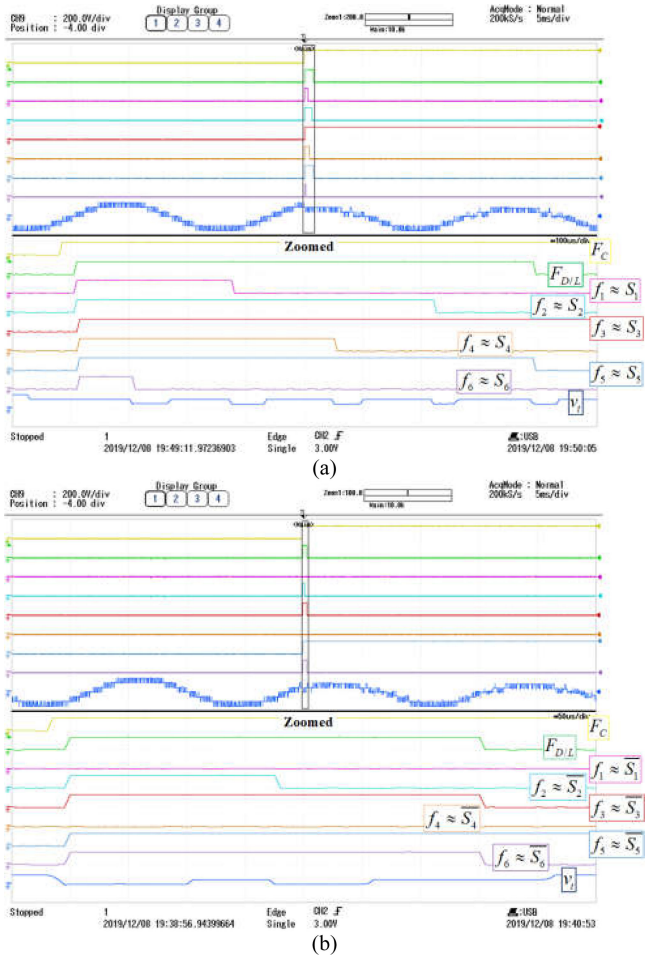

Fig. 11. OCF detection and localization experimental results for the seven-level HB-FCMC. (a) OCF on S_3. (b) OCF on $\overline{S_5}$. The waveforms from top to bottom are 1–fault command, 2–fault detection-localization, 3, 4, 5, 6,7, 8–fault flags associated with the labeled switch, and 9–terminal voltage, v_t.

D. Fault Localization

As discussed in the previous section, when the rising edge of any switch's PWM signal comes into the FPGA, it will be detected and the new switching state will be latched. Then the predicted level associated with the latched state will be updated. The FPGA will wait for 600 μs for the input from the windows detector. If the predicted level and the actual ones are matched, no fault is observed, otherwise, a fault has happened and signals will be passed to the proposed fault localization algorithm (Fig. 3).

Fig. 11 shows the experimental OCF localization results for fault on S_3 [Fig. 11(a)] and $\overline{S_2}$ [Fig. 11(b)]. An OCF is mimicked by signaling OFF to the targeted switches despite the commanded switch state from the DSP. To do so, an additional logic circuit is implemented on the DSP expansion board to control the location and type of fault. In Fig. 11, the fault command, F_c, or occurrence of the fault is the transition of the top waveform from low to high. The second waveform from the top is the status of the FPGA fault detection (transition from low to high) and fault localization (transition from high to low). The remaining waveforms are the six FPGA fault flags, F_x, associated with the switches in the path of the current flow at the moment that the fault is applied and the terminal voltage of the converter, v_t. Additional fault flag elements are not shown because of the limitation of the number of oscilloscope channels. The time required to detect and localize the faults in Fig. 11(a) are 24 and 808 μs and in Fig. 11(b) 15 and 352 μs respectively.

VI. Conclusion

The theory and algorithm of a new simple, general and fast OCF detection and localization strategy for FCMCs and CHB converters is proposed using just measurements of the terminal voltage and direction of terminal current. Simulations for buck, single-phase, three-phase FCMC and H-bridge MCs validated the proposed strategy for general family of FCMC and H-Bridge cascaded converters. The algorithm was experimentally tested on a prototyped single phase FCMC using an FPGA and windows detector circuit. Delay and asynchronous issues for operation of system are discussed and solutions are provided. Fault detection times of 24 and 15 μs and fault localization times of 808 and 352 μs were experimentally measured verifying the speed of the proposed algorithm.

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